JESD204B Xilinx/Analog Devices AD9250 Interoperability Report

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CONTENTS

Introduction

This document describes the method and tests carried out to test interoperability between The Xilinx® LogiCORE™ JESD204 IP and the Analog Devices AD9250 ADC.

Location

Analog Devices, Wilmington MA.

Date

April 21st – 23rd 2013.

Scope

Interoperability testing was limited to use existing hardware supporting JESD204B Subclass 0 and Subclass 1. The AD9250 device does not support Subclass 2 functionality.

Hardware

Xilinx KC705 Evaluation Board

The Kintex®-7 FPGA KC705 Evaluation Kit includes all the basic components of hardware, design tools, IP, and a pre-verified reference design for system designs that demand high-performance, serial connectivity and advanced memory interfacing. The included pre-verified reference designs and industry-standard VITA-57 FPGA Mezzanine Connectors (FMC) allow scaling and customization with daughter cards.

The Xilinx KC705 board is described in detail here: http://www.xilinx.com/products/boards-and-kits/EK-K7-KC705-G.htm

Analog Devices AD9250-Z FMC Evaluation Board

The ADI AD9250 FMC Evaluation Board (HSC 12010 Rev A / 9250FMC01A) is a VITA-57 FMC card which includes 2 x ADI AD9250 A/D Convertor devices.

The AD9250 is a Dual Convertor, 14-bit 250 MSamples/sec Analog to Digital Convertor, with a 2-lane JESD204B compliant interface operating at line rates up to 5 Gb/s. The AD9250 FMC Evaluation Board provides a device/reference clock input with clock buffering and distribution to the onboard ADC devices and to the FPGA via the FMC connector.

Hardware Setup

The Kintex-7 XC7K325T FPGA on the KC705 board is configured with one of several FPGA design bitstreams to support the various operating modes of the AD9250. The FPGA designs are based around the Xilinx JESD204 v5.0 LogiCORE IP with additional external supporting logic. Xilinx Chipscope Pro is used to configure, monitor and control the operation of the hardware. The FPGA designs support initial device setup and on-the-fly configuration changes via control register accesses. These facilities allow access to both the AXI-Lite accessible registers of the Xilinx LogiCORE and the SPI accessible registers of the AD9250.

The FPGA designs also provide generation of the master SYSREF signal used by both devices in Subclass 1 mode.

The AD9250 Evaluation board is connected to the HPC FMC of the KC705 board. An external Device Clock/GT Reference clock is connected to the FMC card, this clock is forwarded via the FMC interface to a GT reference clock input of the FPGA. The AD9250 configuration and status registers are accessible via an SPI interface which interfaces to the FPGA. Analog inputs are available for each of the ADC input channels.

The AD9250 received its sample clock via J1, and analog inputs to the ADC were provided via J100 (converter 0) and J600 (converter 1). For deterministic latency tests, the clock and analog inputs were sourced from a Tektronix HFS9003 Stimulus System. For other tests, the clock was sourced by a Rhode & Schwarz SML03, and the analog inputs were sourced from a Tektronix AWG2021.

Power for the AD9250 is sourced from the KC705 board over the FMC connector. No additional connections to the AD9250 board were used. The KC705 board was connected to AC power via the standard power supply and to a PC over USB for a JTAG connection to the FPGA for image loading and debug.

Deterministic Latency Test Setup

In order to prove deterministic latency for the entire system (analog in to samples out), the following test setup was used. An HFS pulse generator output a 250MHz clock, for the AD9250's sample clock, as well as a one-shot pulse upon a manual trigger button press. The pulse was fed into the analog input of the ADC along with one channel of an oscilloscope.

The FPGA IP output the data stream into a transport layer decoding block, which decoded the data back into samples. The MSB of Converter 0's samples was fed to a SMA jack on the KC705 board. This was then connected to the second channel on the oscilloscope.

This setup allowed the time between the pulse entering the ADC and when the MSB toggled at the output of the IP to be measured. This incorporates the entire system latency, not just the JESD204B link latency.

The pulse was timed relative to the AD9250 sample clock to ensure minimal sampling uncertainty. The AD9250 added an artificial offset to the data samples digitally. This ensured a clean transition of the MSB. The ADC board has an AC coupled analog input, so a DC signal (as was present whenever the pulse was not triggered) could cause significant toggling around mid-scale as any noise was received.

Xilinx IP Configuration

The Xilinx LogiCORE JESD204 v5.0 IP Core supports JESD204B on Kintex-7 and Virtex®-7 devices. See the IP User Guide for details. The IP is configured for Kintex-7 devices using the GTX transceiver for this interoperability testing.

The designs used in this interop testing used the LogiCORE configured as 2-lane, JESD204B, Subclass 1. For single lane modes of the AD9250, software selectable lane disable was used to disable the unused lane.

AD9250 Configurations

The AD9250 device supports the four JESD204 configurations shown below :

AD9250 Mode	Convertors (M)	Sample Rate (MHz)	Lanes (L)	Serial Line Rate (Gb/s)	Octets per frame (F)	Frames per Multiframe (K)	Multiframe Size (octets)	GT Reference Clock (MHz)	Core Clock (MHz)
22	2	250	2	5	2	32	64	250	125
11	1	250	1	5	2	32	64	250	125
12	1	250	2	2.5	1	32	32	250	62.5
21	2	125	1	5	4	32	128	125	125

Table 1- AD9250 JESD204 configurations

Interoperability Test Results

The following table outlines the tests carried out.

Test Number	Test	Description	Interoperable	Notes
1	Sync request	Test correct operation when sync~ is requested by the receiver. The receiver should request sync following reset. It also possible to force sync~ low when the FPGA is the receiver to re-request sync.		
1.1		Check K28.5 transmitted by transmitter in response to sync request.	Yes	The receiver was seen to drive SYNC~ low after a reset and using test design “Force Resync” facility. K28.5 characters were seen at the receiver in response to a sync request.

1.2		Check ILA or Data follows K28.5 when sync~ goes high.	Yes	The ILA was seen after SYNC~ goes high. Data/No ILA mode not tested – not supported by AD9250.
1.3		Check ILA or Data following K28.5 is aligned to frame clock.	Yes	At the receiver data was observed to be correctly aligned after the ILA in chipscope. Data/No ILA mode not tested – not supported by AD9250
2	Initialization	Test the link initializes correctly from reset and power on.		
2.1		Check Alignment correct at receiver by inspecting sync~ de-assertion.	Yes	The link was seen to initialize correctly. Lane Alignment was seen to be correct for 2 lane modes.
2.2		Check ILA transmitted and received following K28.5 when ILA supported.	Yes	Duplicate of 1.2.
2.3		Check data frames transmitted and received following K28.5 when ILA disabled.	N/A	No ILA not supported by AD9250.
3	Framing	Test the data passes correctly for all framing formats supported by the hardware.		
3.1		For each frame format supported by the ADC the IP will be reconfigured and the link reestablished and the sample data verified by comparing the analogue data with the expected pattern.	Yes	Modes tested : (see Table 1) 22 OK 11 OK 12 OK 21 OK Data was captured at the receiver after demapping using chipscope and displayed as “analog” using bus plot at sample

				clock rate. Both Analog signal sources and AD9250 built-in Test Modes were observed.
4	Initial Lane Sync Sequence	Test the initial lane sequence is generated and received correctly including correct passing of the JESD204 configuration bytes.		
4.1		Check the ILA is generated with the correct frame and multiframe numbers.	Yes	Captured and viewed in chipscope ILA.
4.2		Check the Configuration data bytes are transferred correctly by inspecting register contents.	Yes	The configuration bytes were captured and viewed in chipscope ILA, and by interrogating captured values in Xilinx LogiCORE registers.
5	Data Samples and Control Bits	Test the sample data is passed without error.		
5.1		Check the data received by the IP matches the analogue data stimulating the ADC. A repeating data pattern shall be injected into the ADC and captured by the IP using Xilinx Chipscope with a 2ksample window.	Yes	Modes tested : (see Table 1) 22 OK 11 OK 12 OK 21 OK Data was captured at the receiver after demapping using chipscope and displayed as “analog” using bus plot at sample clock rate. Both Analog signal sources and AD9250 built-in Test Modes were observed.
6	Scrambling	Test for correct link operation with scrambling enabled and disabled.		

6.1		Check for correct data with scrambling disabled.	Yes	Correct demapped analog output data observed. When the AD9250 scrambling was enabled, but not in the IP, incorrect data was received, as expected. Both Analog signal sources and AD9250 built-in Test Modes were observed.
6.2		Check for correct data with scrambling enabled.	Yes	Correct demapped analog output data observed. Both Analog signal sources and AD9250 built-in Test Modes were observed.
6.3		Check the first few octets following the ILA are correct by using logic analyzer to check early sync option if applicable.	N/A	AD9250 does not support early sync option.
7	Deterministic Latency	Test Subclass 1 deterministic latency		
7.1	LMFC Alignment	Check ADC and FPGA correctly align to all supported LMF periods	Yes	Implied LMFC alignment observed via chipscope ILA, observing relative alignment of SYSREF, received ILA sequence and IP core data output.
7.2	SYSREF Capture	Check ADC and FPGA capture SYSREF correctly and restart LMF Counter.	Yes	Implied LMFC alignment (hence SYSREF capture) observed via chipscope ILA, observing relative alignment of SYSREF, received ILA sequence and IP core data output.
7.3	End to End Latency	Check Latency is fixed between resets and using all supported lane and	Yes	Repetitive single “square” pulse applied to ADC input, and via a splitter to

		frame formats.		oscilloscope channel. Test output (sign bit of output demapped data = “zero crossing”) displayed on 2nd oscilloscope channel. Overall end-to-end latency is thus directly measured. This showed excellent repeatability of the end-to-end latency. Observed Latency: Mode 22: 463ns Mode 11: 463ns Mode 12: 649ns Mode 21: 426ns
8	Test Patterns	Test generation and reception of all test patterns detailed in JESD204B.		
8.1	(Transport Layer Test Patterns)	Check patterns defined in section 5.1.6 are transmitted and verified correctly.	N/A	AD9250 does not directly support transport Layer test patterns
8.2	(Datalink Layer Test Modes)	Check Sequences defined in section 5.3.3.8.2 are transmittedby the Tx device, and verified correctly by the Rx device where appropriate.	Yes D21.5 K28.5 Repeated ILA RPAT JSPAT	 Not supported Not supported Repeated ILA - OK RPAT - OK Not supported by AD9250
9	Supported Line Rates	Test correct operation at all rates supported by hardware.		
9.1		Check operation at MIN Gbps line rate.	Yes	The link was tested at the 2.5Gbps line rate (Mode 12)
9.2		Check operation at MAX Gbps line rate.	Yes	The link was tested at the 5Gbps line rate (Modes 22,11,21). In addition, reference

				clock rate was reduced as low as 229 MHz (4.58 Gbps line rate) with correct link operation retained.
10	Alignment character replacement	Test the correct insertion (Tx) and reinstatement (Rx) of alignment characters during normal data transmission as per 5.3.3.4.2 and 5.3.3.4.3. Check for alignment character insertion using logic analyzer in FPGA.		
10.1		Check for alignment character insertion when scrambling disabled and ILA supported.	Yes	Alignment characters were observed on chipscope at the receiver.
10.2		Check for alignment character insertion when scrambling disabled and ILA not supported.	N/A	No ILA mode was not tested – not supported by AD9250.
10.3		Check for alignment character insertion when scrambling enabled.	Yes	Alignment characters were observed on chipscope at the receiver.

Compliance to JESD204A Specification

The interoperability tests in the previous section shall cover the items detailed in the table below.

Spec section	Contents	Tested by Interop	Notes
1	Scope	N/A	
2	References	N/A	
3	Terminology	N/A	
4	Electrical	Partial	Electrical interoperability is tested but compliance is not.
4.1	Overview	Partial	Electrical interoperability is tested but compliance is not.
4.2	Compliance Types	Partial	Electrical interoperability is tested but compliance is not.
4.3	Interconnect	Partial	Electrical interoperability is tested but compliance is not.
4.4	Compliance to OIF SxI-5	Partial	Electrical interoperability is tested but compliance is not.
4.5	Compliance to LV-OIF-6G-SR	Partial	Electrical interoperability is tested but compliance is not.
4.6	Compliance to LV-OIF-11G-SR	Partial	Electrical interoperability is tested but compliance is not.
4.7	Device Clock	Partial	Limited range of Device Clock frequencies.
4.8	Frame Clock & LMF Clock	Partial	Limited range of LMF periods.
4.9	SYNC Interface	Partial	SYNC~ signal is used in interop testing but compliance not tested.
4.10	Lane-to-lane Inter-device Sync	Yes	
4.11	SYSREF Signal	Yes	

4.12	Skew Budget	No	Unable to test in interop.
4.13	Control Interfaces	Partial	Left to user in JESD204B Spec. SPI used in interop.
5	Data Stream	Partial	See subsections
5.1	Transport Layer	Partial	See subsections
5.1.1	Overview	N/A	
5.1.2	User Data Format for and Independent Lane	No	Multi-lane devices used in interop
5.1.3	User Data Format for Multiple Lanes	Partial	Only formats supported by AD9250 were tested (Table 1)
5.1.4	Tail Bits	No	Formats supported by interop hardware do not require tail bits.
5.1.5	Idle Mode	No	Unable to test in interop.
5.1.5.1	General	No	Unable to test in interop.
5.1.5.2	Dummy Samples	No	Unable to test in interop.
5.1.6	Test Modes	Yes	
5.1.6.1	General	N/A	
5.1.6.2	Short test pattern	No	
5.1.6.3	Long test pattern	No	
5.2	Scrambling	Yes	
5.2.1	Polynomial	Yes	
5.2.2	Bit Order	Yes	
5.2.3	Scrambler Type	Yes	
5.2.4	Early Sync Option	N/A	Not supported by AD9250.
5.2.5	Initial State	N/A	Not supported by AD9250.
5.2.6	Scrambling Disable	Yes	
5.3	Data Link Layer	Partial	See subsections
5.3.1	8B10B	Yes	
5.3.2	Transmission Order	Yes	
5.3.3	Link Operation	Partial	See subsections
5.3.3.1	Code Group Sync	Yes	
5.3.3.2	SYNC~ Signal Combining	Yes	
5.3.3.3	Initial Frame Sync	Yes	
5.3.3.4	Frame Alignment monitoring and Correction	Partial	See subsections
5.3.3.4.1	Alignment Characters	Yes	
5.3.3.4.2	Character Replacement without Scrambling	Yes	
5.3.3.4.3	Character Replacement with Scrambling	Yes	
5.3.3.4.4	Frame Alignment Correction in Rx	No	Not possible to inject alignment errors
5.3.3.5	Initial Lane Synchronisation	Yes	
5.3.3.6	Lane alignment monitoring and correction	No	Not possible to inject alignment errors
5.3.3.7	Link re-initialization	Yes	

5.3.3.8	Test Modes	Yes	
5.3.3.9.1	General	Yes	
5.3.3.9.2	Test Sequences	Yes	
6	Deterministic Latency	Yes	
6.1	Introduction	N/A	
6.2	No Support (SC0)	N/A	
6.3	Using SYSREF (SC1)	Yes	
6.4	Using SYNCB (SC2)	No	
6.4.1	Principles of SYNCB sampling	No	
6.4.1.1	SYNCB Generation	No	
6.4.1.2	Adjustment Resolution & Clock	No	
6.4.1.3	Detection resolution at Tx	No	
6.4.1.4	SYNCB de-assertion	No	
6.4.2	Master & slave configurations	No	
6.4.2.1	ADC	No	
6.4.2.2	DAC	No	
6.5	Interop with JESD204A	N/A	Both devices are JESD204B in this interop
7	Receiver Operation	Partial	See subsections
7.1	Code Group Synchronisation	Yes	
7.2	Initial Frame Synchronization	Yes	
7.3	Frame Alignment monitoring and correction	No	Not possible to inject alignment errors
7.4	Initial Lane Synchronisation	Yes	May not be possible to check time to align
7.5	Lane alignment monitoring and correction	No	Not possible to inject alignment errors
7.6	Error Handling	No	Not possible to inject errors
7.6.1	Error Kinds	No	Not possible to inject errors
7.6.2	Data Output on Error	No	Not possible to inject errors
7.6.3	Errors Requiring re-initialization	No	Not possible to inject errors
7.6.4	Error Reporting via SYNC interface	No	Not possible to inject errors
7.6.5	Error Reporting via control interface	No	Not possible to inject errors
8	Transmitter Operation	Yes	
8.1	Synchronisation	Yes	
8.2	Initial Lane Alignment Sequence	Yes	
8.3	Link Configuration Data and Encoding	Yes	
8.4	SYNCB Signal Decoding	Yes	
8.5	SYNCB detection	N/A	Subclass 2 only
9	Device Classification	N/A	