Spartan®-6 FPGA Consumer Video Kit 2.0 FAQ

General Questions:

Q: What is the Spartan®-6 FPGA Consumer Video Kit (CVK 2.0) 2.0?

A: The Spartan-6 FPGA Consumer Video Kit 2.0 consists of a Spartan-6 LX150T base board, four interface specific FMC (FPGA Mezzanine Card) daughter cards, a device locked version of the Xilinx® ISE® Design Suite Embedded Edition**, documentation including a Getting Started Guide, Xilinx Platform Cable USB-II, access to evaluation versions of the DisplayPort LogiCORE™ and V-by-One® HS IP cores and pre-validated reference designs.

** ISE® Design Suite Embedded Edition is available with CVK 2.0 Pro only. CVK 2.0 Foundation comes with ISE® Design Suite Logic Edition.

Q: Who makes the CVK 2.0 2.0?

A: The CVK 2.0 2.0 is manufactured and distributed by Inrevium, a Tokyo Electron Device Ltd. Company (TED). The CVK 2.0 is also available from TED distributors in regions outside of Japan. Please see the TED product webpage for more details.

- *English http://www.inrevium.jp/eng/x-fpga-board/tb-6s-CVK 2.0 2.html*
- *Japanese:http://ppg.teldevice.co.jp/m_board/inrevium/b_s6.htm#tb-6s-CVK 2.0 2*

Q: When is the CVK 2.0 available?

A: The CVK 2.0 is open for pre-order through TED's website starting January 6, 2011.

Q: How much is the CVK 2.0 ?

A: The CVK 2.0 will be offered in two configurations:

- *CVK 2.0 Pro (including all FMC daughter cards and a device-locked version of IDS Embedded Edition) has a suggested resale price of $3,395*
- *CVK 2.0 Foundation (including 1.05Gbps LVDS FMC card and an evaluation version of IDS Embedded Edition) has a suggested resale price of $1,395*
- *FMC cards may be purchased individually directly from TED*

Q: Who is the kit designed for?

A: The CVK 2.0 is designed for digital television (DTV) designers and others who are creating video applications like 3D, LED local dimming and 4K2K (e.g. designers of video enhancement algorithms in both video processing and display panels). Additionally, this kit is useful for any customer using or evaluating the Spartan-6 family of FPGAs.

Q: What are the key features of the CVK 2.0?

A: Key Features:

- *Spartan-6 LX150T FPGA*
- *1 x High Pin Count (HPC) FMC connector with up to eight GTP connections*
- *2 x Low Pin Count (LPC) FMC connectors*

- *3 x DDR3 SDRAM (Chip): Micron MT41J64M16LA-187E (2Gbits x 3) 800Mbps*
- *Multiple clock sources*
- *Xilinx Platform Cable USB-II*
- *Evaluation version of DisplayPort LogiCORE IP*
- *Evaluation version of V-by-One HS core*
- *DisplayPort, V-by-One HS, 1.05 Gbps LVDS, HDMI 1.4a (Tx/Rx) FMC daughter cards*

Q: What is included in the CVK 2.0?

A: RoHS compliant Spartan-6 LX 150T evaluation base board

Included FMC Option Boards:
- *LVDS FMC card*
- *V-by-One HS FMC card*
- *DisplayPort FMC card*
- *HDMI 1.4a (Tx/Rx) FMC cards*

ISE Design Suite: Embedded Edition (device-locked for the Spartan-6 LX150T FPGA)**

- *ISE & XPS design suites for FPGA design implementation*
- *Planahead™ Design Analysis Tool – Streamline your design process between synthesis and place-and-route as well as providing intuitive IO planning*
- *Timing Driven Place and Route – Delivers optimal quality of results with advanced implementation algorithms*
- *SmartGuide™ - Delivers industry's fastest incremental implement runtimes*
- *SmartXplorer Technology – Leverage computing resources for optimal quality of results*
- *ISE Simulator – Integrated RTL simulation environment*
- *ChipScope™ Pro and ChipScope Pro Serial IO Toolkit – Perform on-chip design verification for logic and serial connectivity analysis and measurement.*

** ISE® Design Suite Embedded Edition is available with CVK 2.0 Pro only. CVK 2.0 Foundation comes with ISE® Design Suite Logic Edition.

Documentation:

- *Hardware Setup Guide – Easy to follow instructions for getting your development board up and running in minutes so you can begin evaluation*
- *Getting Started Guide – Complete instructions enabling you to evaluate and modify designs included in your evaluation kit*
- *Hardware Users Guide – Detailed guide providing information about the hardware included in your kit*
- *Reference Design and Example User Guide – Instructions for using the included reference design and design examples included in your kit.*

Cables:
Power supply and cables
LVDS Cables
MMCX to SMA connectors
Xilinx Platform Cable USB-II
V-by-One HS cables

Q: Will other FMC daughter cards work with the CVK 2.0?

A: While FMCs developed according to the Xilinx FMC standard (ANSI) VITA 57.1-2008) should work with the CVK 2.0, only the five included FMCs have been validated to work with the CVK 2.0.

Q: What speed grade of Spartan-6 LX150T FPGA is on the board?

A: Kits will ship with -3C speed/temp grade devices.

Q: What is the maximum size of the on-board DDR3?

A: The base board contains DDR3 SDRAM at 800Mbps (3 banks, 16 bit).

Q: What are the configuration options for the CVK 2.0?

A: The CVK 2.0 can be configured either via JTAG or SPI Flash.

Q: What is the CVK 2.0 marketing part number?

A: The ordering part number for the CVK 2.0 is TB-6S-CVK2-PRO (Pro edition) or TB-6S-CVK2-FND (Foundation edition).

Q: The CVK 2.0 ships with Device-Locked ISE Software. Can I use the software for other Xilinx devices?

A: While the included ISE Design Suite software is device-locked to the Spartan-6 LX150T, the included EDK software can be used with any supported Xilinx device.

Q: What is ISE Design Suite Device-Locked?

A: This option has all features of the full version but provides access only to the Spartan-6 LX150T device.

Q: What software do I need to run these reference designs and where do I get it?

A: You need ISE Design Suite Embedded Edition. A full, device-locked, version is included with the Pro version of this kit and an evaluation version is included with the Foundation version.

Q: What other software would be helpful? Why?

A: While ISE software will support all the features of the CVK 2.0 board, there are some additional software tools that may be helpful. These are found in the ISE Logic, Embedded, DSP or System Editions. For more information see: http://www.xilinx.com/tools/designtools.htm

- *Depending on the end application MATLAB from Mathworks™ may be used for video algorithm development. MATLAB is not included in the CVK 2.0*
- *ChipScope Pro™ - an FPGA debug and verification tool. Using the ChipScope Core Generator or Core Inserter, you put ChipScope-specific logic into your design, called a ChipScope core. Then, you can connect to ChipScope cores later using the ChipScope Analyzer software to debug or validate your design*
- *The AccelDSP™ Synthesis Tool - a product that allows you to transform a MATLAB® floating-point design into a hardware module that can be implemented in a Xilinx FPGA. The AccelDSP Synthesis Tool features an easy-to-use Graphical User Interface that controls an integrated environment with other design tools such as MATLAB, Xilinx ISE tools, and other industry-standard HDL simulators and logic synthesizers*
- *System Generator - a DSP design tool from Xilinx that enables the use of The*

Mathworks model-based design environment Simulink for FPGA design. Designs are captured in the DSP friendly Simulink modeling environment using a Xilinx-specific block set. All of the downstream FPGA implementation steps including synthesis and place-and-route are automatically performed to generate an FPGA programming file

- *PlanAhead – a design and analysis software product used to design large FPGA devices. The core technology includes a hierarchical floorplanning tool that can partition the physical design into smaller, more manageable pieces, thus reducing the time to understand, design, verify, and implement the FGPA.*

Q: Where do I get more information?

A: Please check back to the Spartan-6 FPGA Consumer Video Kit product page found at www.xilinx.com/s6CVK 2.0

Questions Related to the FMC daughter cards:

High Speed LVDS FMC

 Q: What is the maximum speed supported on the High Speed LVDS FMC card?

 A: The fastest speed supported is 1.05Gbps for kits containing -3C.

 Q: How many signal pairs/channels supported?

 A: One input one output up to ten pairs for each.

DisplayPort FMC

 Q: Does this support Rx and or Tx on a single FMC?

 A: Yes, the DisplayPort FMC supports both Rx and Tx on the same FMC.

 Q: Does the FMC have VESA specified Rx/Tx receptacles?

 A: Yes.

 Q: What connector does this FMC use on the baseboard?

 A: The high pin count (HPC) connector is used on the CVK 2.0 base board.

 Q: What kind of DisplayPort lane configurations does this FMC support?

 A: The DisplayPort FMC supports x1, x2, x4 lane configurations.

 Q: What link speeds are supported?

 A: 1.65 and 2.7 Gbps.

HDMI FMCs:

 Q: Does the core run natively on the FPGA MGTs?

 A: No, this particular implementation is run in an external PHY.

 Q: What version of HDMI is supported?

A: Version 1.4a is supported on these FMCs.

Q: What color depths are supported?

A: Deep color up to 12-bits per component (36-bit color).

Q: How do you pass audio data to the FPGA or the user?

A: Audio is not supported.

Q: Does this FMC and reference design support HDCP?

A: HDCP is not implemented or supported.

Q: V-by-One HS FMC

Q: What is V-by-One HS?

A: V-by-One HS is an internal display interface that connects a DTV tuner board to the TCON/Panel board. V-by-One HS supports higher data rates using much less wiring pairs than LVDS and can support higher resolution displays, e.g. 4K ultra high definition HDTVs.

Q: How many channels are supported and in what direction?

A: Up to two channels for both Rx and Tx and each channel can be configured to support x1, x2, x4 pairs.

Q: What is the maximum speed the V-by-One HS core can run?

A: Up to 3.125Gbps.

Q: What kind of V-by-One HS lane configurations does this FMC support?

A: The V-by-One HS FMC supports x1, x2, x4 lane configurations.

Questions Related to IP:

Q: Does the kit include IP cores like V-by-One HS, DisplayPort, LVDS and HDMI?

DisplayPort: DisplayPort LogiCORE IP is available from Xilinx; however, users must first fill out a system evaluation license agreement before being granted access to the core via the Xilinx web site.

V-by-One HS: Contact TED for access to the V-by-One HS IP core.

HDMI: HDMI is a free reference design included in the kit to work with the ADI PHY.

High Speed LVDS: LVDS is a free reference design based on XAPP1064 and can be downloaded from the Xilinx website free of charge.

Q: What other resources are available for download?

A: Xilinx application note XAPP495 "Implementing a TMDS Video Interface in the Spartan-6 FPGA" is available for download and includes the following reference design files:

- *DVI Transmitter*

- *DVI Receiver*

- *DVI Common Modules*

- *DVI Evaluation*

Questions Related to Technical Support:

Q: Who should I contact for technical support?

A: Please contact TED at <u>CVK 2.0 -support@teldevice.co.jp</u>.