VIRTEX 6

Virtex-6 LXT FPGAs

Optimized for High-performance Logic and DSP
with Low-power Serial Connectivity
(1.0 Volt, 0.9 Volt)

	Part Number	XC6VLX75T	XC6VLX130T	XC6VLX195T	XC6VLX240T	XC6VLX365T	XC6VLX550T	XC6VLX760
	EasyPath™ FPGA Cost Reduction Solutions (1)	XCE6VLX75T	XCE6VLX130T	XCE6VLX195T	XCE6VLX240T	XCE6VLX365T	XCE6VLX550T	XCE6VLX760
Logic Resources	Slices (2)	11,640	20,000	31,200	37,680	56,880	85,920	118,560
	Logic Cells (3)	74,496	128,000	199,680	241,152	364,032	549,888	758,784
	CLB Flip-Flops	93,120	160,000	249,600	301,440	455,040	687,360	948,480
Memory Resources	Maximum Distributed RAM (Kbits)	1,045	1,740	3,040	3,650	4,130	6,200	8,280
	Block RAM/FIFO w/ ECC (36Kbits each)	156	264	344	416	416	632	720
	Total Block RAM (Kbits)	5,616	9,504	12,384	14,976	14,976	22,752	25,920
Clock Resources	Mixed Mode Clock Managers (MMCM)	6	10	10	12	12	18	18
I/O Resources (4, 5)	Maximum Single-Ended I/O	360	600	600	720	720	1,200	1,200
	Maximum Differential I/O Pairs	180	300	300	360	360	600	600
Embedded Hard IP Resources (6)	DSP48E1 Slices	288	480	640	768	576	864	864
	PCI Express® Interface Blocks	1	2	2	2	2	2	–
	10/100/1000 Ethernet MAC Blocks	4	4	4	4	4	4	–
	GTX Low-Power Transceivers	12	20	20	24	24	36	–
	GTH High-Speed Transceivers	–	–	–	–	–	–	–
Speed Grades	Commercial	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2	-L1, -1, -2
	Industrial	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2	-L1, -1	-L1, -1
Configuration	Configuration Memory (Mbits)	25.0	41.7	58.7	70.4	91.6	137.4	176.3

Package (7)	Area	Available User I/O: SelectIO Pins (4, 5) (GTX Low-power Transceivers, GTH High-speed Transceivers)						
FFA Packages (FF): flip-chip fine-pitch BGA (1.0 mm ball spacing)								
FF484	23 x 23 mm	240 (8, 0)	240 (8, 0)					
FF784	29 x 29 mm	360 (12, 0)	400 (12, 0)	400 (12, 0)	400 (12, 0)			
FF1156	35 x 35 mm		600 (20, 0)	600 (20, 0)	600 (20, 0)	600 (20, 0)		
FF1759	42.5 x 42.5 mm				720 (24, 0)	720 (24, 0)	840 (36, 0)	
FF1760	42.5 x 42.5 mm						1,200 (0, 0)	1,200 (0, 0)

Notes:

1. EasyPath™ solutions provide a conversion-free, low-risk path for volume production.
2. A single Virtex-6 FPGA CLB comprises two slices, with each containing four 6-input LUTs and eight Flip-Flops (twice the number found in a Virtex-4 FPGA slice), for a total of eight 6-LUTs and 16 Flip-Flops per CLB.
3. Virtex-6 FPGA logic cell ratings reflect the increased logic capacity offered by the 6-input LUT architecture.
4. Digitally Controlled Impedance (DCI) is available on I/Os of all devices.
5. I/O standards supported: HT, LVCMOS (2.5V, 1.8V, 1.5V, 1.2V), HSTL I (1.2V,1.5V,1.8V), HSTL II (1.5V,1.8V), HSTL III (1.5V,1.8V), LVDS, Extended LVDS, RSDS, Bus LVDS, LVPECL, SSTL I (1.8V, 2.5V), SSTL II (1.8V, 2.5V), SSTL (1.5V).
6. One system monitor block included in all devices.
7. All products available Pb-free and RoHS-Compliant (FFG).
8. Preliminary product information, subject to change. Please contact your Xilinx representative for the latest information.