Xilinx Club Vivado Seminar 2015 Seoul

Building rapid prototype using Zynq & Xilinx development system
1. Overview

2. About HyBus
   1. History
   2. Business area
   3. Products

3. Feature of Zynq & V210 System
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   2. Compare V210 with Zynq

4. Design of rapid prototype with Zynq

5. Implement the design using Xilinx development environment

6. Conclusion
<table>
<thead>
<tr>
<th>Venture Company</th>
<th>INNO-BIZ</th>
<th>Research Institute</th>
</tr>
</thead>
</table>

**CEO**: Mr. Tae Hyung Kim

**Establish**: Sep. 28. 2001

**Capital**: USD 450,000

**Sales(volume)**: USD 7 Million

**Employee**: 39 people (21 engineer)

**Main Products**:
- Embedded System Solution
- Mobile Display Tester/Jig
- Embedded OEM/ODM(HMI) Service
- Embedded Education Service

- **Develop HMI (Human Machine Interface) OEM product for LSIS**
- **LG Display Mobile LCD in-Line inspection (Long life cycle, pattern)**
- **Export LCD inspection (china BOE, TIANMA)**
- **Develop Medical Device Embedded System Main Platform (Dental, CT, Patient monitor, aesthetic Lager device)**
- **Build Ass’y Line (Line, Chamber, ICT machine, ESD)**

- **Develop AFC (Automatic Fare Collection) System (Korea subway)**
- **Partnership with ORACLE for Embedded DB business**
- **Participating into intelligent U-City project by Ministry of Land, Transport, and Maritime Affairs**
- **Develop U-Sensor Network System (based TI CC2430, 2420)**

- **Certified as INNO-BIZ (Technical Innovation Business Company)**
- **Certified as ISO14001/ISO9001 by Korean Government**
- **Contract of Embedded Training with Samsung Electronics**
- **Contract of Ubiquitous Sensor Network Crossbow Korea Distributor**
- **Established Ubiquitous Sensor Network Research Institute (in Yonsei Univ.)**
- **branch HyBustech (at Deagu city)**

- **Export Embedded Linux Education Kit at 150 Chinese Universities (through Intel China)**
- **Certified as a Venture Company by Korean Government**
- **Established HyBus Research Institute**
- **Distributor Contract in Japan/USA/Taiwan/China/India/Singapore**

- **Established HyBus Co., Ltd. (Sep. 2001)**
- **Released Embedded Linux System DK based Intel SA1110 AP**
- **Released Embedded Linux based MPC850 AP**
- **Contract of Intelligence Information Terminal Development with ETRI**
- **Enrolled as a Member of Korea embedded software industry association**
About HyBus: BUSINESS AREA

1. **Embedded System Business**
   - Embedded Development Tool
   - Embedded CPU Design House
   - Embedded S/W

2. **Programmable FPGA System Business**
   - FPGA OEM/ODM
   - FPGA Design Service
   - ALTERA Board & Design Partner

3. **Customer**
   - Samsung
   - LSIS

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**Embedded Division**

1. **Display PG & Tester**
2. **Display Panel Inspection**
3. **Customer**
   - LG Display
   - Samsung Display
   - TOC, BOE Hydis (China)

**Display Division**

1. **Education Consulting & Tool**
   - Embedded Linux Education kit
   - FPGA Education kit

2. **IoT Platform**
3. **Customer**
   - University
   - Polytechnic college and high school
   - Education center
# Classification by performance

<table>
<thead>
<tr>
<th>List</th>
<th>Low-End</th>
<th>Middle-End</th>
<th>High-End</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core</td>
<td>Cortex-M series Atmega128/256 (Arduino UNO/MEGA)</td>
<td>Cortex-A8 Single core Cortex-A9 MPcore</td>
<td>Cortex-A15 Quad core Cortex-A5x w/ A7 mixed core</td>
</tr>
<tr>
<td>OS</td>
<td>Firmware, RTOS, Arduino</td>
<td>RTOS, Linux, Window, Arduino</td>
<td>Linux, Window, Android</td>
</tr>
<tr>
<td>App</td>
<td>Biological Signal processing (ECG, SpO2, etc) Arduino IoT</td>
<td>Patient Monitor AFC LCD inspection equipment HMI Etc</td>
<td>LCD inspection equipment Education equipment etc</td>
</tr>
<tr>
<td>Products</td>
<td>TI/ST Cortex-M Microcontroller Atmel Atmega series</td>
<td>Samsung s5pv210 Marvell PXA3/2xx series Freescale i.MX2xx series Freescale i.MX6/7 series</td>
<td>Nvidia Tegra series Qualcomm Snapdragon series</td>
</tr>
</tbody>
</table>
# Feature of Zynq & V210 System

## Zynq®-7000 All Programmable SoCs

<table>
<thead>
<tr>
<th></th>
<th>Low-End Portfolio</th>
<th>Mid-Range Devices</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Device Name</strong></td>
<td>Z-7010</td>
<td>Z-7030</td>
</tr>
<tr>
<td><strong>Part Number</strong></td>
<td>XC7Z010</td>
<td>XC7Z030</td>
</tr>
<tr>
<td><strong>Processor Core</strong></td>
<td>Dual ARM® Cortex™-A9 MPCore™ with CoreSight™</td>
<td></td>
</tr>
<tr>
<td><strong>Processor Extensions</strong></td>
<td>NEON™ &amp; Single / Double Precision Floating Point for each processor</td>
<td></td>
</tr>
<tr>
<td><strong>Maximum Frequency</strong></td>
<td>866MHz</td>
<td>Up to 1GHz(1)</td>
</tr>
<tr>
<td><strong>L1 Cache</strong></td>
<td>32KB Instruction, 32KB Data per processor</td>
<td>512KB</td>
</tr>
<tr>
<td><strong>L2 Cache</strong></td>
<td>2656KB</td>
<td></td>
</tr>
<tr>
<td><strong>On-Chip Memory</strong></td>
<td>DDR3, DDR3L, DDR2, LPDDR2</td>
<td>2x Quad-SPI, NAND, NOR</td>
</tr>
<tr>
<td><strong>External Memory Support(2)</strong></td>
<td></td>
<td>RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot</td>
</tr>
<tr>
<td><strong>External Static Memory Support(2)</strong></td>
<td>2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO</td>
<td></td>
</tr>
<tr>
<td><strong>DMA Channels</strong></td>
<td>8 (4 dedicated to Programmable Logic)</td>
<td>16 Interrupts</td>
</tr>
<tr>
<td><strong>Peripherals</strong></td>
<td>2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO</td>
<td>2x AXI 32b Master, 2x AXI 32b Slave</td>
</tr>
<tr>
<td><strong>Peripherals w/ built-in DMA(2)</strong></td>
<td>2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO</td>
<td>4x AXI 64b/32b Memory</td>
</tr>
<tr>
<td><strong>Security(3)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Processing System to Programmable Logic Interface Ports</strong> (Primary Interfaces &amp; Interrupts Only)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 7 Series Programmable Logic Equivalent

<table>
<thead>
<tr>
<th>Logic Cells (Approximate ASIC Gates(4))</th>
<th>Artix®-7 FPGA</th>
<th>Artix-7 FPGA</th>
<th>Artix-7 FPGA</th>
<th>Kintex®-7 FPGA</th>
<th>Kintex-7 FPGA</th>
<th>Kintex-7 FPGA</th>
<th>Kintex-7 FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>28K (~430K)</td>
<td>74K (~1.1M)</td>
<td>85K (~1.3M)</td>
<td></td>
<td>125K (~1.9M)</td>
<td>275K (~4.1M)</td>
<td>350K (~5.2M)</td>
<td>444K (~6.6M)</td>
</tr>
<tr>
<td>Look-Up Tables (LUTs)</td>
<td>17,600</td>
<td>46,200</td>
<td>53,200</td>
<td>78,600</td>
<td>171,900</td>
<td>218,600</td>
<td>277,400</td>
</tr>
<tr>
<td>Flip-Flops</td>
<td>35,200</td>
<td>92,400</td>
<td>106,400</td>
<td>157,200</td>
<td>343,800</td>
<td>437,200</td>
<td>554,800</td>
</tr>
<tr>
<td>Total Block RAM (# 36Kb Blocks)</td>
<td>2.1Mb (60)</td>
<td>3.3Mb (95)</td>
<td>4.9Mb (140)</td>
<td>9.3Mb (265)</td>
<td>17.6Mb (500)</td>
<td>19.1Mb (545)</td>
<td>26.5Mb (755)</td>
</tr>
<tr>
<td>Programmable DSP Slices (18x25 MACCs)</td>
<td>80</td>
<td>160</td>
<td>220</td>
<td>400</td>
<td>900</td>
<td>900</td>
<td>2,020</td>
</tr>
<tr>
<td>Peak DSP Performance (Symmetric FIR)</td>
<td>100 GMACs</td>
<td>200 GMACS</td>
<td>276 GMACs</td>
<td>593 GMACs</td>
<td>1,334 GMACs</td>
<td>1,334 GMACs</td>
<td>2,622 GMACs</td>
</tr>
<tr>
<td>PCI Express® (Root Complex or Endpoint)</td>
<td>Gen2 x4</td>
<td>Gen2 x4</td>
<td>Gen2 x8</td>
<td>Gen2 x8</td>
<td>Gen2 x8</td>
<td>Gen2 x8</td>
<td></td>
</tr>
<tr>
<td>Analog Mixed Signal (AMS) / XADC(2)</td>
<td>AES</td>
<td>SHA 256b</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. 1 GHz processor frequency is available only for -3 speed grades for devices in flip-chip packages. Please see the data sheet for more details.
3. Security block is shared by the Processing System and the Programmable Logic.
4. Equivalent ASIC gate count is dependent on the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.

* In the Xilinx doc excerpt
### Feature of Zynq & V210 System

#### Compare V210 with Zynq

<table>
<thead>
<tr>
<th>V210 Spec</th>
<th>Zynq Spec</th>
<th>Compare</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cortex-A8 Single core 1GHz - 32/32KB I/D Cache, 512KB L2 Cache</td>
<td>Cortex-A9 Single/Dual core up to 1GHz - 32/32KB I/D Cache, 512KB L2 Cache</td>
<td>Better</td>
</tr>
<tr>
<td>2D/3D Graphic Accelerator</td>
<td>None</td>
<td>Used 3\textsuperscript{rd} party IP</td>
</tr>
<tr>
<td>USB 2.0 OTG</td>
<td>USB 2.0 OTG x2</td>
<td>Almost same</td>
</tr>
<tr>
<td>SD/SDIO/HS-MMC x4</td>
<td>SD/SDIO/HS-MMC x2</td>
<td>Almost same</td>
</tr>
<tr>
<td>LPDDR1/2, DDR2</td>
<td>LPDDR2/3, DDR2/3</td>
<td>Better</td>
</tr>
<tr>
<td>NAND/OneNAND/NOR</td>
<td>QSPI/NAND/NOR</td>
<td>Almost same</td>
</tr>
<tr>
<td>10CH 12bit ADC</td>
<td>17CH 12bit ADC x2</td>
<td>Better</td>
</tr>
<tr>
<td>None</td>
<td>1Gbit Ethernet</td>
<td>Better</td>
</tr>
<tr>
<td>MIPI-DSI/CSI</td>
<td>None</td>
<td>Used 3\textsuperscript{rd} party IP</td>
</tr>
<tr>
<td>HDMI TX</td>
<td>None</td>
<td>Used 3\textsuperscript{rd} party IP</td>
</tr>
<tr>
<td>Many peripheral</td>
<td>FPGA</td>
<td>?</td>
</tr>
</tbody>
</table>
Accelerated Design Productivity

**Reduced Time To Market**
- Fixed processor system with large set of built in peripherals
- Standardizing on AMBA-4 AXI enhances portability of IPs
- Scalable optimized architecture for IP re-use; AXI interfaces for plug & play IP
- Accelerate development with targeted design platforms

**Increased Time In Market**
- Software and hardware re-programmability
- Field upgradable
- Address Processor/ASSPs short shelf life

* In the Xilinx doc excerpt

* Feature of Zynq & V210 System

* Extended Product life

* In the Xilinx doc excerpt
Why is Zynq?

- Similar CPU
- Similar S/W development environment
- One chip solution
- Long period of EOL

How effectively the Zynq system will be able to replace the V210 system?

One solution is rapid prototype test.
Main concept

1. Find classified AP (ex Samsung V210) products that can be replaced by Zynq.

2. Fix the specification of the PS area is used in common.
   - Basic development environment (include Linux) can be development without significant change even if the PL is changed
   - Linux hardware development and porting, a development environment that can save setup time.

3. The PL area is used to change to suit your needs.
   - Designed to take full advantage of the Xilinx AXI-IP.
   - In addition to the development of PL added to the area do not need to set up a new Linux environment and development
   - PL area validation verifies fast as bare-metal c code.
Main concept

1. Find classified AP (ex Samsung V210) products that can be replaced by Zynq.
Main concept

2. Fix the specification of the PS area is used in common.
   - Basic development environment (include Linux) can be development without significant change even if the PL is changed
   - Linux hardware development and porting, a development environment that can save setup time.
   - Fixed PS area
     - ARM Cortex-A9 Core
     - DDR3 1GB x32
     - SD/MMC
     - USB 2.0 OTG
     - 1Gbit Ethernet
     - I2C/UART/SPI/GPIO
3. The PL area is used to change to suit your needs.
   - Designed to take full advantage of the Xilinx AXI-IP.
   - In addition to the development of PL added to the area do not need to set up a new linux environment and development.
   - PL area validation verifies fast as using bare-metal c code.
Main concept

3. The PL area is used to change to suit your needs.
   - Exam 1: AFC System PL spec
     - RGB x1 (Used Xilinx Video IP)
     - UART x8 (Used Xilinx UART IP)
     - GPIO x8 (Used Xilinx GPIO IP)
     - PWM x2 (Used Xilinx Timer IP)
3. The PL area is used to change to suit your needs.

- Exam 2: Display Inspection Equipment PL spec
  - MCU System (Used Xilinx MicroBlaze IP)
  - SPI (Used Xilinx QSPI IP)
  - UART (Used Xilinx UART IP)
  - RGB x2 (Used Xilinx Video IP)
  - GPIO x29 (Used Xilinx GPIO IP)
  - PWM x4 (Used Xilinx Timer IP)
Main concept

3. The PL area is used to change to suit your needs.
   - Exam 3: Arduino spec
     - DPRAM for IPC (Used Xilinx IP)
     - Arduino System (Used FPGArduino platform)
       - FPGArduino platform website: http://www.nxlab.fer.hr/fpgarduino/
     - Arduino UNO/MEGA port
Implement the Design: Exam.1 AFC System

Used Vivado block design tool
Implement the Design: Exam.1 AFC System

Video IP block

Used Vivado block design tool
Implement the Design: Exam.2 Display

Used Vivado block design tool
Implement the Design: Exam.2 Display

- Used Xilinx SDK & Bare metal library

Debug Console MSG.
- Used FPGArduino platform
- The FPGArduino platform is BSD or MIT license.
- The FPGArduino provides **pre-built software tools** and **FPGA configuration bitstreams** which transform popular FPGA development boards into microcontroller systems programmable using the intuitive **Arduino** development environment.

* FPGArduino platform website: [http://www.nxlab.fer.hr/fpgarduino/](http://www.nxlab.fer.hr/fpgarduino/)
**Conclusion**

**Development and duration**

- **AFC System**: 7 days!
- **Display**: 14 days!
- **Arduino**: 1 day!

**Proto-type Board**
- HyBus DevKit
- ZedBoard
- ZC706/ZC702
- Etc

**Design flow**
- Takes time
- Must
- Option
- Xilinx Tools
- Dev. Board

**3rd Party IP verification & integration**
- Xilinx Simulation
- Xilinx Create and Package IP Tool

**Architecture draw & Implement**
- Vivado block design

**Bare Metal C code verification**
- Xilinx SDK
- Bare metal library

**The principal & atomic problem debugging & analysis**
- Vivado Implementation (Planahead) & ChipScope

**Verification on Linux-based applications**
- Xilinx Linux BSP

**Development and duration**

- AFC System: 7 days!
- Display: 14 days!
- Arduino: 1 day!
Thank you

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Q&A