Xilinx Medical Clinical Solutions

Xilinx provides compressive solutions for medical devices ranging from small FPGAs to complete integration with our Zynq All Programmable SoCs. The solutions include a wide range of leading devices of FPGAs and SOCs, easy-to-use development tools, drop-in and customizable IP, and risk mitigation techniques. All of our solutions are developed while maintaining the highest medical device standards for regulatory compliance, device longevity, and decreased risk.
### Device Table

<table>
<thead>
<tr>
<th>Device Name</th>
<th>Product #</th>
<th>Logic</th>
<th>CPU</th>
<th>MHz</th>
<th>Package Size</th>
<th>IO Counts</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spartan®-6</td>
<td>LX9, LX16,</td>
<td>9kLC – 75kLC</td>
<td>Microblaze</td>
<td>80MHz</td>
<td>8x8 – 19x19</td>
<td>132…408</td>
</tr>
<tr>
<td></td>
<td>LX25, LX45,</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LX75</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Artix®-7</td>
<td>A15T – A75T</td>
<td>16kLC – 75kLC</td>
<td>Microblaze</td>
<td>100MHz</td>
<td>10x10 – 17x17</td>
<td>250…300</td>
</tr>
<tr>
<td>Zynq® All Programmable SoC</td>
<td>7010 – 7045</td>
<td>28kLC – 144kLC</td>
<td>Dual Cortex™ A9 + Neon</td>
<td>1Ghz</td>
<td>13x13 – 19x19</td>
<td>PL: 54…200 PS: 32 or 54</td>
</tr>
<tr>
<td>Zynq Ultrascale™ MPSoC</td>
<td>ZU6EG</td>
<td>376kLC</td>
<td>Quad Cortex A53 + Dual Cortex R5</td>
<td>1.3Ghz</td>
<td>31x31</td>
<td>524</td>
</tr>
</tbody>
</table>

### Selected Development Kits

Development boards and kits from Xilinx and Xilinx Alliance Members allow customers to explore the advantages of Xilinx FPGA and All Programmable SoCs for medical clinical applications. SOM and modules accelerate the prototyping and deploying in market.

<table>
<thead>
<tr>
<th>Product Picture</th>
<th>Features</th>
<th>Cost</th>
<th>Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>SP601</td>
<td>Spartan-6 FPGA Evaluation kit featuring the Spartan-6 XC6SLX16 device with 15k LC</td>
<td>$295</td>
<td>Xilinx or Avnet</td>
</tr>
<tr>
<td>AC701</td>
<td>Artix-7 FPGA Evaluation kit featuring the XC7A200T FPGA with 215k LC</td>
<td>$1,295</td>
<td>Xilinx or Avnet</td>
</tr>
<tr>
<td>ZC702</td>
<td>Zynq-7000 All Programmable SoC Evaluation Kit featuring the XC7020 SoC FPGA, dual ARM Cortex A9 CPUs with Artix-7 FPGA with 85k LC</td>
<td>$895</td>
<td>Xilinx or Avnet</td>
</tr>
<tr>
<td>KC705</td>
<td>Kintex-7 FPGA KC705 Evaluation Kit featuring the Kintex-7 325T FGPA with 326kLC</td>
<td>$1,695</td>
<td>Xilinx or Avnet</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Partner Development Kits</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Kit Med 7015</strong></td>
</tr>
<tr>
<td><strong>Kit Med 7030</strong></td>
</tr>
<tr>
<td><strong>Xilinx OZ745 Dev Platform</strong></td>
</tr>
</tbody>
</table>

### SOMs

- **PicoZed MicroZed MicroZed-SBC**
  Zynq-7000 based modules, various form factors, compatible migration between different device sizes
  Contact Avnet
- **SOM-MIAMIXC7015**
  Zynq-7015 based module from Topic Embedded Products, for Medical Devices, ISO13485 Certified
  $580
- **SOM-MIAMIXC7030**
  Zynq-7030 based module from Topic Embedded Products, for Medical Devices, ISO13485 Certified
  $718
### IP Libraries for Medical Clinical

Xilinx and Xilinx’s Alliance Members offer a wide variety of IP cores and functions that accelerate the design of Medical devices on Xilinx FPGA and All Programmable SoCs.

<table>
<thead>
<tr>
<th>Xilinx</th>
<th>Reference Designs</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Multiprotocol Solutions</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Functional Safety</strong></td>
<td>Functional Safety Data Package for ISE1.47 and devices to accelerate and simplify Functional Safety Certification following the IEC 61508 standard</td>
</tr>
<tr>
<td><strong>HDMI</strong></td>
<td>Xilinx HDMI reference design is to connect Video Source and Display and features support for HDMI v1.0 - 2.0</td>
</tr>
</tbody>
</table>
| &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &nbsp; &nbsp; &nbsp; | &n
**Partner IP**

**Qdesys Motor Control IP**

**Electric Drive IP**

- Suite of IP enabling fast FOC implementation in FPGA
  - Sensorless FOC
  - Multi-Axis control for 1-, 2-, 3-, 4-, channel Servo Drives
  - 20 Full featured motor control IP functions
    - CLARKE, PARK, PID, ATAN2, SIN/COS, SMO, SVM, RPFM.
    - IIR (minimal phase) filters
    - Poly-phase filters for Sigma-Delta sampling frequency improvement
  - Sinc3 Filters for current acquisition via Sigma-Delta ADC
  - Data-logging and Analysis
  - Control and sequencing
  - Drivers supporting: Bare Metal, Linux, QNX on ARM® Cortex™ A9 on Zynq

**Motor Control Manager GUI**

The MCM GUI program is a user application program to communicate with the motor control application in a Zynq AP SoC device. Supports API of The Mathworks, SciLab, Visual Basic, C, Labview.

**Topic Embedded Products**

**Dyplo**

Dyplo is a middleware that allows software developers the ability to quickly connect various processing units and perform dynamic real-time process acceleration in FPGA fabric.

- Sensorless FOC
- The next step in data and signal acceleration
- Simplified Zynq™ development
- Out-of-the-box integration of CPU & FPGA
- Proven development time reduction of 30%
- FPGA programming made software-friendly
- Runtime re-use of FPGA fabric
- Plug-in IP blocks, zero integration effort
- Architectural freedom

**Omnitek**

**OmniTek Scalable Video Processor**

A highly configurable set of IP blocks and optional features that together provide a powerful range of tools for multi-video format conversion and image enhancement for video formats up to 60Hz Ultra HD, with 120Hz Ultra HD output as a further option.

- Asynchronous I/O timing
- Cadence detector
- Chroma resampler
- Cropper
- Deinterlacer
- Detail Enhance
- Format Converter
- Frame Synchronizer
- Frame rate up to 120Hz
- Motion and Low-angle adaptive deinterlacing
- Resizer (scaler)
- Video Graphic Overlay support

**HMI**

**Xylon Operator Panel**

IP and reference design for Xilinx Zynq devices implementing an operator panel that enables interaction between humans and machines. Human Machine Interface in 2D/2.5D and 3D (HMI)
Reference Designs

**Topic Medical Development Kit / Reference Design**

The Development Kit provides you with a complete system to start developing your embedded software application on a Xilinx Zynq SoC and seamlessly integrate your FPGA and CPU functionality. Reference designs in this kit include, Signal Filtering for ECG, MRI Video Processing and more. Demos and designs include, pre-installed linus BSP and Dyple®, the operating system extension for FPGA and CPU integration. Kit also has 10in touch screen and 24 channels of ADCs for Biotelemetry.

**Omnitek OZ745 Video Development Platform**

Xilinx RTVE 3.1 Reference Design

The OZ745 board is delivered with an evaluation reference design (ERD) which recognizes and displays SDI, HDMI and analogue video inputs and displays a test pattern on the SDI and HDMI video outputs. The ERD provides a convenient way to test many of the board’s features and gives a skeleton design upon which users can build their own firmware and software applications. Source is provided to allow initial designs to be built up.

The Reference Design has the OmniTek Scalable Video Processor IP (OSVP) at its core and performs de-interlace and resize of four video inputs, and composites them onto the video output. Control software runs on the ARM processor, which uses a Linux build with Qt graphics support. An OmniTek 2D Graphics IP core provides graphics acceleration. The control software generates a web page which can be hosted locally and composited over the video on the SDI, HDMI or LVDS flat panel display output and controlled via mouse and keyboard. Alternatively, the UI may be hosted on a remote web browser.

The diagram below illustrates the OZ745 OSVP Reference design which runs under Linux and makes use of the Zynq ARM CPU on Omnitek’s OZ745 Video Development kit.

**Xilinx/Qdesys 3-Level Silicon Carbide Reference platform**

Basic building blocks:
- Laptop size 10KW 3-Level TNPC (or NPC2 or also 3LT2C) Silicon Carbide Inverter
- Zynq-7000 MicroZed and PicoZed SOM
- RP FM Modulation drives 12 SiC switches allowing extremely low EMI and very low THD
- 6 Temperature probes can be connected to the carrier to monitor the inverter dissipation
- Hardware-in-the-Loop Zynq 1 Gigabit hardened Ethernet port is used for gateway and control connection toward the National instruments lab-studio graphical user interface, residing in a PC. Lab-view, Matlab, SciLab, Microsoft dot net, C ++, and Visual Basic for applications can also communicate by using this interface allowing investigation and further development
- Complete FOC (Field Oriented Control) and SFOC (Sensorless Field Oriented Control) is available in the reference design
- ISM-NET networking module allows connectivity for EtherCAT®, PowerLink, Profinet, Ethernet/IP, and all the major industrial networking protocols to control the reference design

**Avnet/Xilinx Zynq-7000 All Programmable SoC/Analogue Devices Intelligent Drives Kit**

Basic building blocks:
- Analog Devices ADFMCMOTCON1- EBZ module
- Drive BLDC / PMSM / Brushed DC / Stepper motors up to 48 V @ 18 A
- AD7401A Isolated 20 MHz Sigma-Delta modulator
- AD8251 Programmable Gain Amplifiers for full-scale current measurement
- ADuM5000/7640 power and digital signal isolation
- Dual Gigabit IEE1588 Ethernet PHYs for high speed industrial communication
- Xilinx XADC interface for sensored or sensoreless position measurement
- The Mathworks Simulink HW/SW Codesign Reference design
- **HDL Reference design** (ADI)
Xilinx Training

**Industrial Motor Control Using FPGAs and SoCs**
Learn how to implement motor control solutions using Xilinx All Programmable devices. This course requires basic knowledge of motor control; this comprehensive course covers motor control concepts; identifies the challenges in typical motor control solutions such as brushless direct current (DC), stepper, and permanent magnet synchronous motor (PMSM) motor control solutions and then demonstrates motor control techniques in Xilinx FPGAs and SoCs with the help of IPs provided by QDESYS.

**Dyplo Introduction Hands-On**
In this 1-day hands-on workshop you will learn how to get started using Dyplo®, preparing you for practical project readiness. Step by step you will be guided through the process of building a complete demonstration application using a Zynq® based Miami System on Module. At the end of the day you will be able to build your own application and get a head-start in maximising your design choices.

If you want to join the Dyplo® Introduction workshop to learn how to get started with Dyplo® you can register on this page for one of the available dates.

Design Tools & Methodologies

**SDSoC Development Environment**
The SDSoC™ development environment provides a greatly simplified ASSP-like C/C++ programming experience including an easy to use Eclipse IDE and a comprehensive design environment for heterogeneous Zynq® All Programmable SoC and MPSoC deployment. Complete with the industry's first C/C++ full-system optimizing compiler, SDSoC delivers system level profiling, automated software acceleration in programmable logic, automated system connectivity generation, and libraries to speed programming.

**Vivado Design Suite**
The Vivado® Design Suite delivers a SoC-strength, IP-centric and system-centric, next generation development environment that has been built from the ground up to address the productivity bottlenecks in system-level integration and implementation.

**Digital Design Using Vivado IPI**
Xilinx has developed a basic functional IP blocks library which can be used to create digital designs in a schematic view. The tutorial and laboratory exercises are created and available for use with the Xilinx University Program supported boards.

**Xilinx System Generator**
System Generator for DSP™ is the industry's leading high-level tool for designing high-performance DSP systems using Xilinx All Programmable devices. With System Generator for DSP, create production-quality DSP algorithms in a fraction of time compared to traditional RTL.

**MathWorks**
In recent years, software modeling and simulation tools, such as Simulink from MathWorks, have allowed model-based design to evolve into a complete design flow – from model creation to implementation.

Partner Profiles

**NI**
National Instruments transforms the way engineers and scientists around the world design, prototype, and deploy systems for test, control, and embedded design applications.

**Omnitek**
OmniTek is the product division of Image Processing Techniques Ltd., a leading UK consultancy company providing electronics design services to the broadcast, post-production and professional AV industries since 1998.

**Qdesys**
QDESYS designs, develop and produces industrial embedded systems. Specialized in motor control, control systems, and industrial networking. QDESYS produces original design and custom designs.

**Topic Embedded Systems**
Topic is Premier Partner of Xilinx. Topic Products offers an ecosystem of embedded acceleration solutions consisting of System on Modules (Miami), carrier boards (Florida), development kits, IP blocks (IPware), Design Services (Dsign) and a unique Dynamic Process Loader (Dyplo).

**Xylon**
Xylon is an electronic company focused on design of optimized IP cores for Xilinx All Programmable devices and design services that lower production costs and improve efficiency of electronics designers.