The Ultimate System Integration Platform

Low-Power Transceivers
Built-in PCIe™ & Ethernet

65nm ExpressFabric™

XILINX®
THE WORLD’S FIRST
65nm FPGA

One Family—Multiple Platforms

The Virtex™-5 family of FPGAs offers a choice of four new platforms, each delivering an optimized balance of high-performance logic, serial connectivity, signal processing, and embedded processing.

Virtex-5 LXT FPGAs, optimized for high-performance logic with serial I/O, expand the Virtex-5 family offering, joining the Virtex-5 LX platform devices released earlier. Discover how this new family delivers even higher performance, lower power, and lower system cost than previous-generation Virtex-4 FPGAs.

Meet Your Performance Targets Easily

- Achieve a 30% performance gain with new ExpressFabric™ technology
- 550 MHz clocking technology and performance-tuned IP blocks
- 1.25 Gbps LVDS I/O: up to 600 pin pairs

Optimize I/O Bandwidth, Power and Cost with Easy-to-Use High-Speed Serial Solutions

- RocketIO™ GTP transceivers deliver 100 Mbps – 3.2 Gbps serial connectivity
- First FPGA with hardened PCI Express endpoint blocks and Tri-mode Ethernet MACs
- Lowest power in the industry: less than 100 mW per transceiver at 3.2 Gbps
- Advanced equalization techniques to drive backplanes beyond 40"
- Protocol solutions kits accelerate development

Beat Your Power Budget while Maximizing Performance

- 35% lower dynamic power with 65nm ExpressFabric and power-saving IP blocks
- Reduce serial connectivity power consumption: RocketIO GTP transceivers consume less than 100 mW at 3.2 Gbps
Solve Signal Integrity Challenges and Simplify PCB Layout

- Second-generation sparse chevron packaging delivers SSO noise and crosstalk benefits, essential for reliable operation of high-bandwidth parallel interfaces (e.g. memories)
- On-substrate bypass capacitors and a unique pinout simplify PCB design, improve power integrity, and reduce system cost
- Built-in serial connectivity reduces pin/trace count and eliminates parallel interface design challenges

Reduce Cost through System Integration with a Selection of Optimized Platform FPGAs

- Choose a smaller device: 65nm process shrinks die size and new 6-input LUT increases utilization and efficiency
- Meet aggressive performance targets in the least expensive speed grade
- Reduce part count with built-in, low-power transceivers
- Increase logic efficiency with built-in PCI Express® endpoint and Ethernet MAC blocks
- Select smaller heat sinks, fans, and power supplies enabled by reduced power consumption
- Bring your product to market faster with proven development and verification tools
- Reduce component cost in volume production with Virtex-5 EasyPath™ FPGAs

Finish Your Design Ahead of Schedule

- Achieve FPGA performance goals quickly with ISE™ Fmax technology and PlanAhead™ design analysis tools
- Design faster and reduce risk with over 225 pre-verified IP cores
- Reduce debug cycle time with the real-time verification capabilities of ChipScope™ Pro tools
- Build complete embedded processing systems with Platform Studio and Embedded Development Kit
- Implement DSP algorithms in custom-configured hardware with the AccelDSP™/MATLAB™ tool flow
- Accelerate product development with online resources, training courses, and premium support services
- Get Xilinx Productivity Advantage (XPA) bundles of software, education, support services, and IP cores
- Augment your development team with a worldwide network of Xilinx Design Service (XDS) and partner experts

VIRTEX-5
EASYPATH™ FPGAs

The conversion-free cost-reduction path for volume production.

- EasyPath FPGAs reduce component cost by 30–75% with no risk of conversion, no hidden costs
- Enjoy unprecedented flexibility and fastest turn-around times
65nm ExpressFabric™ Technology
Achieve highest performance, most efficient utilization on 65nm triple-oxide process
- 30% higher speed, 35% lower dynamic power, and 45% less area than the previous generation
- Industry's first LUT with six independent inputs for fewer logic levels
- Flexible LUTs are configurable as logic, distributed RAM or shift registers
- Advanced diagonally symmetric interconnect enables shortest, fastest routing
- From 30,000 to 330,000 logic cells for system-level integration

550 MHz Clocking Technology
Achieve highest speeds with high-precision, low-jitter clocking
- 12 DCMs provide phase control of less than 30 ps for better design margin
- 6 PLLs reduce reference clock jitter by more than 2x
- Differential global clocking ensures low skew and jitter

The Right Memory for Any Application
Distributed RAM—Small
- Build 256-bit memory per CLB
- 64 bits per LUT

550 MHz, 36 Kbit Block RAM—Medium
- Configure Block RAM as multi-rate FIFO
- Built-in ECC for high-reliability systems
- Automatic power conservation circuitry

389 Gbps External Memories—Large
- ChipSync™ technology for reliable interfaces
**Ethernet Media Access Controller:**
10/100/1000 Mbps

Connect to the Internet via an integrated tri-mode EMAC
- UNH-verified compliance
- Built-in hard IP frees user logic resources and reduces power
- Four Ethernet MAC blocks on every Virtex-5 LXT device

**RocketIO™ GTP Transceivers:**
100 Mbps–3.2 Gbps

Implement serial protocols at lowest power
- Flexible SERDES supports multi-rate applications
- Designed to work with integrated PCIe™ and EMAC blocks
- 77% lower power consumption: <100 mW at 3.2 Gbps

**Sparse Chevron Packaging Technology**

Keep system noise under control and simplify PCB layout
- Unique PWR/GND pin pattern minimizes crosstalk and reduces PCB layers
- On-substrate bypass capacitors shrink PCB area

**PCI Express® Endpoint Block:**
1/2/4/8-lane

Built-in support for ubiquitous serial connectivity standard
- PCI SIG-verified compliance (on integrators list)
- Works with RocketIO GTP transceivers to deliver full PCIe endpoint function
- Built-in hard IP frees user logic resources and reduces power
1.25 Gbps SelectIO™ with ChipSync™ Source-Synchronous Technology

Implement industry-standard and custom protocols
- Simplify board design with built-in input delay and new output delay circuits that compensate for unequal trace lengths
- Adaptive delay setting recalibrates automatically to compensate for changing operating conditions
- Interface to popular standards with 1.25 Gbps differential and 800 Mbps single-ended I/O
- Digitally controlled impedance reduces component count and board size

550 MHz DSP48E Slice

Create high-performance DSP systems
- New 25 x 18 multipliers enable single-precision floating-point math and wide filters with fewer slices
- Configurable for DSP, arithmetic, and bit-wise logic
- Enables efficient adder-chain architectures
- 40% lower power consumption: 1.38mW/100MHz at a 38% toggle rate

Enhanced Configuration and Bitstream Protection

Reduce system cost, increase reliability, and safeguard your design
- Configure with commodity SPI and parallel flash memory
- Easier partial reconfiguration and smaller frame size
- Greater reliability for in-system reconfiguration with multi-bitstream management
- Protect your designs with 256-bit AES (Advanced Encryption Standard) security
Implement Parallel Networking and System Interface Standards

SelectIO circuitry, combined with pre-verified IP cores, make it easy to support all popular interface standards
- 1.25 Gbps LVDS, 800 Mbps single-ended
- Interface or bridge to virtually any external component
- Support multiple electrical standards in the same device with 35 individually configurable I/O banks
- Design with PCI, RapidIO, XSBII, SPI4.2, and more
- Configure I/Os to support HSTL, LVDS (SDR and DDR), and more, at voltages from 1.2V to 3.3V

Accelerate Development with Complete Serial Solutions

Build chip-to-chip, board-to-board, and box-to-box applications quickly and easily
- Obtain assured compliance with popular standards
- Reduce design time with integrated interface blocks and pre-verified IP
- Implement custom solutions
- Reduce pin/trace count to simplify board design and reduce manufacturing cost
- Start designing with ready-to-use solution kits including protocol-specific characterization reports, boards, and simulation models

Simplify Source-Synchronous Interfacing

ChipSync technology in every SelectIO block provides precise control over critical timing for high-performance source-synchronous interfaces
- Achieve performance targets and simplify PCB layout with flexible per-bit deskew
- Synchronize incoming data to FPGA internal clock with built-in Serializer/Deserializer

Build Highest-Bandwidth Memory Interfaces

ChipSync technology and the Memory Interface Generator tool make it easy to build reliable interfaces to the latest high-performance memories, including:

<table>
<thead>
<tr>
<th>Memory Interface</th>
<th>Data Rate (Mbps)</th>
<th>Data Width (# of bits)</th>
<th>Bandwidth (Gbps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR SDRAM</td>
<td>400</td>
<td>576</td>
<td>230</td>
</tr>
<tr>
<td>DDR2 SDRAM</td>
<td>667</td>
<td>576</td>
<td>384</td>
</tr>
<tr>
<td>QDR II SRAM</td>
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<td>2 x 324</td>
<td>389</td>
</tr>
<tr>
<td>RLDRAM II</td>
<td>600</td>
<td>648</td>
<td>389</td>
</tr>
</tbody>
</table>

Bridge Protocols

Protect your investment by interfacing easily to legacy ASSPs or ASICS
- Reduce design time with built-in support for PCI Express and Ethernet
- Implement other popular protocols with pre-verified IP
- Connect external peripheral components to any processor with standards-compliant I/O
EVERY PLATFORM

Implement PCI Express with Reduced Cost, Power, and Complexity

Minimize design risk with hardened PCIe blocks to connect to next-generation graphics, storage, networking, and I/O devices

- Integrate multiple functions into a single PCIe-enabled FPGA
- Preserve software investment and extend infrastructure life with scaleable bandwidth (x1, x2, x4, x8)
- Re-target designs without changing your PCIe interface implementation as your project evolves

EVERY PLATFORM

Accelerate development with ready-to-use solution kits

- Protocol compliance reports
- Device characterization
- Reference designs
- Development boards
- Simulation models
- Pre-verified IP
- Development tools
- User documentation
- Partner solutions

PCI Express Design Example: High-End Desktop/Server System
Create Efficient, High-Performance DSP Systems

Increase DSP algorithm performance
- Implement video compression, digital up/down conversion, single instruction multiple data (SIMD) functions, and filters efficiently
- DSP processor acceleration with FPGA pre/post-processing
- ExpressFabric enables fine granularity data shifting and control, and small bit-width arithmetic functions
- Dynamically control DSP48E to create more than 40 functions, such as Mult/MAC, Add, and Mux, without consuming other resources
- Build filters with cascadable DSP48E slices that eliminate the performance bottlenecks imposed by traditional adder trees

RocketIO GTP transceivers enable efficient data transport when using Virtex-5 LXT FPGAs for DSP acceleration
- Interface to latest DSP processors with RapidIO and free up bandwidth on system memory bus
- Ideal for HD video, baseband co-processing in wireless base stations, and adding image processing acceleration to surveillance cameras and remote servers

Integrate a Soft Embedded Processor

Embedded development tools and IP make it easy to build a processor subsystem tailored to your requirements
- Start with the MicroBlaze™ soft processor core
- Add an IBM CoreConnect™ bus for flexible connectivity and guaranteed performance
- Connect a custom hardware accelerator through the fast simplex link (FSL)
- Complete your subsystem with pre-verified peripheral IP cores
### TAKE THE NEXT STEP

Visit us online at [www.xilinx.com/virtex5](http://www.xilinx.com/virtex5)

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**VIRTEX-5 FAMILY**

<table>
<thead>
<tr>
<th>Package</th>
<th>Area</th>
<th>IO MGT</th>
<th>CLK Resources</th>
<th>IO Resources</th>
<th>Clock Resources</th>
<th>Mem Resources</th>
<th>Core Area</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1200</td>
<td>640</td>
<td></td>
<td>640</td>
<td></td>
<td>640</td>
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<td></td>
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**VIRTEX-5 LX PLATFORM**

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<tr>
<td>LX110T</td>
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<td>LX330T</td>
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**VIRTEX-5 LXT PLATFORM**

<table>
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<td>LX45</td>
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<tr>
<td>LX85T</td>
<td>540</td>
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<tr>
<td>LX110T</td>
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<tr>
<td>LX330T</td>
<td>32</td>
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<tr>
<td>LX330T</td>
<td>16</td>
</tr>
</tbody>
</table>

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**Notes:**
1. EasyPath™ solutions provide a conversion-free cost reduction path for volume production.
2. A single Virtex-5 CLB comprises two slices, with each containing four Real 6-input LUTs and four Flip-Flops (twice the number found in a Virtex-4 slice), for a total of eight 6-LUTs and eight Flip-Flops per CLB.
3. Virtex-5 logic cell ratings reflect the increased logic capacity offered by the new Real 6-input LUT architecture.
4. I/O Packages: flip-chip fine-pitch PGA (1.00-mm ball spacing).
5. Number of available RocketIO™ multi-gigabit transceivers (MGTs) for each device/package combination shown in parentheses.
6. I/O standards supported: HT, LVDS, LVCSSST, KDS, BEVD, LEVD, LVCSSST2, LVCSSST22, LVCSSST218, LVCSSST380, LVPECL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVTTL, PCI33, PCI66, PCI-X, SSTL, SSTL1, SSTL2, SSTL22, SSTL18, SSTL15, SSTL12V8, SSTL18V8, SSTL22V8, SSTL25V15, SSTL27V15, SSTL30V18, SSTL35V18, SSTL42V18, SSTL55V18, SSTL68V18, SSTL90V18, SSTL102V18, SSTL124V18, SSTL150V18, SSTL180V18, SSTL200V18.

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