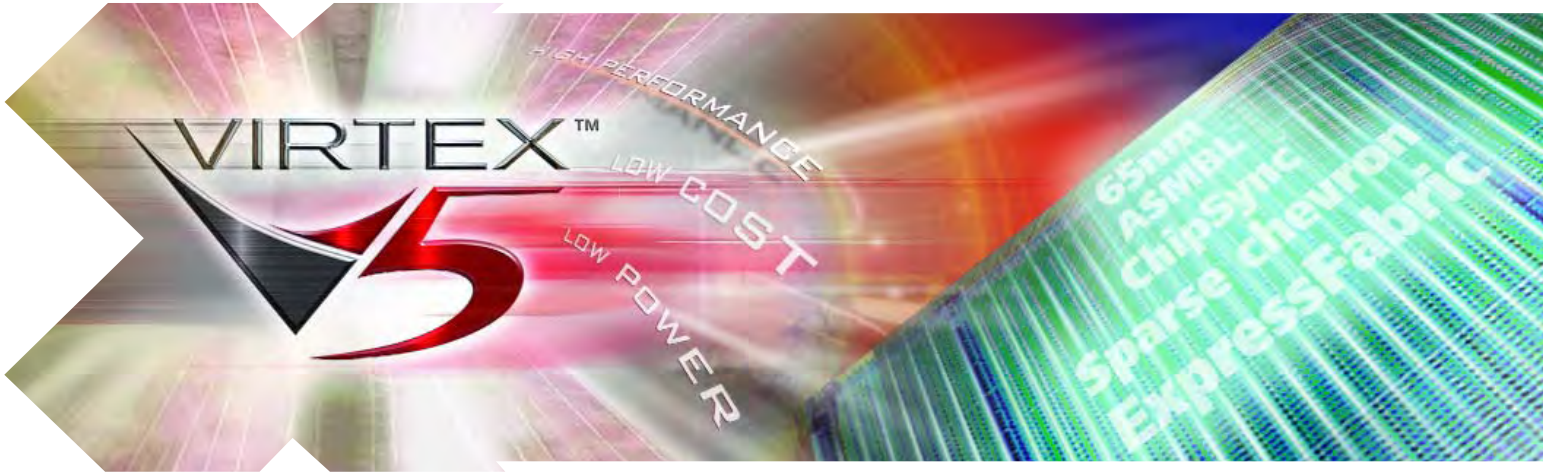# The Ultimate System Integration Platform

XILINX®

THE WORLD'S FIRST
65nm FPGA

One Family—Multiple Platforms

The Virtex™-5 family of FPGAs offers a choice of four new platforms, each delivering an optimized balance of high-performance logic, serial connectivity, signal processing, and embedded processing. Virtex-5 LX FPGAs, optimized for high-performance logic, are the first platform devices from the Virtex-5 family. Discover how this new family delivers even higher performance, lower power, and lower system cost than Virtex-4 FPGAs.
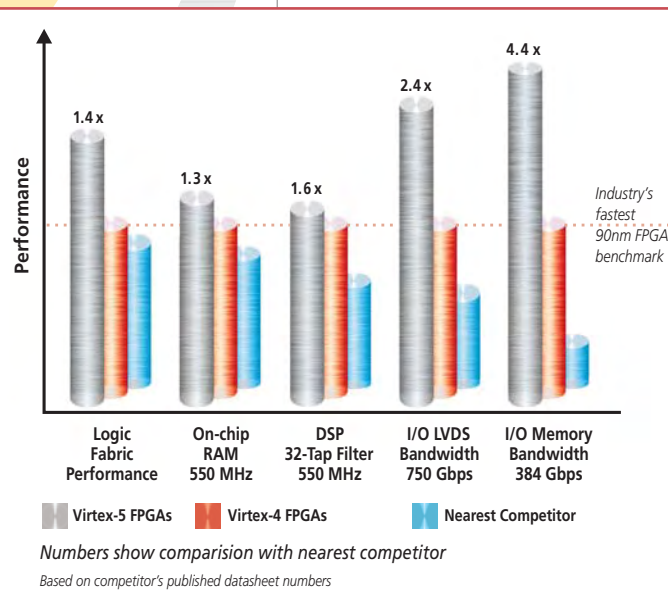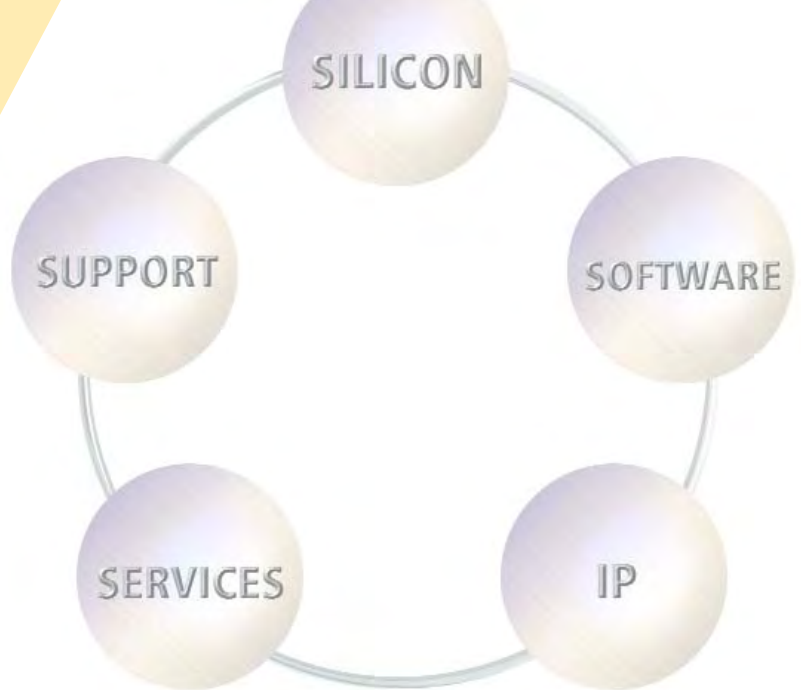
Meet Your Performance Targets Easily

- Achieve a 30% performance gain with new ExpressFabric™ technology
- 550 MHz clocking technology and performance-tuned IP blocks
- 1.25 Gbps LVDS I/O: up to 600 pin pairs

Beat Your Power Budget while Maximizing Performance

- 35% lower dynamic power with 65nm ExpressFabric and power-saving IP blocks
- Maintain low static power with 65nm Triple-Oxide Technology

Numbers show comparision with nearest competitor
Based on competitor's published datasheet numbers

Solve Signal Integrity Challenges and Simplify PCB Layout

- Second-generation sparse chevron packaging delivers SSO noise and crosstalk benefits, essential for reliable operation of high-bandwidth parallel interfaces (e.g. memories)
- On-substrate bypass capacitors and a unique pinout simplify PCB design, improve power integrity, and reduce system cost

Reduce Cost through System Integration with a Selection of Optimized Platform FPGAs

- Choose a smaller device: 65nm process shrinks die size and new Real 6-input LUT increases utilization and efficiency
- Meet aggressive performance targets in the least expensive speed grade
- Choose smaller heat sinks, fans, and power supplies enabled by reduced power consumption
- Bring your product to market faster with proven development and verification tools
- Reduce component cost in volume production with Virtex-5 EasyPath FPGAs

Finish Your Design Ahead of Schedule

- Achieve FPGA performance goals quickly with ISE™ Fmax technology and PlanAhead™ design analysis tools
- Design faster and reduce risk with over 225 pre-verified IP cores
- Reduce debug cycle time with the real-time verification capabilities of ChipScope™ Pro tools
- Build complete embedded processing systems with Platform Studio and Embedded Development Kit
- Implement DSP algorithms in custom-configured hardware with the AccelDSP™/MATLAB™ tool flow
- Accelerate product development with online resources, training courses, and premium support services
- Get Xilinx Productivity Advantage (XPA) bundles of software, education, support services, and IP cores
- Augment your development team with a worldwide network of Xilinx Design Service (XDS) and partner experts

VIRTEX-5
EASYPATH™ FPGAs

The conversion-free cost-reduction path for volume production.

- EasyPath FPGAs reduce component cost by 30–75% with no risk of conversion, no hidden costs
- Enjoy unprecedented flexibility and fastest turn-around times

THE ULTIMATE
SYSTEM INTEGRATION
PLATFORM

65nm ExpressFabric™ Technology

**Achieve highest performance, most efficient utilization on 65nm triple-oxide process**
- 30% higher speed, 35% lower dynamic power, and 45% less area than the previous generation
- Industry's first LUT with six independent inputs for fewer logic levels
- Flexible LUTs are configurable as logic, distributed RAM or shift registers
- Advanced diagonal interconnect enables shortest, fastest routing
- From 30,000 to 330,000 logic cells for system-level integration
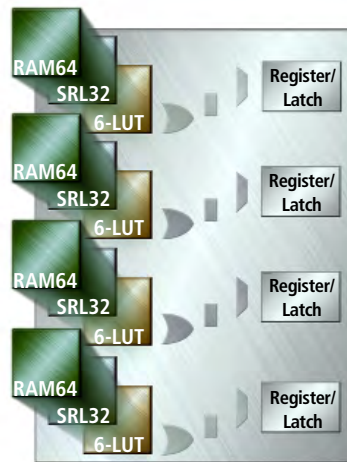
Enhanced Configuration and Bitstream Protection

Reduce system cost, increase reliability, and safeguard your design
- Configure with commodity SPI and parallel flash memory
- Easier partial reconfiguration and smaller frame size
- Greater reliability for in-system reconfiguration with multi-bitstream management
- Protect your designs with 256-bit AES (Advanced Encryption Standard) security
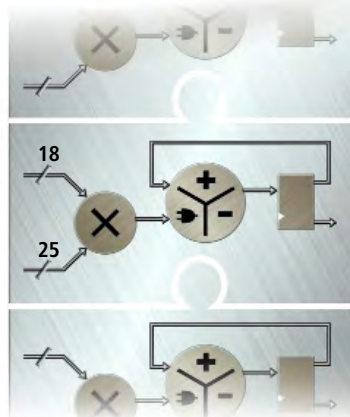
550 MHz DSP48E Slice

Create high-performance DSP systems
- New 25 x 18 multipliers enable single-precision floating-point math and wide filters with fewer slices
- Configurable for DSP, arithmetic, and bit-wise logic
- Enables efficient adder-chain architectures
- 40% lower power consumption: 1.38mW/100MHz at a 38% toggle rate
- 192 slices on Virtex-5 LX330 FPGA for 105 GMACS

550 MHz Clocking Technology

Achieve highest speeds with high-precision, low-jitter clocking
- 12 DCMs provide phase control of less than 30 ps for better design margin
- 6 PLLs reduce reference clock jitter by more than 2x
- Differential global clocking ensures low skew and jitter

ECC and Interconnect

18 Kbit

FIFO Logic

18 Kbit

The Right Memory for Any Application

Distributed RAM—Small
- Build 256-bit memory per CLB
- 64 bits per LUT

550 MHz, 36 Kbit Block RAM—Medium
- Configure Block RAM as multi-rate FIFO
- Built-in ECC for high-reliability systems
- Minimize power by turning off unused 18 Kbit sub-blocks

389 Gbps External Memories—Large
- ChipSync technology for reliable interfaces
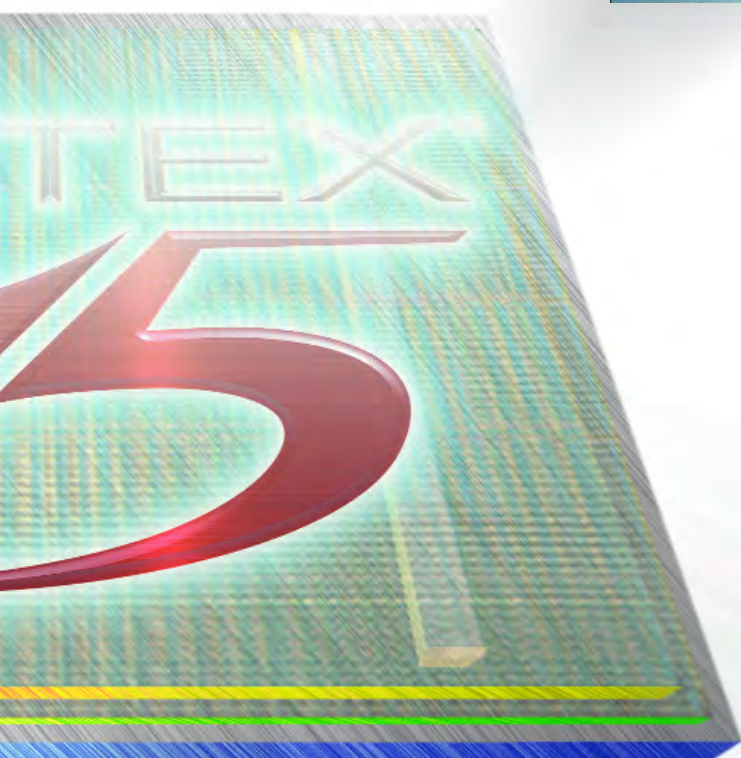
1.25 Gbps SelectIO™ with ChipSync™ Source-Synchronous Technology

Implement industy-standard and custom protocols
- Simplify board design with built-in input delay and new output delay circuits that compensate for unequal trace lengths
- Adaptive delay setting recalibrates automatically to compensate for changing operating conditions
- Interface to popular standards with 1.25 Gbps differential and 800 Mbps single-ended I/O
- Digitally controlled impedance reduces component count and board size

μP

ASIC

ASSP

XILINX
VIRTEX V5

SRAM

Flash
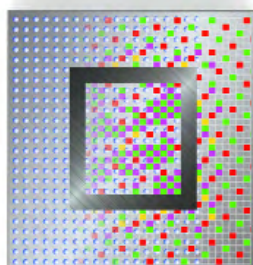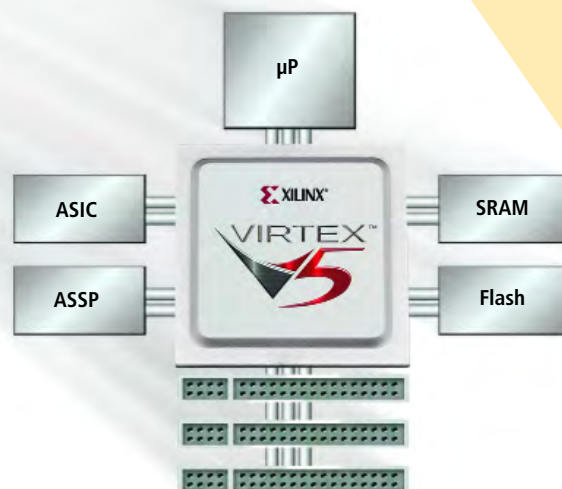
Sparse Chevron Packaging Technology

Keep system noise under control and simplify PCB layout
- Unique PWR/GND pin pattern minimizes crosstalk and reduces PCB layers
- On-substrate bypass capacitors shrink PCB area

A SOLUTION FOR EVERY
PLATFORM DESIGN CHALLENGE

Implement Networking and System Interface Standards

1.25 Gbps LVDS and 800 Mbps single-ended SelectIO circuitry, combined with pre-verified IP cores, make it easy to support all popular interface standards
- Interface or bridge to virtually any external component
- Support multiple electrical standards in the same device with 35 individually configurable I/O banks
- Design with PCI, RapidIO, XSBI, SPI4.2, and more
- Configure I/Os to support HSTL, LVDS (SDR and DDR), and more, at voltages from 1.2V to 3.3V
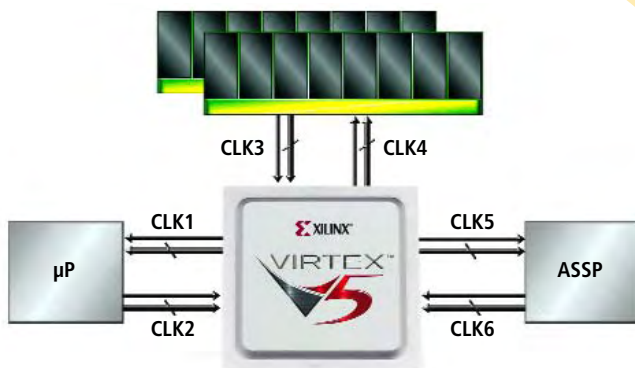
Simplify Source-Synchronous Interfacing

ChipSync technology in every SelectIO block makes it easy to create high-performance source-synchronous interfaces
- Achieve performance targets and simplify PCB layout with flexible per-bit deskew
- Synchronize incoming data to FPGA internal clock with built-in Serializer/Deserializer

Build Highest-Bandwidth Memory Interfaces

ChipSync technology and the Memory Interface Generator tool make it easy to build reliable interfaces to the latest high-performance memories, including:

Memory Interface	Data Rate (Mbps)	Data Width (# of bits)	Bandwidth (Gbps)
DDR SDRAM	400	576	230
DDR2 SDRAM	667	576	384
QDR II SRAM	600	2 x 324	389
RLDRAM II	600	648	389

Integrate a Soft Embedded Processor

Embedded development tools and IP make it easy to build a processor subsystem tailored to your requirements
- Start with the MicroBlaze™ soft processor core
- Add an IBM CoreConnect™ bus for flexible connectivity and guaranteed performance
- Connect a custom hardware accelerator through the fast simplex link (FSL)
- Complete your subsystem with pre-verified peripheral IP cores
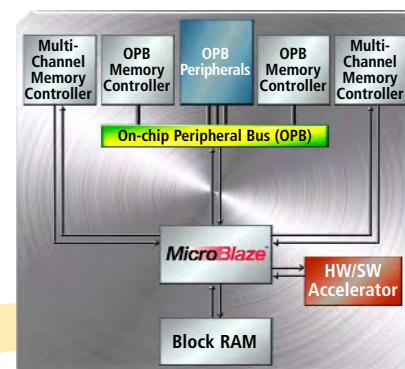
Create Efficient, High-Performance DSP Systems

Increase DSP algorithm performance
- Implement video compression, digital up/down conversion, single instruction multiple data (SIMD) functions, and filters efficiently
- DSP processor acceleration with FPGA pre/post/co-processing
- ExpressFabric enables fine granularity data shifting and control, and small bit-width arithmetic functions
- Dynamically control DSP48E to create more than 40 functions, such as Mult/MAC, Add, and Mux, without consuming other resources
- Build filters with cascadable DSP48E slices that eliminate the performance bottlenecks imposed by traditional adder trees
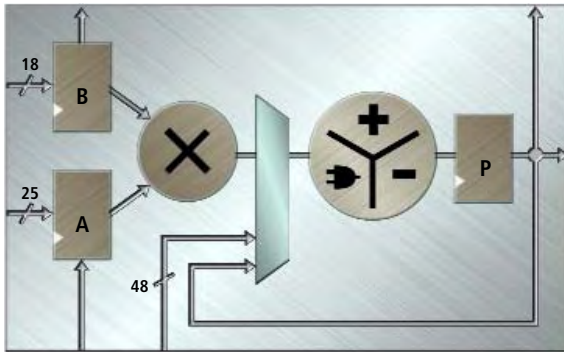
DSP48E enhanced for higher performance
- Independent 48-bit C input for multiply-add/subtract
- 48-bit A:B concatenate path for quad 12-bit or dual 24-bit SIMD arithmetic
- New pattern detector supports convergent rounding and saturation arithmetic
- 33% lower latency

WHAT'S NEW
IN THE VIRTEX-5 FPGA FAMILY

Feature/capability LX Platform	Virtex-5 family	Virtex-4 family	Virtex-5 benefit
Process Technology	65nm, 1.0v V$_{CC}$ Triple-oxide	90nm, 1.2v V$_{CC}$ Triple-oxide	Higher density and performance with lower power and cost
LUT	Real 6-input LUT with 6 independent inputs	4-input LUT	Fewer logic levels—higher density and speed and lower power
Distributed RAM	256 bits per CLB	64 bits per CLB	More memory
Shift Registers (SRL)	128-bit in one CLB	64-bit in one CLB	Deeper pipelines
Interconnect	New diagonal routing	Segmented routing	Fast, predictable routing
Clock Management	550 MHz PLL and DCM	500 MHz DCM	Higher speed PLL: lower jitter DCM: flexible clock synthesis
Block RAM/FIFO with ECC	550 MHz 36 Kbits per block (2 x 18Kb) with power saving circuits	500 MHz 18 Kbits per block	Higher speed More memory, low power
SelectIO™ Technology	1.25 Gbps differential 800 Mbps single-ended 40 pins per bank Up to 1,200 pins per FPGA	1 Gbps differential 600 Mbps single-ended 64 pins per bank Up to 960 pins per FPGA	Higher bandwidth More multi-standard interfaces Greater I/O capability, flexibility
ChipSync™ Technology	ODELAY and IDELAY	IDELAY	Fix PCB skew problems Reduce SSO noise
Sparse Chevron Pin Pattern	Rectangular bank pin-out	Triangular bank pin-out	Fewer PCB layers
DSP Blocks	550 MHz 25 x 18-bit MAC, plus bit-wise comparator 1.38 mW/100MHz @ 38% toggle rate	500 MHz 18 x 18-bit MAC 2.3 mW/100MHz @ 38% toggle rate	Higher performance Higher precision using 50% fewer slices Lower power
Device Configuration	New parallel and SPI flash support, Platform Flash, others	Platform Flash, others	Reduce cost with commodity memories

VIRTEX-5 LX

	Part Number	LX30 XC5VLX30	LX50 XC5VLX50	LX85 XC5VLX85	LX110 XC5VLX110	LX220 XC5VLX220	LX330 XC5VLX330
	EasyPath™ Cost Reduction Solutions [1]	–	–	XCE5VLX85	XCE5VLX110	XCE5VLX220	XCE5VLX330
CLB Resources	CLB Array Size (Row x Column)	80 x 30	120 x 30	120 x 54	160 x 54	160 x 108	240 x 108
	Slices [2]	4,800	7,200	12,960	17,280	34,560	51,840
	Logic Cells [3]	30,720	46,080	82,944	110,592	221,184	331,776
	CLB Flip-Flops	19,200	28,800	51,840	69,120	138,240	207,360
Memory Resources	Maximum Distributed RAM (Kbits)	320	480	840	1,120	2,280	3,420
	Block RAM/FIFO w/ECC (36 Kbits each)	32	48	96	128	192	288
	Total Block RAM (Kbits)	1,152	1,728	3,456	4,608	6,912	10,368
Clock Resources	Digital Clock Manager (DCM)	4	12	12	12	12	12
	Phase Locked Loop/PMCD	2	6	6	6	6	6
I/O Resources[7]	Maximum SelectIO™ Pins	400	560	560	800	800	1,200
	SelectIO™ Banks	13	17	17	23	23	35
	Digitally Controlled Impedance	Yes	Yes	Yes	Yes	Yes	Yes
	Maximum Differential I/O Pairs	200	280	280	400	400	600
DSP Resources	25 x 18 DSP48E Slices	32	48	48	64	128	192
	Configuration Memory (Mbits)	8.4	12.6	21.8	29.1	53.1	79.7

Package [6]	Area	IO						
FF324	19 x 19 mm	220	220	220				
FF676	27 x 27 mm	440	400	440	440	440		
FF1153	35 x 35 mm	800		560	560	800		
FF1760	42.5 x 42.5 mm	1200				800	800	1200

Notes:
[1] EasyPath™ solutions provide a conversion-free cost reduction path for volume production.
[2] A single Virtex-5 CLB comprises two slices, with each containing four Real 6-input LUTs and four Flip-Flops (twice the number found in a Virtex-4 slice), for a total of eight 6-LUTs and eight Flip-Flops per CLB.
[3] Virtex-5 logic cell ratings reflect the increased logic capacity offered by the new Real 6-input LUT architecture.
[4] Virtex-5 commercial grade devices come in three speedgrades: -1, -2, -3 (-3 being the fastest).
[5] Virtex-5 industrial grade devices come in two speedgrades: -1, -2 (-2 being the fastest).
[6] FFA Packages: flip-chip fine-pitch BGA (1.00 mm ball spacing).
[7] I/O standards supported: HT, LVDS, LVDSEXT, RSDS, BLVDS, ULVDS, LVPECL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVTTL, PCI33, PCI66, PCI-X, GTL, GTL+, HSTL I (1.2V,1.5V,1.8V), HSTL II (1.5V,1.8V), HSTL III (1.5V,1.8V), HSTL IV (1.5V,1.8V), SSTL2 I, SSTL2 II, SSTL18 I, SSTL18 II

For details on availability of specific development tools and IP for Virtex-5 FPGAs, please check with your local Xilinx sales representative

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