Audio Sample Rate Converter Reference Design for Xilinx FPGAs

Industry challenges
- Be able to handle any audio frequency in-and-out
- Maintain highest audio quality while remaining cost competitive

Xilinx solutions
- Free reference design for audio SRC
- -130dB THD+N typical performance
- Supports 8kHz to 192kHz sample frequency
- Input/output ratios 8:1 to 1:7.5
- Automatic or manual ratio management
- Synchronous channels easily added with minimal additional resources
- Reduce or remove cost of external audio ASSPs

High quality asynchronous sample rate converter with ultimate flexibility
Audio applications require different sampling frequencies depending on the sources and destinations of the audio streams. Source material recorded with one sample rate often must be converted to another sample rate for processing. The asynchronous sample rate converter (SRC) reference design addresses these conversion requirements by leveraging the unrivalled DSP horsepower of Xilinx® FPGAs.

Ideal for a wide range of markets and applications
Implementing the sample rate converter on a Xilinx FPGA offers a low-cost alternative to standard products that can be easily integrated into system-on-chip designs. The flexible and reprogrammable nature of Xilinx devices enables you to configure and adapt the SRC to meet the specific needs of your application.

Unlike a standard off-the-shelf device, complete programmability in the FPGA offers the ability to include additional interfaces, augment audio, video or system processing tasks, as well as support many channels in a single device. Applications range from professional audio and broadcast equipment, to consumer and in-car audio systems.
Sample rate converter overview and operation

The asynchronous sample rate converter converts stereo audio from one sample frequency to another. The input and output sample frequencies may be an arbitrary fraction of one, or another or the same frequency but based on different clocks.

The output is a band-limited version of the input, re-sampled to match the output sample timing. The ratio detection logic tracks input and output frequencies automatically or selectable manual ratio mode allows direct input of a desired conversion ratio. The calculated ratio, and input FIFO fill level are provided as outputs to facilitate external ratio management. Also, additional synchronous channels can be added with minimal additional resources required by replicating the input sample storage and FIR filter section. The reference design has examples of 2, 4 and 16 channel configurations. The SRC retains full performance over the AES3-2003 jitter tolerance curve.

Reference Design Specifications and FPGA Resources

| Input rates: | 8 kHz to 192 kHz | Fully asynchronous: | ✓ |
| Output rates: | 8 kHz to 192 kHz | Automatic ratio detection: | ✓ |
| Up conversion: | 8:1 continuous | Rate change tracking: | ✓ |
| Down conversion: | 1:7.5 continuous | Deterministic latency: | ✓ |
| Audio word width: | 24 bits In & Out | Sample clock jitter rejection: | ✓ |
| Performance: | -130db THD + N | Lock status for external mute: | ✓ |
| Source code: | VHDL & Verilog | 1:1 asynchronous conversion: | ✓ |

Note: Reference designs also available for Virtex®-II Pro and Virtex®-4 families

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Japan
Xilinx K.K
Art Village Osaki Central Tower 4F
1-2-2 Osaki, Shinagawa-Ku
Tokyo 141-0032 Japan
Phone: +81-3-6744-7777
Fax: +81-3-5436-0532
Web: japan.xilinx.com

Asia Pacific Pte. Ltd.
Xilinx, AsiaPacific
5 Changi Business Park
Singapore 486040
Tel: (65) 6407-3000
Fax: (65) 6789-8886
Web: www.xilinx.com

Corporate Headquarters
Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Tel: 408-559-7778
Fax: 408-559-7114
Web: www.xilinx.com

Europe Headquarters
Xilinx Ireland
One Logic Drive
Citywest Business Campus
Saggart, County Dublin
Ireland
Tel: +353-1-464-0311
Fax: +353-1-464-0324
Web: www.xilinx.com

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