

## SPACE-GRADE FPGAS



### Design Challenges for High-End Electronic Systems in Space

- Design complex functionality and high performance into systems for space applications
- Reduce mission development cycle time and overall risk
- Allow design changes without hardware modifications

### The Xilinx Radiation-Hard Virtex-5QV FPGA Solution

- High-density, performance, and integration versus ASICs and OTPs
- Radiation-hardened-by-design for SEU
- 1Mrad(Si) TID performance
- First 65nm rad-hard device
- Fully reconfigurable pre/post-launch
- Ultimate in connectivity
- Xilinx V-grade flow quality and reliability

### SPACE-GRADE RAD - HARD VIRTEX-5QV FPGA Highest-Density, Highest-Performance Rad-Hard FPGA

Until now, rad-hard solutions were limited to ASICs and one-time-programmable (OTP) solutions, forcing designers of leading-edge space applications to live with long development cycles as well as high non-recurring expenses or limited design flexibility. The Xilinx® Virtex®-5QV Space-Grade FPGA is SEU-hard and rad-hard, combining the industry's highest density and performance, allowing more complex and capable systems to be fully reconfigurable.

The rad-hard Virtex-5QV FPGA provides exceptional protection from Single-Event Upsets (SEU), Single-Event Latchup, Single-Event Transients, and high Total Ionizing Dose (TID) — 1Mrad(Si). Space system designers can significantly reduce mission risk using dramatically simplified mitigation techniques.

### Advanced Logic Designs and High-Speed Communications

The Virtex-5QV FPGA is built on the second-generation ASMBL™ column-based architecture of the proven Virtex-5 FPGA family. The Virtex-5QV FPGA offers 131,072 logic cells with flexible processing and high-performance integration and connectivity capabilities, enabling designers to address a wide variety of advanced logic designs.

The Virtex-5QV FPGA provides the first integrated high-speed SERDES solution for space, with 18 channels of >3GHz multi-gigabit serial transceivers allowing high-bandwidth for chip-to-chip, board-to-board, and box-to-box communication. 840 user I/Os are programmable to more than 30 different standards, simplifying interfacing to a wide variety of system components.

The new rad-hard FPGA also integrates many of the same embedded system-level blocks, such as powerful 36-Kbit block RAM/FIFOs, second-generation 25x18 DSP slices, power-optimized high-speed serial transceiver blocks for enhanced serial connectivity, and PCI Express™-compliant integrated endpoint blocks.



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## New Milestones in Manufacturing and Testing

Like Xilinx radiation-tolerant devices, the rad-hard Virtex-5QV FPGA is backed by Xilinx's commitment to manufacturing and testing excellence. Twenty years of continuous service to the Aerospace and Defense markets are behind the Xilinx V-grade flow process and ruggedized ceramic column grid array packaging. Additionally, extensive in-beam testing—equivalent to millions of device years in space radiation environments—yields results that can operate reliably, upholding Xilinx's heritage of successful space missions.

## Prototyping Solutions

To utilize the Virtex-5QV FPGA for flight, developers can instantly begin prototyping with off-the-shelf pin compatible commercial parts. To accelerate the prototyping process designers are supported by the Xilinx portfolio of IP and commercial development tools. Daisy chain products are also available for assembly process testing. Combined, the Xilinx solutions streamline the start-to-finish development process and offer the convenience of a single source for all required tools and solutions.

Package — CN1752 Package: Flip-chip, ceramic column grid array (1.0mm ball spacing)  
Area — 45 x 45mm

Virtex-5QV FPGA—XQR5VFX130			
Core Voltage	1.0V	Maximum Differential I/O Pairs	417
Slices	20,480	Digitally Controlled Impedance	Yes
Logic Cells	131,072	Enhanced DSP Slices (DSP48E)	320
CLB Flip-Flops	81,920	DSP Slices	—
Maximum Distributed RAM (Kb)	1,580	18 x 18 Multipliers	—
Block RAM/FIFO w/ECC (36 Kb each)	298	10/100/1000 Ethernet MAC Blocks	6
Block RAM/FIFO (18 Kb each)	—	PowerPC® Processor Blocks	—
Block RAM (4 Kb each)	—	Multi-Gigabit Serial Transceivers (MGT)	18
Total Block RAM (Kb)	10,728	Speed Grades	-1
Digital Clock Manager (DCM)	12	Configuration Memory (Mb)	49.3
Phase Lock Loop (PLL)	6	Manufacturing Grades	V
Delay Lock Loop (DLL)	—	Total Ionizing Dose (Mrad)	1
Maximum Single-Ended I/Os	840	SEL Immunity (MeV-cm <sup>2</sup> /mg)	>125