Many of today’s applications demand more memory bandwidth and lower power than commodity memories, like DDR4, can deliver. Virtex® UltraScale+™ HBM FPGAs allow users to integrate power efficient compute capabilities with the highest memory capacity and bandwidth/watt in one device. Users can design their systems with low latency and high throughput while reducing power, costs, hardware size, and complexity.

Virtex UltraScale+ HBM FPGAs integrate up to 16GB of high-bandwidth memory (HBM Gen2) at 460GB/s bandwidth and extremely low power, ~7pJ/bit. An integrated HBM controller and switch reduce logic size by 250K LUTs and minimize R&D time. HBM user ports are industry-standard AXI interfaces capable of accessing any HBM pseudo-channel from any user port, unique among competing FPGAs.

Adaptable compute logic with tightly coupled memory enable system designs to adapt with the market to deliver the latest, most valuable applications even as they change over time. Integrated high-speed connectivity provides off-the-shelf interfaces for smaller, simpler designs and shorter design cycles.

**OVERVIEW**

**HIGHLIGHTS**

**Tightly Coupled Compute and Massive Memory Bandwidth**

- 16GB HBM DRAM @ 460GB/s: 20X more bandwidth than DDR4 DIMMs
- Up to 2.9M system logic cells for emerging algorithms and protocols
- Up to 28 TOPs (INT8) of DSP compute performance

**Breakthrough System Integration for Simplified Design**

- Integrated HBM DRAM and SRAM eliminates discrete memories
- PCIe® Gen4 for host control and data interfaces
- 100G Ethernet MAC with KR4-FEC and 150G Interlaken for high-speed connectivity
- Up to 3.1Tb/s SerDes bandwidth for high throughput systems
- Integrated 58Gb/s PAM4 and 32.75Gb/s NRZ SerDes for fast data movement

**Low Power Consumption for Easier Cooling**

- 4X lower power per bit vs. discrete memory solution
- Lidless packages for more efficient cooling
- Voltage scaling options for performance and power

**TARGET APPLICATIONS**

**Data Center**

- Compute Acceleration
- Data Pre-processing and Buffering
- Database Acceleration and Analytics
- AI and High Performance Computing

**Network Acceleration**

- Network Security Acceleration
- Loading Balancing
- Search Applications

**Test and Measurement**

- Network Protocol Testing
- Packet Capturing

Adaptable. Intelligent.
FEATURES

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<th>FEATURE</th>
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<tr>
<td>16nm low power FinFET+ process technology from TSMC</td>
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<tr>
<td>Integrated HBM (Gen2)</td>
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<td>Massive memory interface bandwidth</td>
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<td>Integrated blocks for PCI Express with Cache Coherent Interconnect for Accelerators (CCIX) ports</td>
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<td>Enhanced DSP slices for diverse applications</td>
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<td>UltraRAM for deep memory buffering</td>
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<td>Massive serial bandwidth and dramatic latency reduction</td>
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<td>Integrated 100G Ethernet MAC and 150G Interlaken cores</td>
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<td>Enhanced routing, fabric CLB, and ASIC-like clocking</td>
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<td>High-speed memory cascading</td>
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<td>Advanced security</td>
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<table>
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<th>DESCRIPTION</th>
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| > Industry-leading process from the #1 service foundry TSMC  
> The same scalable architecture and tools from 20nm UltraScale™ FPGAs |
| > Up to 16GB in-package HBM DRAM with 460GB/s bandwidth  
> 4/8/16GB HBM DRAM for optimal memory capacity options  
> Assembled using proven, 3rd generation 3D IC technology (SSI) |
| > DDR4 support of up to 2,666Mb/s  
> Support for server-class DIMMs  
> Up to 30% power-saving low operating voltage mode |
| > Complete end-to-end solution for multi-100G ports  
> Gen3 x16 and Gen4 x8 for 128Gb/s bandwidth  
> Expanded virtualization for data center applications  
> Acceleration for cache coherent compute using CCIX ports |
| > Up to 28 TOPs (INT8) of DSP compute bandwidth  
> Double-precision floating point using 30% fewer resources  
> Complex fixed-point arithmetic in half the resources |
| > Up to 270Mb for SRAM device integration for reduced BOM cost  
> 8X capacity-per-block vs. traditional embedded memory  
> Deep-sleep power modes for power saving |
| > 32.75Gb/s NRZ transceivers for backplane, chip-to-chip, and chip-to-optics connectivity  
> 58Gb/s PAM4 transceivers for latest optic standards and fastest transmission rates  
> High-density I/O for smaller area and greater power efficiency per pin |
| > 60K–100K system logic cell savings per port  
> Built-in KR4-FEC (Ethernet MAC) for error correction  
> 150Gb/s of off-the-shelf Interlaken connectivity for scalable chip-to-chip connectivity |
| > Lower skew, faster performing clock networks  
> Up to one speed-grade advantage vs. comparable solutions  
> Efficient CLB use and placement for reduced interconnect delay |
| > Eliminates FPGA routing usage when building deep memories for faster timing closure  
> Reduces routing congestion  
> Lowers dynamic power consumption |
| > AES-GCM decryption, RSA-2048 authentication  
> DPA countermeasures and permanent tamper penalty  
> Improved SEU resilience |

TAKE THE NEXT STEP


Virtex UltraScale+ HBM FPGAs are supported by comprehensive developments tools, reference designs, an IP catalog, and evaluation platforms. Visit the [Virtex UltraScale+ FPGA VCU128 evaluation kit](http://www.xilinx.com/virtex-ultrascale-plus-hbm) page to get started.