Xilinx T1 Telco Accelerator Card
5G Virtual BBU, O-DU, and O-CU Acceleration

OVERVIEW
Xilinx T1 Telco Accelerator card provides high performance, low latency, and power efficiency needed for 5G O-DU deployments. The turnkey solution enables operators, system integrators, and OEMs to get to market quickly and to simplify the deployment of services at the edge.

T1 card uses 16nm Zynq® UltraScale+™ MPSoC and Zynq UltraScale+ RFSoC devices to accelerate fronthaul and real-time baseband (L1) lookaside processing.

> ZU19EG MPSoC provides the 3GPP O-RAN 7.2 split fronthaul traffic termination for 5G eCPRI/ReE/SyncE protocols. The Zynq UltraScale+ MPSoC also implements IEEE Std 1588 timing functionality with onboard reference clock timing circuit.

> ZU21DR RFSoC includes 4G/5G encode and decode acceleration along with wrapper functions such as rate matching and CRC logic. Zynq UltraScale+ RFSoC has hardened soft-decision forward error correction (SD-FEC), which can perform high-performance encode and decode with low latency and low power.

The T1 card's PCIe® Gen3 x16 connector is bifurcated into dual PCIe Gen3 x8 interfaces, giving each device independent access to the host. The board is a single slot full height, half length (FHHL) form factor with two SFP28 optical interface connectors.

TARGET APPLICATIONS
> 5G ORAN-7.2 Fronthaul termination
> 5G L1 baseband acceleration
> 5G Fronthaul with Low-PHY (optional) functions

PERFORMANCE
Virtualization requires significant acceleration of latency-sensitive and compute-intensive functions. The T1 card performance metrics below are based on in-lab measurements of the card reference design. Watch the launch video at: www.xilinx.com/T1.

Fronthaul Performance

<table>
<thead>
<tr>
<th>Fronthaul Configuration(1)</th>
<th>Performance</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACTIVE-STANDBY with O-RAN Processing on T1</td>
<td>&gt; 25Gb/s Active (2 sectors of 4T4R 100MHz)</td>
<td>For high-reliability deployments</td>
</tr>
<tr>
<td></td>
<td>&gt; 25Gb/s Standby (If Active link fails)</td>
<td></td>
</tr>
<tr>
<td>ACTIVE with O-RAN Processing on T1</td>
<td>&gt; 25Gb/s Active (1 sector of 4T4R 100MHz)</td>
<td>For deployments utilizing fronthaul gateways</td>
</tr>
<tr>
<td></td>
<td>&gt; 25Gb/s Active (1 sector of 4T4R 100MHz)</td>
<td></td>
</tr>
<tr>
<td>ACTIVE With O-RAN in software</td>
<td>&gt; 50Gb/s (4 sectors of 4T4R 100MHz with 4 layers each)</td>
<td>For high-density deployments</td>
</tr>
</tbody>
</table>

L1 (Baseband) Acceleration Performance

<table>
<thead>
<tr>
<th></th>
<th>Performance</th>
<th>Latency</th>
</tr>
</thead>
<tbody>
<tr>
<td>LDPC Encode</td>
<td>17.8Gb/s</td>
<td>14μs</td>
</tr>
<tr>
<td>LDPC Decode</td>
<td>8.1Gb/s</td>
<td>16μs</td>
</tr>
</tbody>
</table>

(1) Other configurations for fronthaul are possible.
### SPECIFICATION

**Xilinx T1 Telco Accelerator Card**

#### SoCs
- **Xilinx | Zynq UltraScale RFSoc | XCZU21DR**
- **Xilinx | Zynq UltraScale+ MPSoC | XCZU19EG**

#### SoC Resources

<table>
<thead>
<tr>
<th>XCZU21DR</th>
<th>XCZU19EG</th>
</tr>
</thead>
<tbody>
<tr>
<td>&gt; System Logic cells - 930K</td>
<td>&gt; System Logic cells - 1,143K</td>
</tr>
<tr>
<td>&gt; CLB LUT - 425K</td>
<td>&gt; CLB LUT - 523K</td>
</tr>
<tr>
<td>&gt; SDFEC - 8</td>
<td>&gt; CLB Flip-Flops - 1,045K</td>
</tr>
<tr>
<td>&gt; DSP Slices - 4,272</td>
<td>&gt; DSP Slices - 1,968</td>
</tr>
<tr>
<td>&gt; BRAM - 38.0Mb</td>
<td>&gt; BRAM - 34.6Mb</td>
</tr>
<tr>
<td>&gt; URAM - 22.5Mb</td>
<td>&gt; URAM - 36.0Mb</td>
</tr>
</tbody>
</table>

#### Form Factor
- Full-height, half-length (FHHL)
- > x16 PCIe form factor
- > Width: 167.65mm
- > Height: 111.15mm
- > Depth: 34.8mm

#### PCIe Interface
- PCIe Gen3 x16 interface bifurcated to two PCIe Gen3 x8

#### Onboard Memory

<table>
<thead>
<tr>
<th>XCZU21DR</th>
<th>XCZU19EG</th>
</tr>
</thead>
<tbody>
<tr>
<td>&gt; 1x Banks of 4GB x72 (64 bit +8bit ECC) - PL</td>
<td>&gt; 1x Banks of 4GB x72 (64 bit +8bit ECC) - PL</td>
</tr>
<tr>
<td>&gt; 1x Banks of 2GB x 40 (32 bit +8bit ECC) - PS</td>
<td>&gt; 1x Banks of 2GB x 40 (32 bit +8bit ECC) - PS</td>
</tr>
<tr>
<td>&gt; Total Capacity 4GB in PL</td>
<td>&gt; Total Capacity 4GB in PL</td>
</tr>
<tr>
<td>&gt; Total Capacity 2GB in PS</td>
<td>&gt; Total Capacity 2GB in PS</td>
</tr>
</tbody>
</table>

#### In System Upgrade
- Standard Xilinx tandem and partial reconfiguration support for both devices

#### Programming
- > 1x 2Gb QSPI NOR Flash for FPGA configuration for ZU19EG
- > 1x 2Gb QSPI NOR Flash for FPGA configuration for ZU21DR

#### Network Interface(s)
- 2xSFP28 optical interfaces to XCZU19EG
  (User Configurable, includes 10/25 Ethernet)

#### Other External Interface(s)
- Micro USB for JTAG support (FPGA programming and debug) and access to BMC

#### Reference Design
- Vivado® design (diagnostic bit file) and commands for testing all datapath interfaces available for diagnostic bit files for both FPGAs

#### Cooling
- Passive cooling, custom heat sink

#### Board Management Controller
- > Power sequencing and reset
- > Field upgrades
- > FPGA configuration and control
- > Clock configuration
- > Temperature monitoring
- > USB 2.0

#### Operating Temperature
- 0–100°C (up to 110°C for NEBS excursion)

#### Power
- < 75W typical

#### Clocking Options
- > Low-Jitter, configurable clock ranging from10MHz to 750 MHz
- > Capable of ITU-T G8273.2
- > 1 PPS input and output mode support
- > Have assembly option for OCXO and/or TCXO for Master and slave mode operation

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**Adaptable. Intelligent.**
**HIGH-LEVEL BLOCK DIAGRAM**

**Xilinx T1 Telco Accelerator Card**

1. **Timing Circuitry**
   - TCXO/OCXO with PPS in and out.
   - PS (A53) for 1588 protocol stack

2. **Fronthaul Termination**
   - 2x25G eCPRI w/TSN & RS-FEC & 1588
   - Aggregation Logic
   - Buffer memory
   - Packet Classification

3. **L1 Offload**
   - LDPC/TURBO codecs
   - Polar codecs
   - HARQ management
   - Codec Surrounding/Wrapper logic
     - CRC logic
     - Rate Matching/De-Matching

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**Figure 1: Xilinx T1 Block Diagram**

- **PPS IN**
- **PPS OUT**
- **SFP28 Optics**
- **25G**
- **6GB DDR4 (PS/PL)**
- **ZU19EG Fronthaul**
  - eCPRI Fronthaul (ORAN 7.2x)
  - IEEE Std 1588 Timing
  - Packet Classification
  - Customer Design Blocks
- **ZU21DR L1 Offload**
  - Hardened LDPC / TURBO Codec
  - Polar Codec
  - HARQ Manager
  - Codec Wrapper
- **PCIe Gen3x8**
- **Gen3x16 with Bifurcation**
- **25G**
- **25G**
- **25G**
- **100G**

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