

Zynq® UltraScale+™ RFSoC Example Design: ZCU111

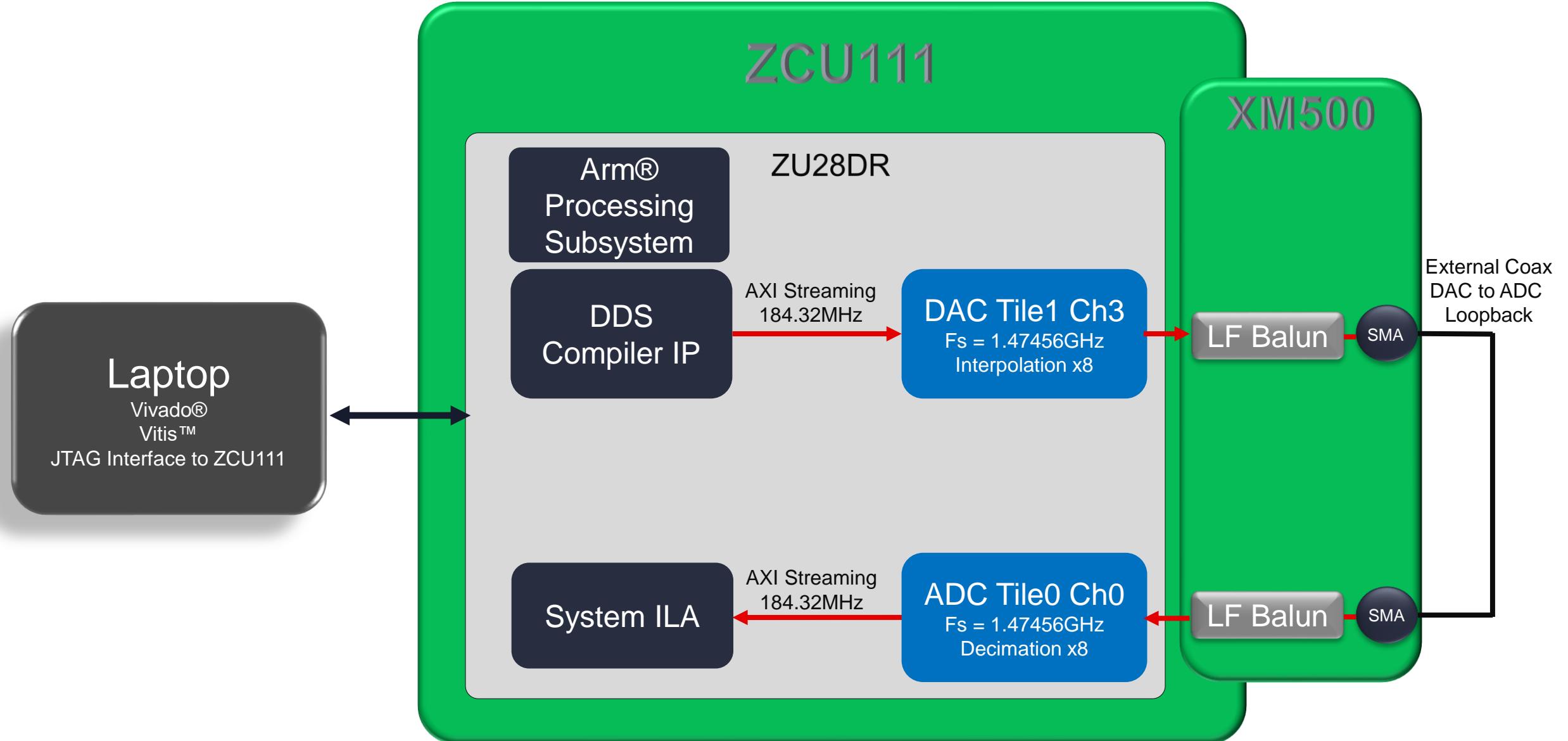
DDS Compiler for DAC and System
ILA for ADC Capture – 2020.2



Introduction

- ▶ This is an example starter design for the RFSoC.
- ▶ It uses the ZCU111 board.
- ▶ It uses a DAC and ADC sample rate of 1.47456GHz.
- ▶ The DAC will continuously play 10MHz sine wave from the DDS Compiler IP.
- ▶ The ADC output will be sent to a System ILA to be displayed in the Hardware Manager.
- ▶ DAC Tile1 Ch3 will be used (LF balun).
- ▶ ADC Tile0 Ch0 will be used (LF balun).
- ▶ 2020.2 Xilinx tools (Vivado® Design Suite and Vitis™ unified software platform).
- ▶ Design tested in the directory `c:\rfsoclex_des\zcu111\v4\`
- ▶ This kit comes with the Vivado HW project and SW source files.

Demo Block Diagram



ZCU111 Clocks

- This design automatically programs the clocks to 1.47456GHz via the SW application.
- ZCU111 ADC/DAC clocks are generated from LMK04208 feeding 3 LMX2594 in parallel. Review 'RF Data Converter Clocking' in [UG1271](#) (ZCU111 board user guide).
- Clocking is configured via an I2C to SPI bridge.

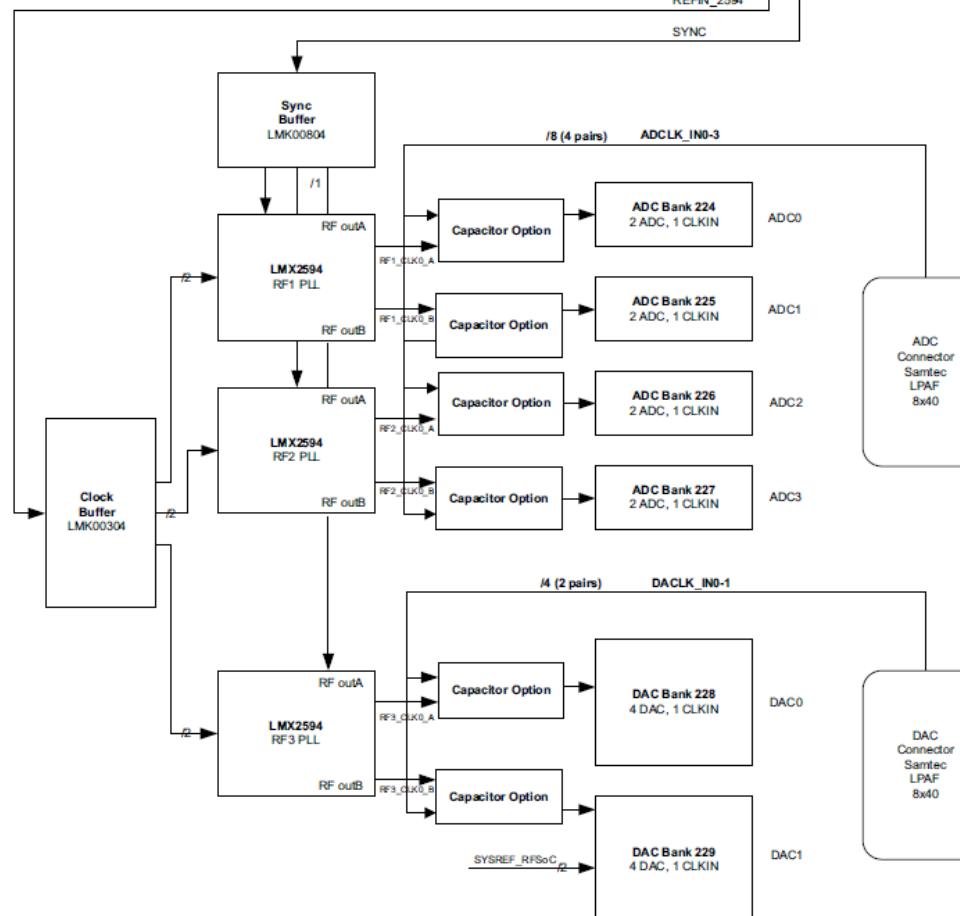
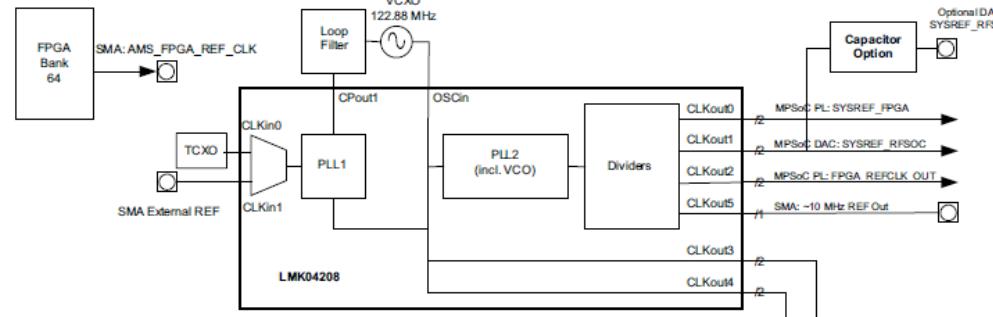


Figure 3-18: RF Clocking Structure for ADC and DAC Banks

DAC Setup

Basic System Clocking Advanced

Converter Setup

Converter Setup Advanced

Changing Converter Setup to Simple will cause current Advanced IP configuration to be lost.

RF-ADC RF-DAC

DAC Tile 228 DAC Tile 229

Multi Tile Sync Converter Band Mode

Enable Multi Tile Sync Band Single

Converter Configuration

DAC Pair 0,1 DAC Pair 2,3

DAC 2

Enable DAC Invert Q Output

Inverse Sinc Filter

Data Settings

Analog Output Data: Real Interpolation Mode: Off Samples per AXI4-Stream Cycle: 16

Mixer Settings

Mixer Type: Off

Analog Settings

Nyquist Zone: Zone 1 Decoder Mode: SNR Optimized

DAC 3

Enable DAC Invert Q Output

Inverse Sinc Filter

Data Settings

Analog Output Data: Real Interpolation Mode: 8x Samples per AXI4-Stream Cycle: 1

Required AXI4-Stream clock: 184.320 MHz

Mixer Settings

Mixer Type: Bypassed Mixer Mode: Real->Real

Analog Settings

Nyquist Zone: Zone 1 Decoder Mode: SNR Optimized

ADC Setup

Basic System Clocking Advanced

Converter Setup

Converter Setup Advanced

Changing Converter Setup to Simple will cause current Advanced IP configuration to be lost.

RF-ADC RF-DAC

ADC Tile 224 ADC Tile 225 ADC Tile 226 ADC Tile 227

Multi Tile Sync Converter Band Mode Link Coupling

Enable Multi Tile Sync Band Single

Link Coupling AC

Converter Configuration

ADC 0

Enable ADC Invert Q Output

Dither Bypass Background Calibration

Data Settings

Digital Output Data Real

Decimation Mode 8x

Samples per AXI4-Stream Cycle 1

Required AXI4-Stream clock: 184.320 MHz

Mixer Settings

Mixer Type Bypassed

Mixer Mode Real->Real

Analog Settings

Nyquist Zone Zone 1

Calibration Mode Mode2

ADC 1

Enable ADC Invert Q Output

Dither Bypass Background Calibration

Data Settings

Digital Output Data Real

Decimation Mode Off

Samples per AXI4-Stream Cycle 8

Mixer Settings

Mixer Type Off

Analog Settings

Nyquist Zone Zone 1

Calibration Mode Mode2

Data Converter Clocking

Basic System Clocking Advanced

AXI4-Lite Interface Configuration

AXI4-Lite Clock (MHz) 

Tile Clocking Settings

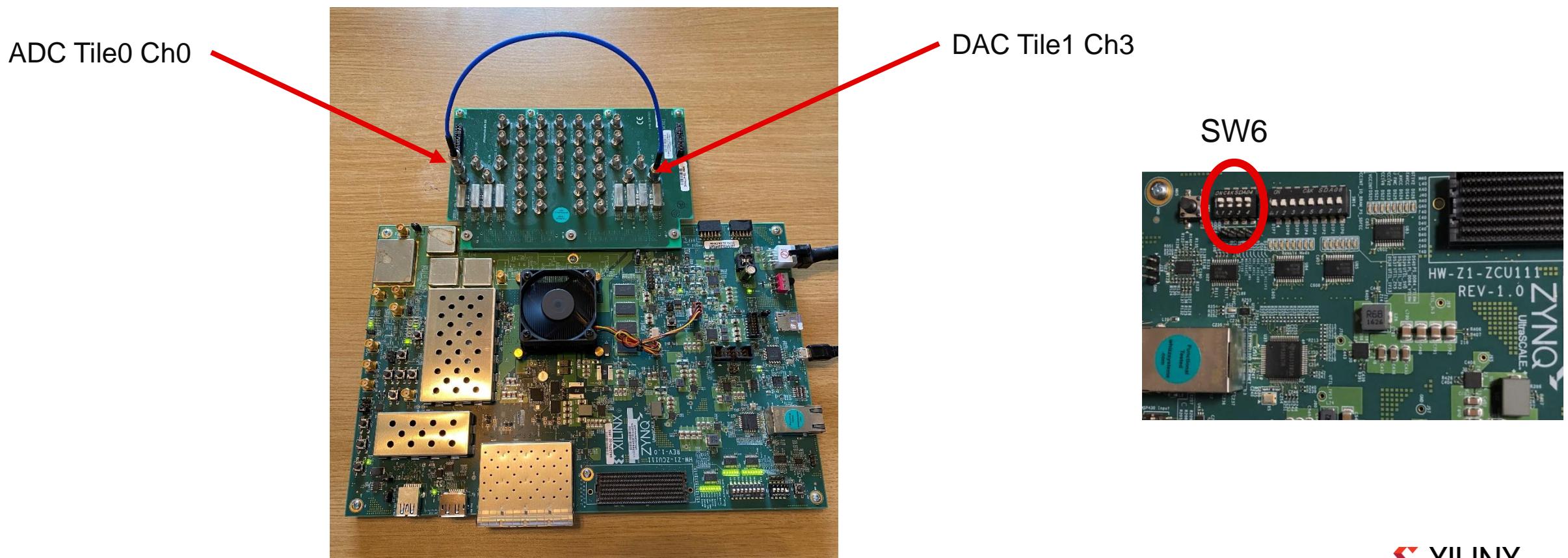
| Tile | Sampling Rate (GSPS) | Max Fs (GSPS) | PLL | Reference Clock (MHz) | PLL Ref Clock (MHz) | Ref Clock Divider | Fabric Clock (MHz) | Clock Out (MHz) |
|---------|---|---------------|--------------------------|-----------------------|---------------------|-------------------|--------------------|-----------------|
| ADC 224 | 1.47456  | 4.096 | <input type="checkbox"/> | 1474.560 | - | 1 | 184.320 | 92.160 |
| ADC 225 | 2.0 | 4.096 | <input type="checkbox"/> | 2000.000 | - | 1 | 0.0 | 15.625 |
| ADC 226 | 2.0 | 4.096 | <input type="checkbox"/> | 2000.000 | - | 1 | 0.0 | 15.625 |
| ADC 227 | 2.0 | 4.096 | <input type="checkbox"/> | 2000.000 | - | 1 | 0.0 | 15.625 |
| | | | | | | | | |
| DAC 228 | 6.4 | 6.554 | <input type="checkbox"/> | 6400.000 | - | 1 | 0.0 | 50.000 |
| DAC 229 | 1.47456  | 6.554 | <input type="checkbox"/> | 1474.560 | - | 1 | 184.320 | 184.320 |

PLL Summary Settings

| Tile | Vco (MHz) | Fb Div | M | R |
|---------|-----------|--------|---|---|
| ADC 224 | - | - | - | - |
| ADC 225 | - | - | - | - |
| ADC 226 | - | - | - | - |
| ADC 227 | - | - | - | - |
| | | | | |
| DAC 228 | - | - | - | - |
| DAC 229 | - | - | - | - |

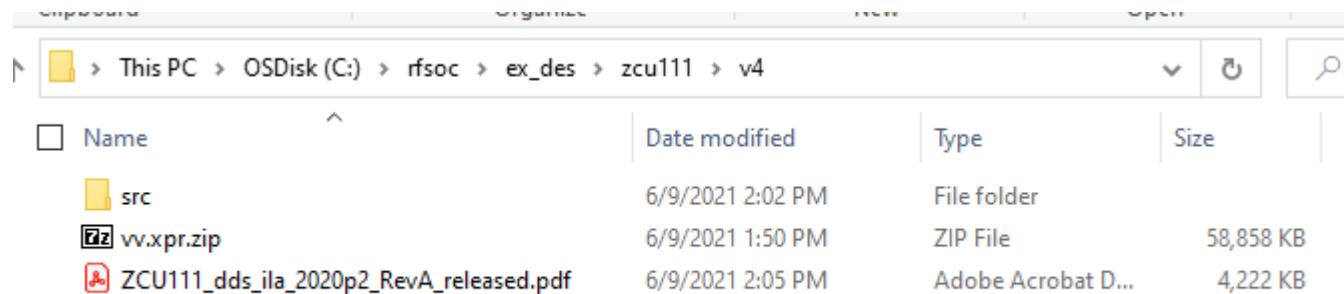
Board Setup for the Upcoming Designs

- ▶ Connect DAC Tile 229 Ch3 output to ADC Tile 224 Ch0 input on XM500 (low frequency balun connections).
- ▶ Set SW6 to on,on,on,on (JTAG boot mode).
- ▶ Connect USB to host for JTAG, PS UART, and System Controller UART access.



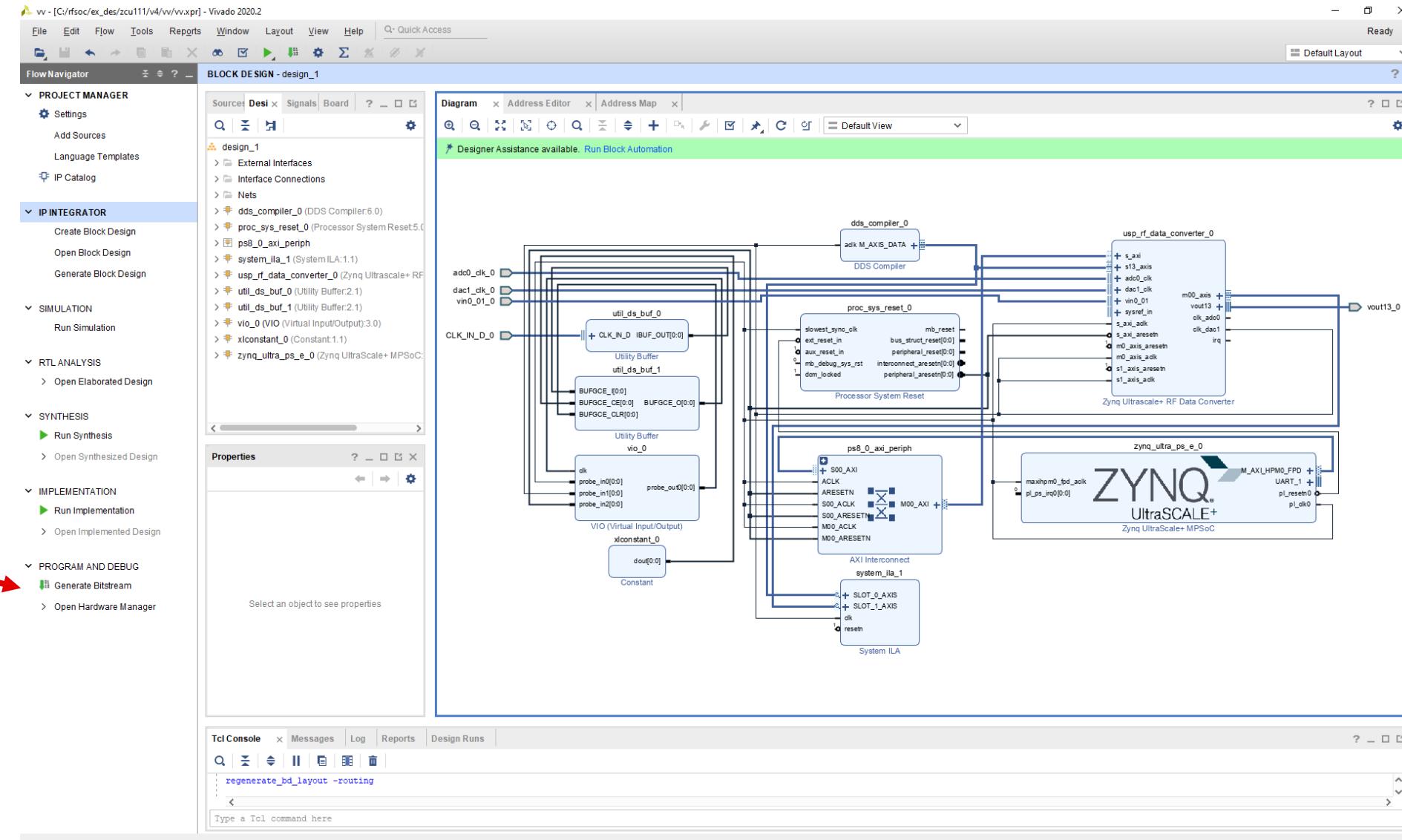
Design Kit Contents

1. Extract the design kit to an appropriate folder—be mindful of the Windows path length requirement.
2. Extract **vv.xpr.zip**, which is the Vivado® project.
3. Software source files in the “src” folder.
4. Design documentation in the .pdf file.

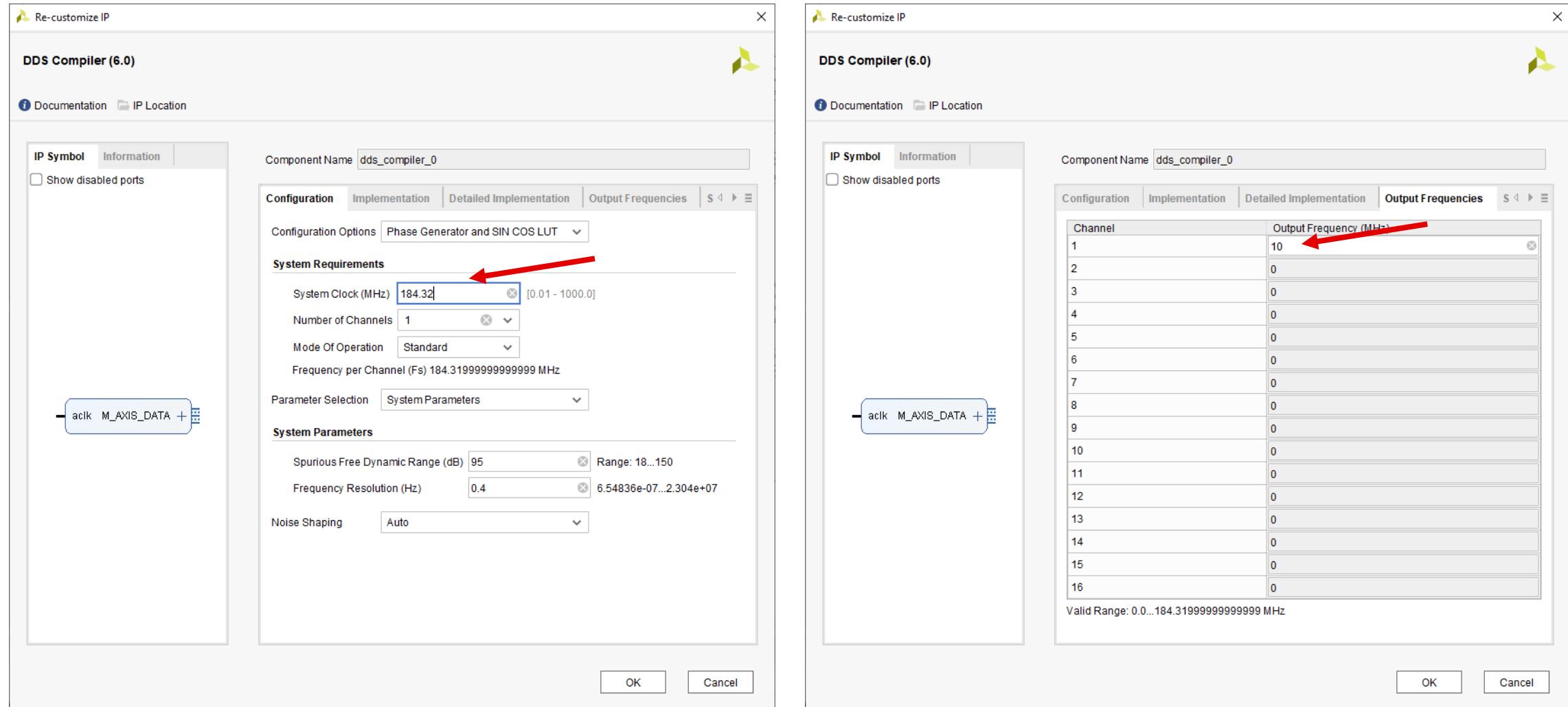


Open Hardware Design and Generate the Bitstream

Extract vv.xpr.zip, open the design in Vivado®, and generate the bitstream.



DAC Sine Wave Generator (DDS Compiler IP)



Configuration Tab (Left Screenshot):

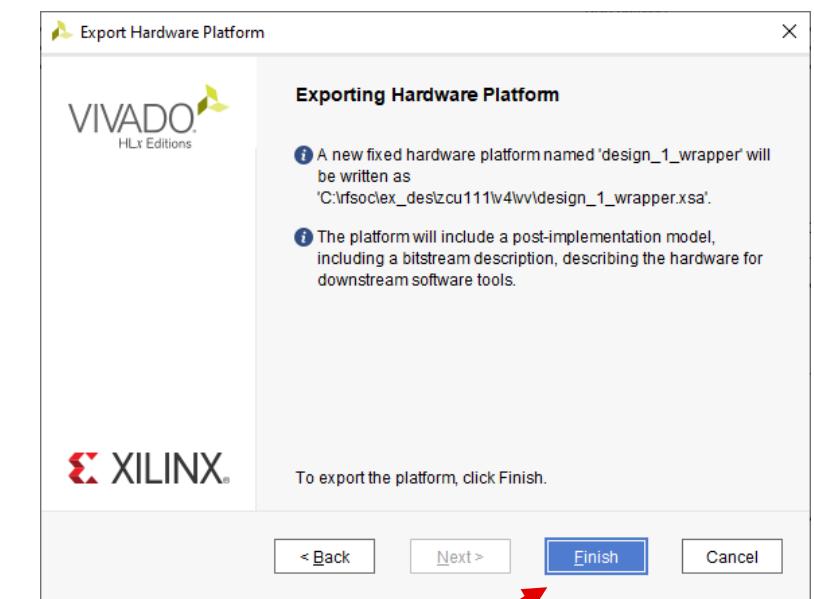
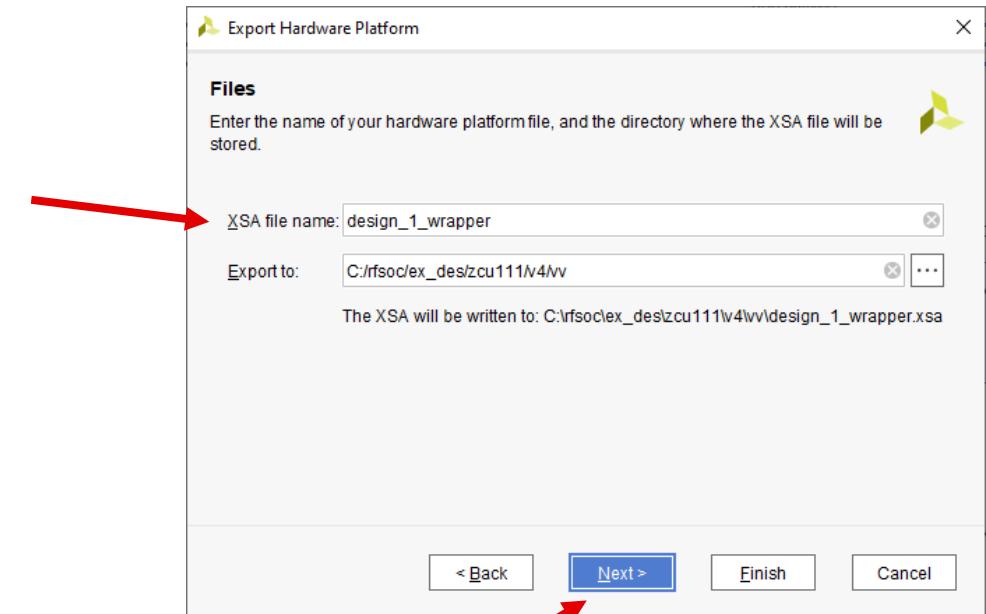
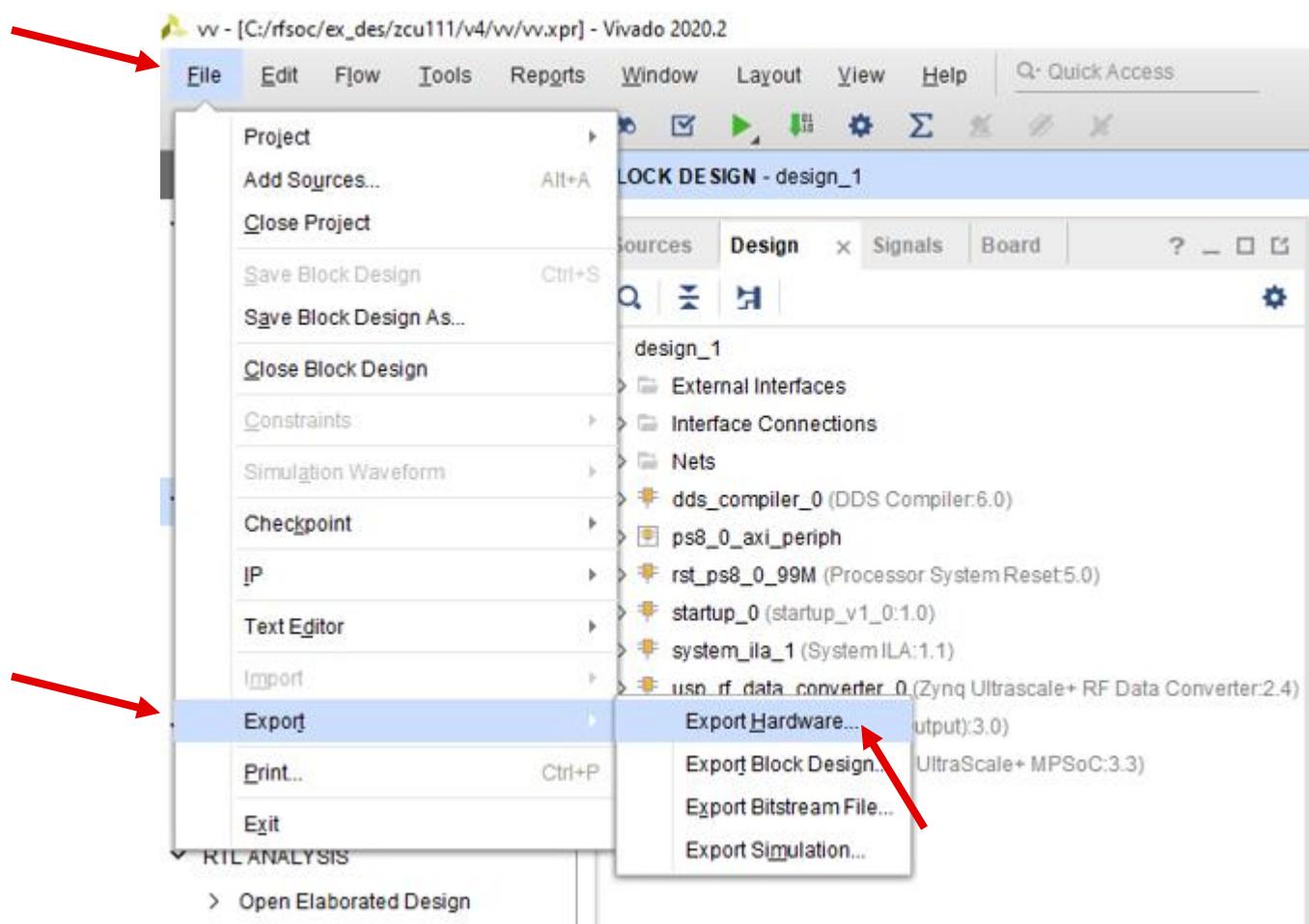
- Component Name: dds_compiler_0
- Configuration Options: Phase Generator and SIN COS LUT
- System Requirements:
 - System Clock (MHz): 184.32 [0.01 - 1000.0]
 - Number of Channels: 1
 - Mode Of Operation: Standard
- Parameter Selection: System Parameters
- System Parameters:
 - Spurious Free Dynamic Range (dB): 95 (Range: 18...150)
 - Frequency Resolution (Hz): 0.4 (6.54836e-07...2.304e+07)
 - Noise Shaping: Auto

Output Frequencies Tab (Right Screenshot):

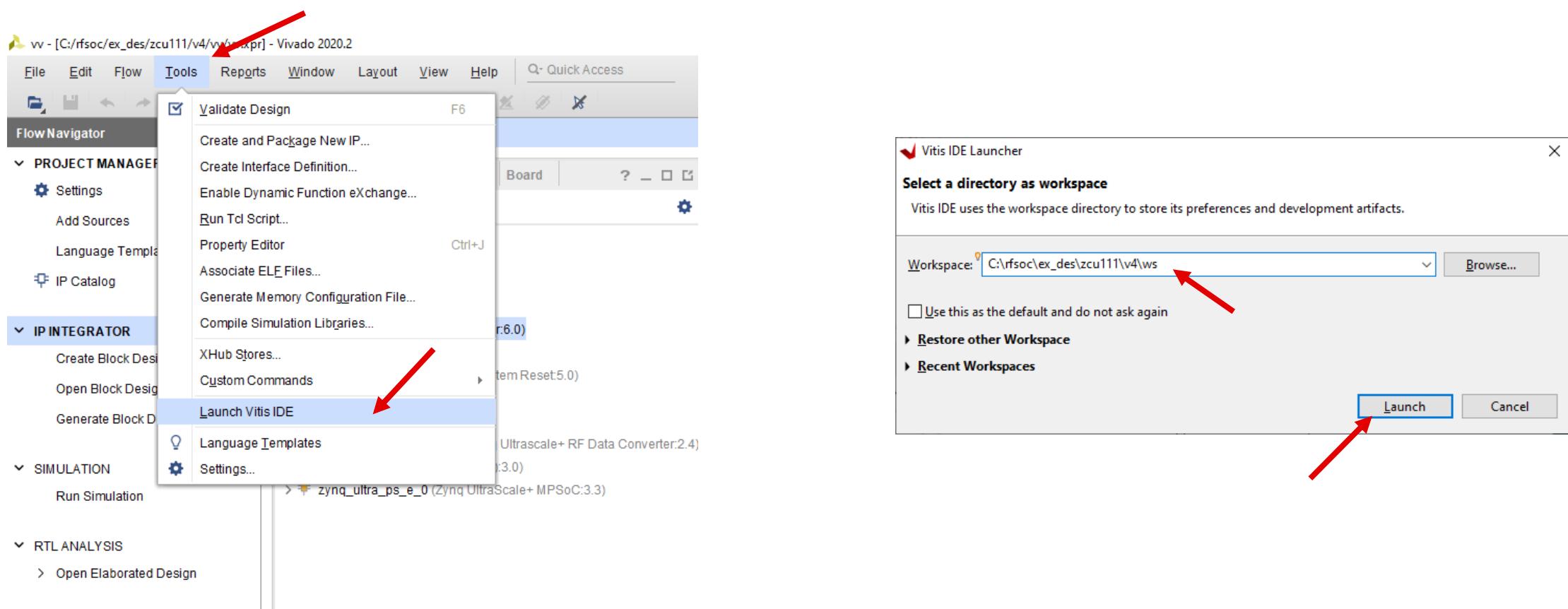
| Channel | Output Frequency (MHz) |
|---------|------------------------|
| 1 | 10 |
| 2 | 0 |
| 3 | 0 |
| 4 | 0 |
| 5 | 0 |
| 6 | 0 |
| 7 | 0 |
| 8 | 0 |
| 9 | 0 |
| 10 | 0 |
| 11 | 0 |
| 12 | 0 |
| 13 | 0 |
| 14 | 0 |
| 15 | 0 |
| 16 | 0 |

Valid Range: 0.0...184.31999999999999 MHz

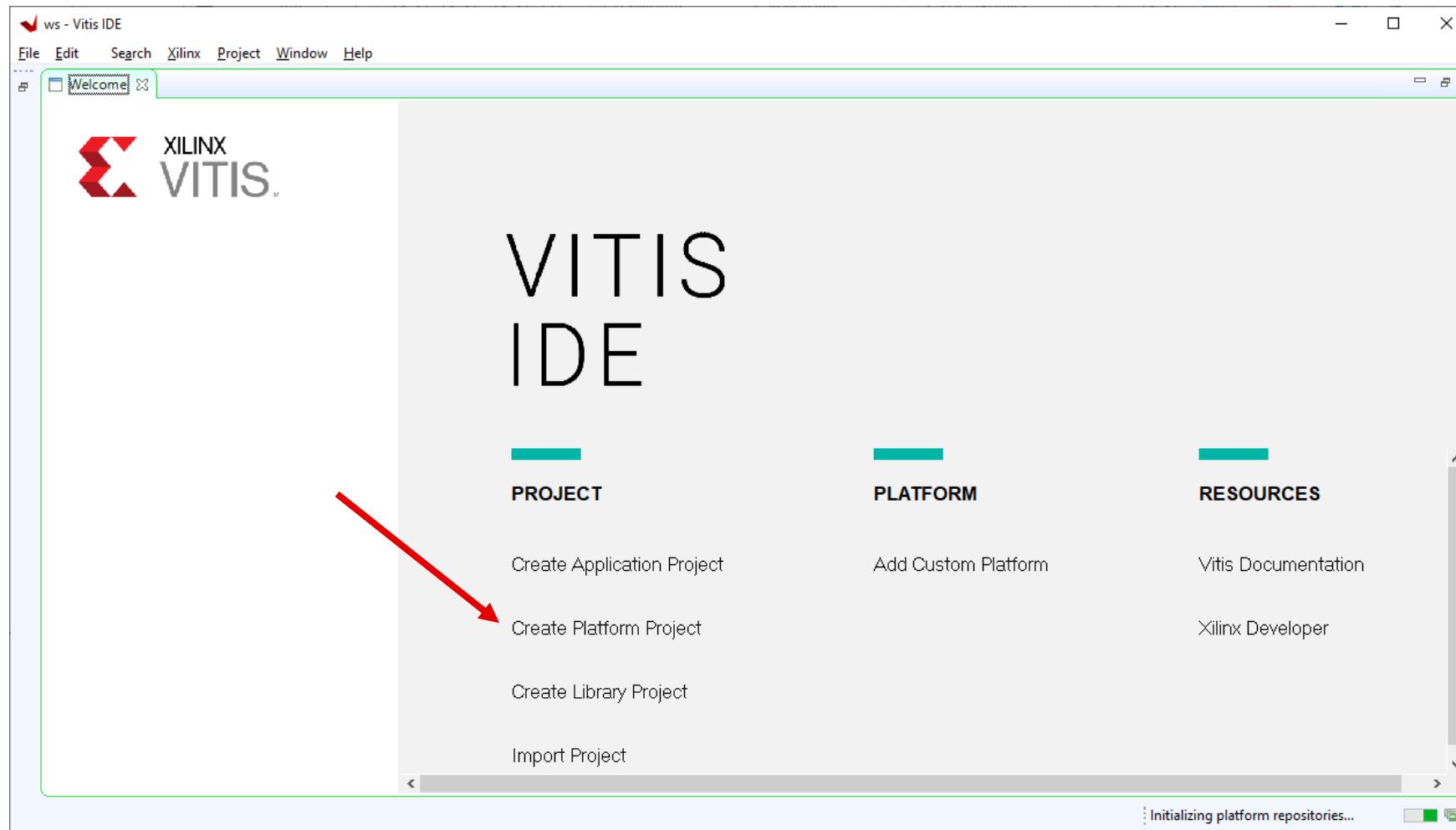
Export Hardware



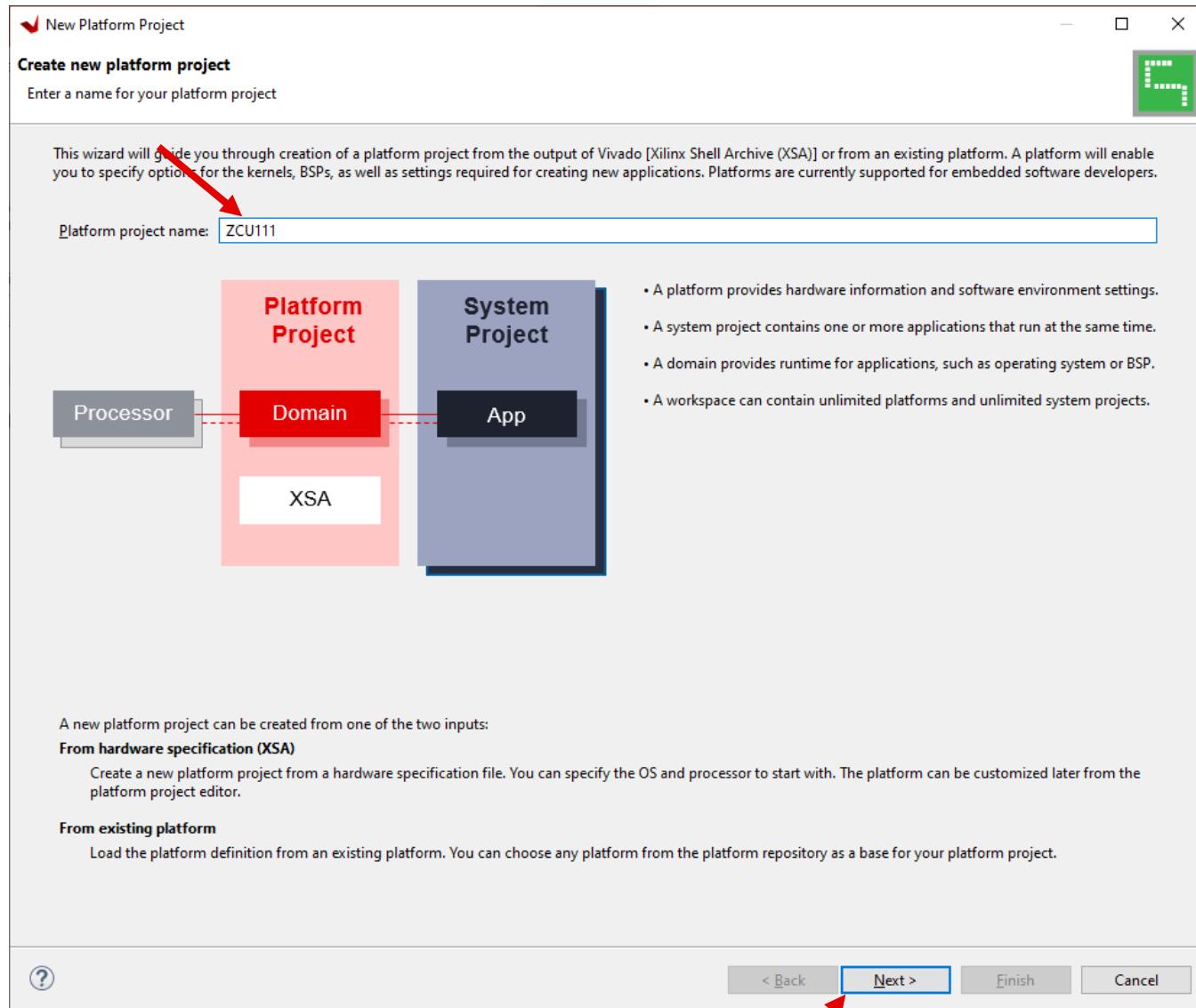
Open Vitis™ Software Platform



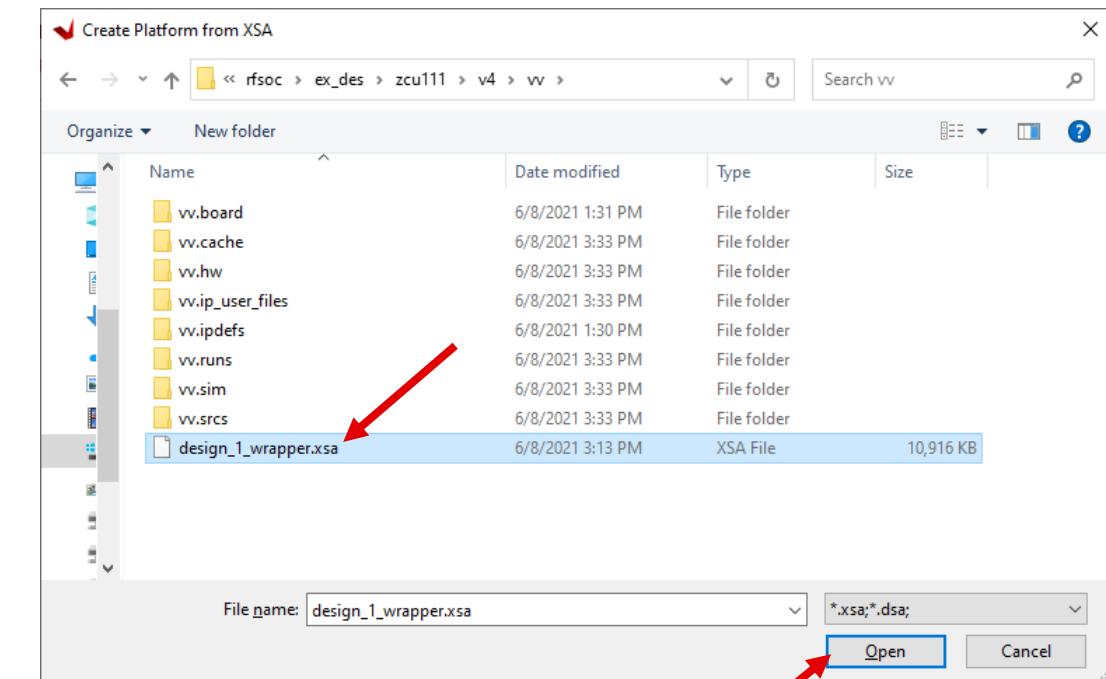
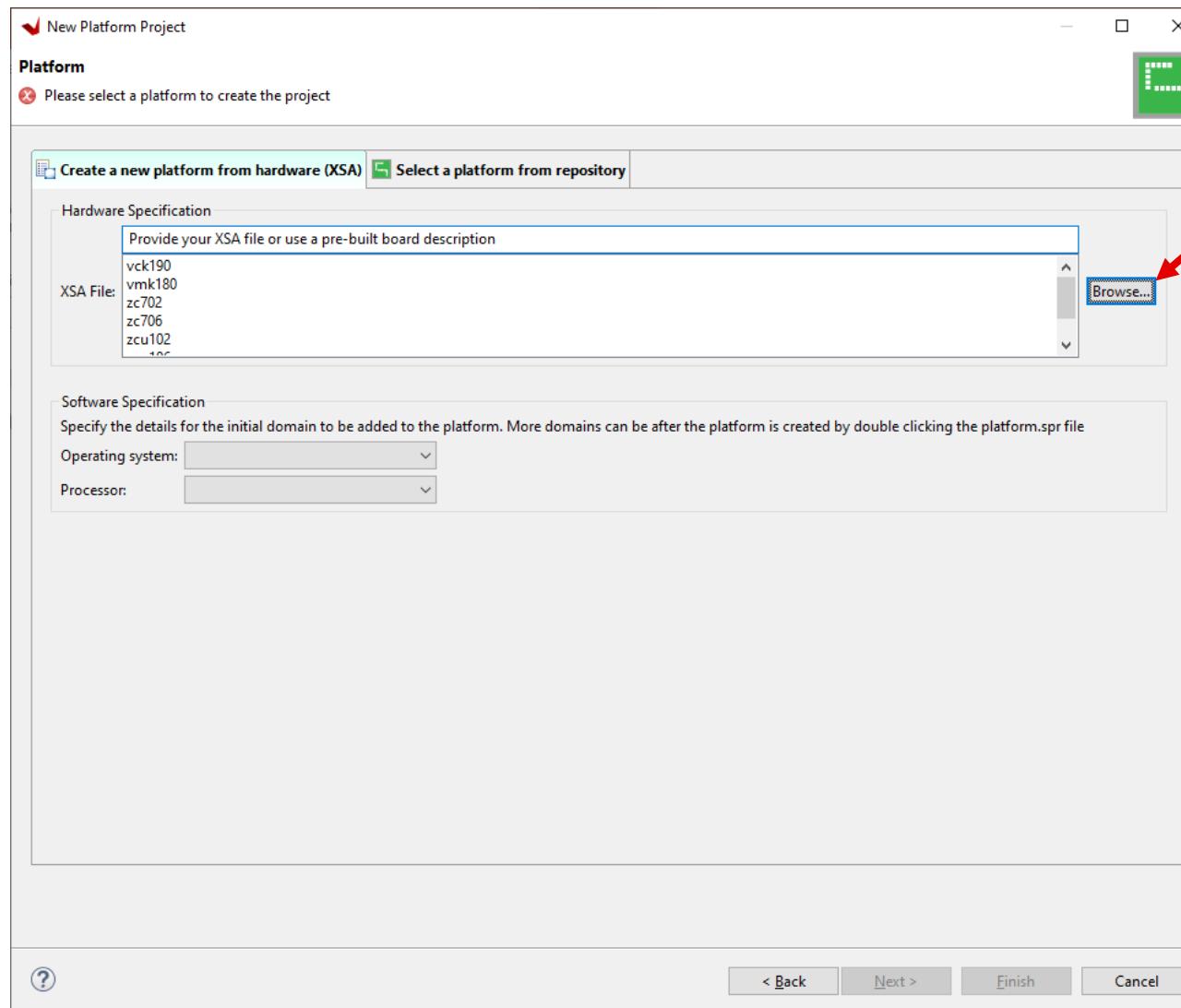
Create Platform Project



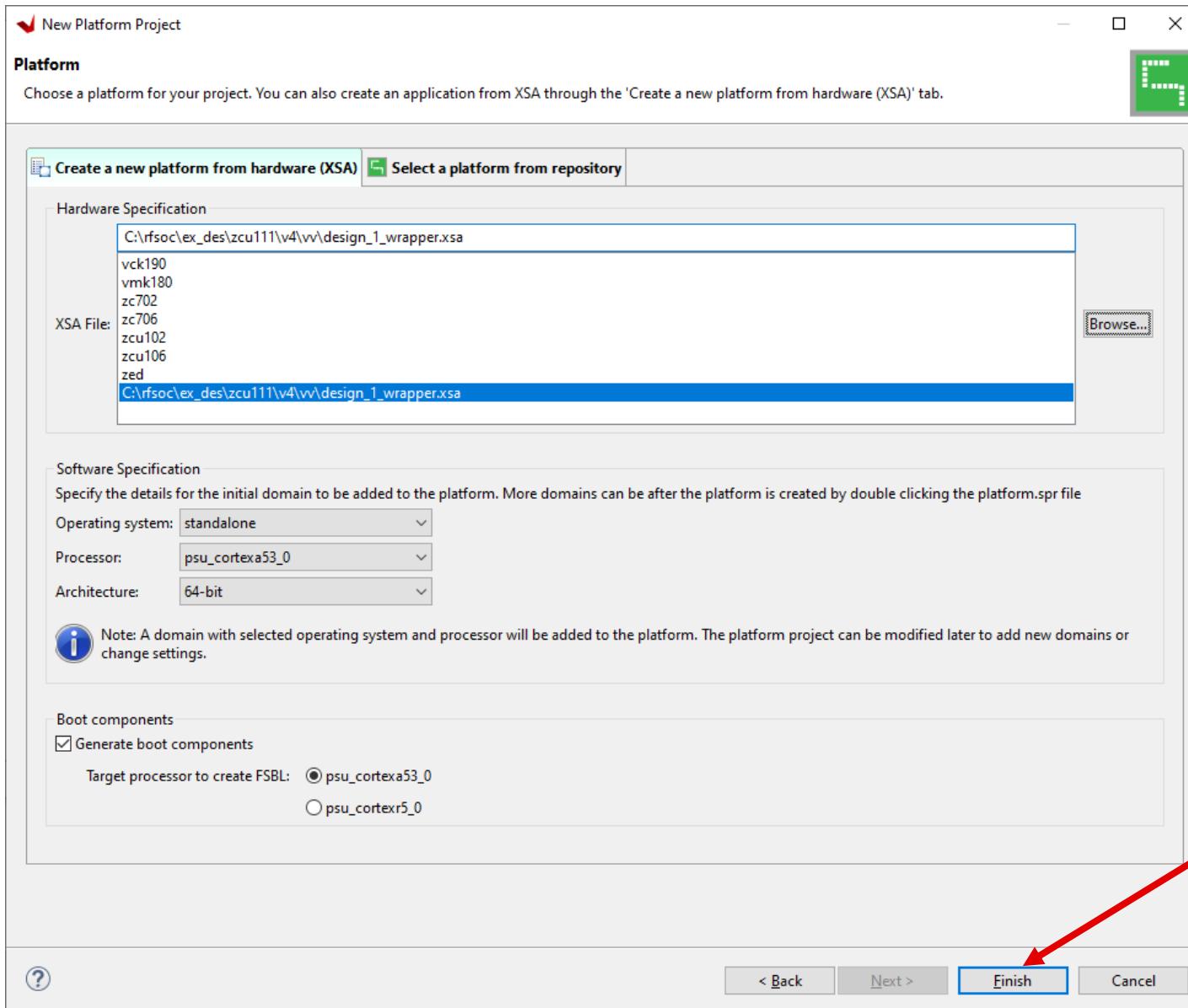
Create Platform Project Cont'd



Create Platform Project Cont'd

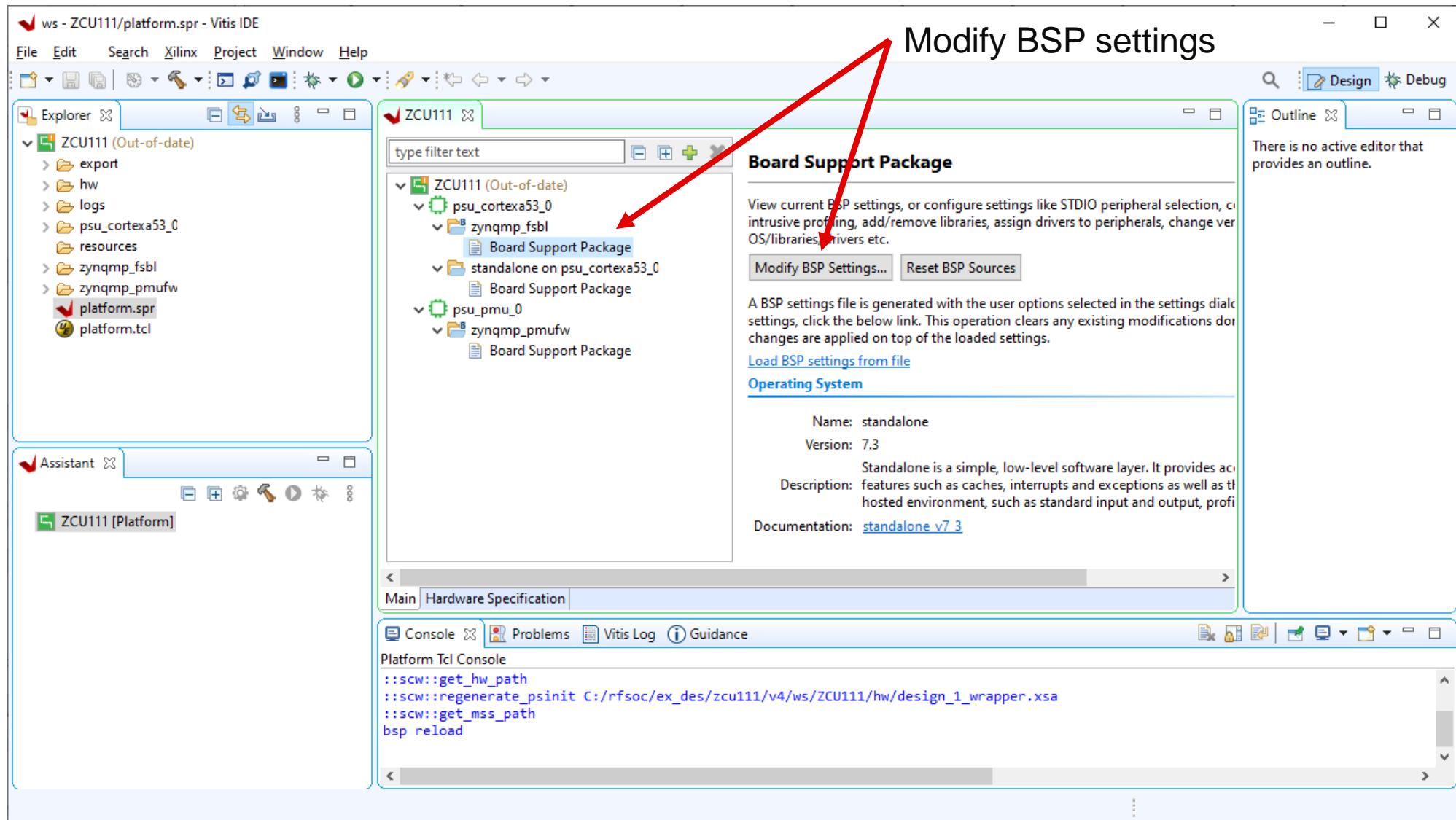


Create Platform Project Cont'd

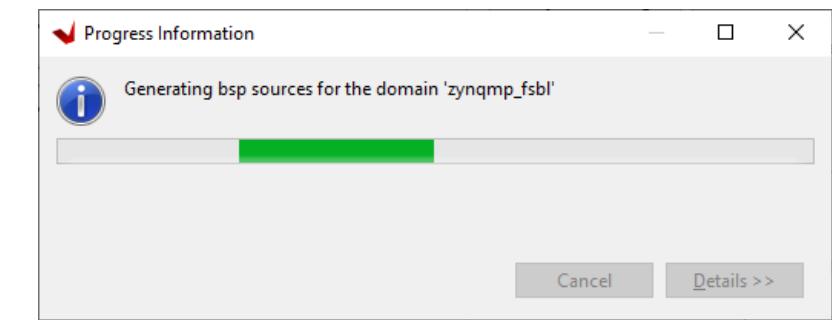
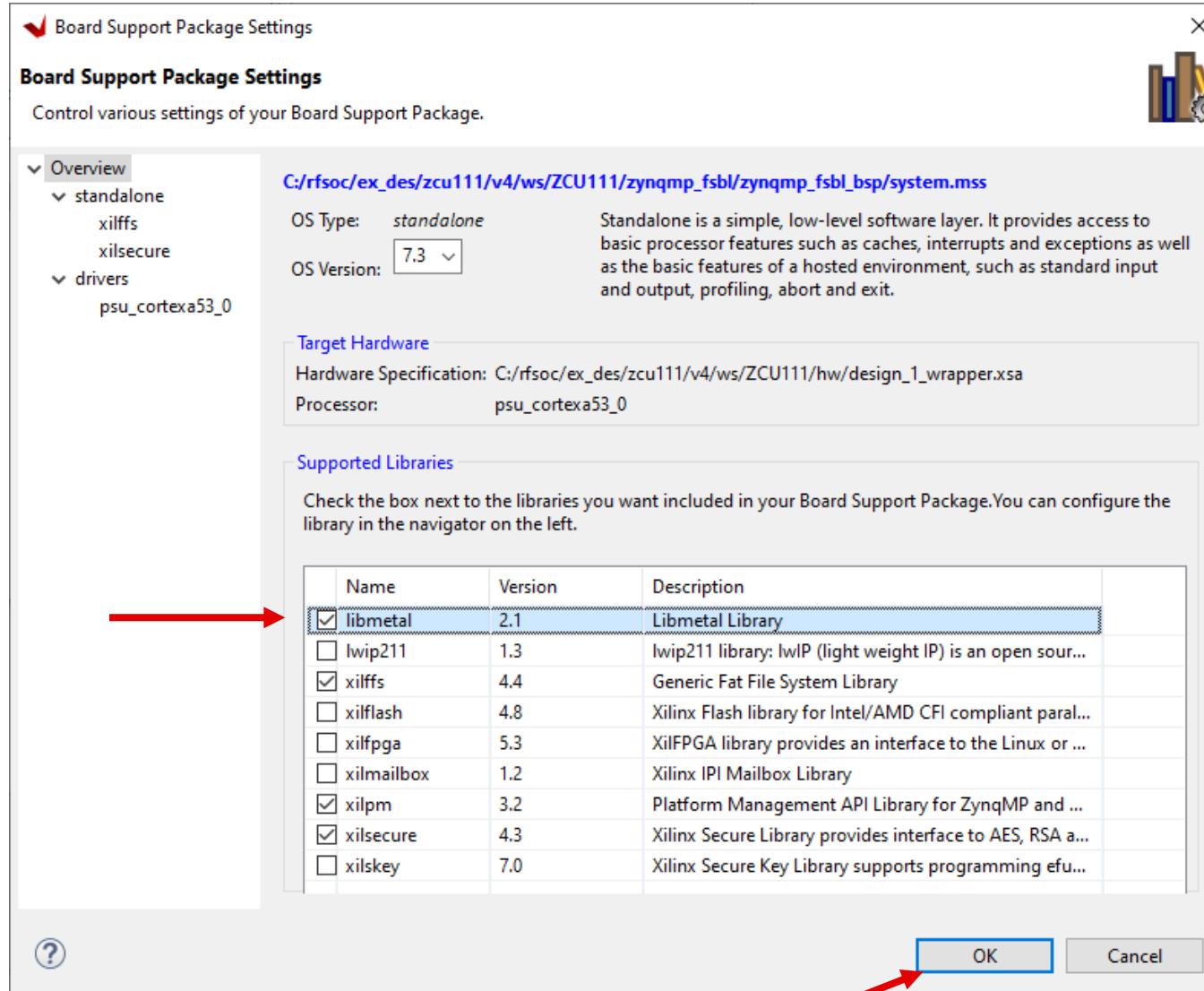


This may take
a few minutes.

Create Platform Project Cont'd

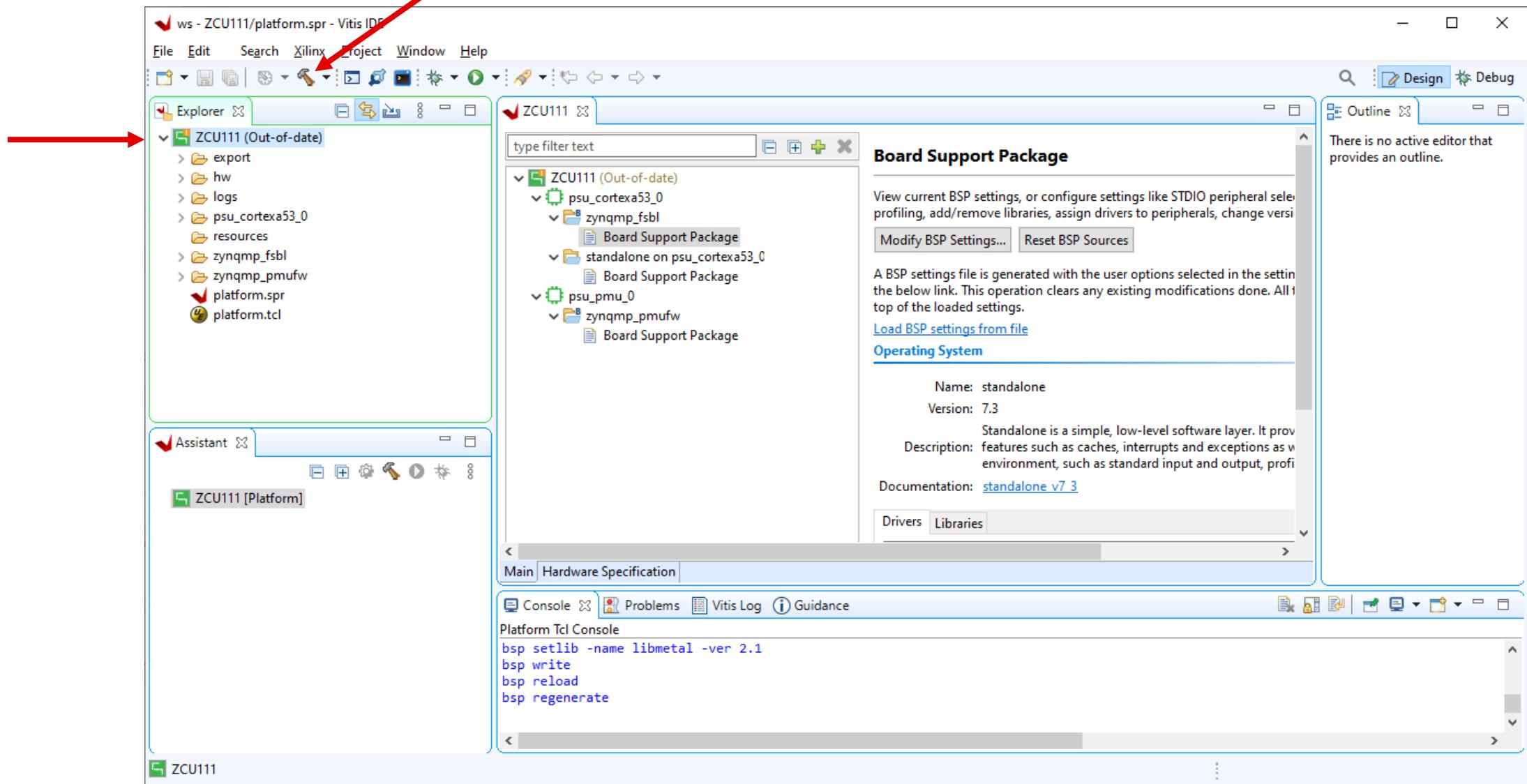


Enable libmetal

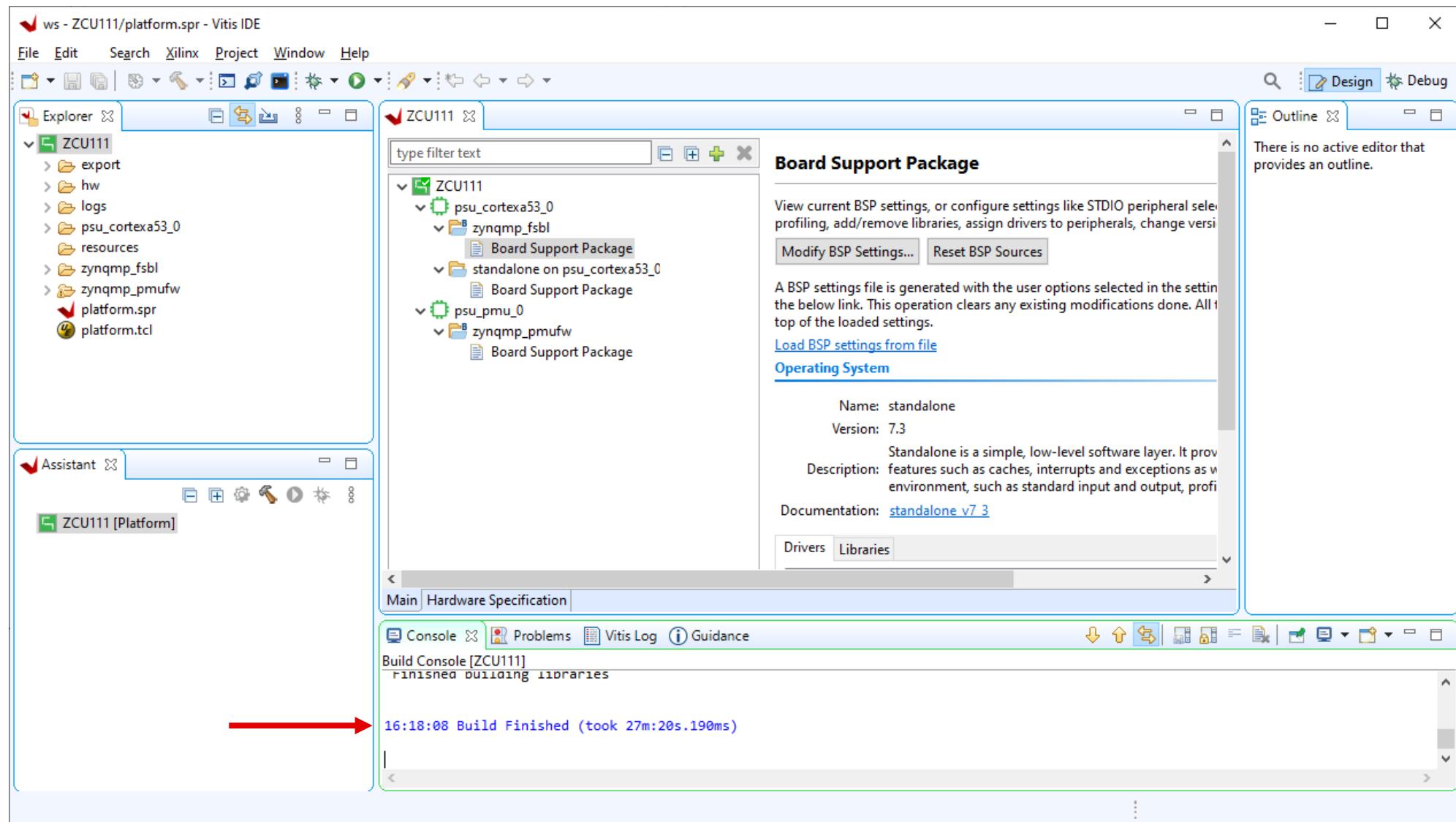


Build Project

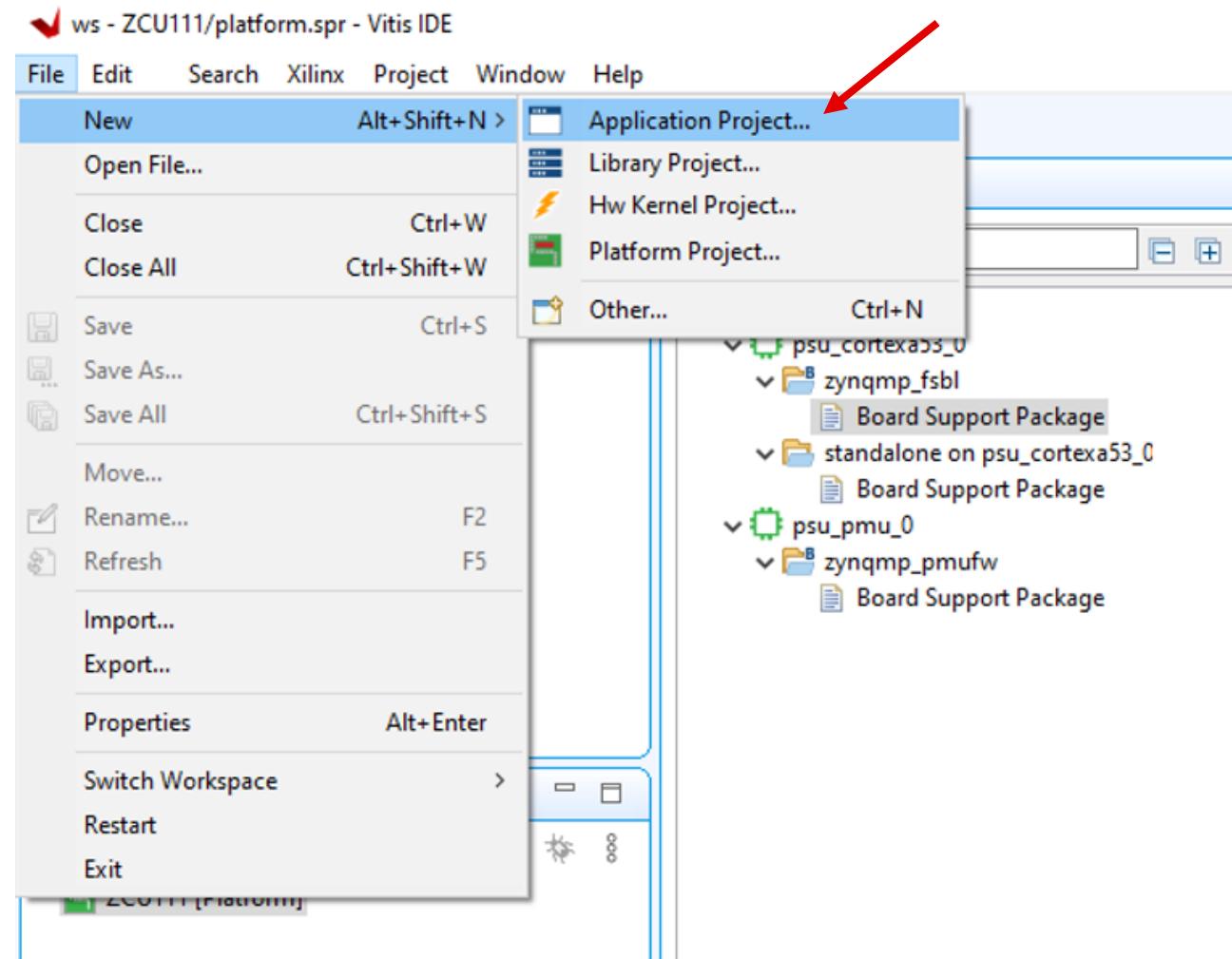
This may take
a few minutes.



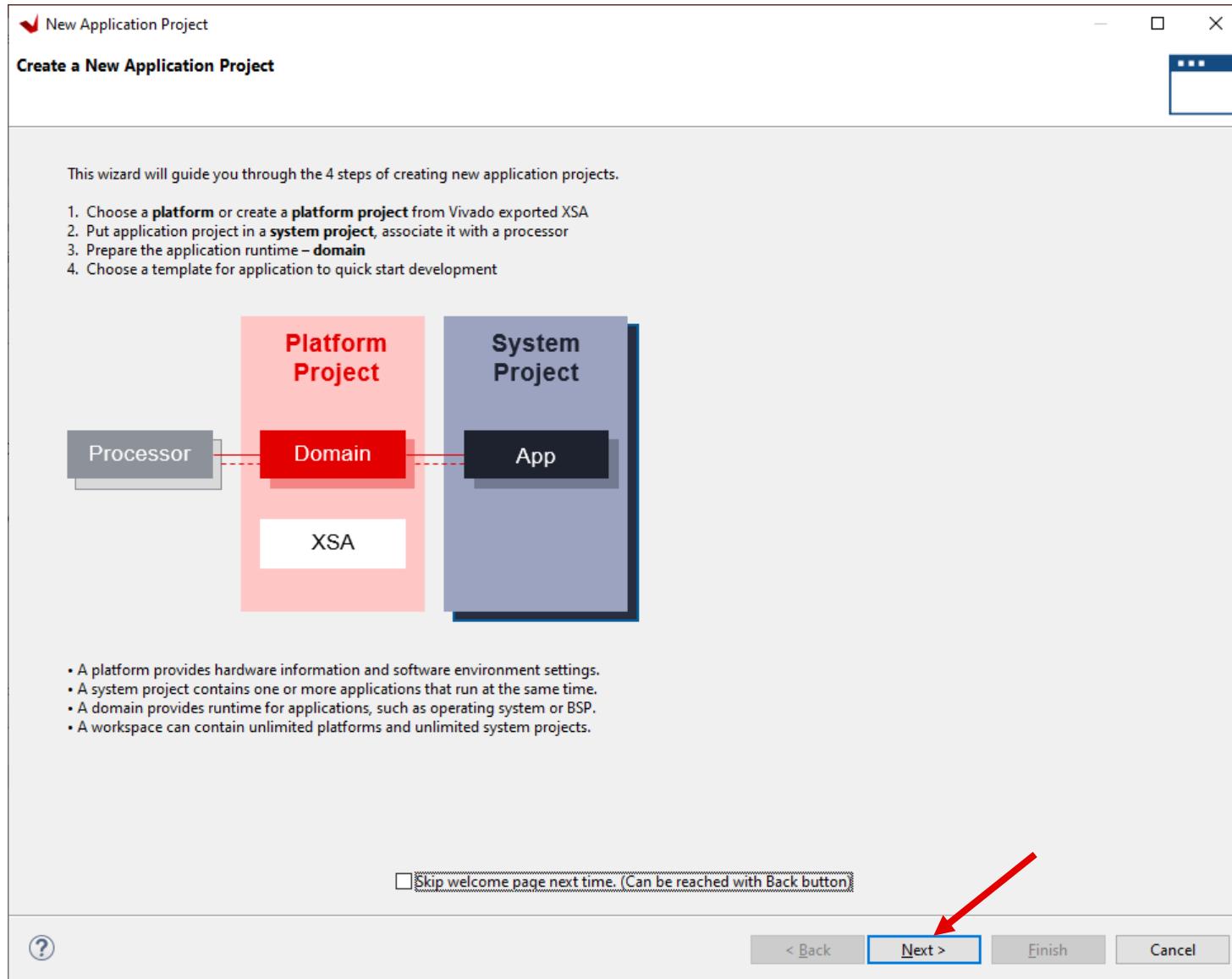
Build Complete



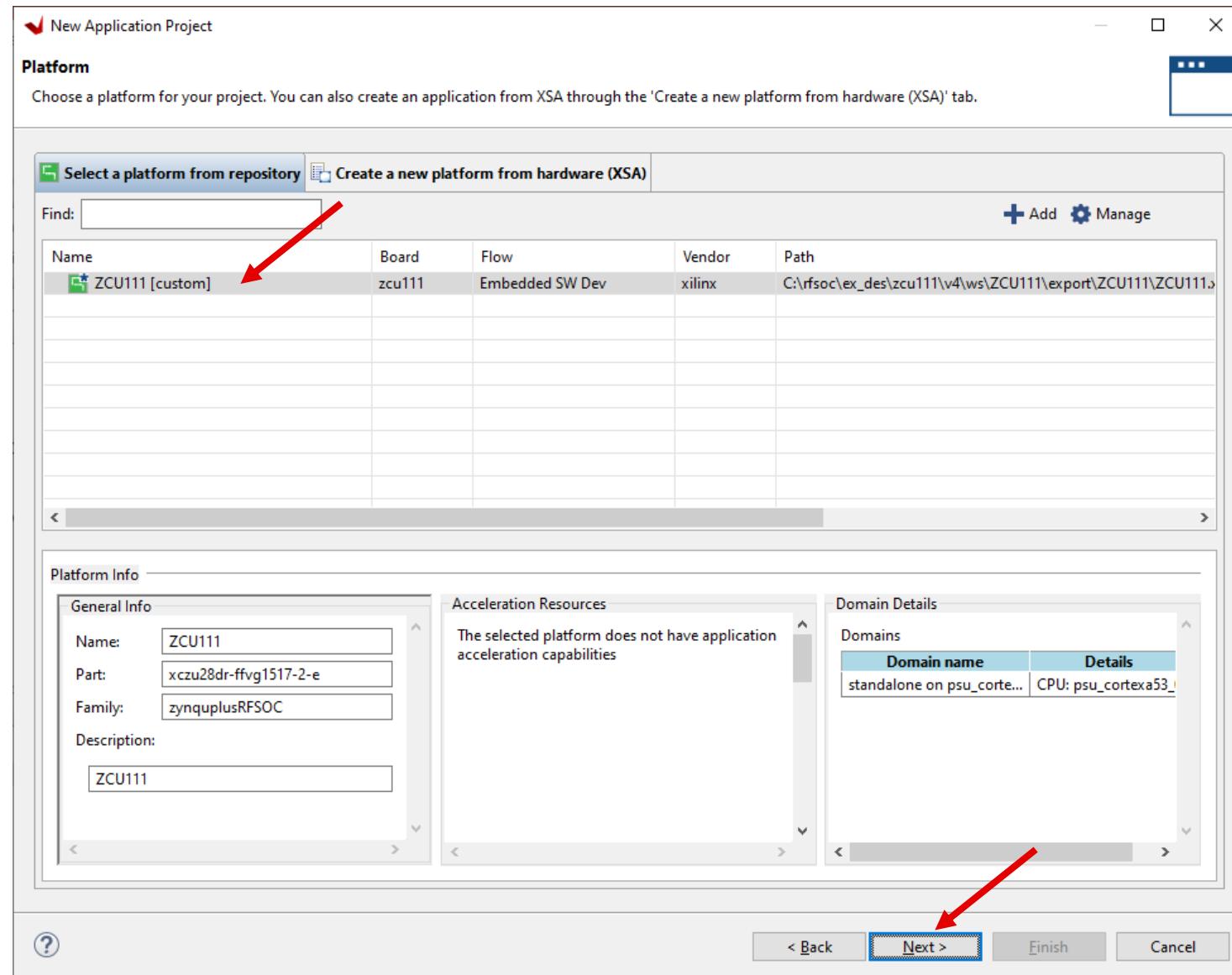
Create Application



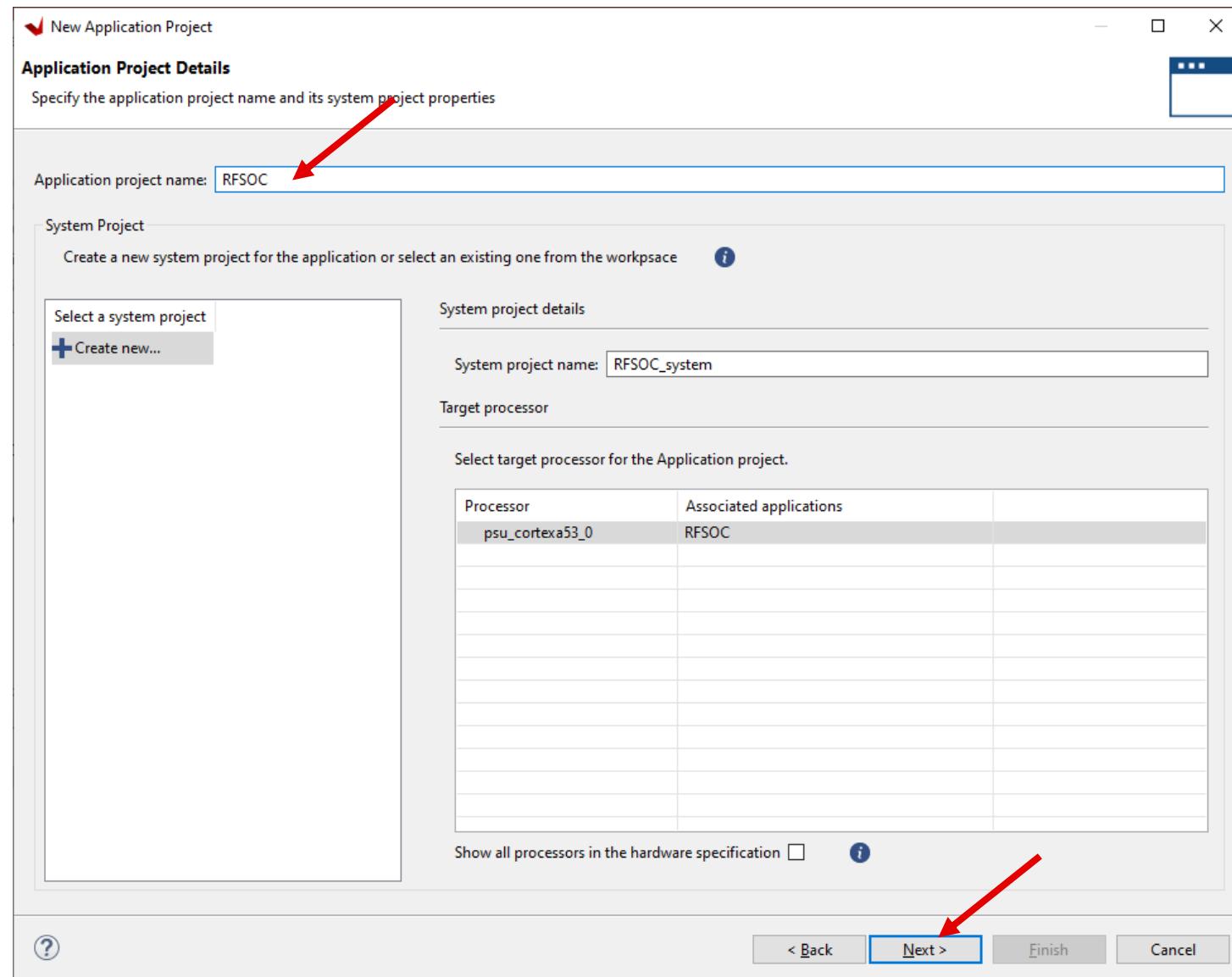
Create Application Cont'd



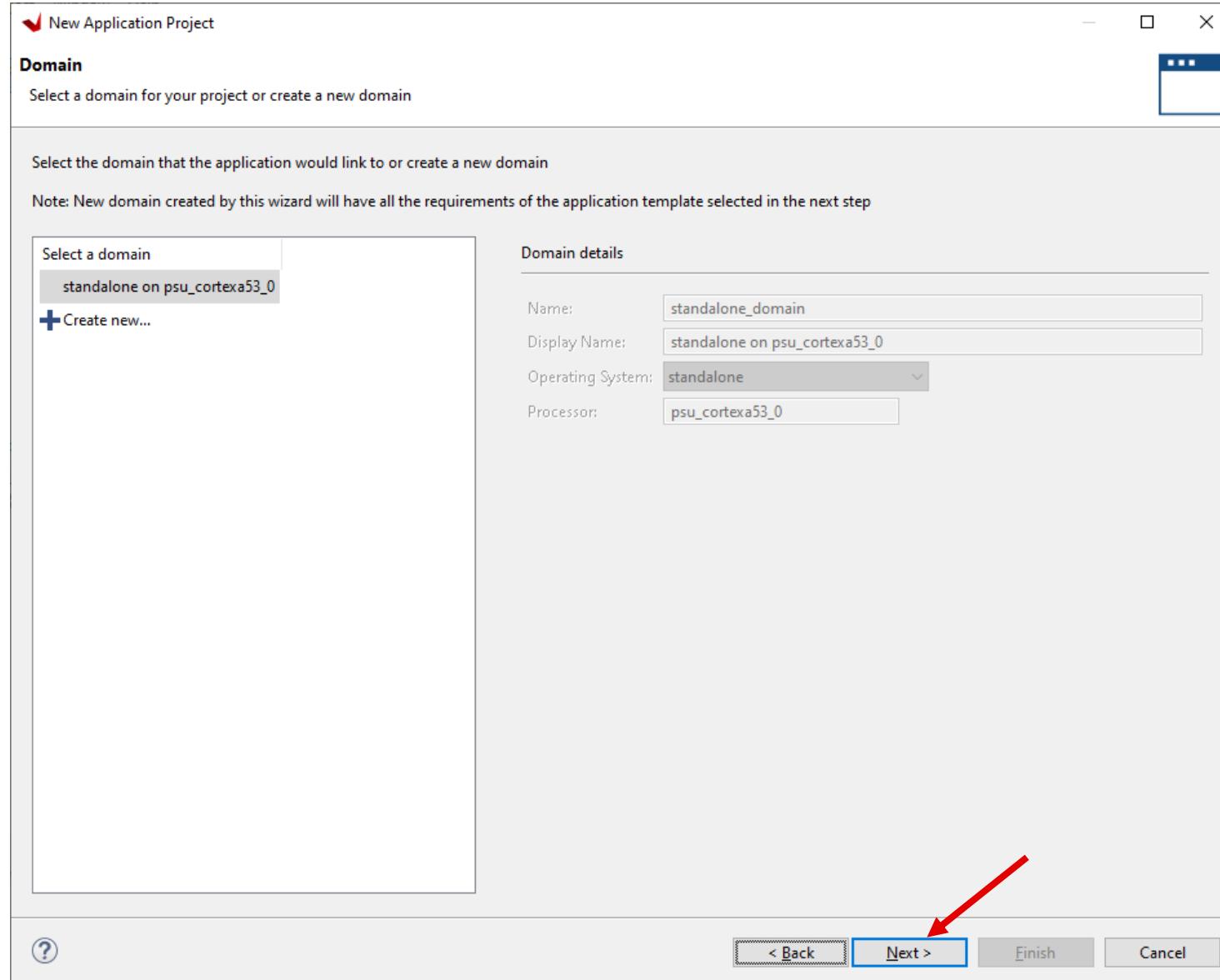
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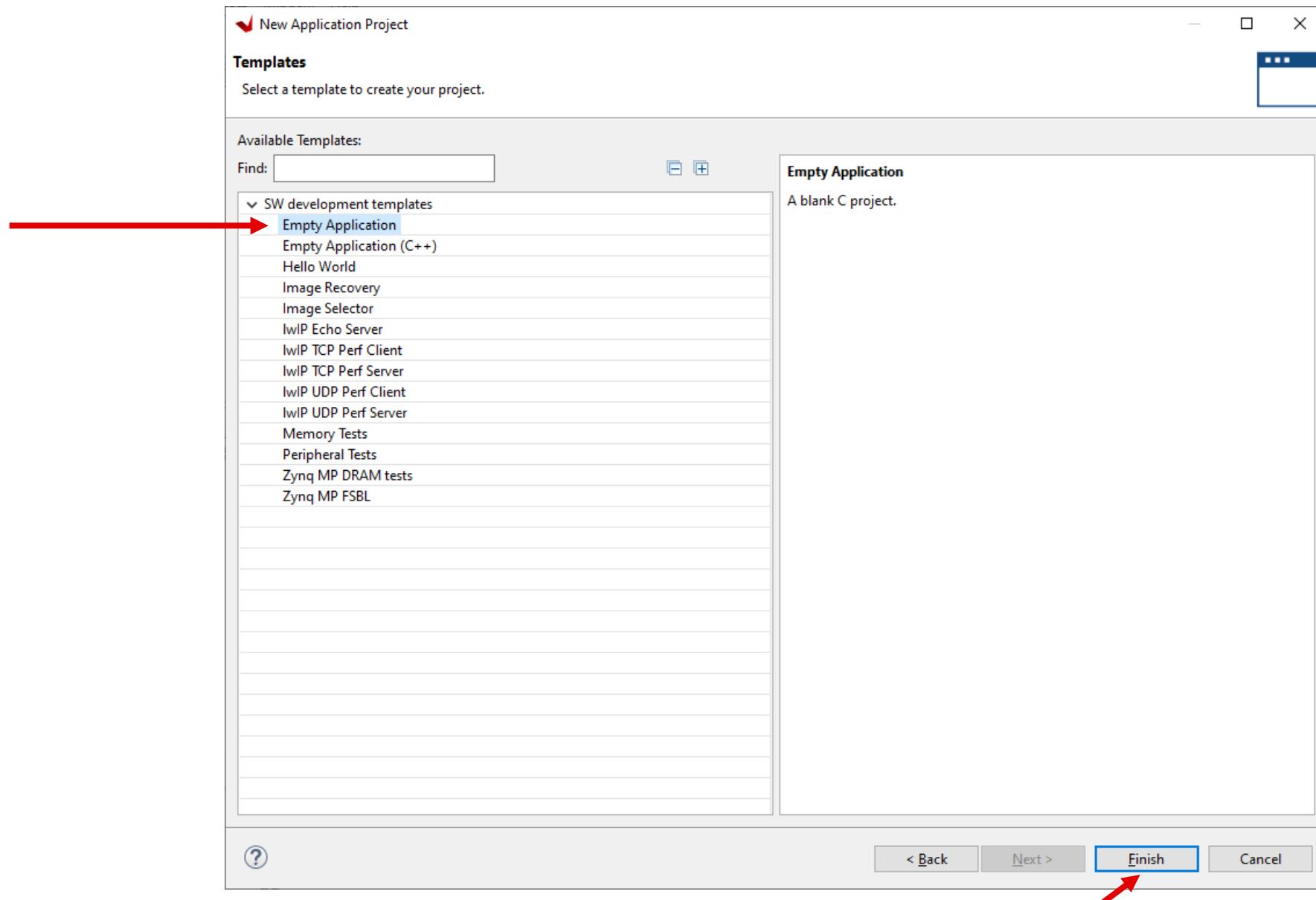
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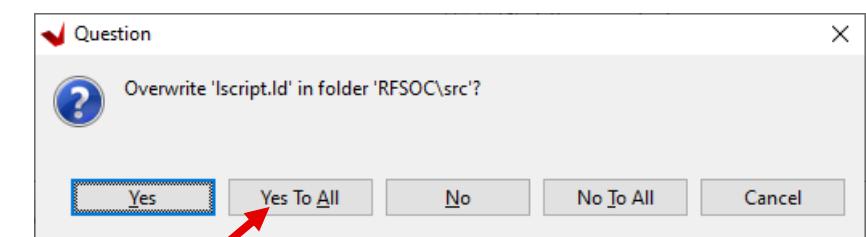
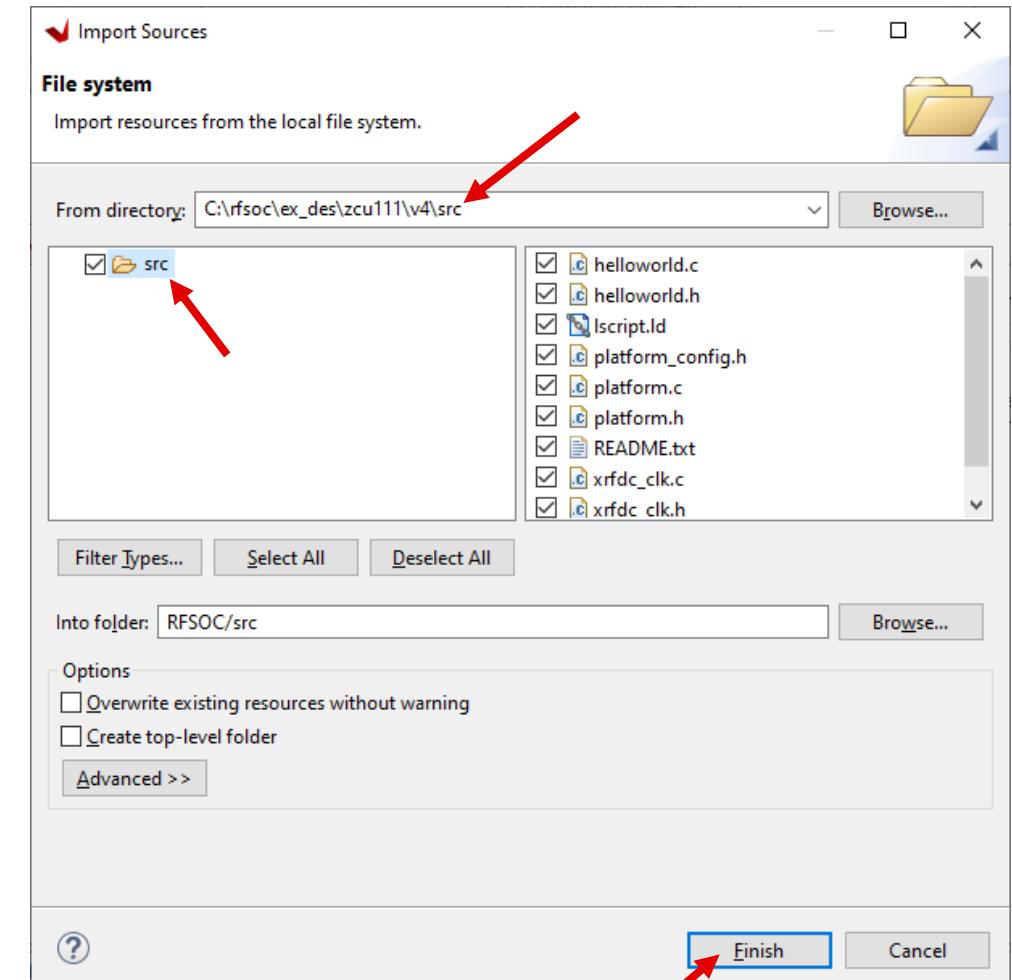
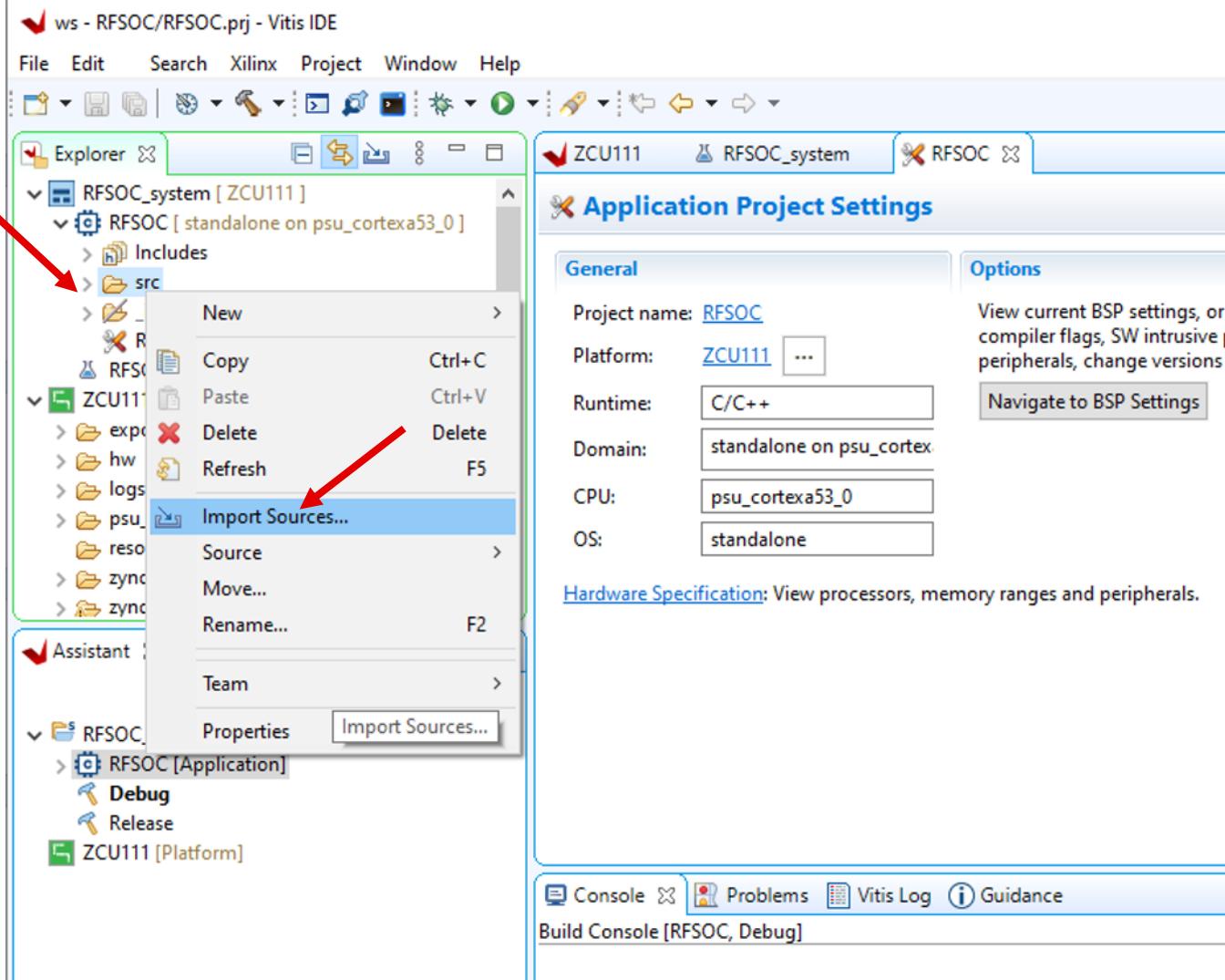
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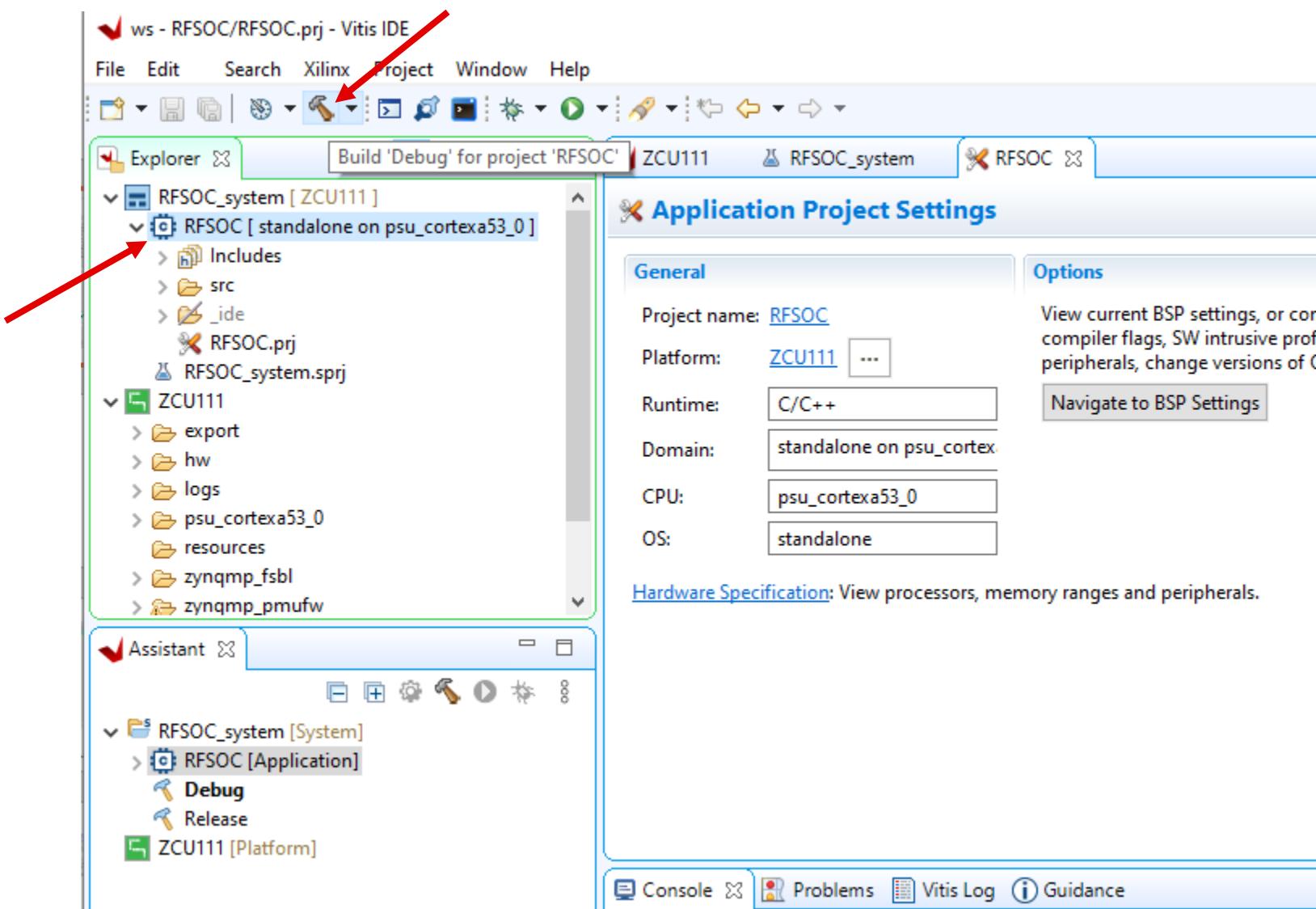
Create Application Cont'd



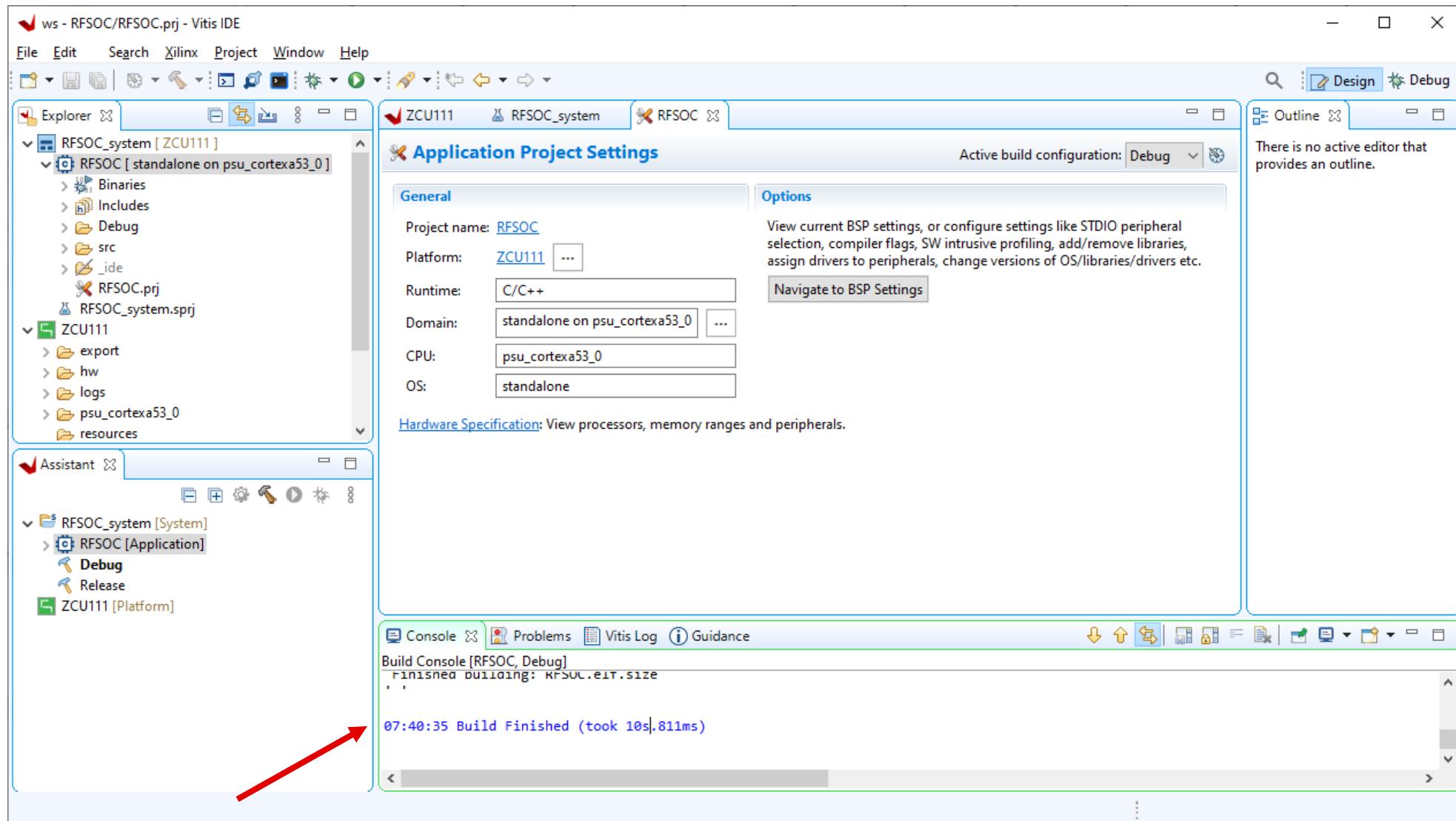
Import Sources



Build Application



Build Complete



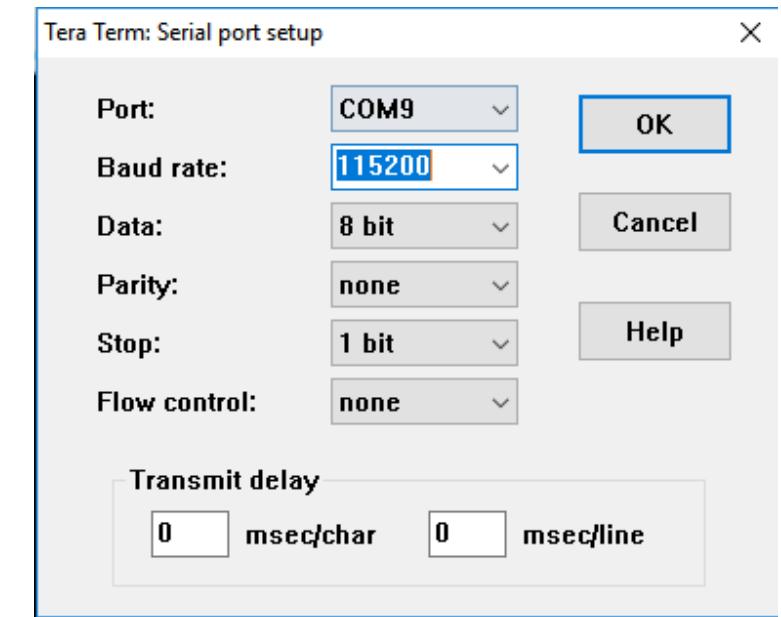
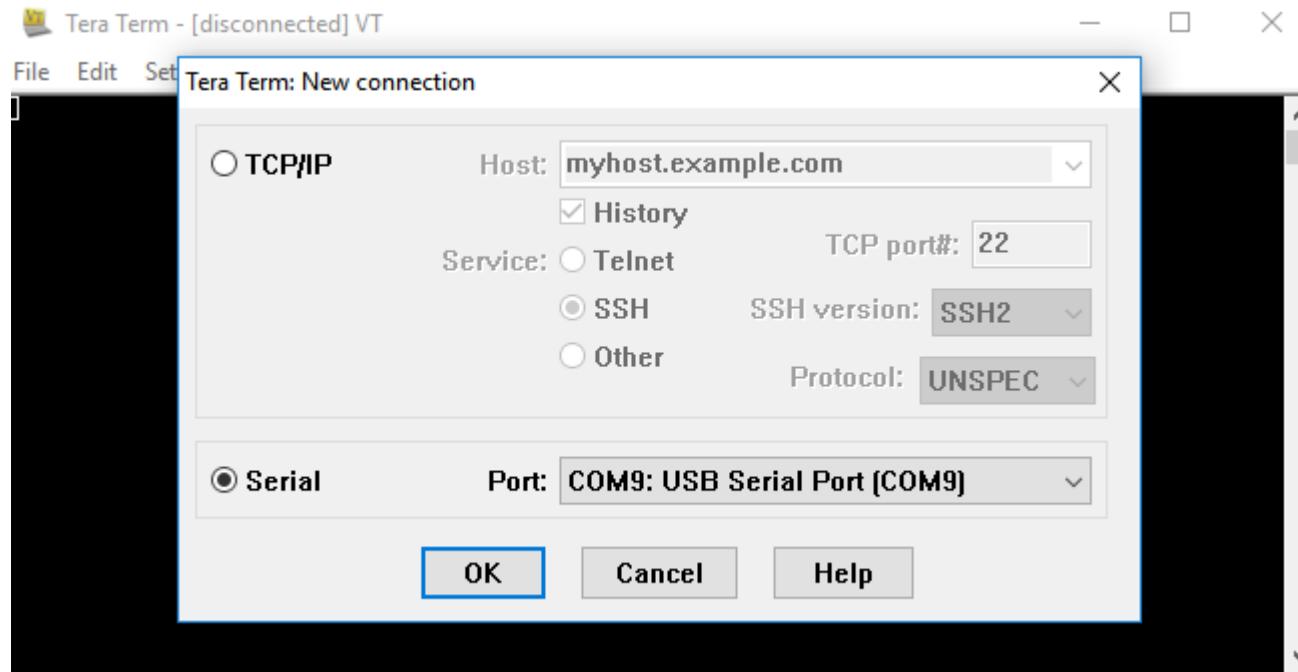


Run Design

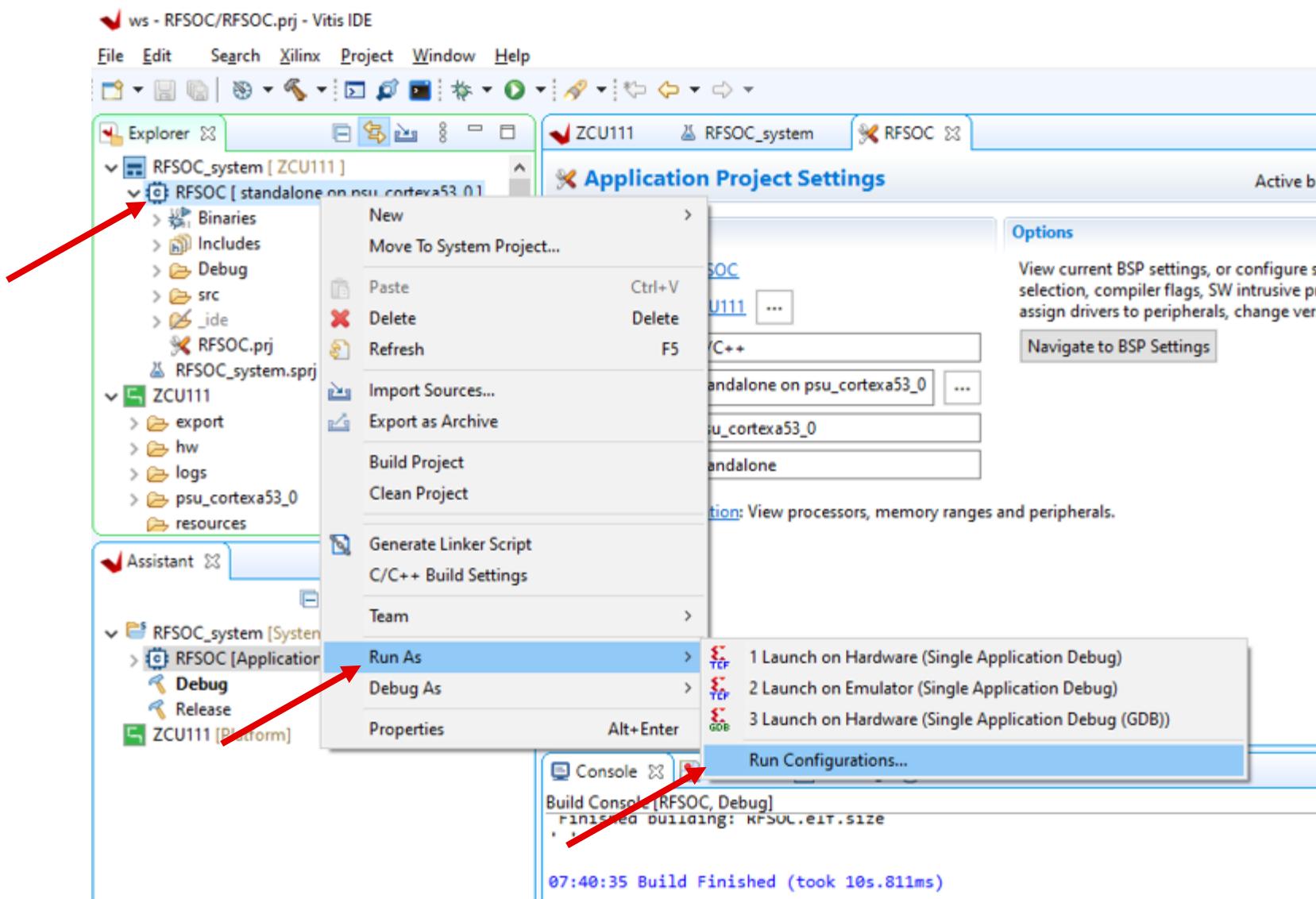
Open a Terminal Window

Open the COM port on the compute and set the rate to 115200.

TeraTerm can be used. See [UG1036](#).

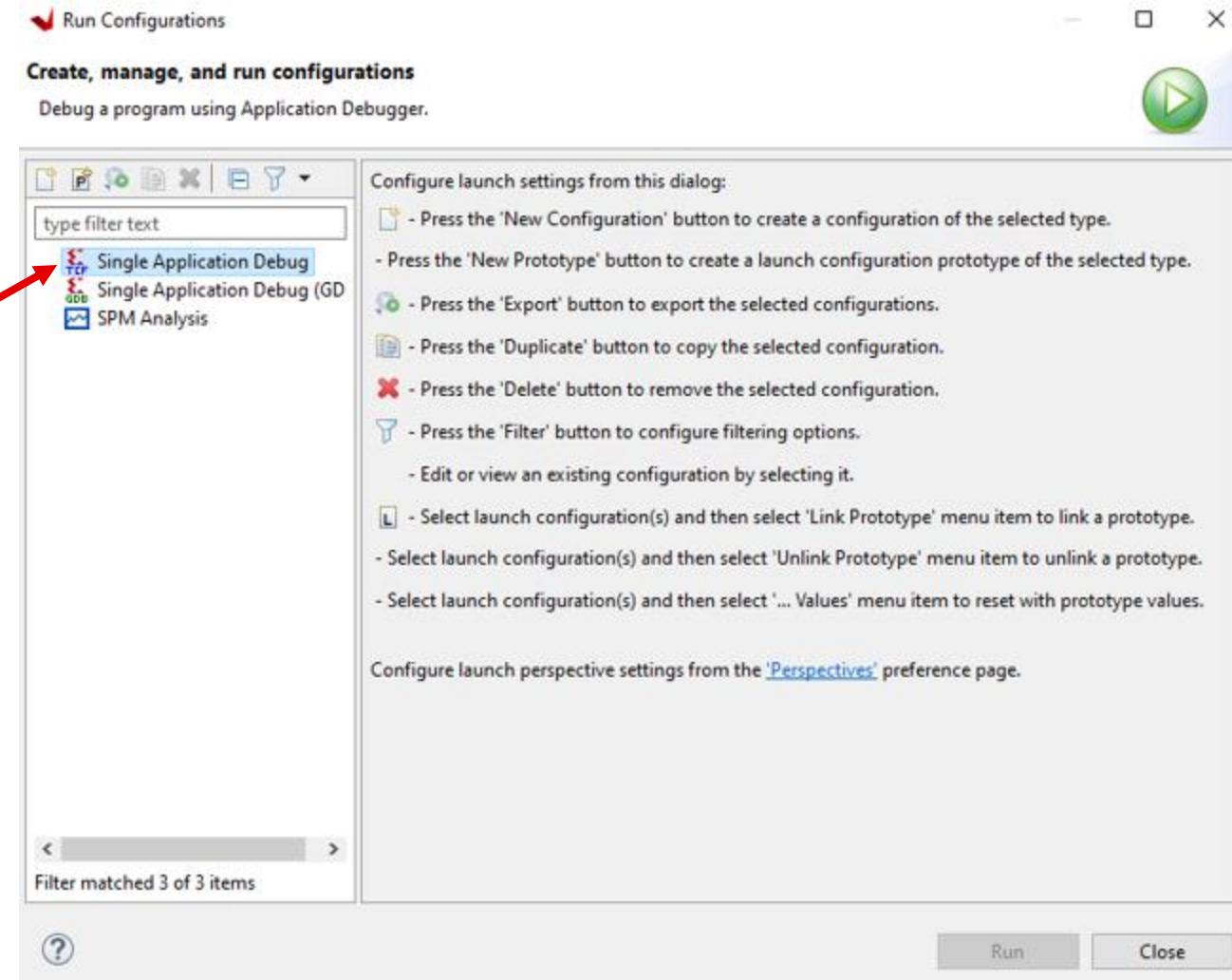


Setup Run Configuration

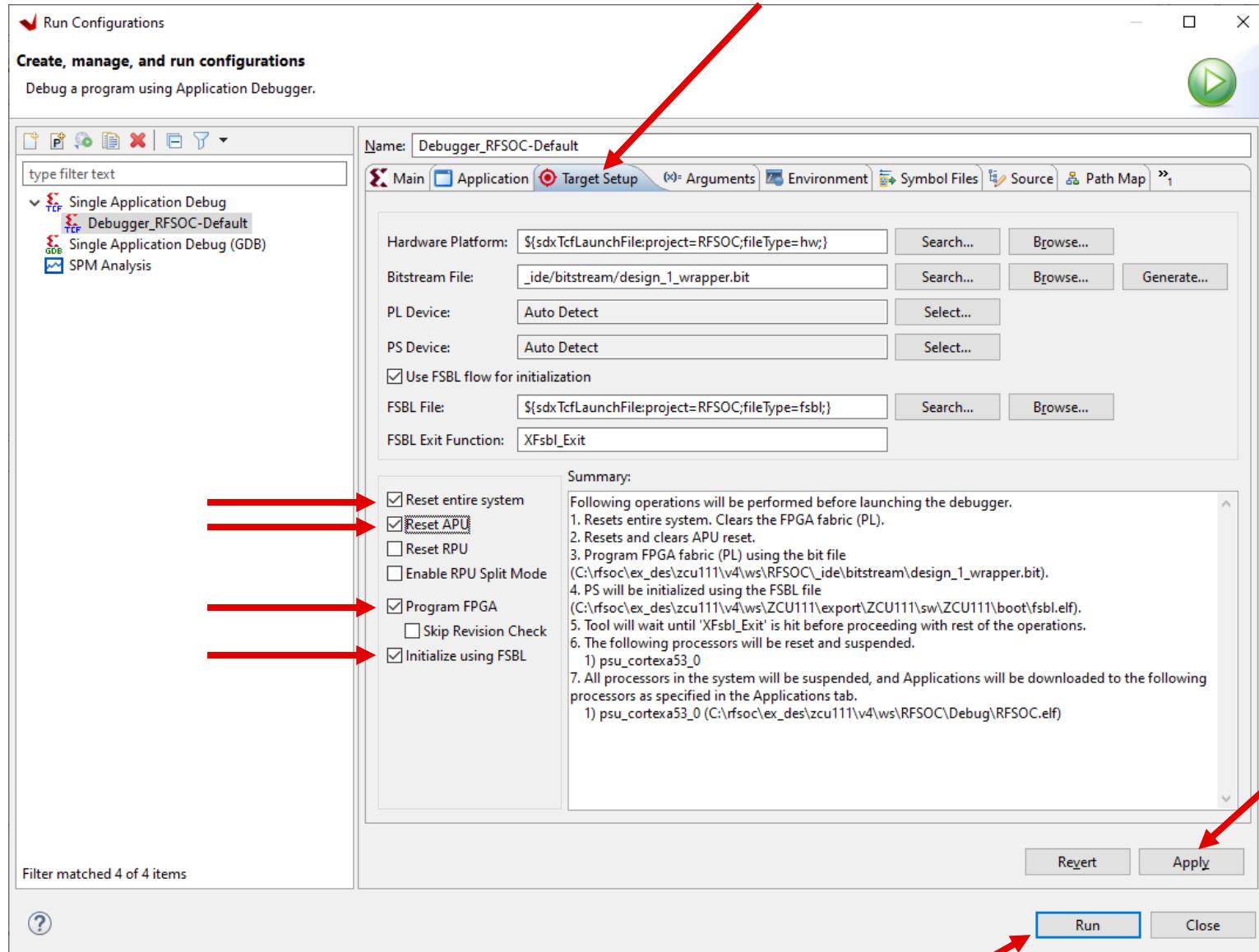


Run Configuration Cont'd

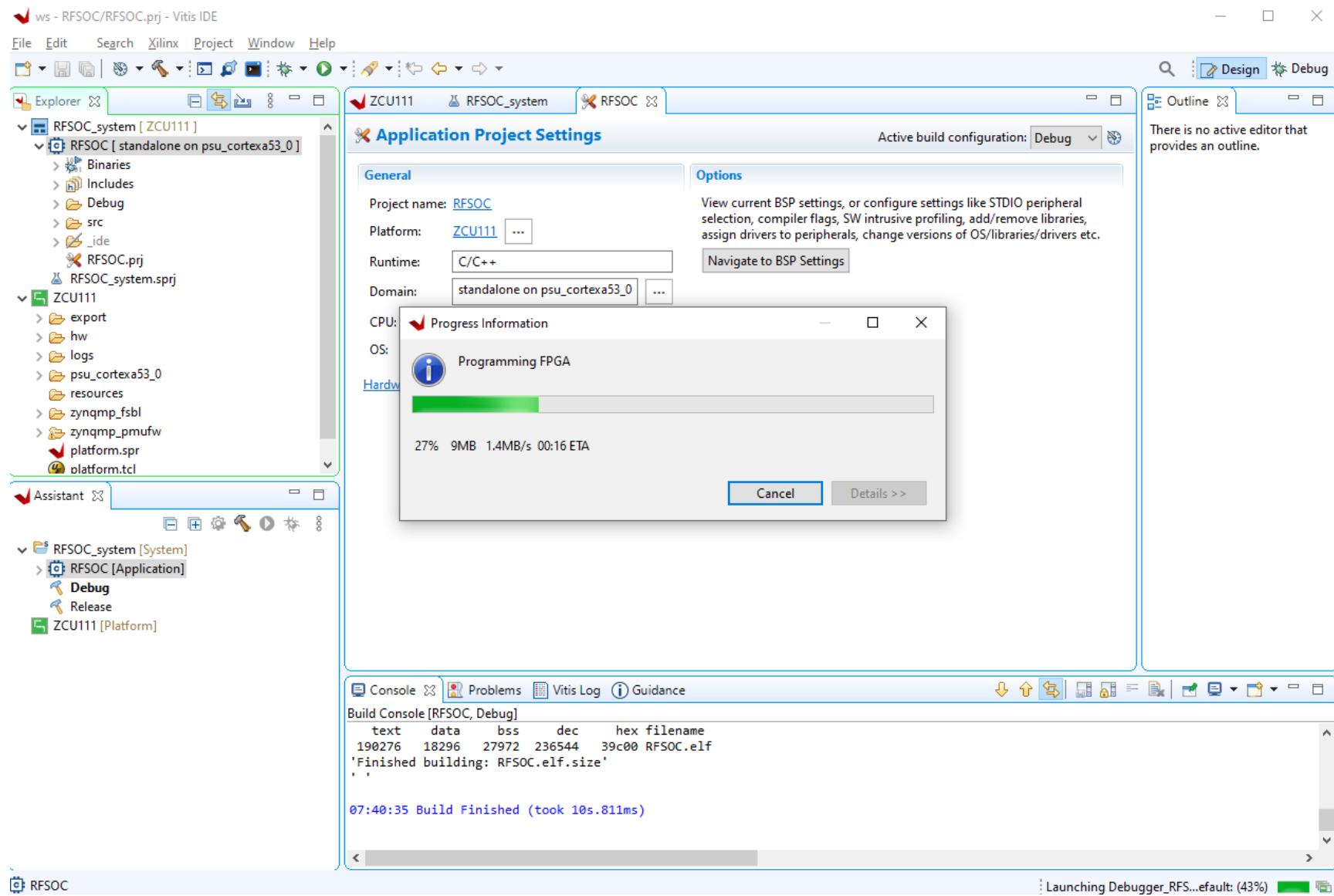
Double Click



Run Configuration Cont'd



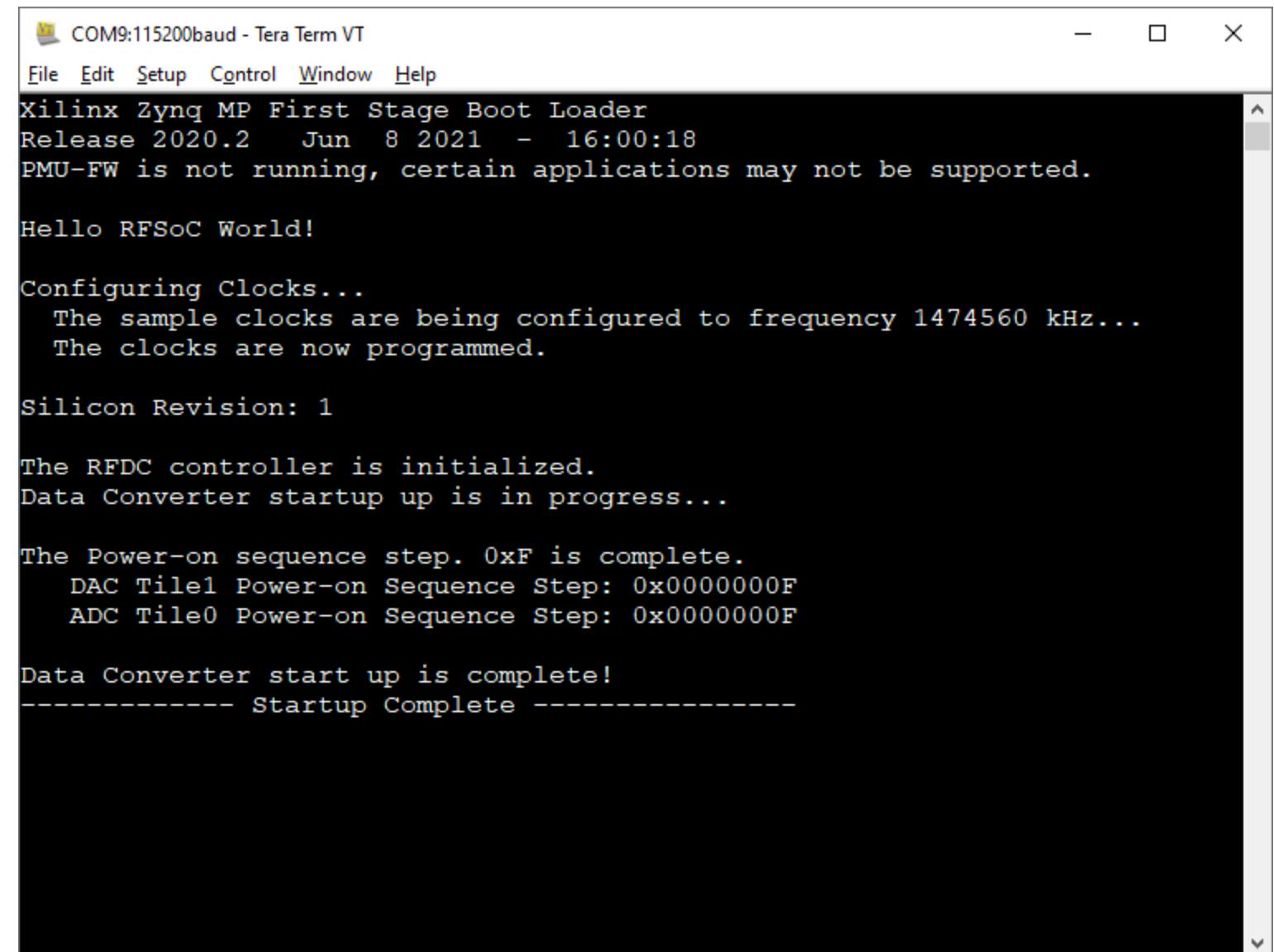
Run Design



Application Startup

The application...

1. Programs the clocks.
2. Issues the data converters master reset.
3. Displays the Power-on Sequence Step of the data converters.



COM9:115200baud - Tera Term VT

Xilinx Zynq MP First Stage Boot Loader
Release 2020.2 Jun 8 2021 - 16:00:18
PMU-FW is not running, certain applications may not be supported.

Hello RFSoC World!

Configuring Clocks...
The sample clocks are being configured to frequency 1474560 kHz...
The clocks are now programmed.

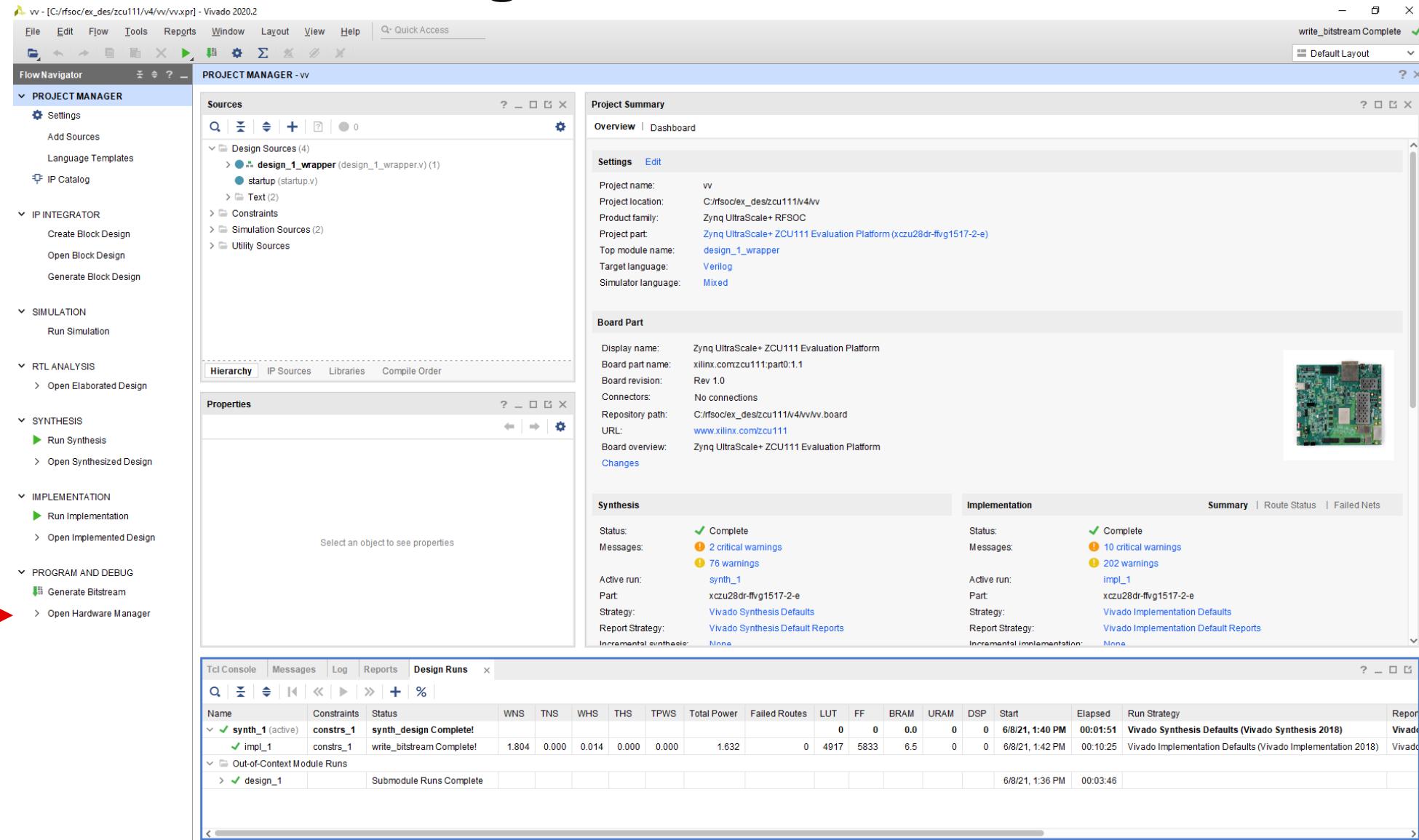
Silicon Revision: 1

The RFDC controller is initialized.
Data Converter startup up is in progress...

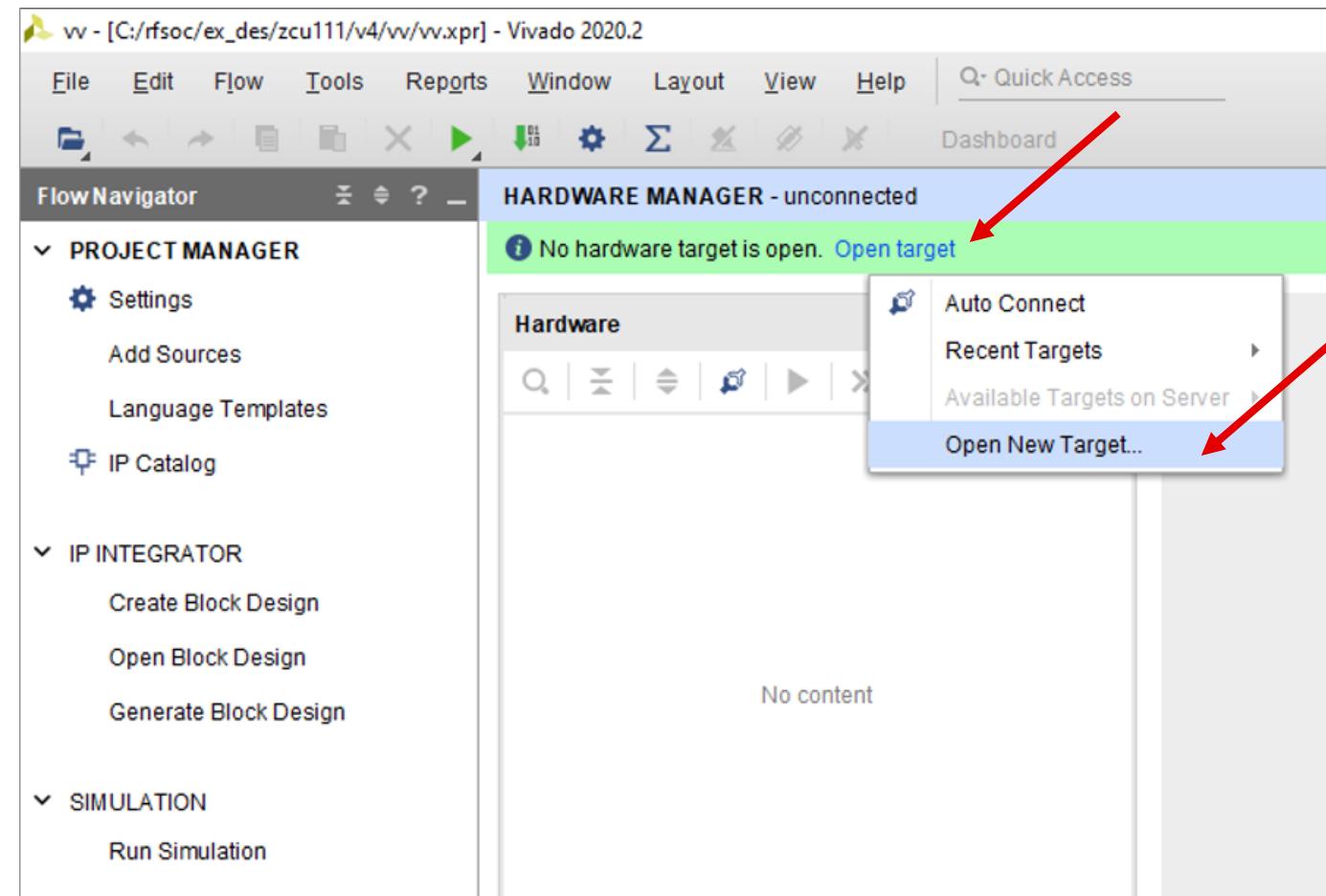
The Power-on sequence step. 0xF is complete.
DAC Tile1 Power-on Sequence Step: 0x0000000F
ADC Tile0 Power-on Sequence Step: 0x0000000F

Data Converter start up is complete!
----- Startup Complete -----

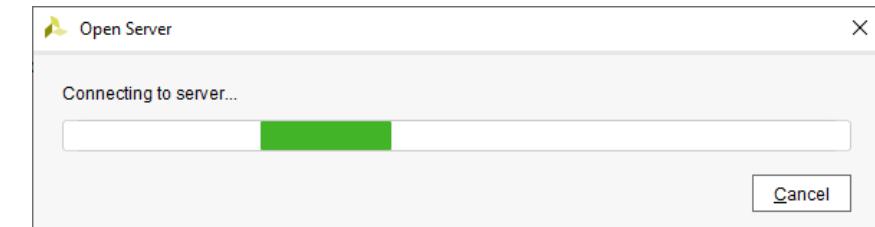
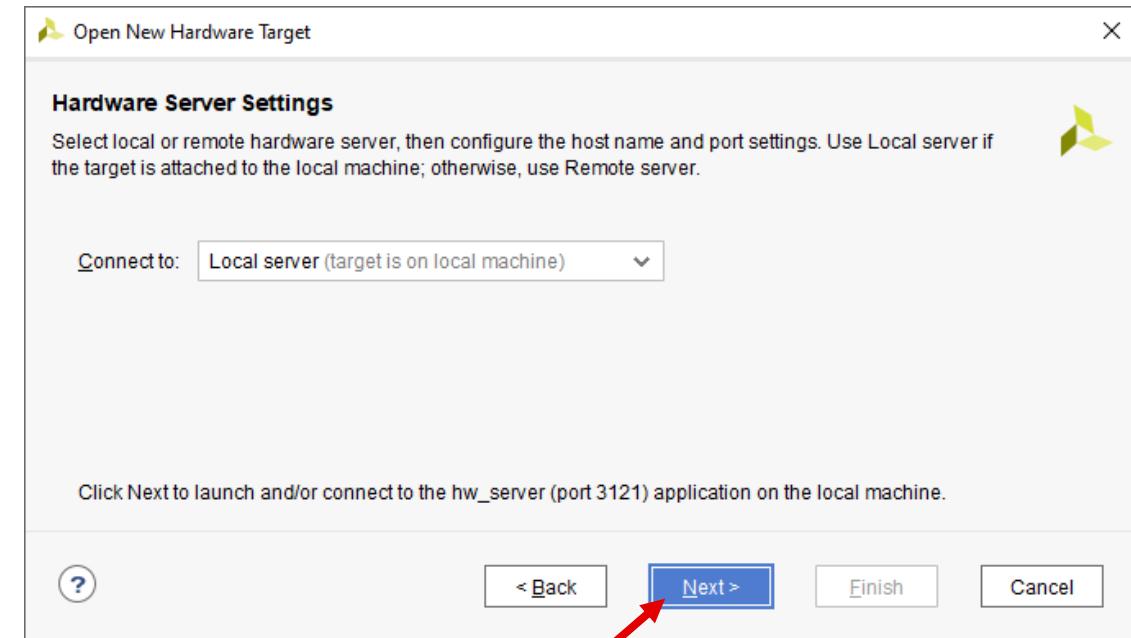
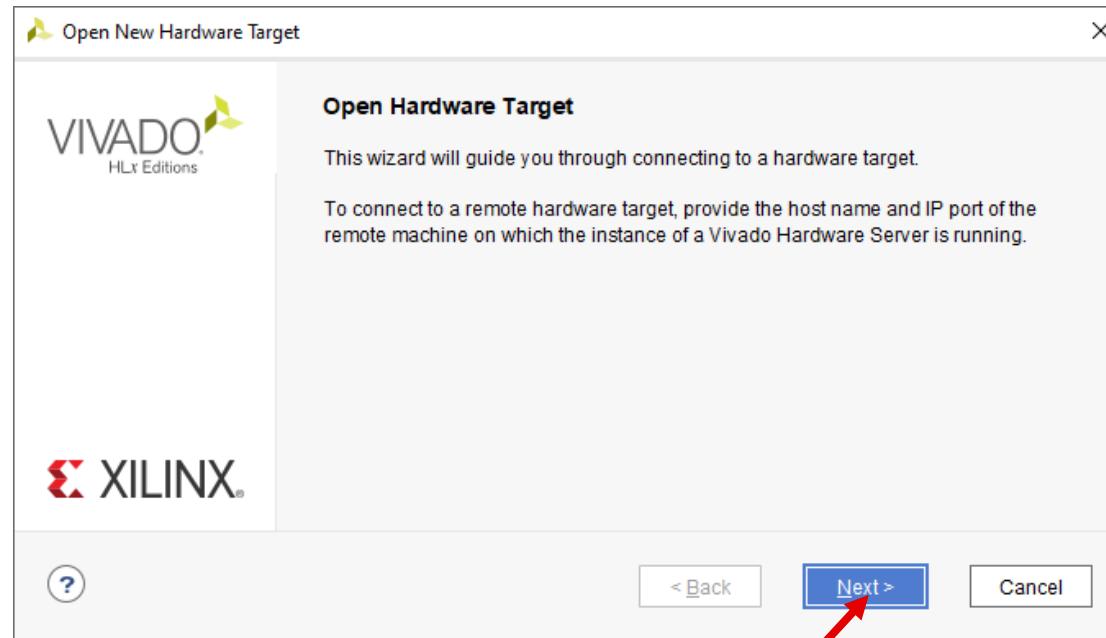
Open Hardware Manager



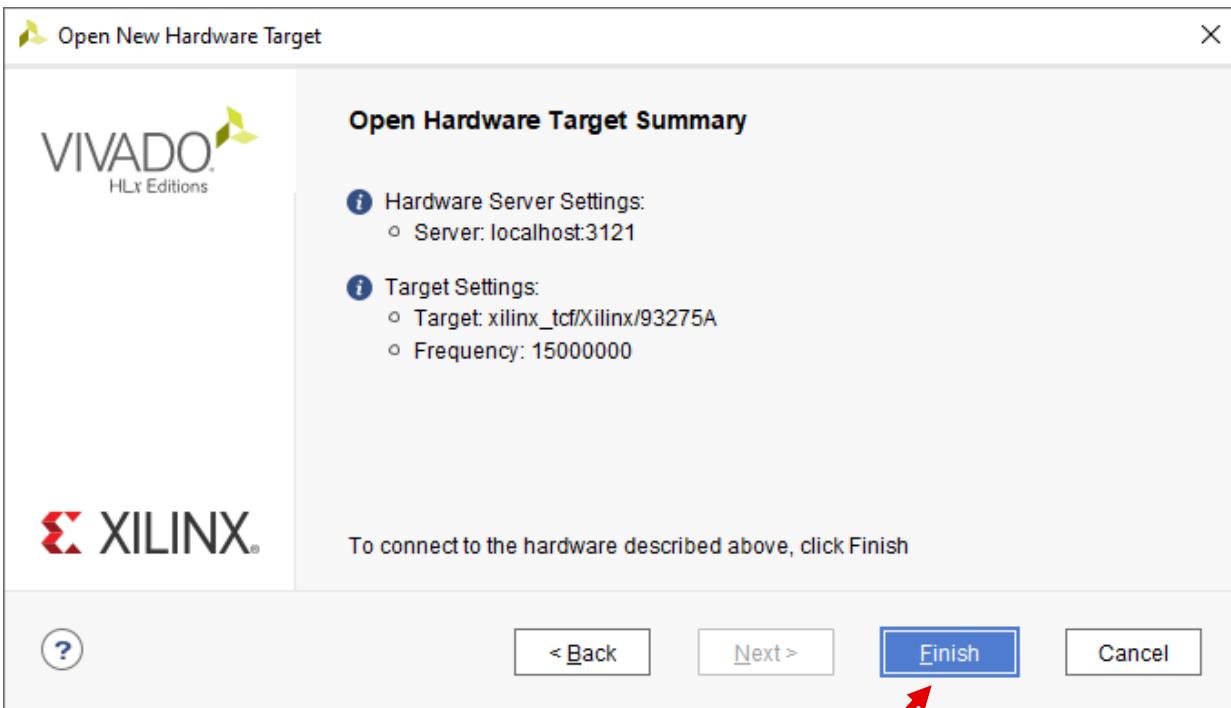
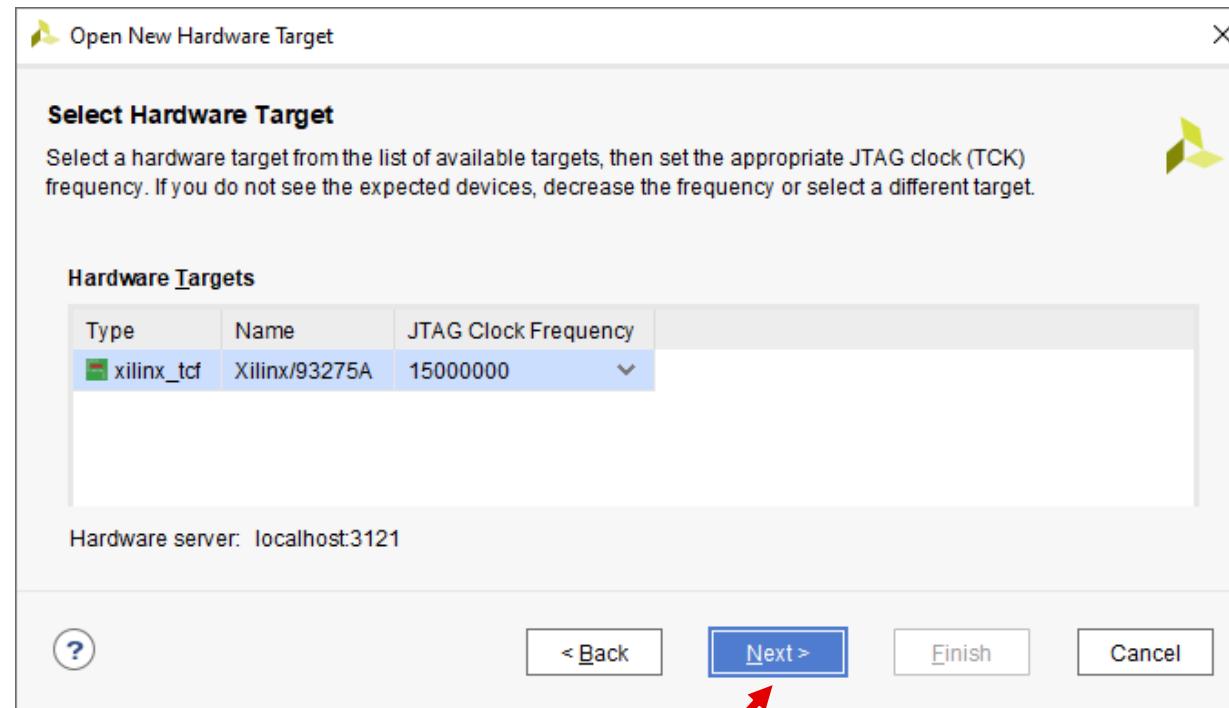
Open New Target



Open Hardware Target



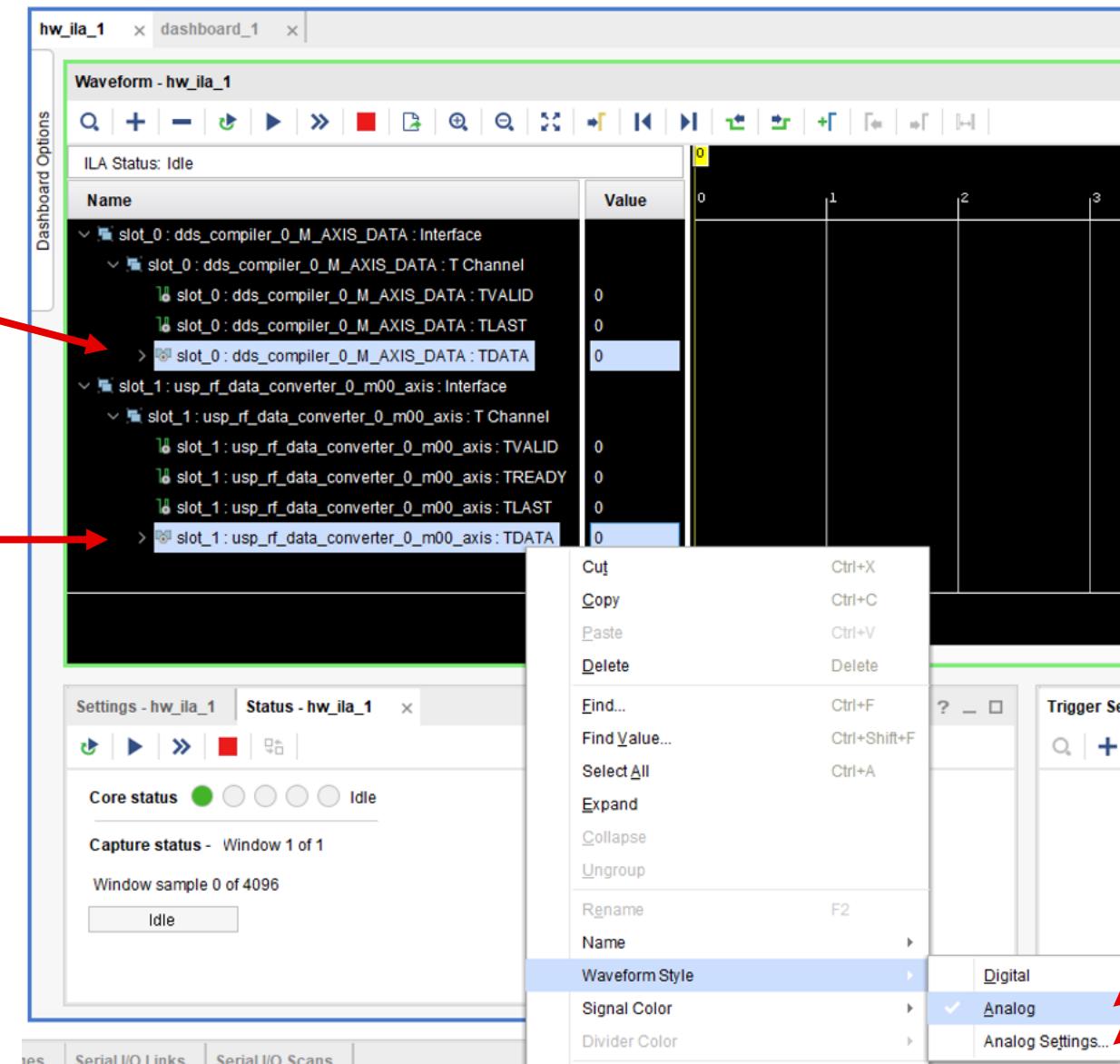
Open Hardware Target Cont'd



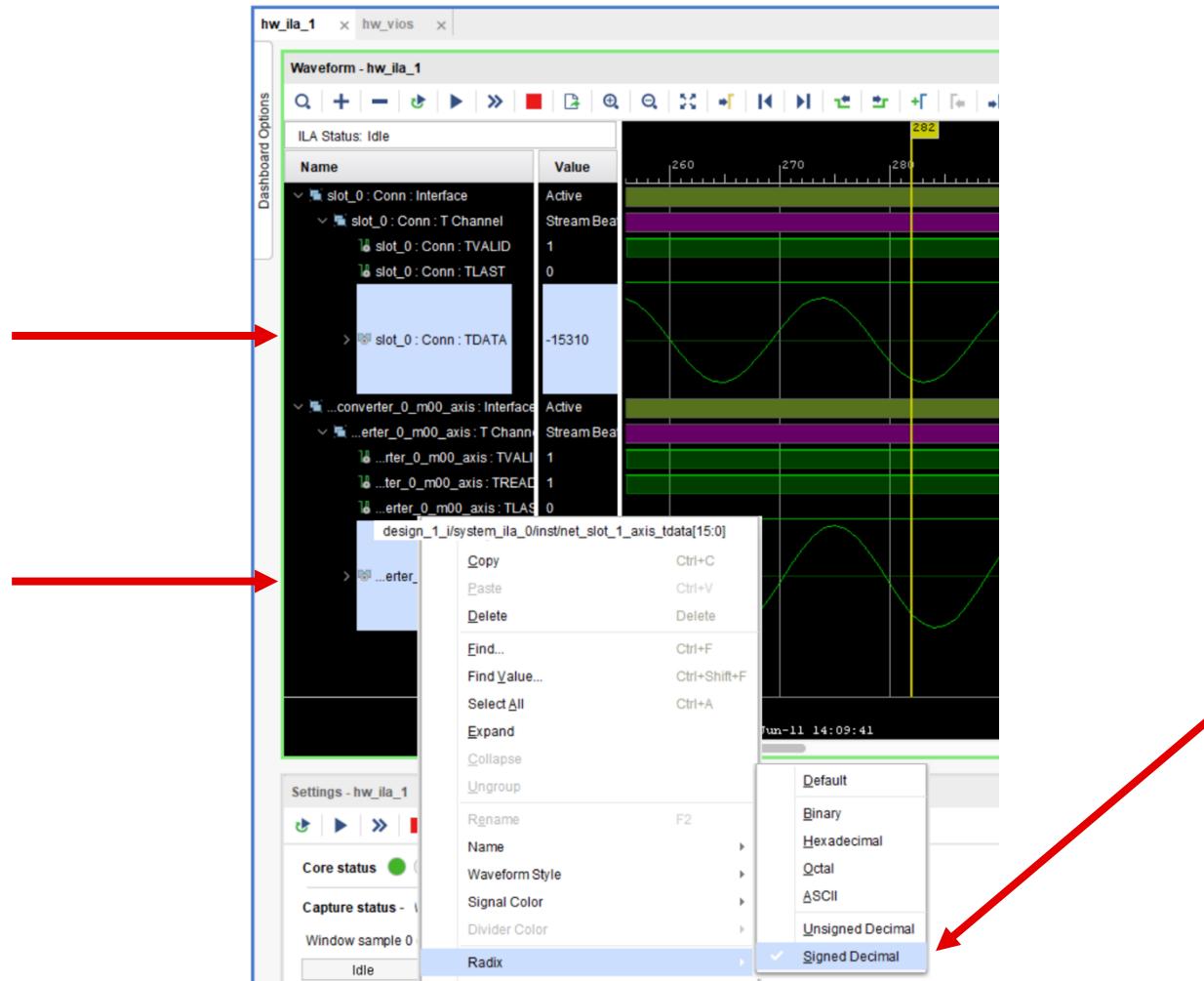
Convert Data to the Analog Waveform Style

10MHz sine wave
going from the DDS
compiler to the DAC.

ADC capture to the
System ILA.



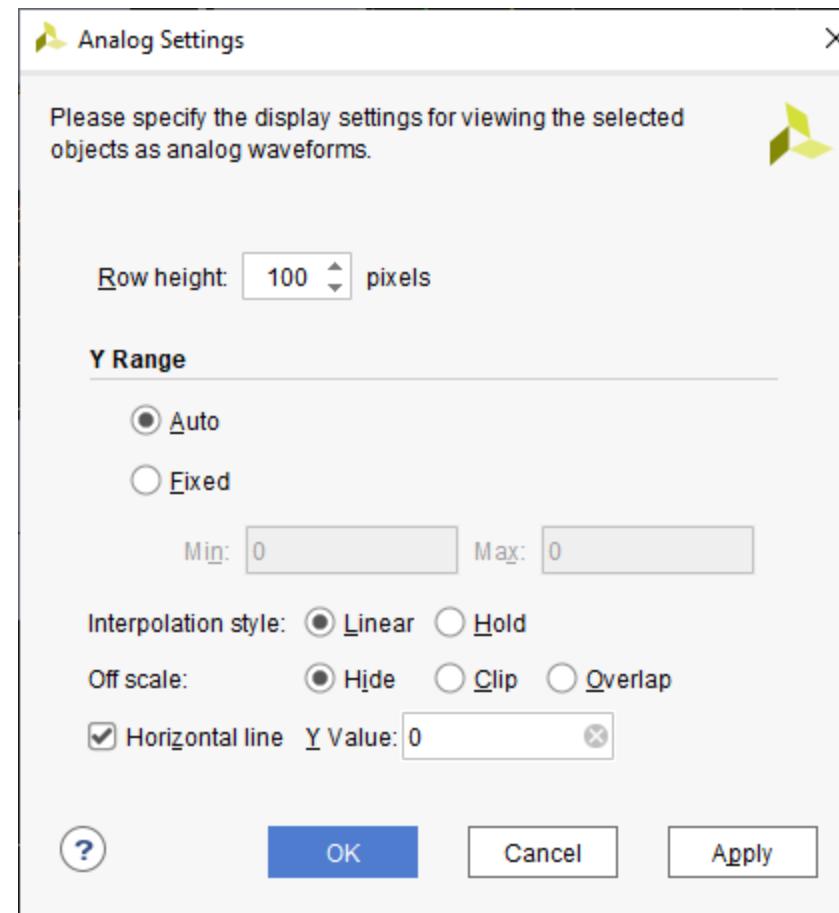
Radix



Use Radix of Signed Decimal.

Analog Settings

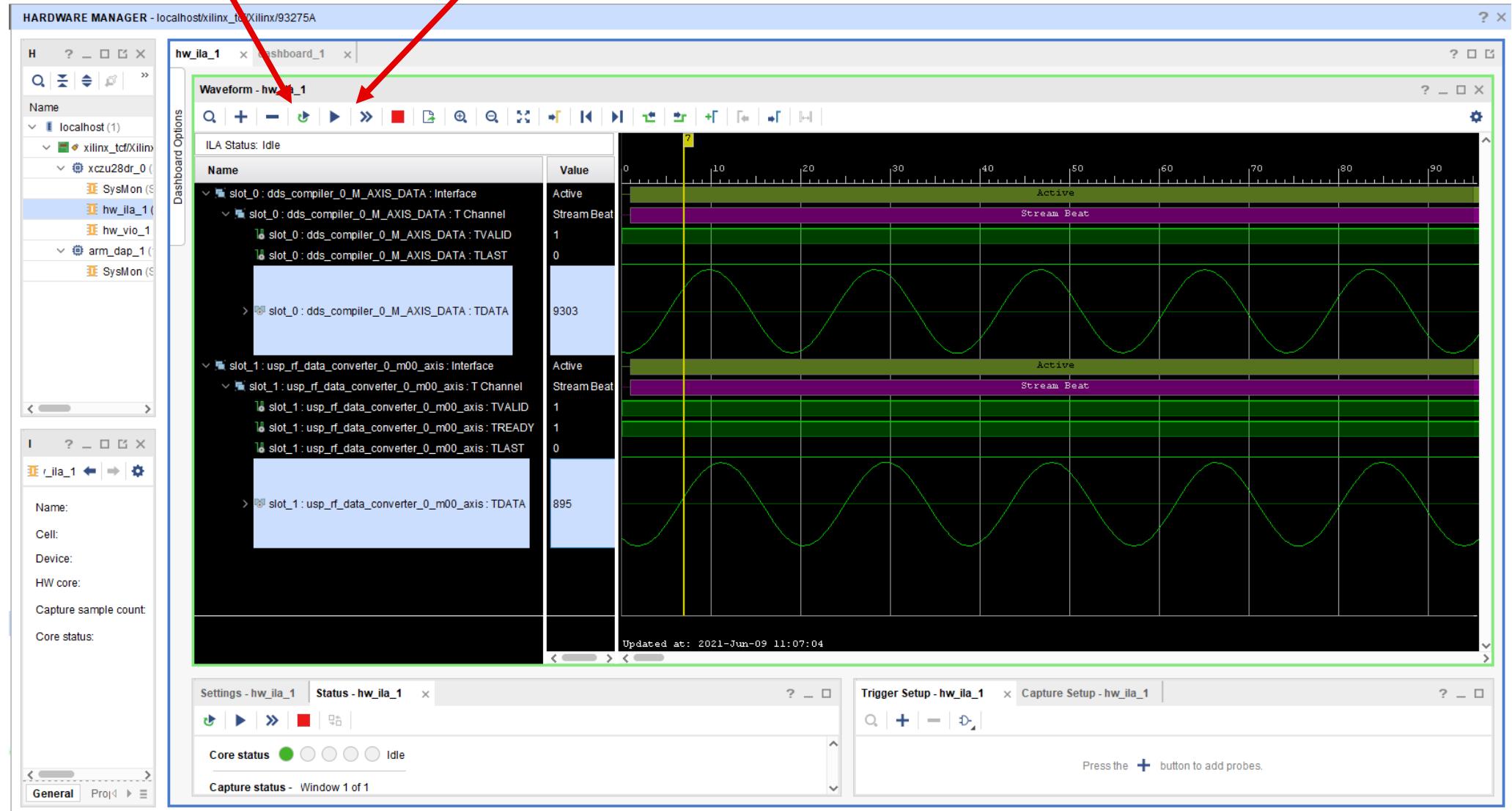
Set Row height to 100.



System ILA Capture

Automatically retrigger

Trigger ILA capture

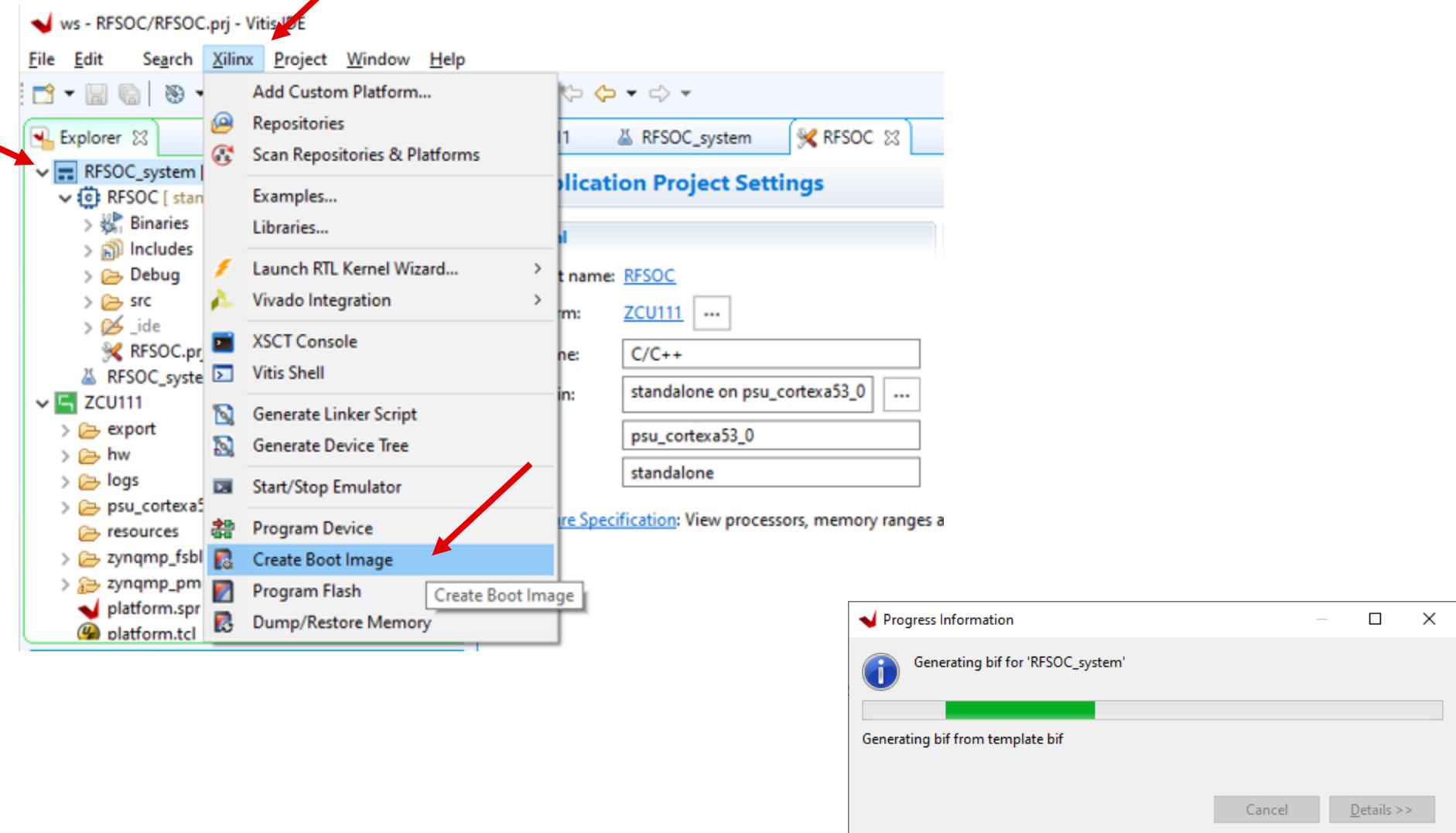




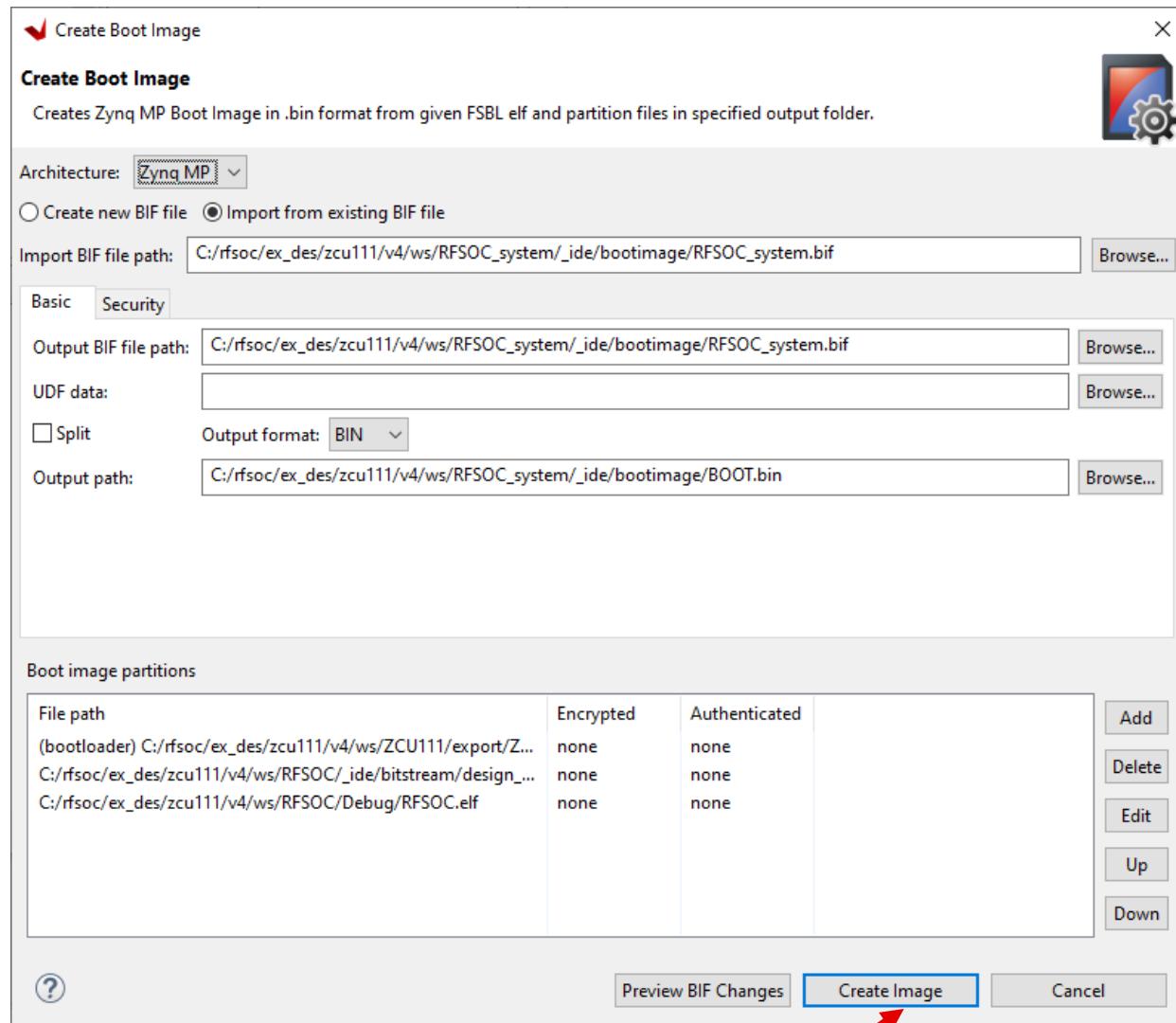
Boot Image

Create Boot Image

To run the application from the SD card rather than directly from Vitis™, create the boot.bin file



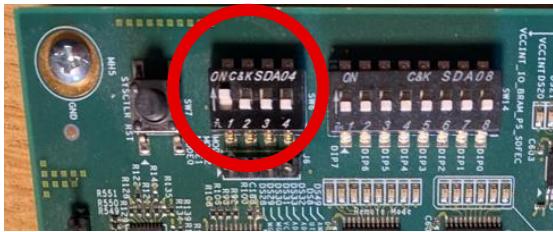
Create boot.bin file



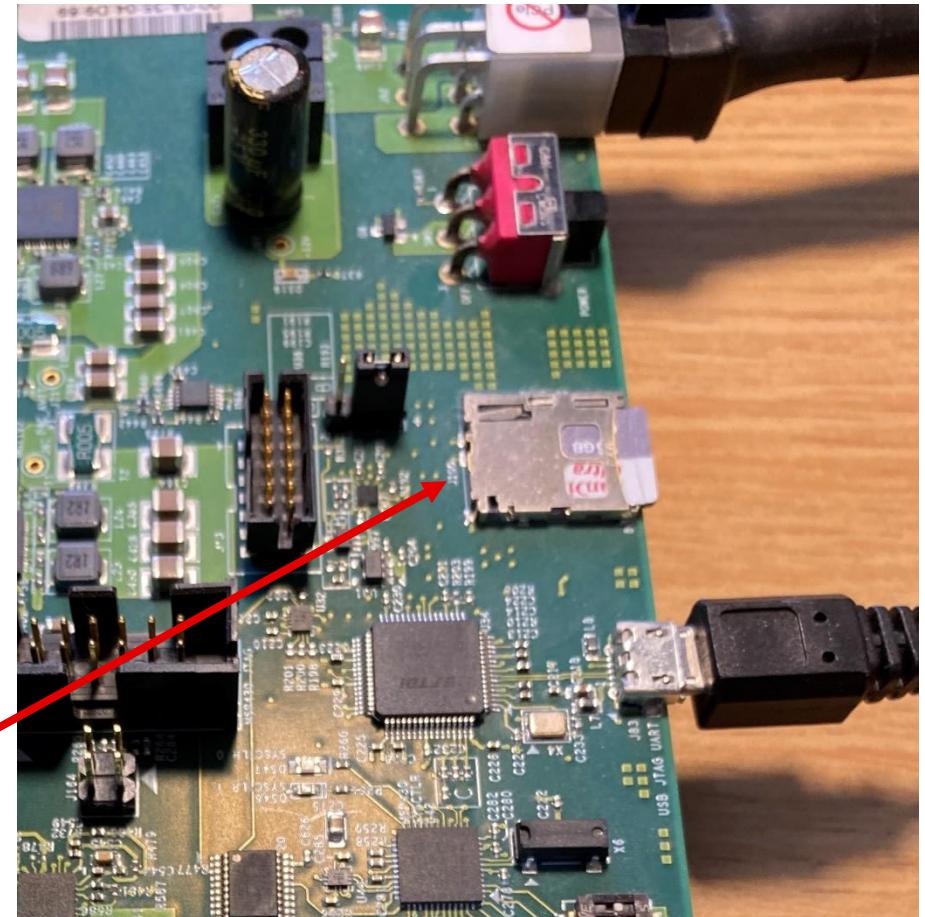
Note the location of the boot.bin file to put at the root level of the SD card.

Boot from SD Card

Set SW6 to on,off,off,off (SD Card boot mode).



Load boot.bin on the SD card, insert it into the board, and turn on the power.





Thank You

