



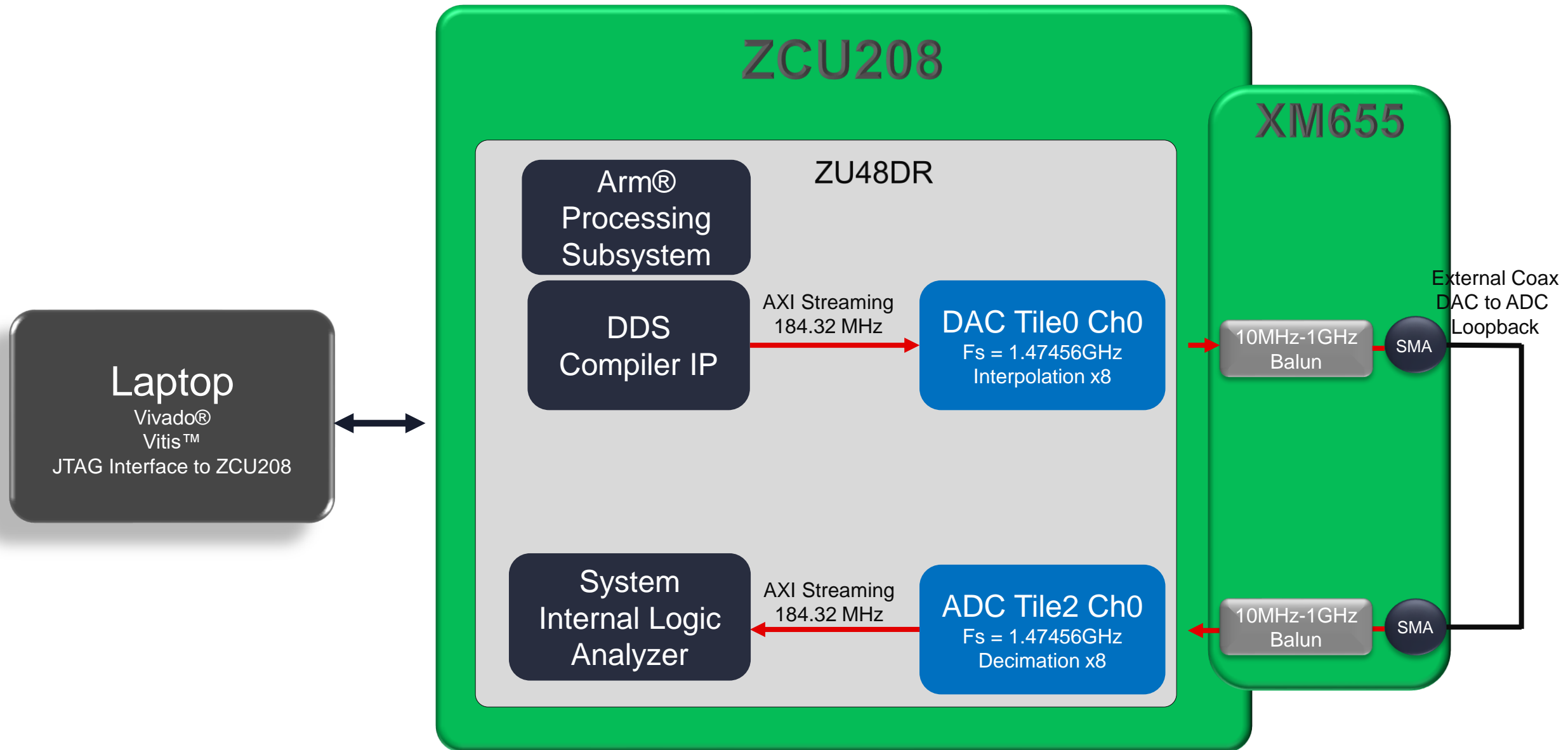
Zynq® UltraScale+™ RFSoc Example Design: ZCU208

DDS Compiler for DAC and
System ILA for ADC Capture – 2020.2

Introduction

- ▶ This is an example starter design for the RFSoc.
- ▶ It uses the ZCU208 board.
- ▶ It uses a DAC and ADC sample rate of 1.47456GHz.
- ▶ The DAC will continuously play 10MHz sine wave from the DDS Compiler IP.
- ▶ The ADC output will be sent to a System ILA to be displayed in the Hardware Manager.
- ▶ DAC Tile228(0) Ch0 will be used (LF balun).
- ▶ ADC Tile226(2) Ch0 will be used (LF balun)
- ▶ 2020.2 Xilinx tools (Vivado® Design Suite and Vitis™ unified software platform).
- ▶ Design tested in the directory *c:\rfsoc\ex_des\zcu208\v3*.
- ▶ This kit comes with the Vivado HW project and SW source files.

Demo Block Diagram

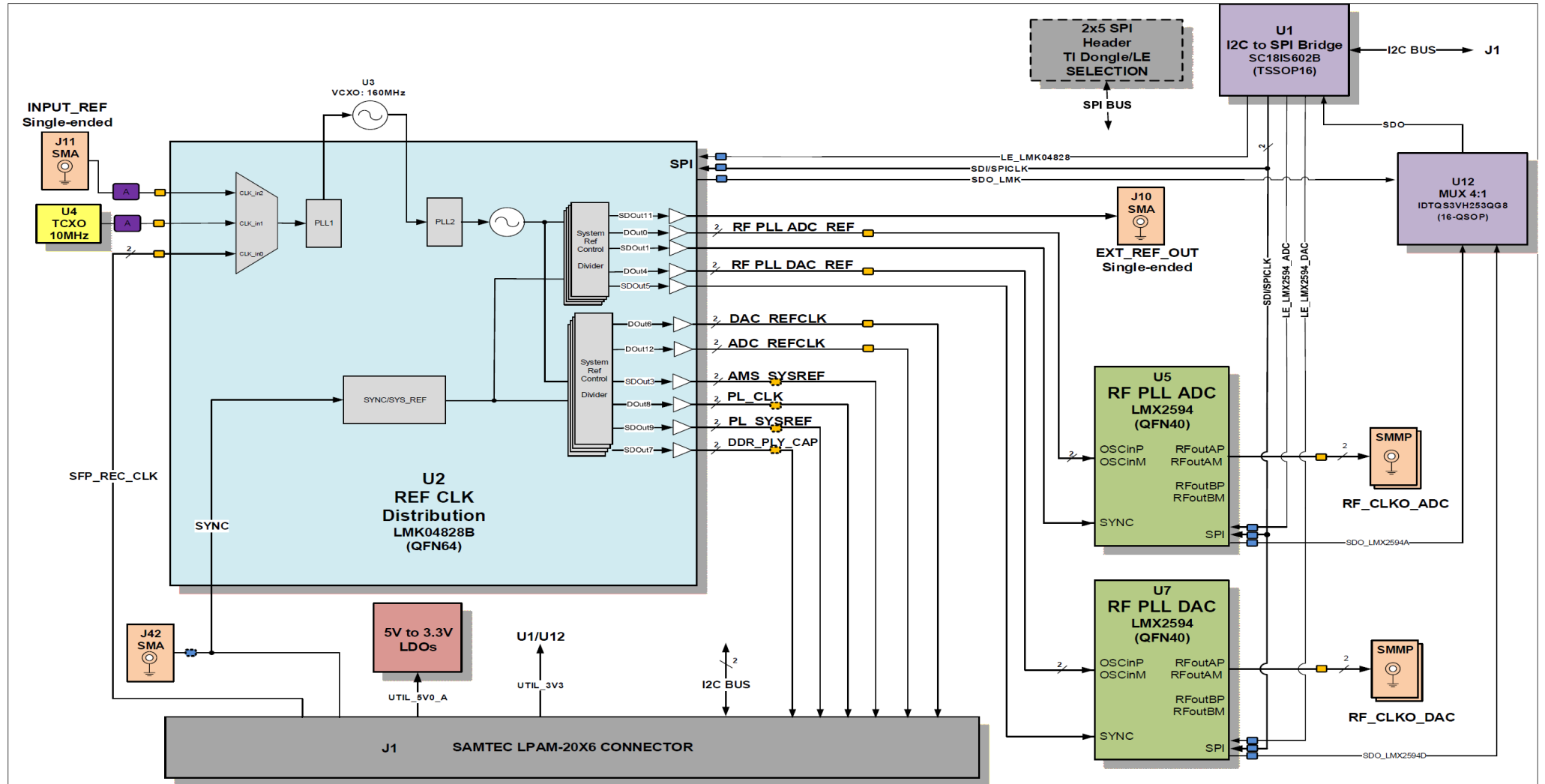


CLK104 Block Diagram

Block Diagram

Only the LMK04828B is used for this design; the LMX2594 outputs are powered down.

Clocking is configured via an I2C to SPI bridge.



Data Converter Clocking

CLK104/ZCU208



DAC Setup

Basic System Clocking Advanced

DAC Tile 228 DAC Tile 229 DAC Tile 230 DAC Tile 231

Multi Tile Sync Converter Band Mode Variable Output Current

☐ Enable Multi Tile Sync Band Single Output Power 20.0 [2.25 - 40.5]

Converter Configuration

DAC 0 DAC 1

☒ Enable DAC

DUC Configuration

DUC 0 DUC 1

☐ Invert Q Output ☐ Inverse Sinc Filter

Enable TDD Real Time Ports Off

Data Settings

Analog Output Data Real Interpolation Mode 8x

Samples per AXI4-Stream Cycle 1

Required AXI4-Stream clock: 184.320 MHz

Datapath Mode DUC 0 to Fs/2

Mixer Settings

Mixer Type Coarse Mixer Mode Real->Real Frequency 0

☐ Invert Q Output ☐ Inverse Sinc Filter

Enable TDD Real Time Ports Off

Data Settings

Analog Output Data Real Interpolation Mode Off

Samples per AXI4-Stream Cycle 16

Datapath Mode DUC 0 to Fs/2

Mixer Settings

Mixer Type Off

Analog Settings

Nyquist Zone Zone 1 Decoder Mode SNR Optimized

ADC Setup

Component Name:

Basic System Clocking Advanced

Converter Setup

Converter Setup:

Changing Converter Setup to Simple will cause current Advanced IP configuration to be lost.

RF-ADC RF-DAC

ADC Tile 224 ADC Tile 225 ADC Tile 226 ADC Tile 227

Multi Tile Sync Converter Band Mode Link Coupling

☐ Enable Multi Tile Sync Band: Link Coupling:

Converter Configuration

ADC 0 ADC 1

☒ Enable ADC ☐ Invert Q Output ☐ Enable ADC Observation Channel Ports

☐ Dither ☐ Enable ADC Observation Channel Ports

Enable TDD Real Time Ports:

Data Settings

Digital Output Data: Decimation Mode: Samples per AXI4-Stream Cycle:

Required AXI4-Stream clock: 184.320 MHz

Mixer Settings

Mixer Type: Mixer Mode: Frequency:

Analog Settings

Nyquist Zone: Calibration Mode:

ADC 1

☐ Enable ADC ☐ Invert Q Output ☐ Enable ADC Observation Channel Ports

☒ Dither ☐ Enable ADC Observation Channel Ports

Enable TDD Real Time Ports:

Data Settings

Digital Output Data: Decimation Mode: Samples per AXI4-Stream Cycle:

Mixer Settings

Mixer Type:

Analog Settings

Nyquist Zone: Calibration Mode:

Data Converter Clocking

Component Name

Basic **System Clocking** **Advanced**

AXI4-Lite Interface Configuration

AXI4-Lite Clock (MHz)

Tile Clocking Settings

| Tile | Sampling Rate (G SPS) | Max Fs (G SPS) | PLL | Reference Clock (MHz) | PLL Ref Clock (MHz) | Ref Clock Divider | Fabric Clock (MHz) | Clock Out (MHz) | Clock Source | Distribute Clock |
|---------|-----------------------|----------------|-------------------------------------|-----------------------|---------------------|-------------------|--------------------|-----------------|--------------|------------------|
| ADC 224 | 4 | 5.000 | <input type="checkbox"/> | 4000.000 | - | 1 | 0.0 | 250.000 | ADC224 | Off |
| ADC 225 | 4 | 5.000 | <input type="checkbox"/> | 4000.000 | - | 1 | 0.0 | 250.000 | ADC225 | Off |
| ADC 226 | 1.47456 | 5.000 | <input checked="" type="checkbox"/> | 184.320 | 184.32 | 1 | 184.320 | 11.520 | ADC226 | Off |
| ADC 227 | 4 | 5.000 | <input type="checkbox"/> | 4000.000 | - | 1 | 0.0 | 250.000 | ADC227 | Off |
| DAC 228 | 1.47456 | 7.000 | <input checked="" type="checkbox"/> | 184.320 | 184.32 | 1 | 184.320 | 184.320 | DAC228 | Off |
| DAC 229 | 4 | 10.000 | <input type="checkbox"/> | 4000.000 | - | 1 | 0.0 | 500.000 | DAC229 | Off |
| DAC 230 | 4 | 10.000 | <input type="checkbox"/> | 4000.000 | - | 1 | 0.0 | 500.000 | DAC230 | Off |
| DAC 231 | 4 | 10.000 | <input type="checkbox"/> | 4000.000 | - | 1 | 0.0 | 500.000 | DAC231 | Off |

ADC226 Warning: Current PLL reference clock may have negative impact on phase noise performance

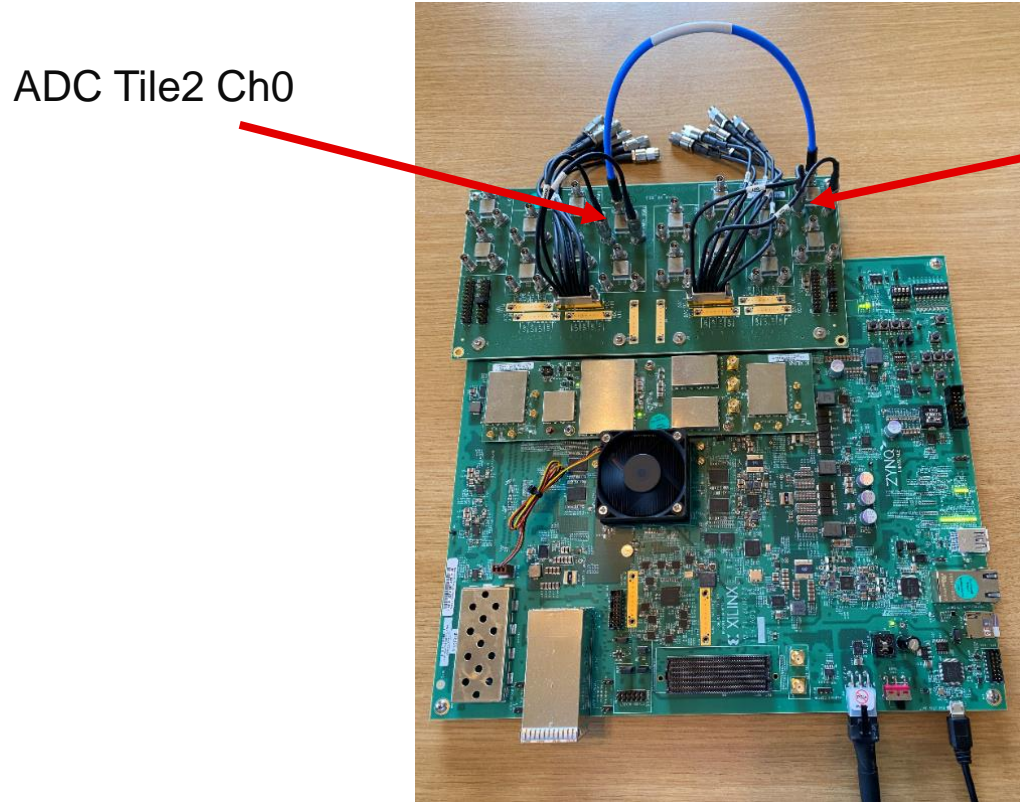
DAC228 Warning: Current PLL reference clock may have negative impact on phase noise performance

PLL Summary Settings

| Tile | Vco (MHz) | Fb Div | M | R |
|---------|-----------|--------|---|---|
| ADC 224 | - | - | - | - |
| ADC 225 | - | - | - | - |
| ADC 226 | 8847.36 | 48 | 6 | 1 |
| ADC 227 | - | - | - | - |
| DAC 228 | 8847.36 | 48 | 6 | 1 |
| DAC 229 | - | - | - | - |
| DAC 230 | - | - | - | - |
| DAC 231 | - | - | - | - |

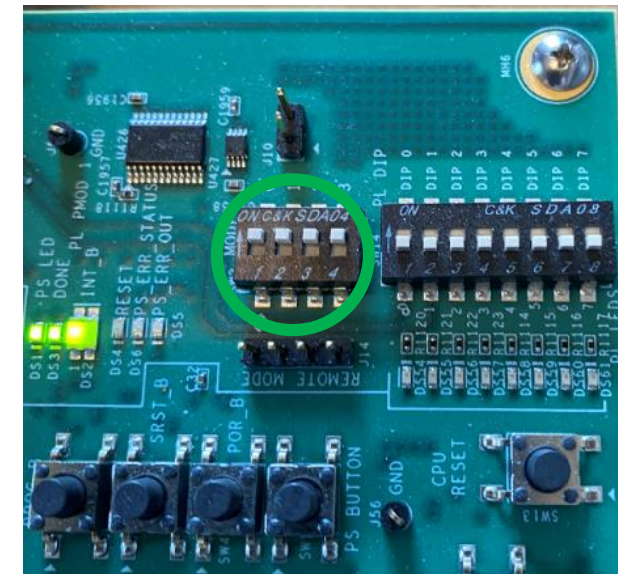
Board Setup for the Upcoming Designs

- ▶ Connect DAC Tile 228 Ch0 output to ADC Tile 226 Ch0 input on XM655 (low frequency balun connections).
- ▶ Set SW2 to on,on,on,on (JTAG boot mode).
- ▶ Connect USB to host for JTAG, PS UART, and System Controller UART access.



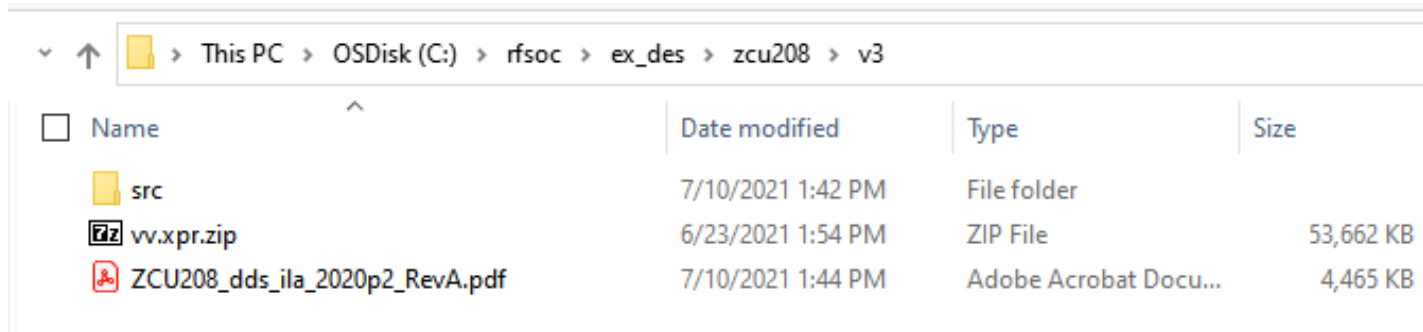
DAC Tile0 Ch0

SW2






Design Kit Contents

1. Extract the design kit to an appropriate folder—be mindful of the Windows path length requirement.
2. Extract vv.xpr.zip, which is the Vivado project.
3. Software source files in the “src” folder.
4. Design documentation in the .pdf file.

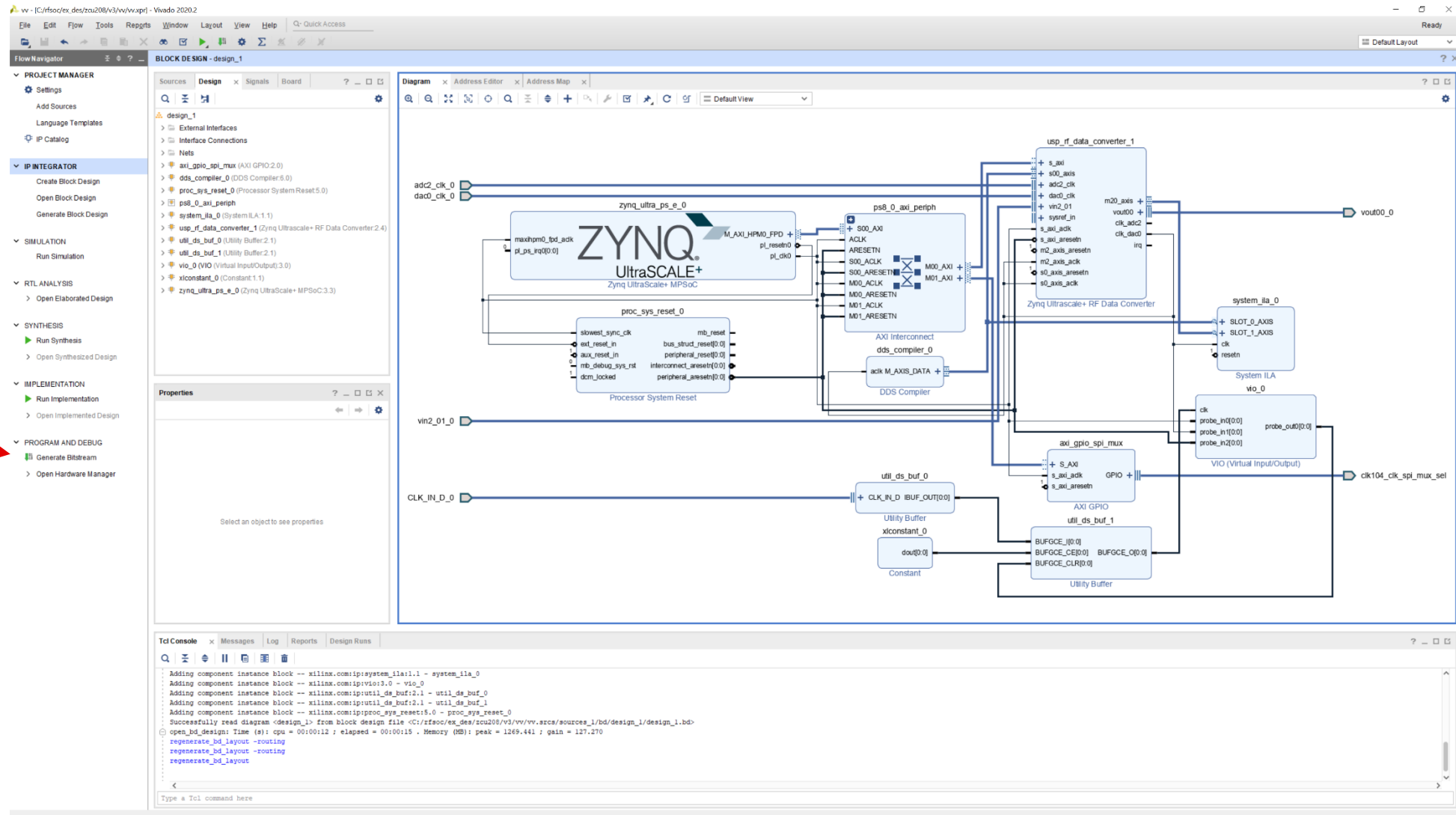


The screenshot shows a Windows File Explorer window with the address bar displaying the path: This PC > OSDisk (C:) > rfsoc > ex_des > zcu208 > v3. The main area shows a table of files and folders.

| <input type="checkbox"/> Name | Date modified | Type | Size |
|--|-------------------|-----------------------|-----------|
|  src | 7/10/2021 1:42 PM | File folder | |
|  vv.xpr.zip | 6/23/2021 1:54 PM | ZIP File | 53,662 KB |
|  ZCU208_dds_ila_2020p2_RevA.pdf | 7/10/2021 1:44 PM | Adobe Acrobat Docu... | 4,465 KB |

Open Hardware Design and Generate the Bitstream

Extract vv.xpr.zip, open the design in Vivado®, and generate the bitstream.



DAC Sine Wave Generator (DDS Compiler IP)

Re-customize IP

DDS Compiler (6.0)

Documentation IP Location

IP Symbol Information

☐ Show disabled ports

Component Name: dds_compiler_0

Configuration Implementation Detailed Implementation Output Frequencies

Configuration Options: Phase Generator and SIN COS LUT

System Requirements

System Clock (MHz): 184.32 [0.01 - 1000.0]

Number of Channels: 1

Mode Of Operation: Standard

Frequency per Channel (Fs): 184.31999999999999 MHz

Parameter Selection: SystemParameters

System Parameters

Spurious Free Dynamic Range (dB): 95 Range: 18...150

Frequency Resolution (Hz): 0.4 6.54836e-07...2.304e+07

Noise Shaping: Auto

clk M_AXIS_DATA

OK Cancel

Re-customize IP

DDS Compiler (6.0)

Documentation IP Location

IP Symbol Information

☐ Show disabled ports

Component Name: dds_compiler_0

Configuration Implementation Detailed Implementation Output Frequencies

Channel Output Frequency (MHz)

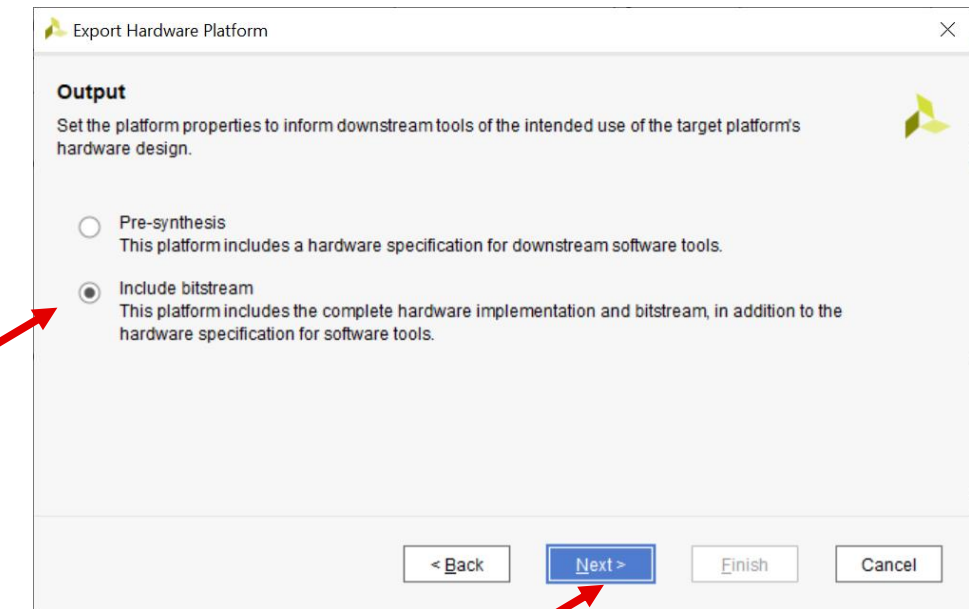
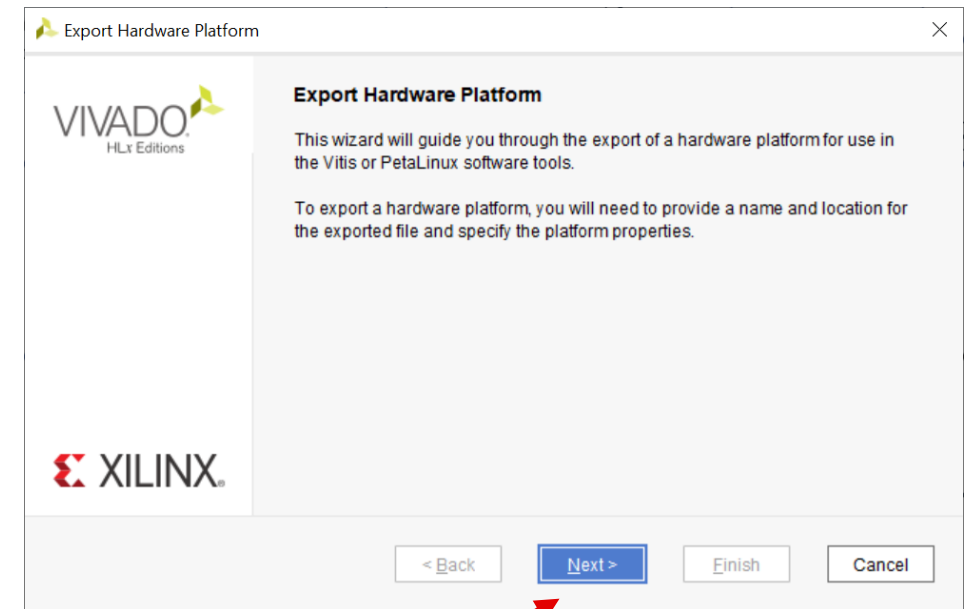
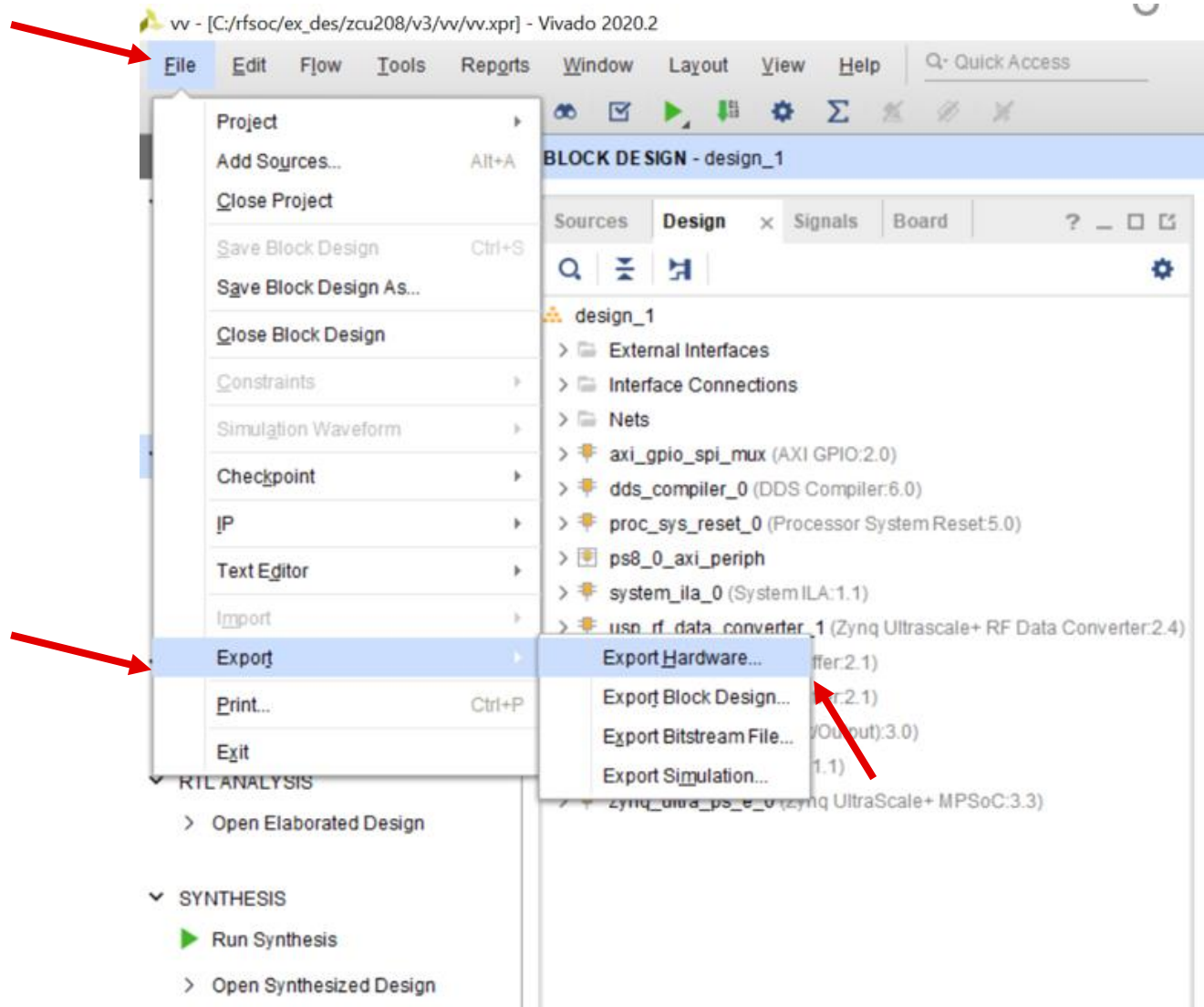
| | |
|----|----|
| 1 | 10 |
| 2 | 0 |
| 3 | 0 |
| 4 | 0 |
| 5 | 0 |
| 6 | 0 |
| 7 | 0 |
| 8 | 0 |
| 9 | 0 |
| 10 | 0 |
| 11 | 0 |
| 12 | 0 |
| 13 | 0 |
| 14 | 0 |
| 15 | 0 |
| 16 | 0 |

Valid Range: 0.0...184.31999999999999 MHz

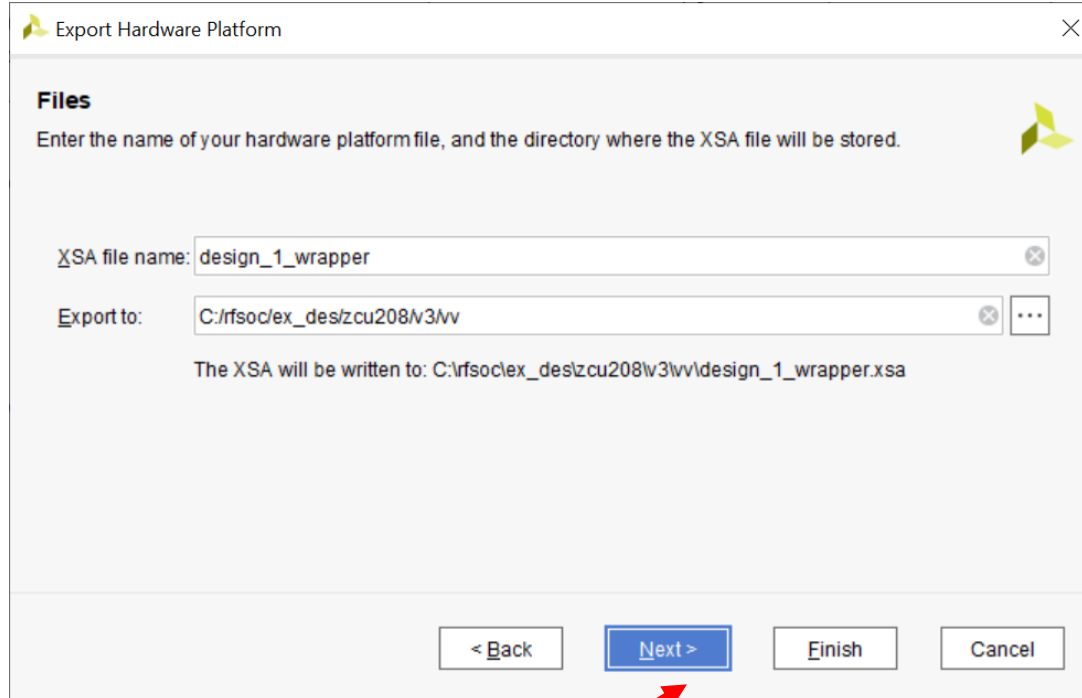
clk M_AXIS_DATA

OK Cancel

Export Hardware



Export Hardware Cont'd



Export Hardware Platform

Files
Enter the name of your hardware platform file, and the directory where the XSA file will be stored.

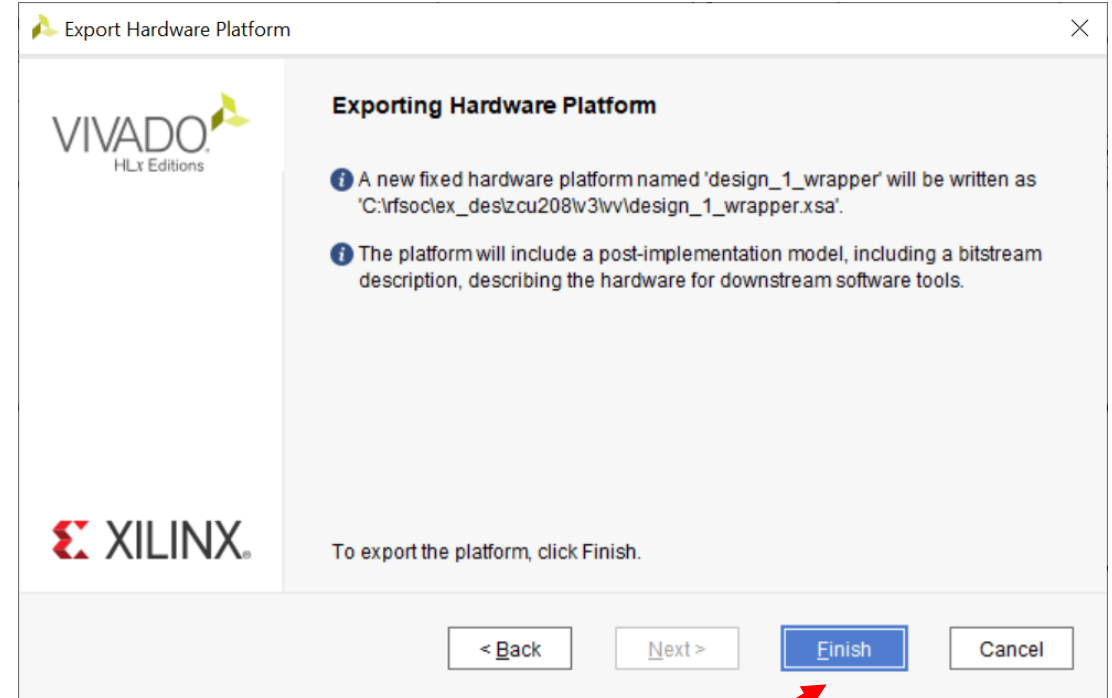
XSA file name:

Export to: ...

The XSA will be written to: C:\rfsoc\ex_des\zc208\w3\vv\design_1_wrapper.xsa

< Back **Next >** Finish Cancel

A red arrow points to the **Next >** button.



Export Hardware Platform

Exporting Hardware Platform

VIVADO
HLx Editions

XILINX

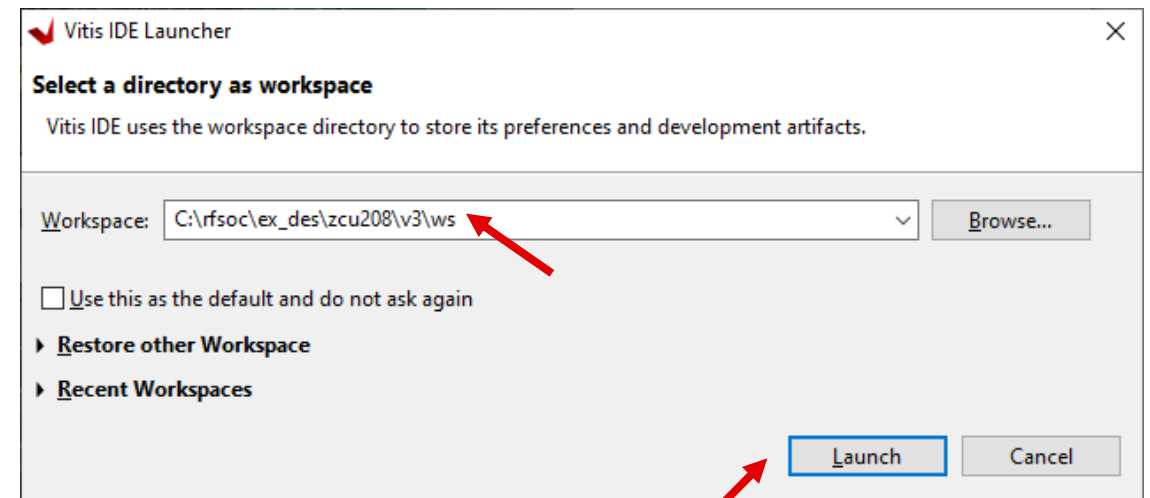
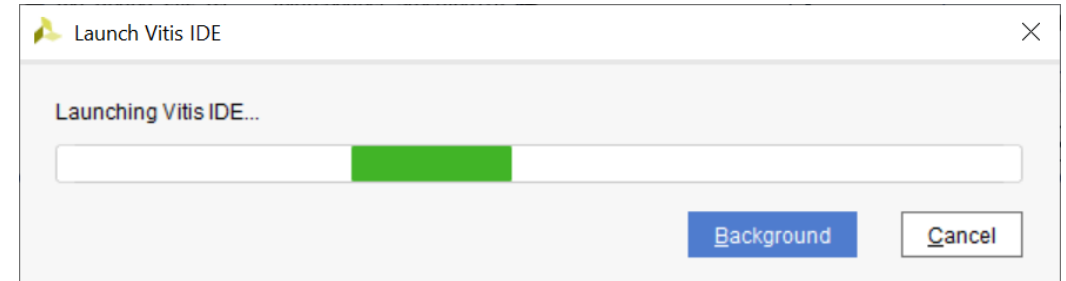
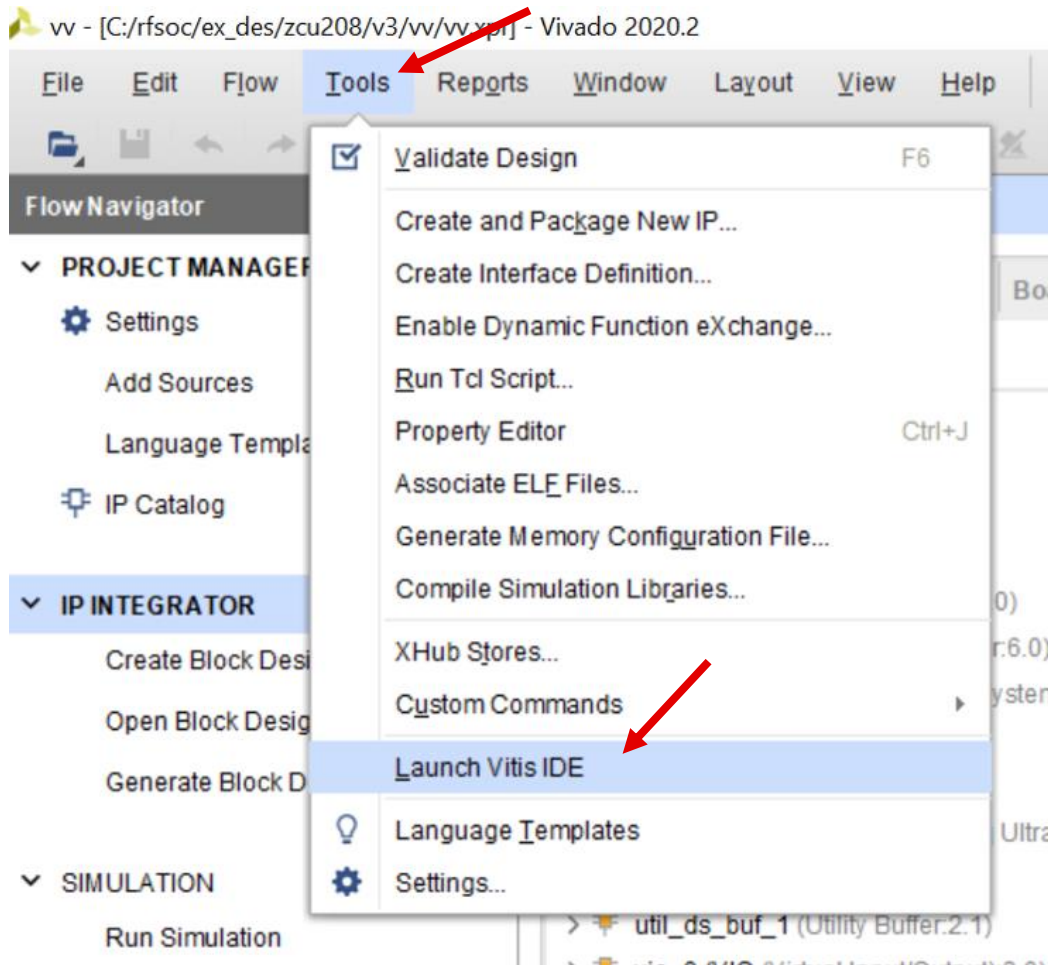
- A new fixed hardware platform named 'design_1_wrapper' will be written as 'C:\rfsoc\ex_des\zc208\w3\vv\design_1_wrapper.xsa'.
- The platform will include a post-implementation model, including a bitstream description, describing the hardware for downstream software tools.

To export the platform, click Finish.

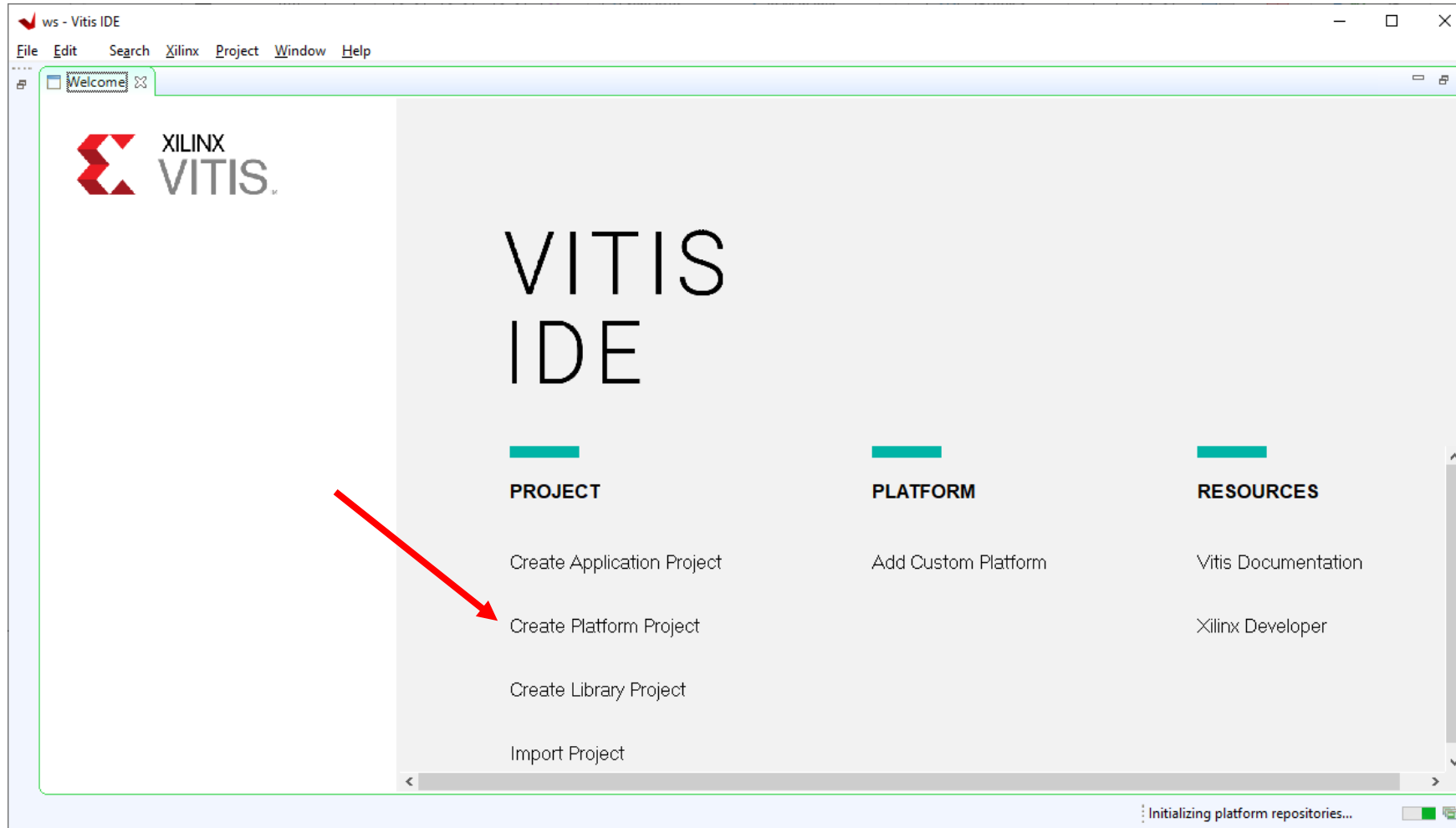
< Back Next > **Finish** Cancel

A red arrow points to the **Finish** button.

Open Vitis™ Software Platform



Create Platform Project



Create Platform Project Cont'd

New Platform Project

Create new platform project

Enter a name for your platform project

This wizard will guide you through creation of a platform project from the output of Vivado [Xilinx Shell Archive (XSA)] or from an existing platform. A platform will enable you to specify options for the kernels, BSPs, as well as settings required for creating new applications. Platforms are currently supported for embedded software developers.

Platform project name: ZCU208

Platform Project

System Project

Processor

Domain

App

XSA

- A platform provides hardware information and software environment settings.
- A system project contains one or more applications that run at the same time.
- A domain provides runtime for applications, such as operating system or BSP.
- A workspace can contain unlimited platforms and unlimited system projects.

A new platform project can be created from one of the two inputs:

From hardware specification (XSA)

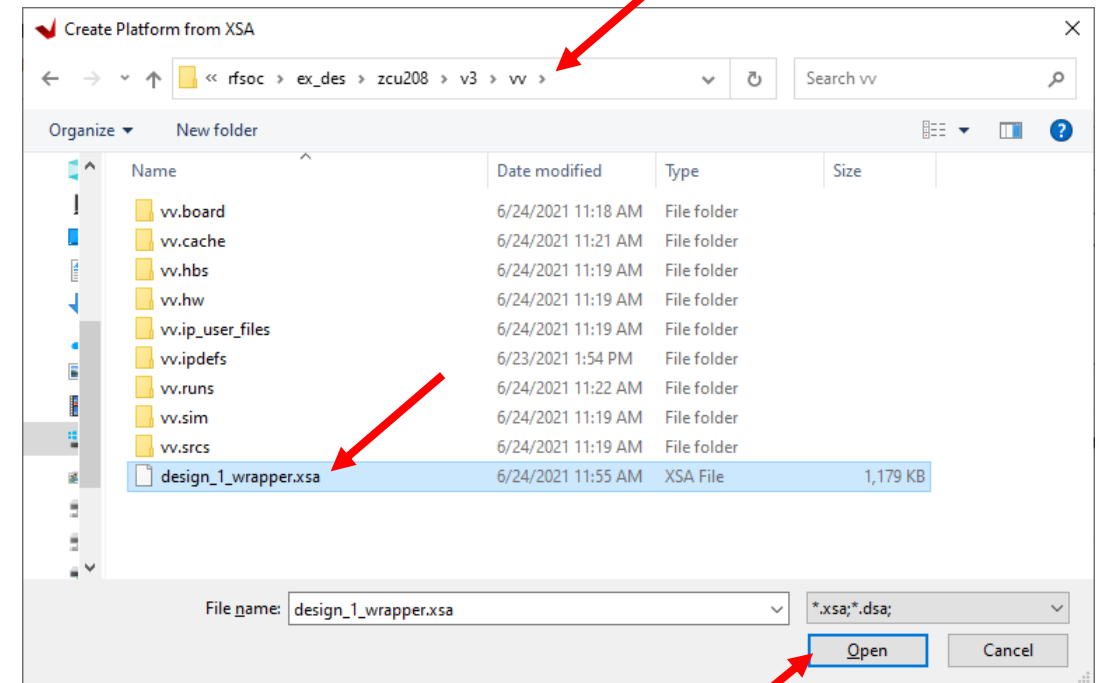
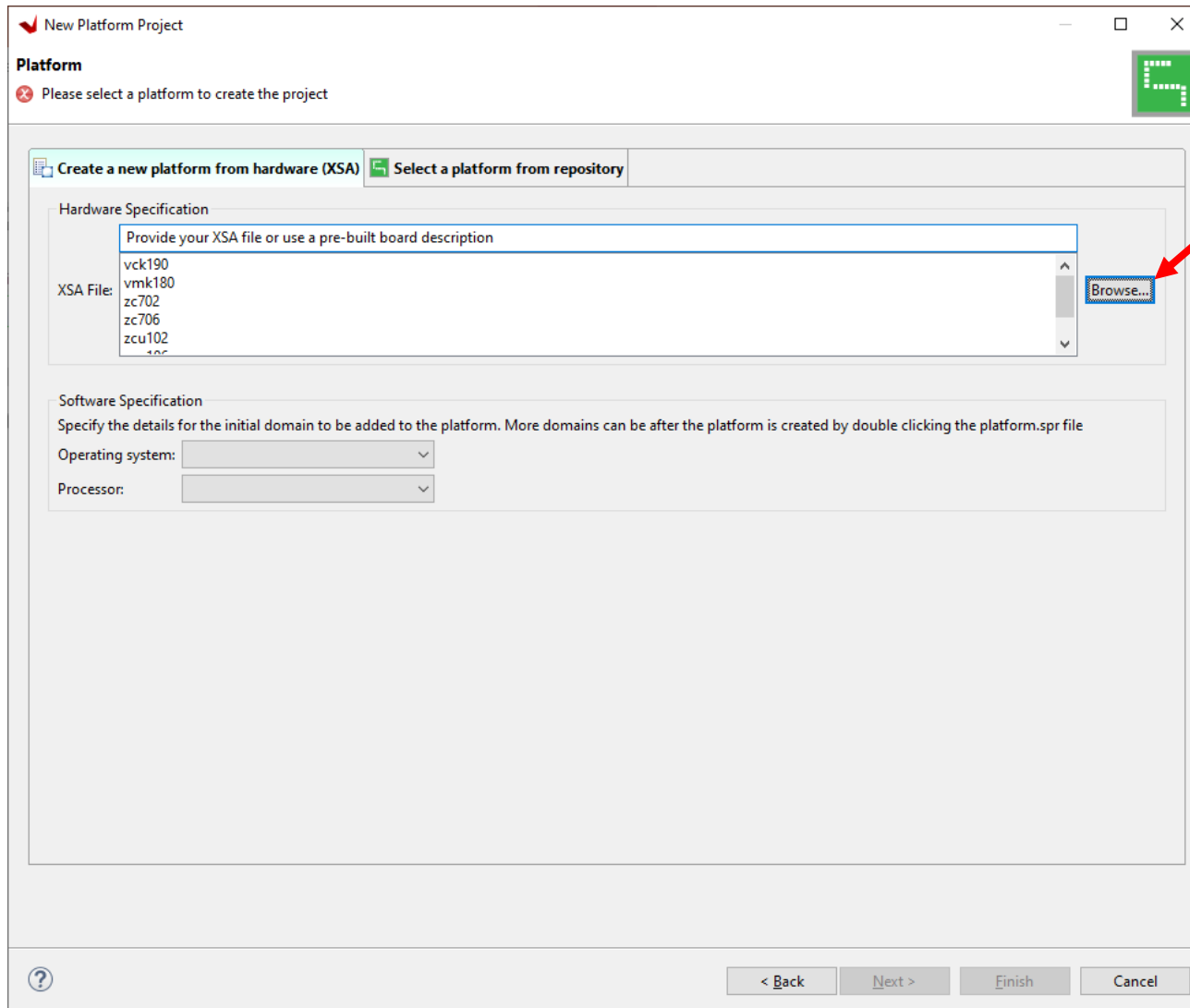
Create a new platform project from a hardware specification file. You can specify the OS and processor to start with. The platform can be customized later from the platform project editor.

From existing platform

Load the platform definition from an existing platform. You can choose any platform from the platform repository as a base for your platform project.

< Back Next > Finish Cancel

Create Platform Project Cont'd



Create Platform Project Cont'd

New Platform Project

Platform
Choose a platform for your project. You can also create an application from XSA through the 'Create a new platform from hardware (XSA)' tab.

Create a new platform from hardware (XSA) | **Select a platform from repository**

Hardware Specification

XSA File:

vck190
vmk180
zc702
zc706
zcu102
zcu106
zed
C:\rfsoc\ex_des\zcu208\v3\vw\design_1_wrapper.xsa

Software Specification
Specify the details for the initial domain to be added to the platform. More domains can be added after the platform is created by double clicking the platform.spr file

Operating system:

Processor:

Architecture:

Note: A domain with selected operating system and processor will be added to the platform. The platform project can be modified later to add new domains or change settings.

Boot components

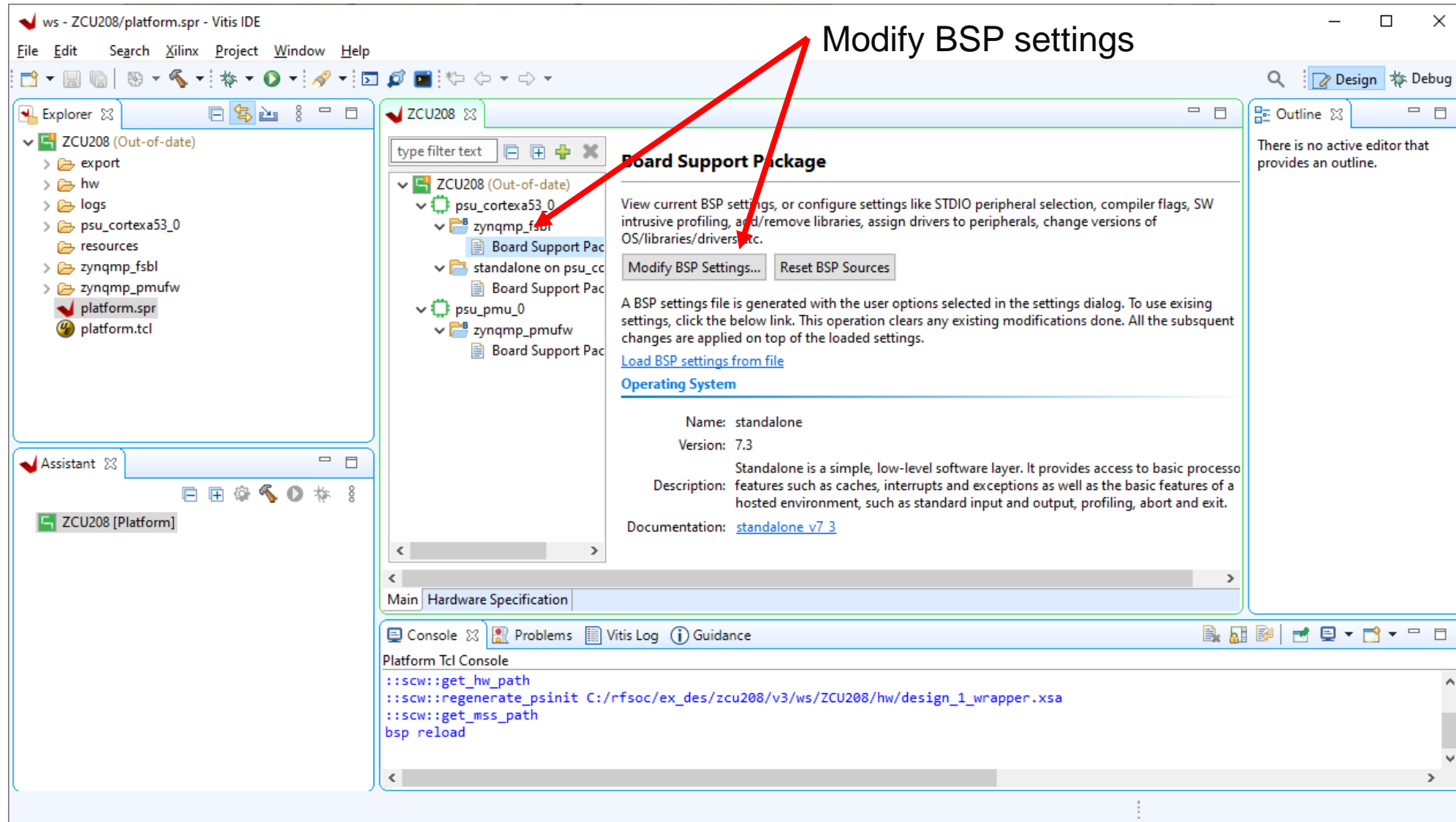
☒ Generate boot components

Target processor to create FSBL: ☒ psu_cortexa53_0
☐ psu_cortexr5_0

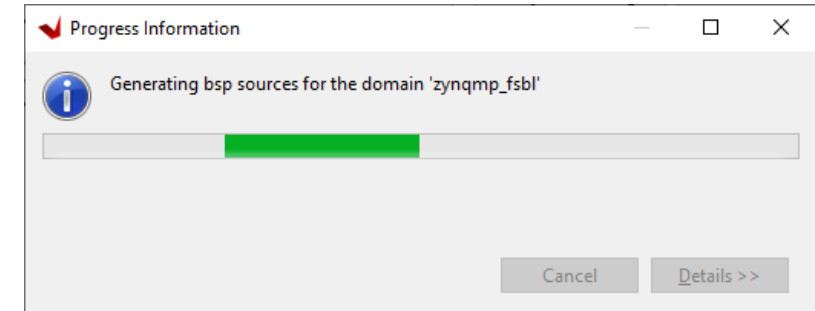
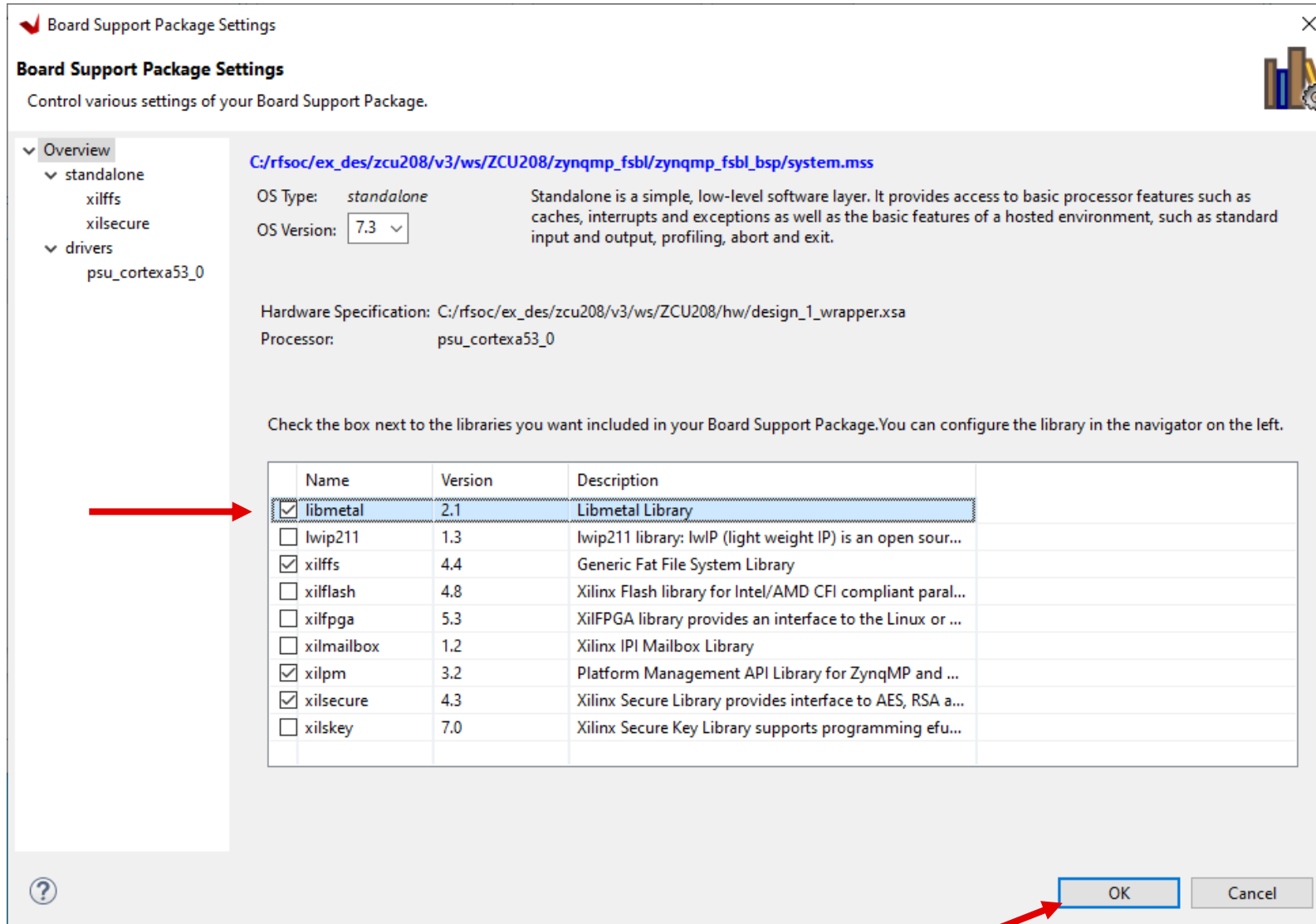
Finish

This may take a few minutes.

Create Platform Project Cont'd

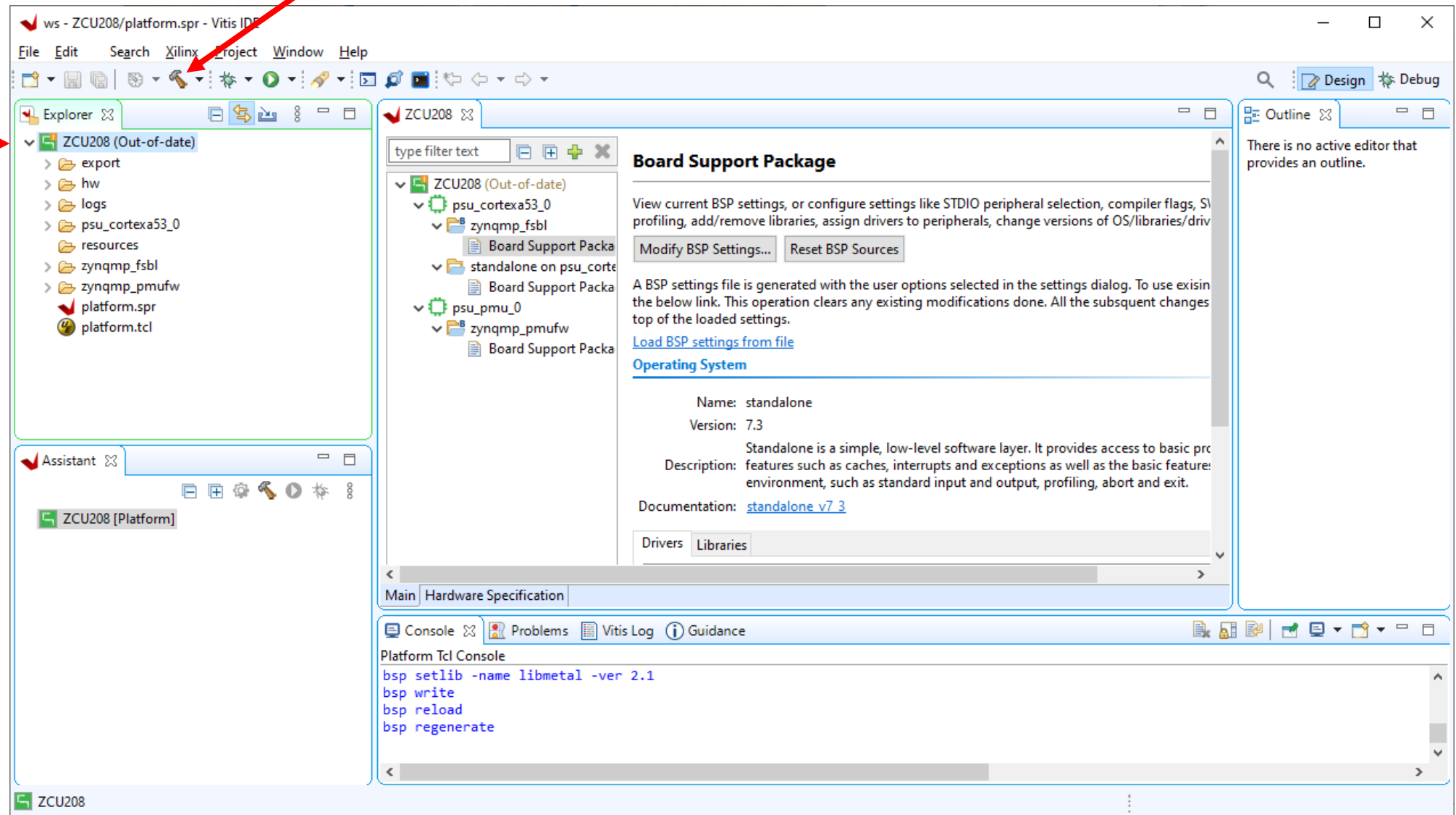


Enable libmetal

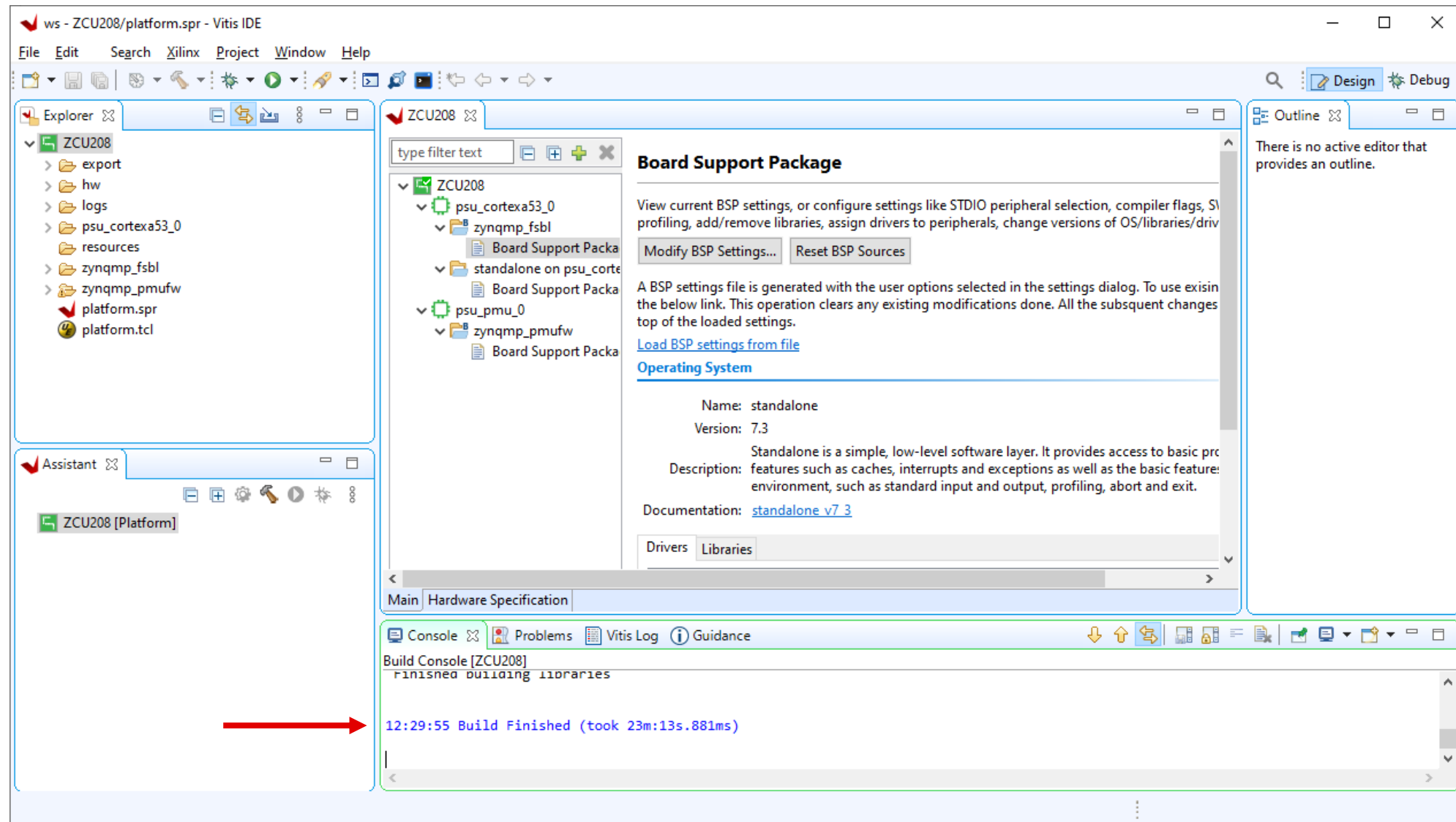


Build Project

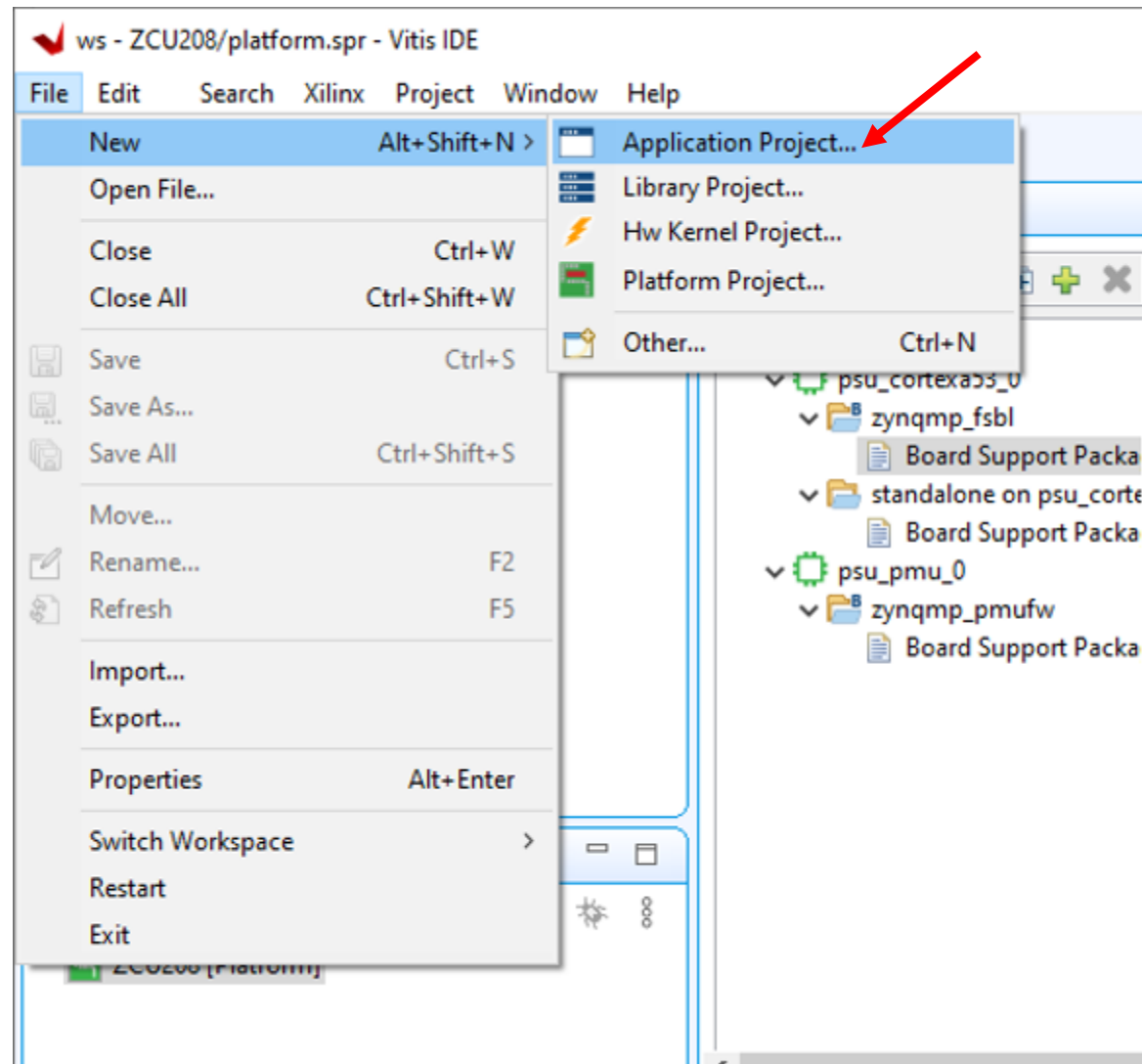
This may take
a few minutes.



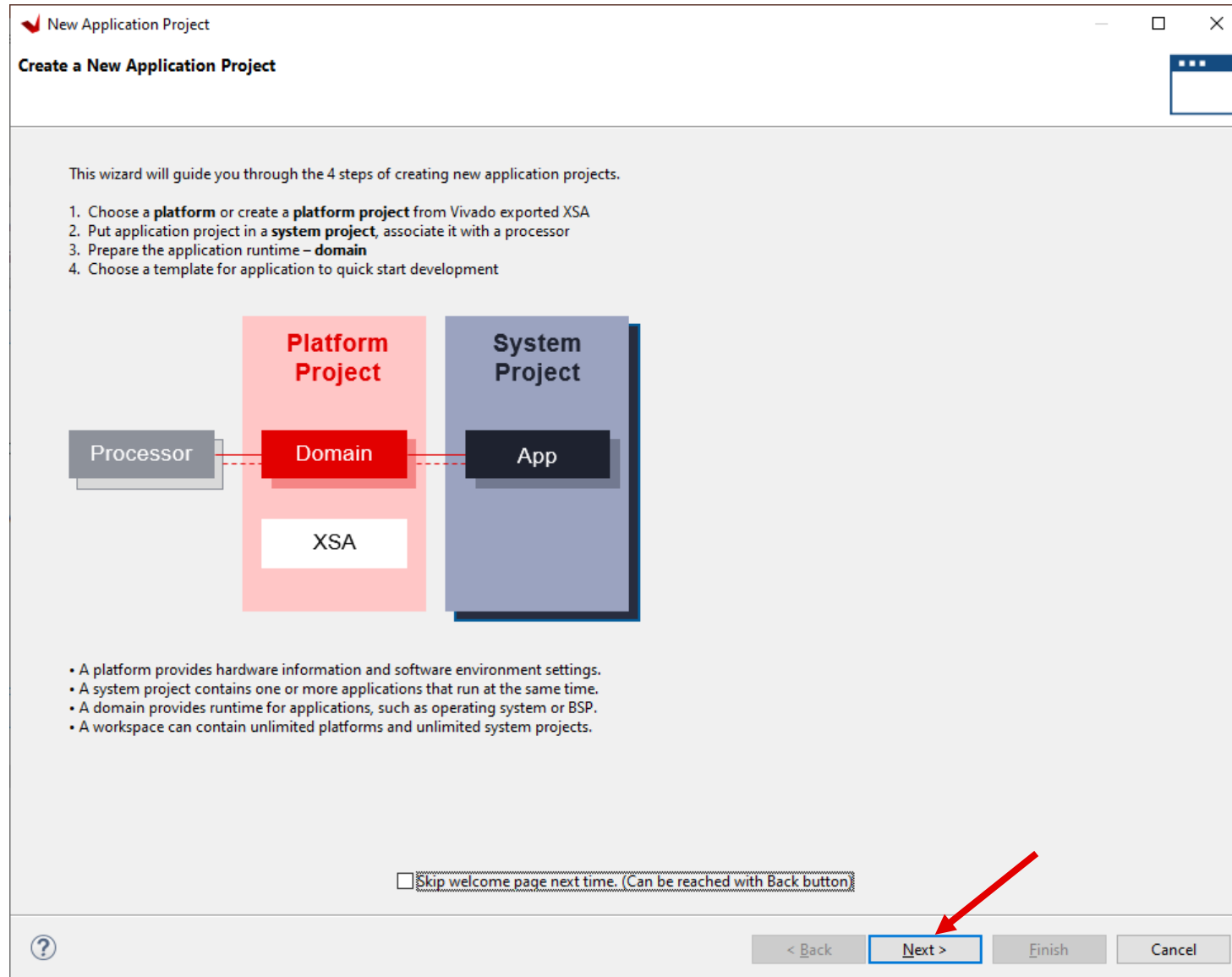
Build Complete



Create Application



Create Application Cont'd



Create Application Cont'd

New Application Project

Platform
Choose a platform for your project. You can also create an application from XSA through the 'Create a new platform from hardware (XSA)' tab.

Select a platform from repository Create a new platform from hardware (XSA)

Find: + Add ⚙ Manage

| Name | Board | Flow | Vendor | Path |
|-----------------|--------|-----------------|--------|---|
| ZCU208 [custom] | zcu111 | Embedded SW Dev | xilinx | C:\rfsoc\ex_des\zcu208\v3\ws\ZCU208\export\ZCU208\ZCU208... |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

Platform Info

General Info

Name:

Part:

Family:

Description:

Acceleration Resources

The selected platform does not have application acceleration capabilities

Domain Details

Domains

| Domain name | Details |
|----------------------------|-----------------------|
| standalone on psu_corte... | CPU: psu_cortexa53... |

? < Back **Next >** Finish Cancel

Create Application Cont'd

New Application Project

Application Project Details
Specify the application project name and its system project properties

Application project name: RFSOC

System Project
Create a new system project for the application or select an existing one from the workspace

Select a system project
+ Create new...

System project details
System project name: RFSOC_system

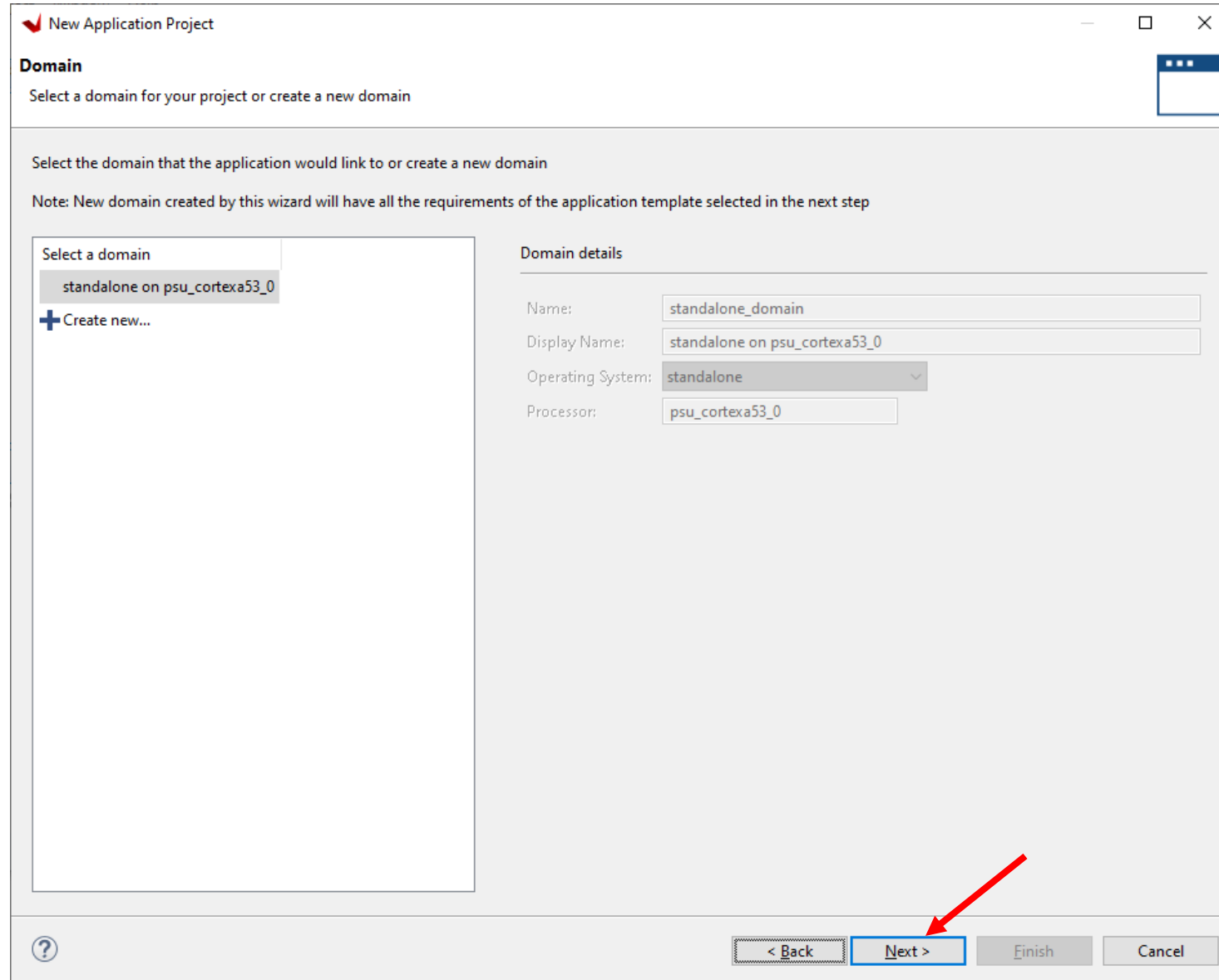
Target processor
Select target processor for the Application project.

| Processor | Associated applications |
|-----------------|-------------------------|
| psu_cortexa53_0 | RFSOC |
| | |
| | |
| | |
| | |
| | |
| | |
| | |
| | |
| | |
| | |

Show all processors in the hardware specification ☐

< Back Next > Finish Cancel

Create Application Cont'd



New Application Project

Domain

Select a domain for your project or create a new domain

Select the domain that the application would link to or create a new domain

Note: New domain created by this wizard will have all the requirements of the application template selected in the next step

Select a domain

- standalone on psu_cortexa53_0
- + Create new...

Domain details

Name: standalone_domain

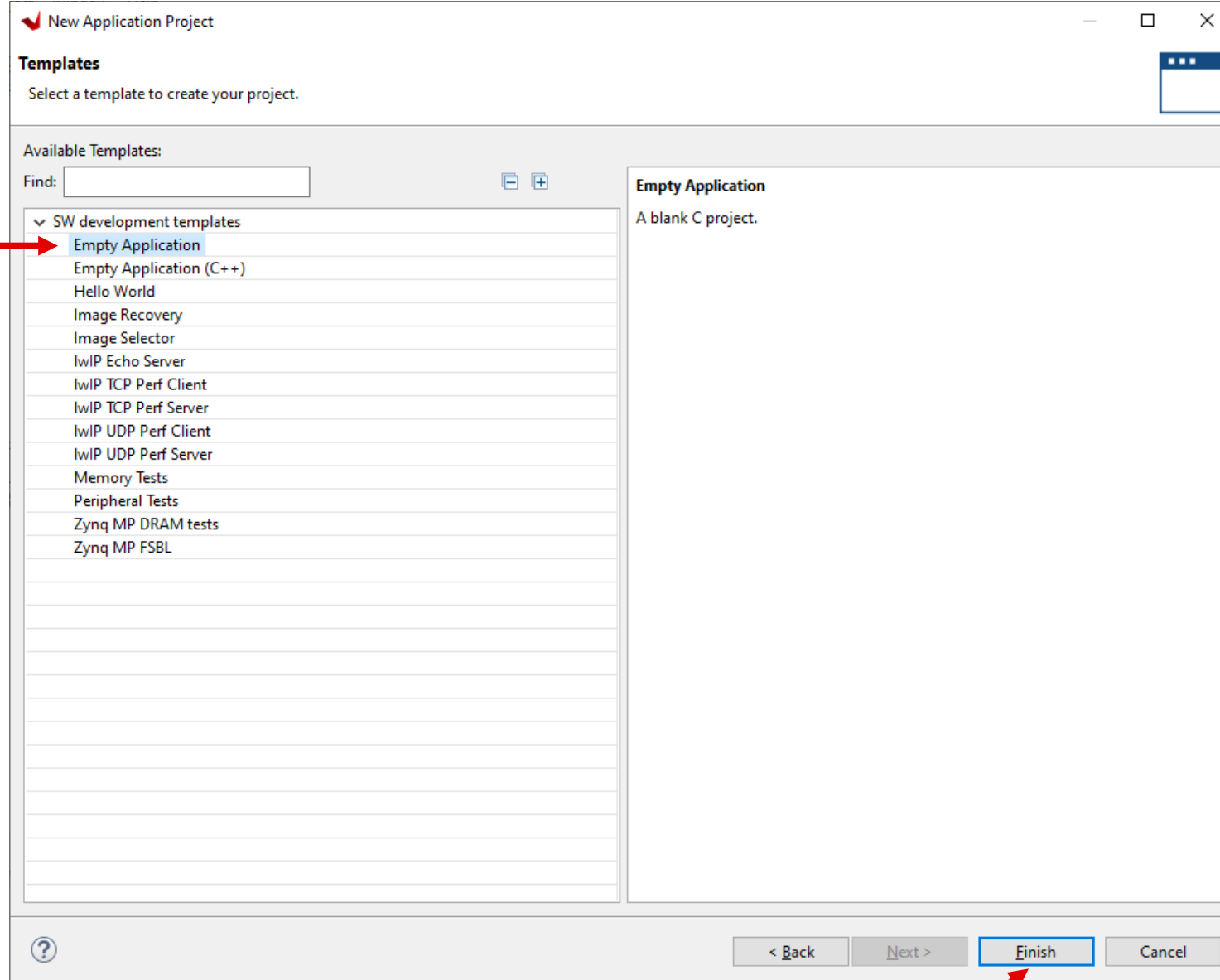
Display Name: standalone on psu_cortexa53_0

Operating System: standalone

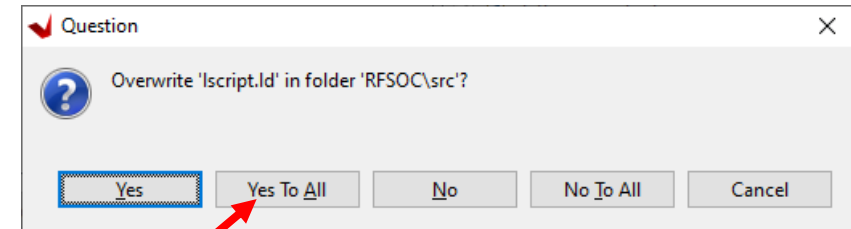
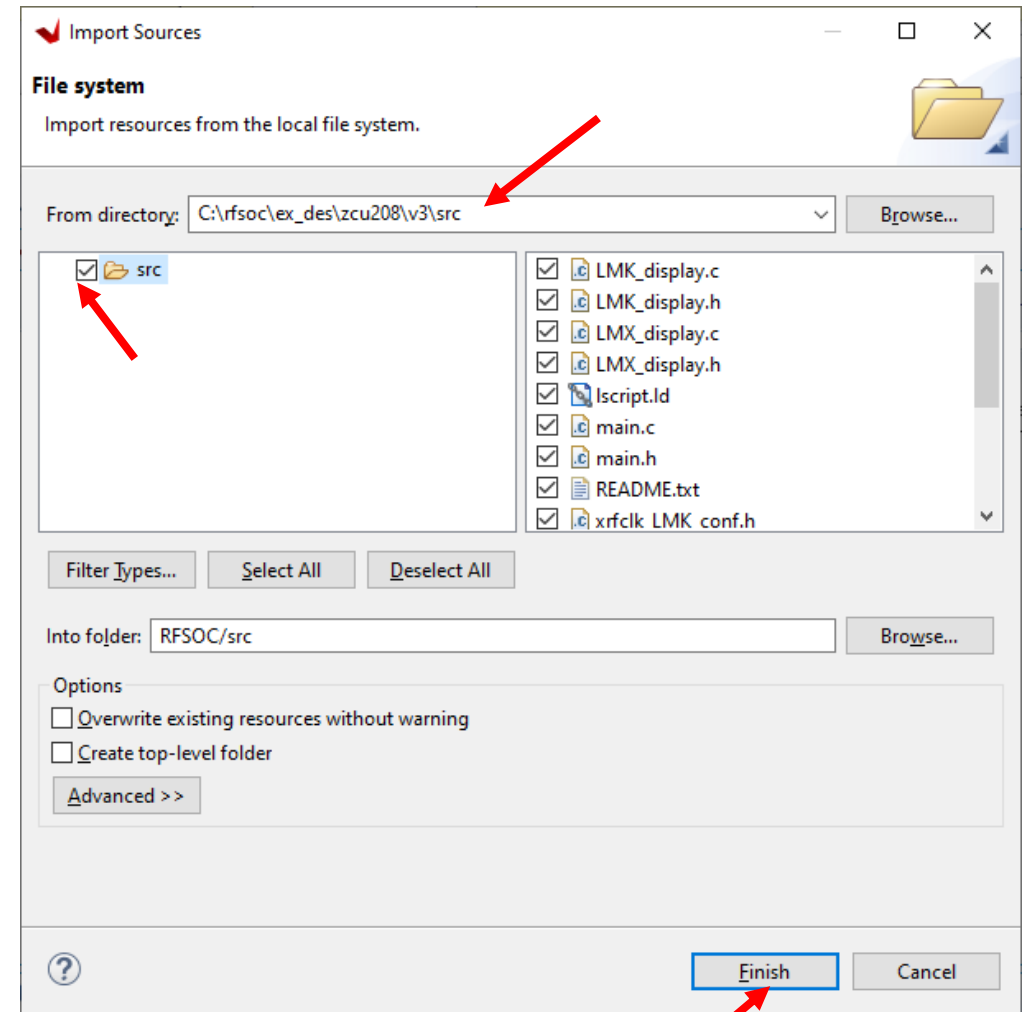
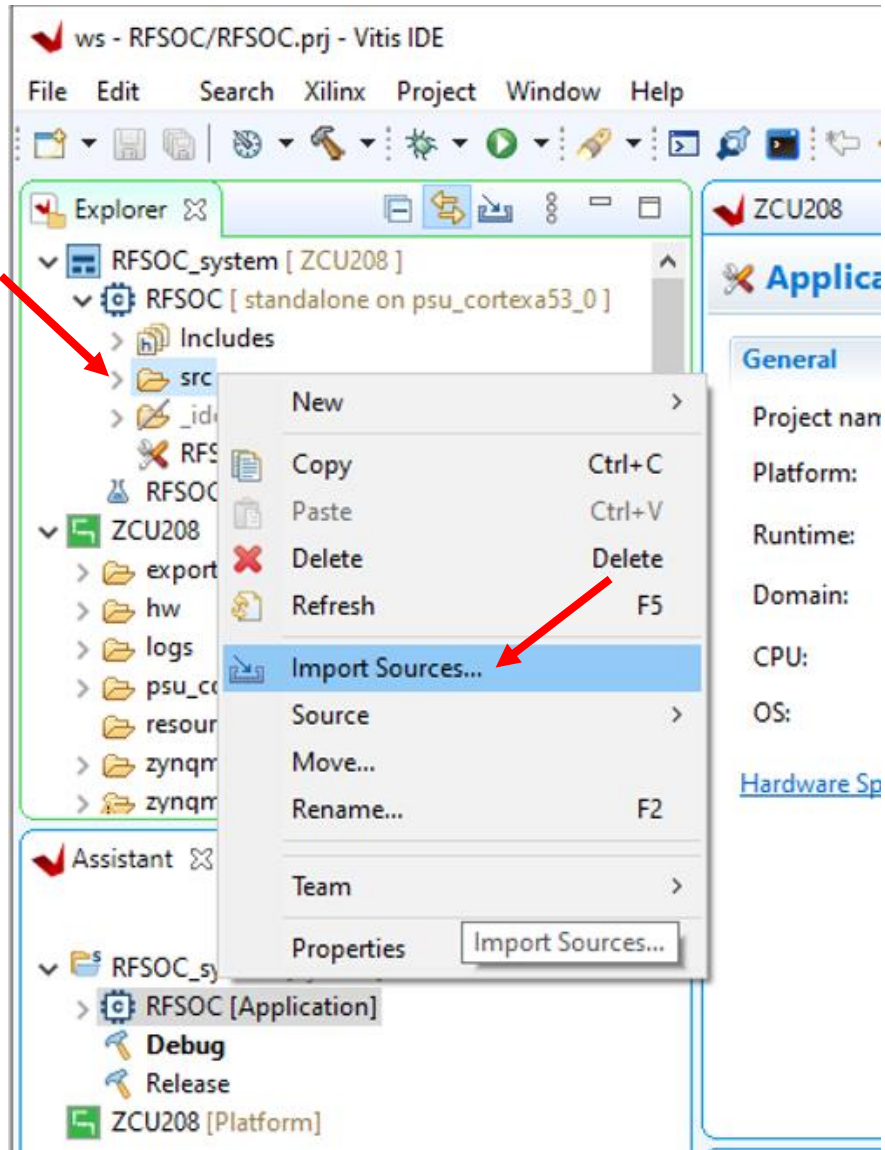
Processor: psu_cortexa53_0

< Back Next > Finish Cancel

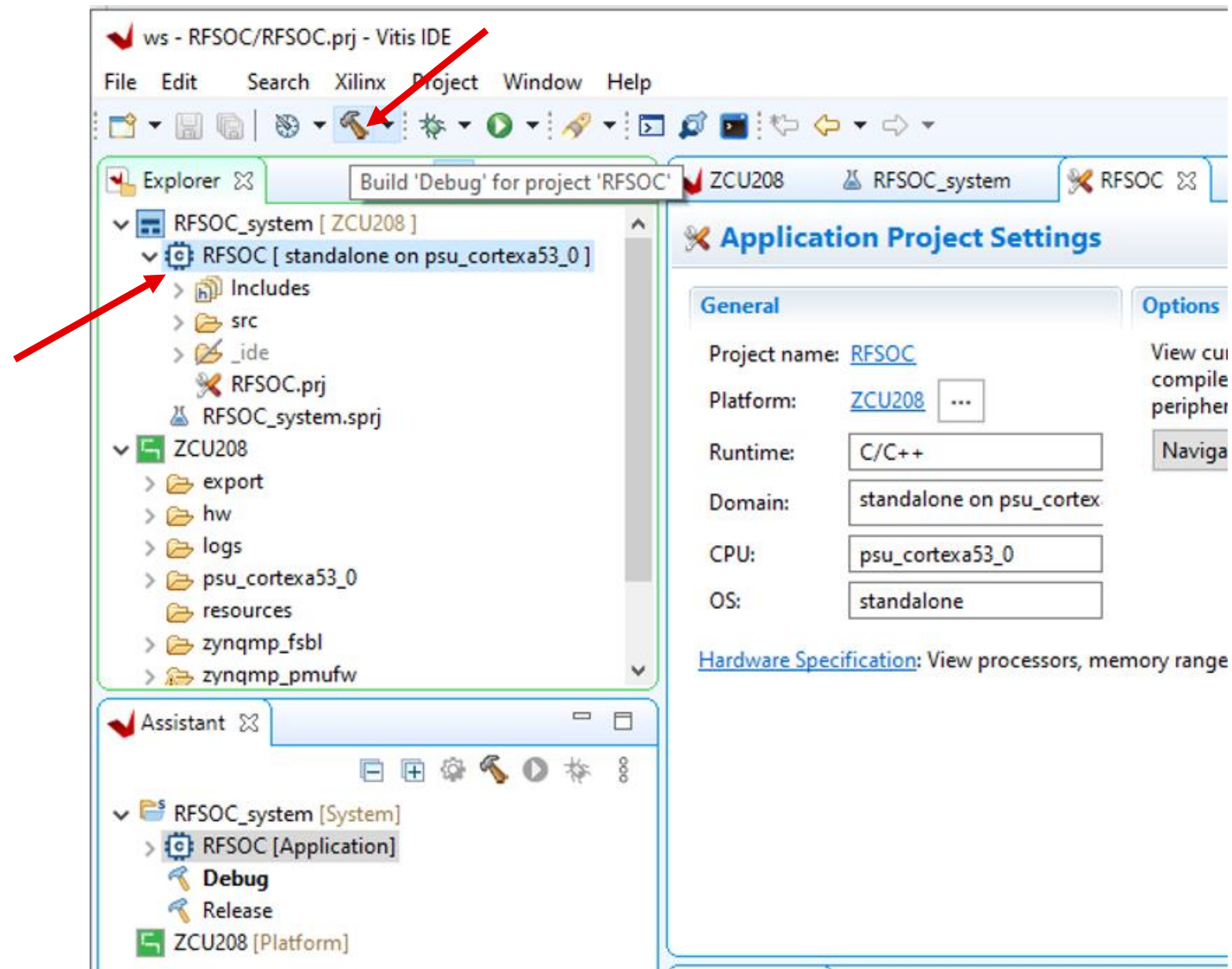
Create Application Cont'd



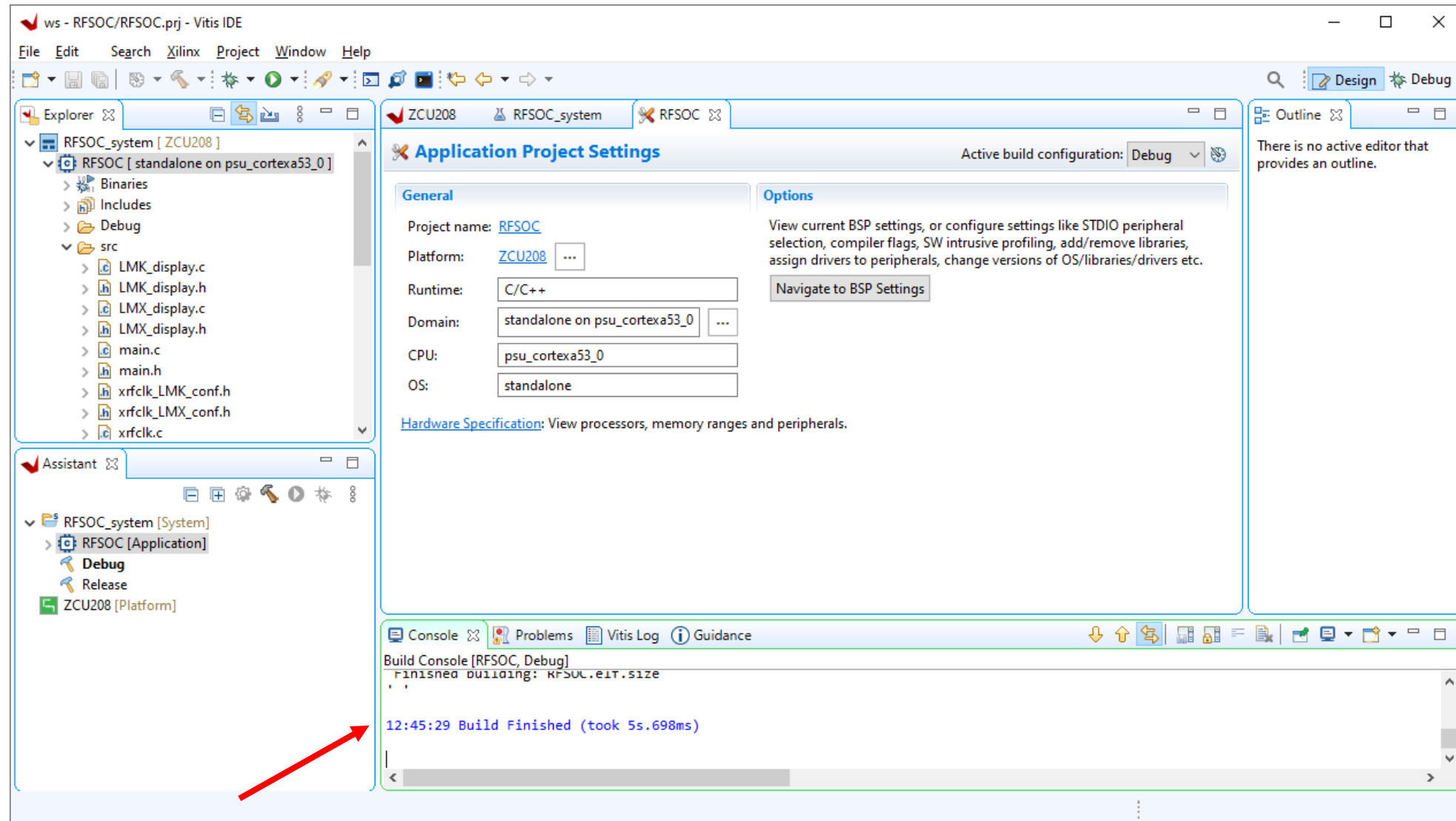
Import Sources



Build Application



Build Complete

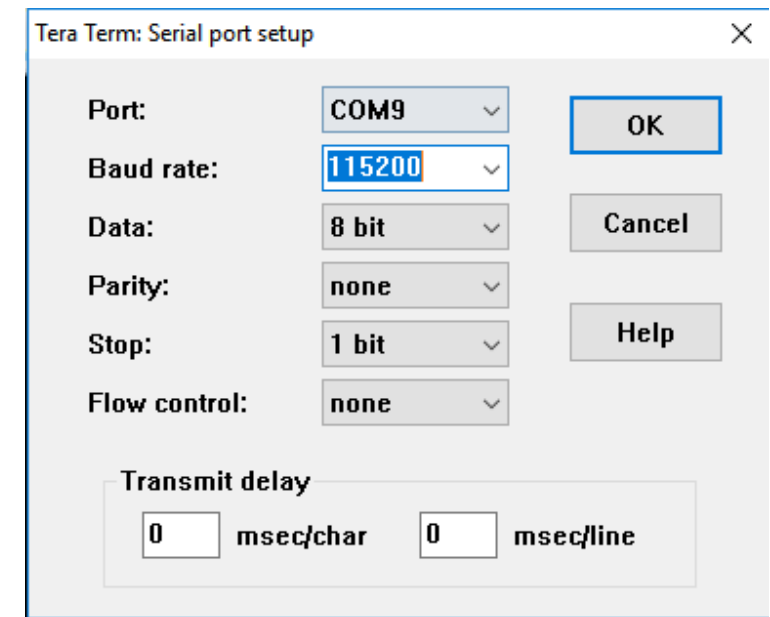
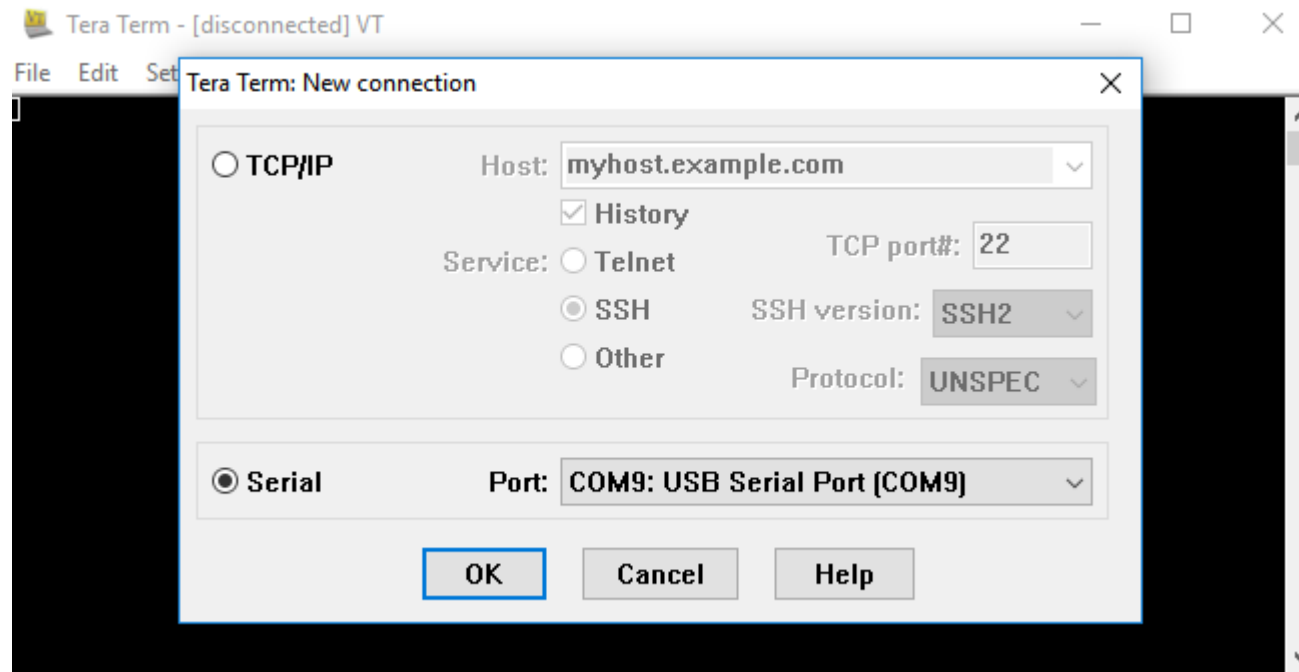


Run Design

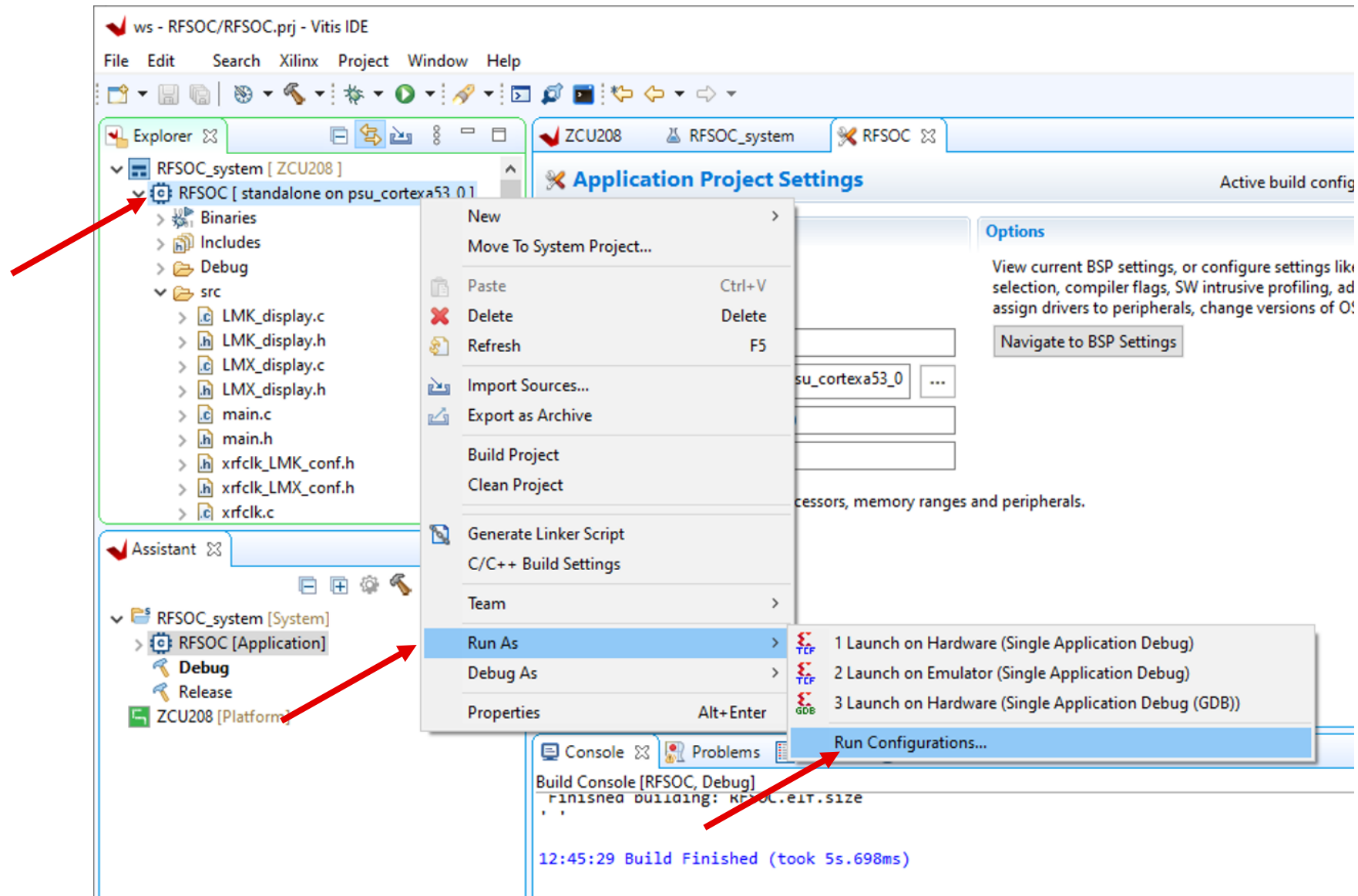
Open a Terminal Window

Open the COM port on the compute and set the rate to 115200.

TeraTerm can be used. See [UG1036](#).

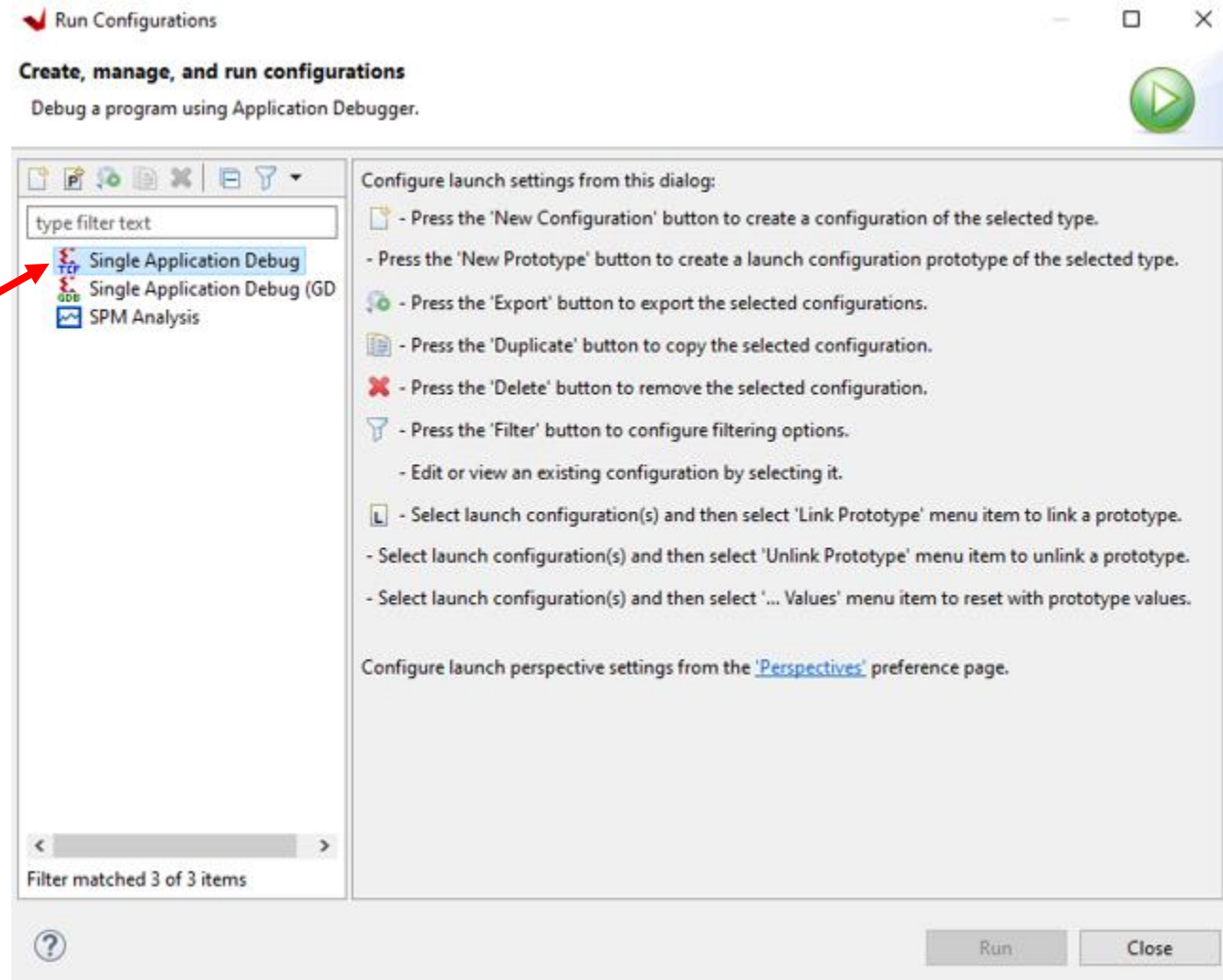


Setup Run Configuration

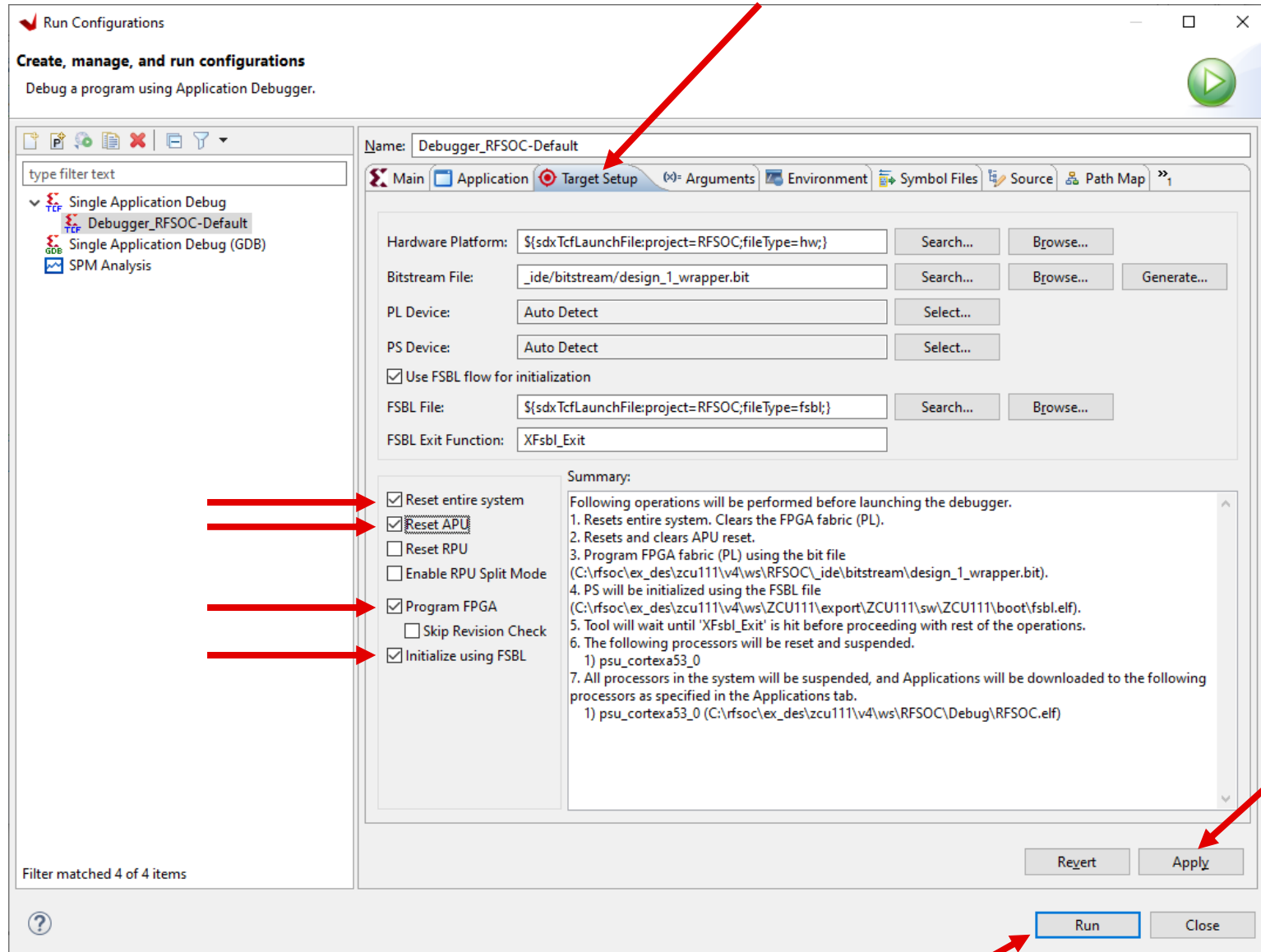


Run Configuration Cont'd

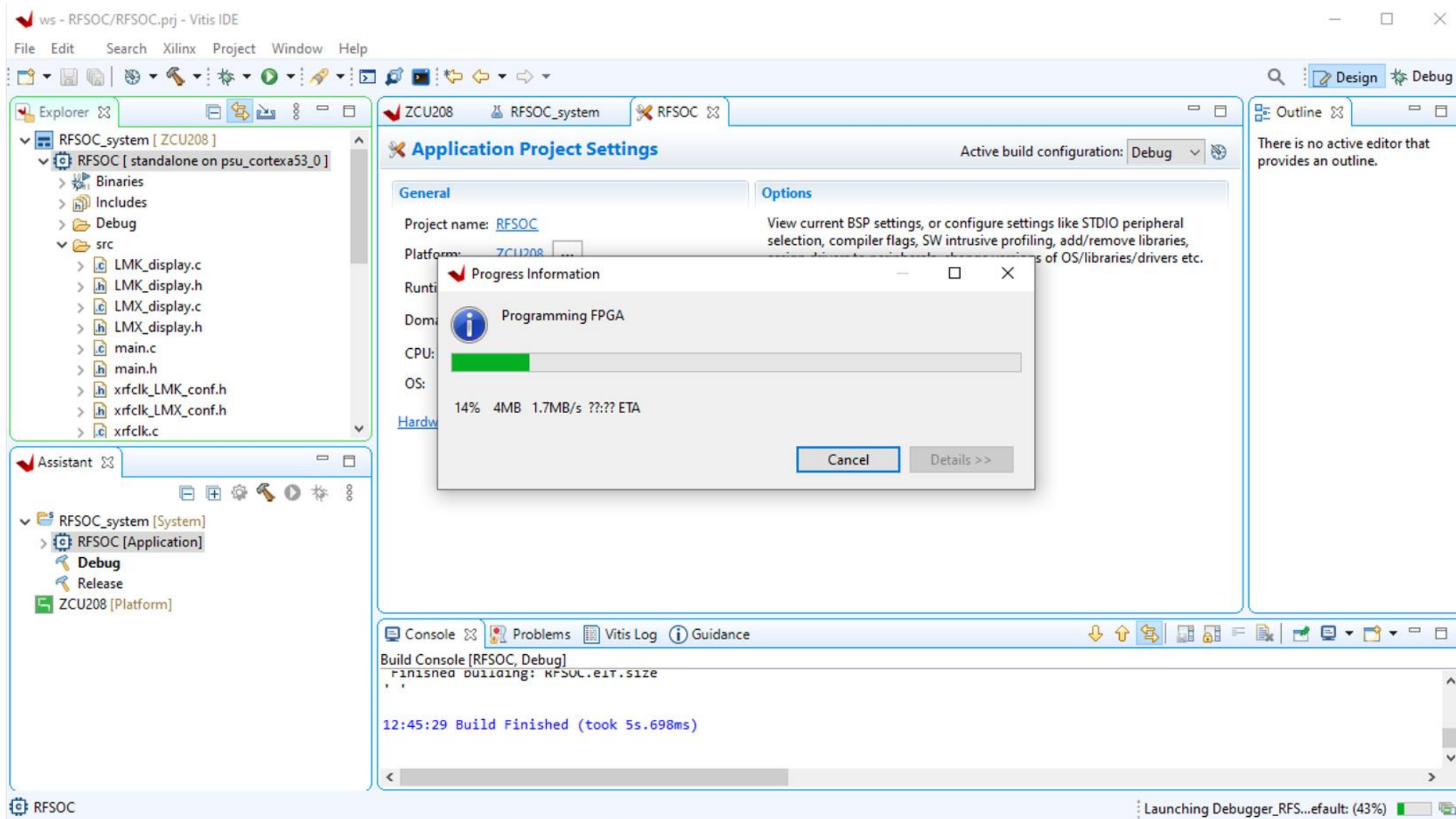
Double
Click



Run Configuration Cont'd



Run Design



Application Startup

The application...

1. Programs the clocks.
2. Issues the data converters master reset.
3. Displays the Power-on Sequence Step of the data converters.

```
COM41:115200baud - Tera Term VT
File Edit Setup Control Window Help

Xilinx Zynq MP First Stage Boot Loader
Release 2020.2 Jun 24 2021 - 12:14:38
PMU-FW is not running, certain applications may not be supported.

#####
Hello RFSoc World!

RFDC IP Version: 2.4

Configuring the data converter clocks...
Configuring CLK104 LMK and LMX devices
Clk settings read from LMK -----
CLKin1_freq: 10000KHz
DCLKout00(RFIN_RF1 ): 184320KHz SDCLKout01(RF1_ADC_SYNC ): -----
DCLKout02(NC ): ----- SDCLKout03(AMS_SYSREF ): -----
DCLKout04(RFIN_RF2 ): 184320KHz SDCLKout05(RF2_DAC_SYNC ): -----
DCLKout06(DAC_REFCLK): 184320KHz SDCLKout07(DDR_PL_CAP_SYNC): -----
DCLKout08(PL_CLK ): ----- SDCLKout09(PL_SYSREF ): -----
DCLKout10(NC ): ----- SDCLKout11(J10_SINGLE_END ): -----
DCLKout12(ADC_REFCLK): 184320KHz SDCLKout13(NC ): -----

Clk settings read from LMX_RF1 -----
CLKin_freq: 184320KHz
RFoutA Freq: -----
RFoutB Freq: -----

Clk settings read from LMX_RF2 -----
CLKin_freq: 184320KHz
RFoutA Freq: -----
RFoutB Freq: -----

=== Metal log enabled ===
metal: debug: registered generic bus

DeviceID: 0
Silicon Revision: 1
The RFDC controller is initialized.
Data Converter startup up is in progress...

The Power-on sequence step. 0xF is complete.
DAC Tile0 Power-on Sequence Step: 0x0000000F
ADC Tile2 Power-on Sequence Step: 0x0000000F

Data Converter start up is complete!
----- Startup Complete -----
```


Open Hardware Manager

The screenshot displays the Vivado 2020.2 Open Hardware Manager interface. The top menu bar includes File, Edit, Flow, Tools, Reports, Window, Layout, View, and Help. The left sidebar shows the PROJECT MANAGER and IP INTEGRATOR sections. The PROJECT MANAGER section includes Settings, Add Sources, Language Templates, and IP Catalog. The IP INTEGRATOR section includes Create Block Design, Open Block Design, and Generate Block Design. The right pane shows a block design diagram with various components like ZYNQ UltraSCALE+, ps8_0_axi_periph, usp_rf_data_converter_1, and system_ila_0. The bottom pane shows the Tcl Console with a log of synthesis and implementation steps.

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

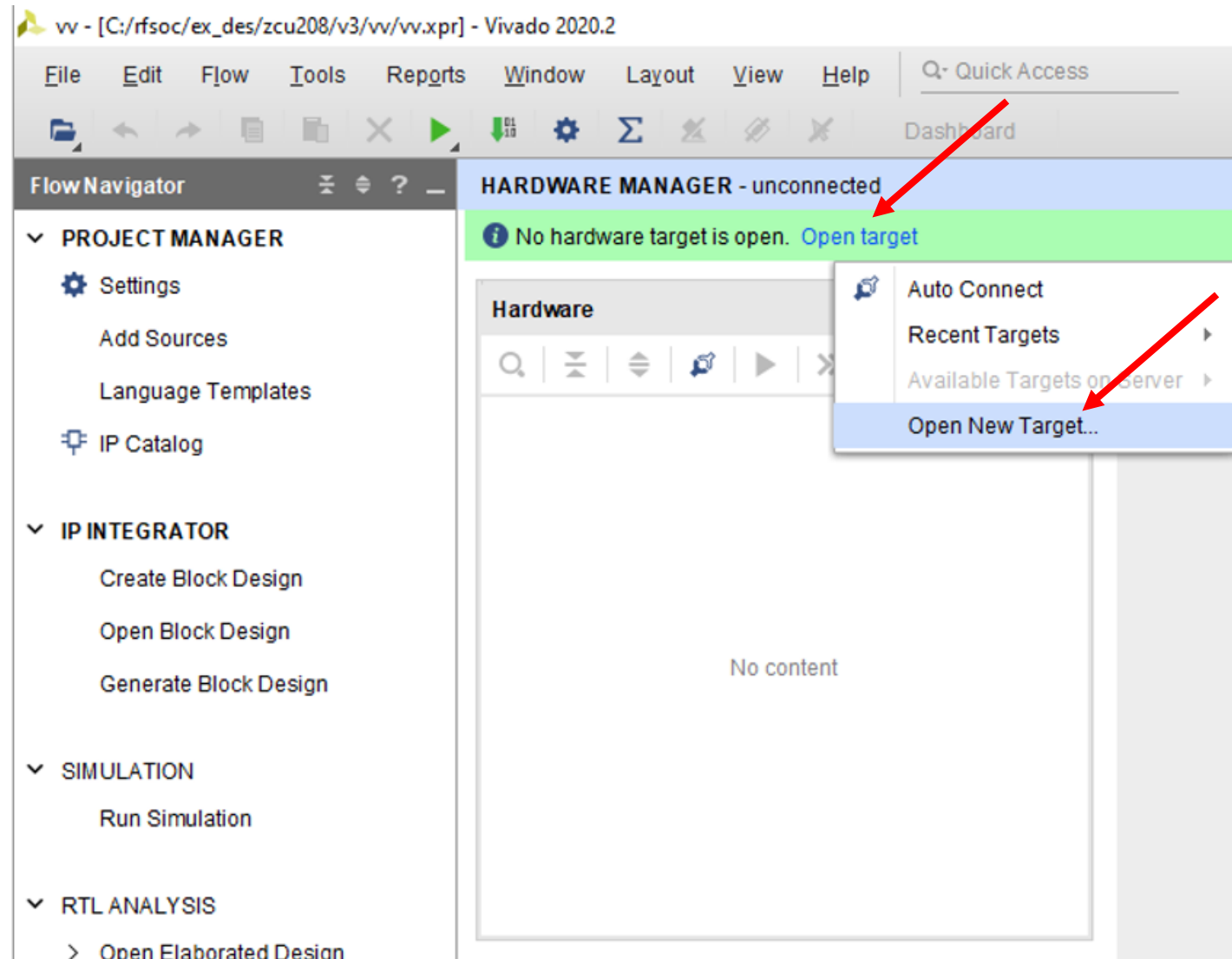
Block Design Diagram:

- Components: ZYNQ UltraSCALE+, ps8_0_axi_periph, usp_rf_data_converter_1, system_ila_0, axi_gpio_spi_mux, util_ds_buf_0, util_ds_buf_1, vio_0 (VIO), and Processor System Reset.
- Interconnections: The diagram shows the internal connections between these components, including data paths, control signals, and clock signals.

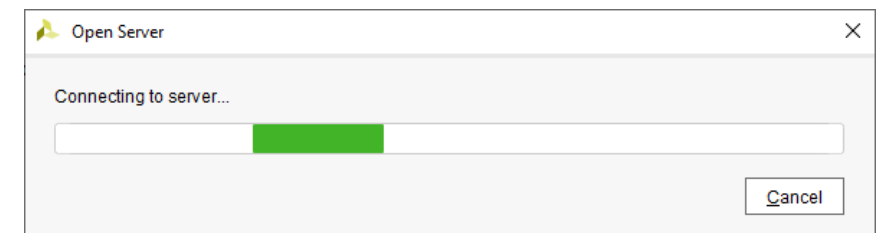
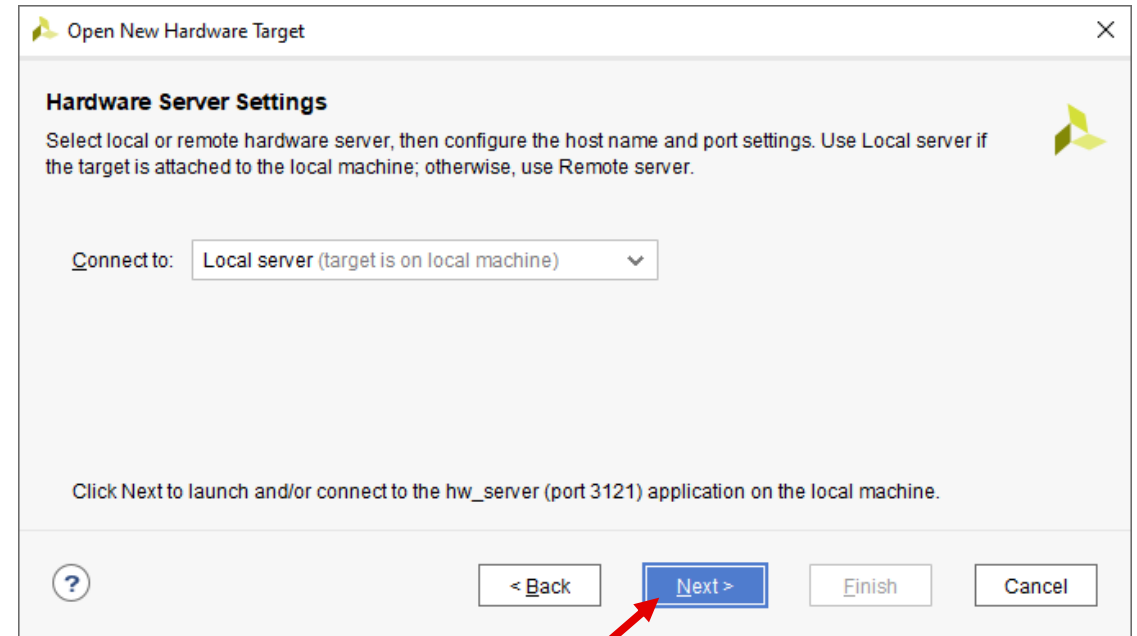
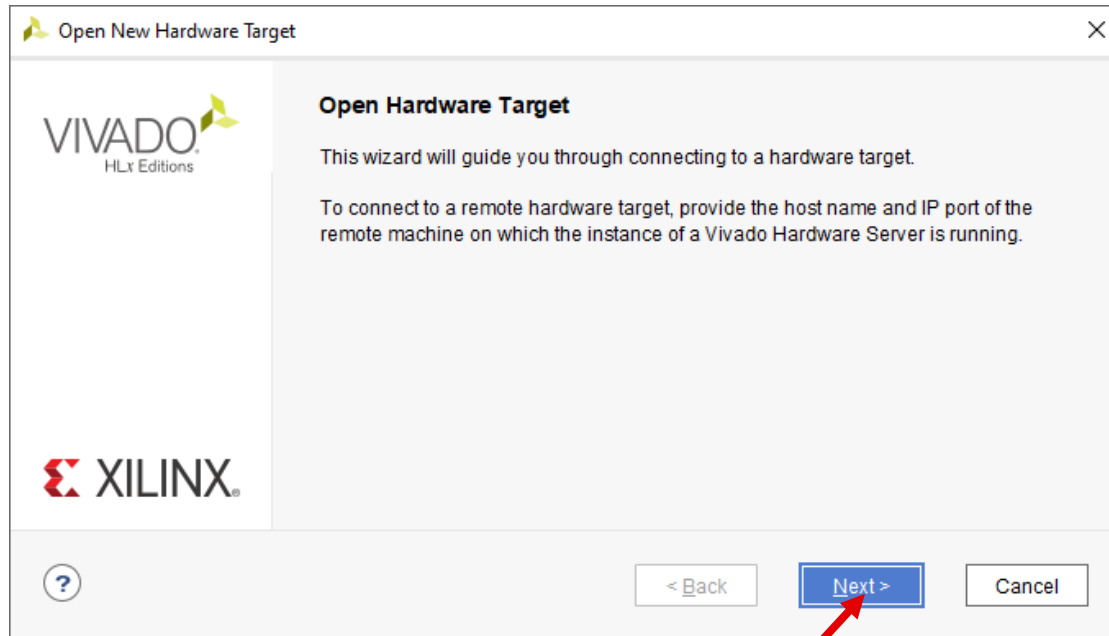
Tcl Console Log:

```
synth_1: C:/rfsoc/ex_des/zcu208/v3/vv/vv.runs/synth_1/runme.log
[Thu Jun 24 11:22:17 2021] Launched impl_1...
Run output will be captured here: C:/rfsoc/ex_des/zcu208/v3/vv/vv.runs/impl_1/runme.log
launch_runs: Time (s): cpu = 00:00:09 ; elapsed = 00:00:18 . Memory (MB): peak = 1392.793 ; gain = 8.746
write_hw_platform -fixed -include_bit -force -file C:/rfsoc/ex_des/zcu208/v3/vv/design_1_wrapper.xsa
INFO: [Vivado 12-4895] Creating Hardware Platform: C:/rfsoc/ex_des/zcu208/v3/vv/design_1_wrapper.xsa ...
INFO: [Hsi 55-2053] elapsed time for repository (E:/Xilinx/Vivado/2020.2/data/embeddedsw) loading 0 seconds
INFO: [Vivado 12-12467] The Hardware Platform can be used for Hardware
INFO: [Vivado 12-4896] Successfully created Hardware Platform: C:/rfsoc/ex_des/zcu208/v3/vv/design_1_wrapper.xsa
write_hw_platform: Time (s): cpu = 00:00:30 ; elapsed = 00:00:30 . Memory (MB): peak = 1603.156 ; gain = 139.488
```


Open New Target



Open Hardware Target



Open Hardware Target Cont'd

Open New Hardware Target

Select Hardware Target

Select a hardware target from the list of available targets, then set the appropriate JTAG clock (TCK) frequency. If you do not see the expected devices, decrease the frequency or select a different target.

Hardware Targets

| Type | Name | JTAG Clock Frequency |
|------------|----------------------|----------------------|
| xilinx_tcf | Xilinx/672036123764A | 15000000 |

Add Xilinx Virtual Cable (XVC)

Hardware Devices (for unknown devices, specify the Instruction Register (IR) length)

| Name | ID Code | IR Length |
|------------|----------|-----------|
| xczu48dr_0 | 147FB093 | 12 |
| arm_dap_1 | 5BA00477 | 4 |

Hardware server: localhost:3121

< Back Next > Finish Cancel

Open New Hardware Target

Open Hardware Target Summary

Hardware Server Settings:

- Server: localhost:3121

Target Settings:

- Target: xilinx_tcf/Xilinx/672036123764A
- Frequency: 15000000

To connect to the hardware described above, click Finish

? < Back Next > Finish Cancel

Open Hardware Target

Opening target...

Background Cancel

Convert Data to the Analog Waveform Style

10MHz sine wave
going from the DDS
compiler to the DAC.

ADC capture to the
System ILA.

The screenshot shows the Vivado 2020.2 interface with the Hardware Manager open. The left sidebar contains the Project Manager, IP Integrator, Simulation, RTL Analysis, Synthesis, Implementation, and Program and Debug sections. The main window displays the Hardware Manager for a local host, showing a list of components including xilinx_tcf/Xilinx, xczu48dr_0, SysMon, hw_ila_1, hw_vio_1, arm_dap_1, and SysMon. A red arrow points from the 'hw_ila_1' component in the list to the 'Waveform - hw_ila_1' window. The waveform window shows a table of data for 'slot_0' and 'slot_1', with columns for Name and Value. A red arrow points from the 'slot_1: usp_rf_data_converter_1_m20_axis: TDATA' entry to the 'Waveform Style' menu. The 'Waveform Style' menu is open, showing options like Digital, Analog, and Analog Settings. A red arrow points from the 'Analog' option to the 'Analog Settings...' option. The 'Analog Settings...' dialog is also visible, showing a 'Trigger Setup - hw_ila_1' section.

Flow Navigator

- PROJECT MANAGER
 - Settings
 - Add Sources
 - Language Templates
 - IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
- PROGRAM AND DEBUG
 - Generate Bitstream
 - Open Hardware Manager
 - Open Target
 - Program Device

HARDWARE MANAGER - localhost/xilinx_tcf/Xilinx/672036123764A

Waveform - hw_ila_1

ILA Status: Idle

| Name | Value |
|---|-------|
| slot_0: Conn: Interface | |
| slot_0: Conn: T Channel | |
| slot_0: axis_data_fifo_0_M_AXIS: TVALID | 0 |
| slot_0: axis_data_fifo_0_M_AXIS: TLAST | 0 |
| slot_0: Conn: TDATA | 0 |
| slot_1: usp_rf_data_converter_1_m20_axis: Interface | |
| slot_1: usp_rf_data_converter_1_m20_axis: T Channel | |
| slot_1: usp_rf_data_converter_1_m20_axis: TVALID | 0 |
| slot_1: usp_rf_data_converter_1_m20_axis: TREADY | 0 |
| slot_1: usp_rf_data_converter_1_m20_axis: TLAST | 0 |
| slot_1: usp_rf_data_converter_1_m20_axis: TDATA | 0 |

Settings - hw_ila_1 Status - hw_ila_1

Core status: Idle

Capture status - Window 1 of 1

Window sample 0 of 4096

Idle

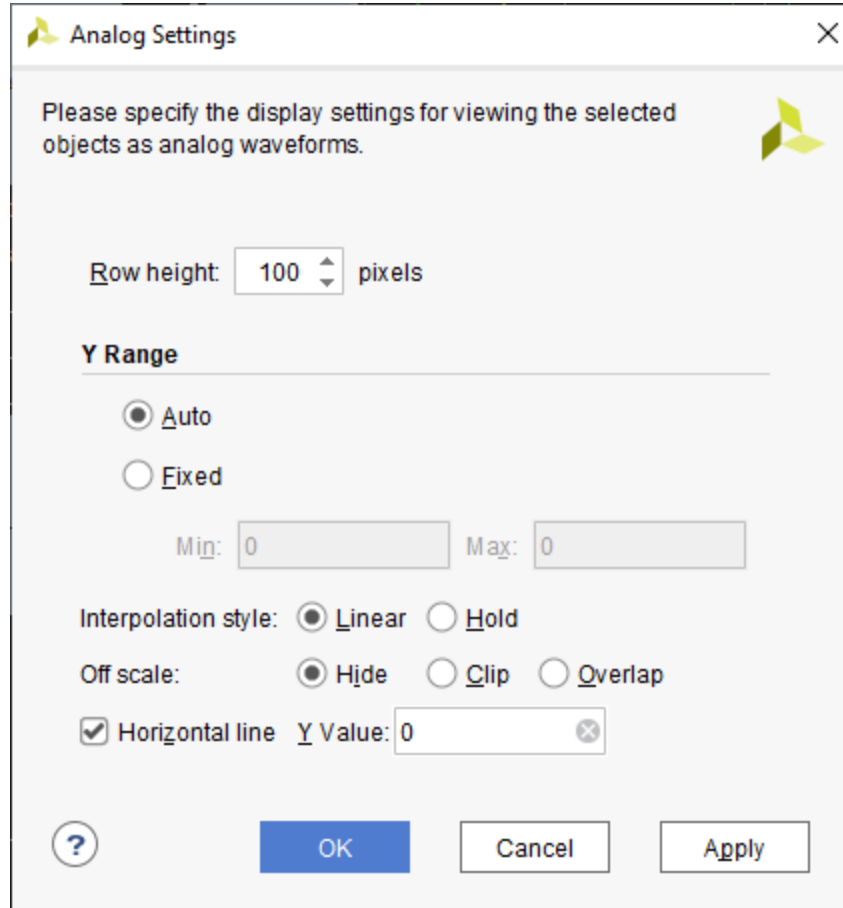
Waveform Style

- Digital
- ✓ Analog
- Analog Settings...

Trigger Setup - hw_ila_1

Analog Settings

Set Row height to 100.



The image shows a dialog box titled "Analog Settings" with a close button (X) in the top right corner. The dialog contains the following elements:

- A message: "Please specify the display settings for viewing the selected objects as analog waveforms." with a small green logo to its right.
- A "Row height" section with a text box containing "100" and a "pixels" label.
- A "Y Range" section with a horizontal line below the title.
 - Two radio buttons: "Auto" (selected) and "Fixed".
 - Below "Fixed", there are "Min:" and "Max:" labels followed by text boxes, both containing "0".
- An "Interpolation style" section with two radio buttons: "Linear" (selected) and "Hold".
- An "Off scale" section with three radio buttons: "Hide" (selected), "Clip", and "Overlap".
- A checked checkbox labeled "Horizontal line" followed by a "Y Value:" label and a text box containing "0" with a small 'x' icon to its right.
- At the bottom, there are four buttons: a help button (question mark in a circle), an "OK" button, a "Cancel" button, and an "Apply" button.

Radix

The screenshot shows the Xilinx ILS (ILA) interface. The main window displays the configuration of the ILA core. The 'Name' column lists the signals, and the 'Value' column shows their current values. The signals are organized into slots:

- slot_0: Conn: Interface
 - slot_0: Conn: T Channel
 - slot_0: axis_data_fifo_0_M_AXIS: TVALID (0)
 - slot_0: axis_data_fifo_0_M_AXIS: TLAST (0)
 - slot_0: Conn: TDATA (0)
- slot_1: usp_rf_data_converter_1_m20_axis: Interface
 - slot_1: usp_rf_data_converter_1_m20_axis: T Channel
 - slot_1: usp_rf_data_converter_1_m20_axis: TVALID (0)
 - slot_1: usp_rf_data_converter_1_m20_axis: TREADY (0)
 - slot_1: usp_rf_data_converter_1_m20_axis: TLAST (0)

Two red arrows point to the 'slot_0: Conn: TDATA' and 'slot_1: usp_rf_data_converter_1_m20_axis: T' signals. A context menu is open over the 'slot_1: usp_rf_data_converter_1_m20_axis: T' signal, showing the 'Radix' option. The 'Radix' menu is open, showing the following options:

- Default
- Binary
- Hexadecimal
- Octal
- ASCII
- Unsigned Decimal
- Signed Decimal** (selected)

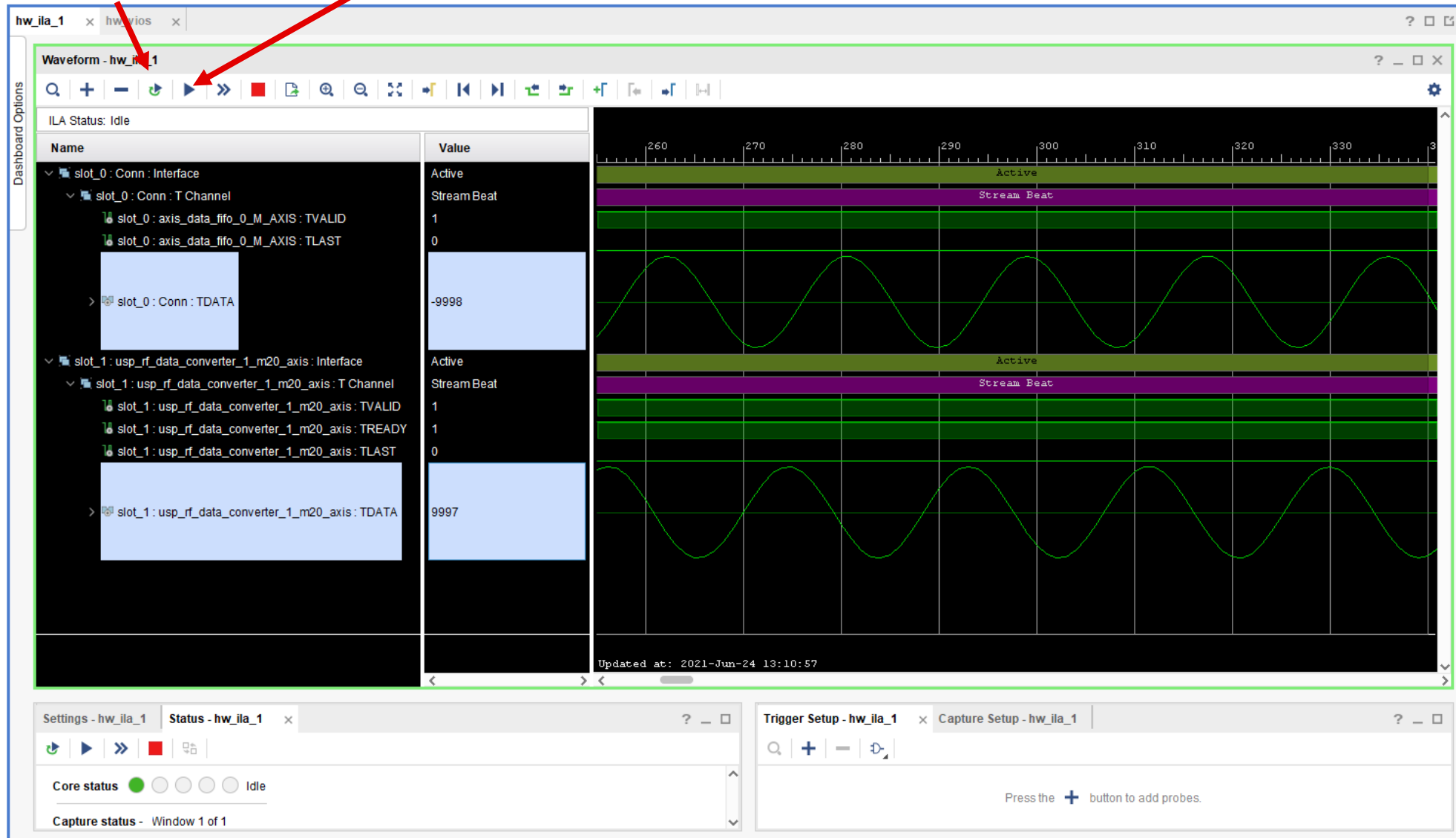
The 'Signed Decimal' option is highlighted with a red arrow. The 'Trigger Setup' window is also visible in the bottom right corner.

Use Radix of Signed Decimal.

System ILA Capture

Automatically retrigger

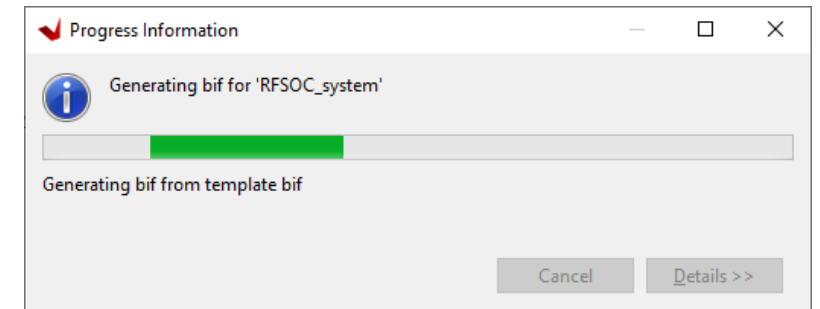
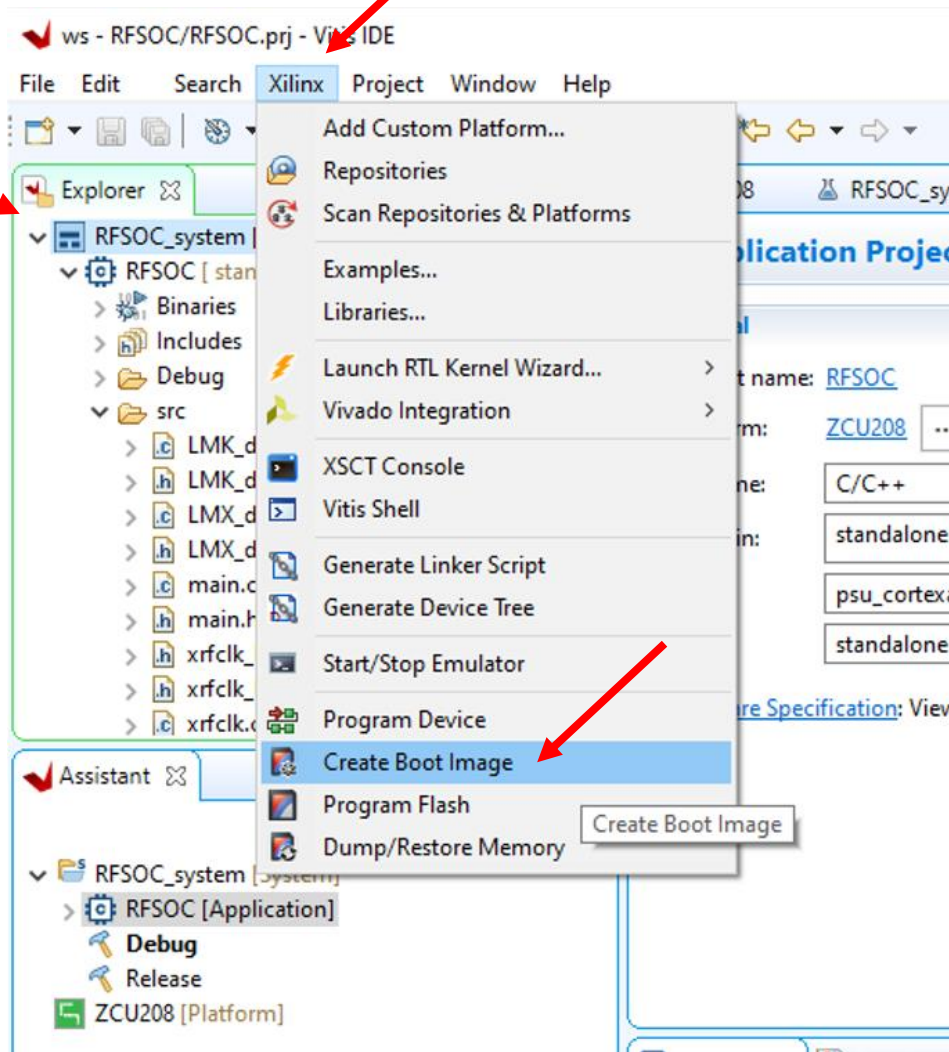
Trigger ILA capture



Boot Image

Create Boot Image

To run the application from the SD card rather than directly from Vitis™, create the boot.bin file.



Create boot.bin File

Create Boot Image

Creates Zynq MP Boot Image in .bin format from given FSBL elf and partition files in specified output folder.

Architecture: **Zynq MP**

☐ Create new BIF file ☒ Import from existing BIF file

Import BIF file path: **Browse...**

Basic **Security**

Output BIF file path: **Browse...**

UDF data: **Browse...**

☐ Split Output format: **BIN**

Output path: **Browse...**

Boot image partitions

| File path | Encrypted | Authenticated | |
|--|-----------|---------------|--|
| (bootloader) C:/rfsoc/ex_des/zcu208/v3/ws/ZCU208/export/Z... | none | none | Add Delete Edit Up Down |
| C:/rfsoc/ex_des/zcu208/v3/ws/RFSOC/_ide/bitstream/design_... | none | none | |
| C:/rfsoc/ex_des/zcu208/v3/ws/RFSOC/Debug/RFSOC.elf | none | none | |

Preview BIF Changes **Create Image** **Cancel**

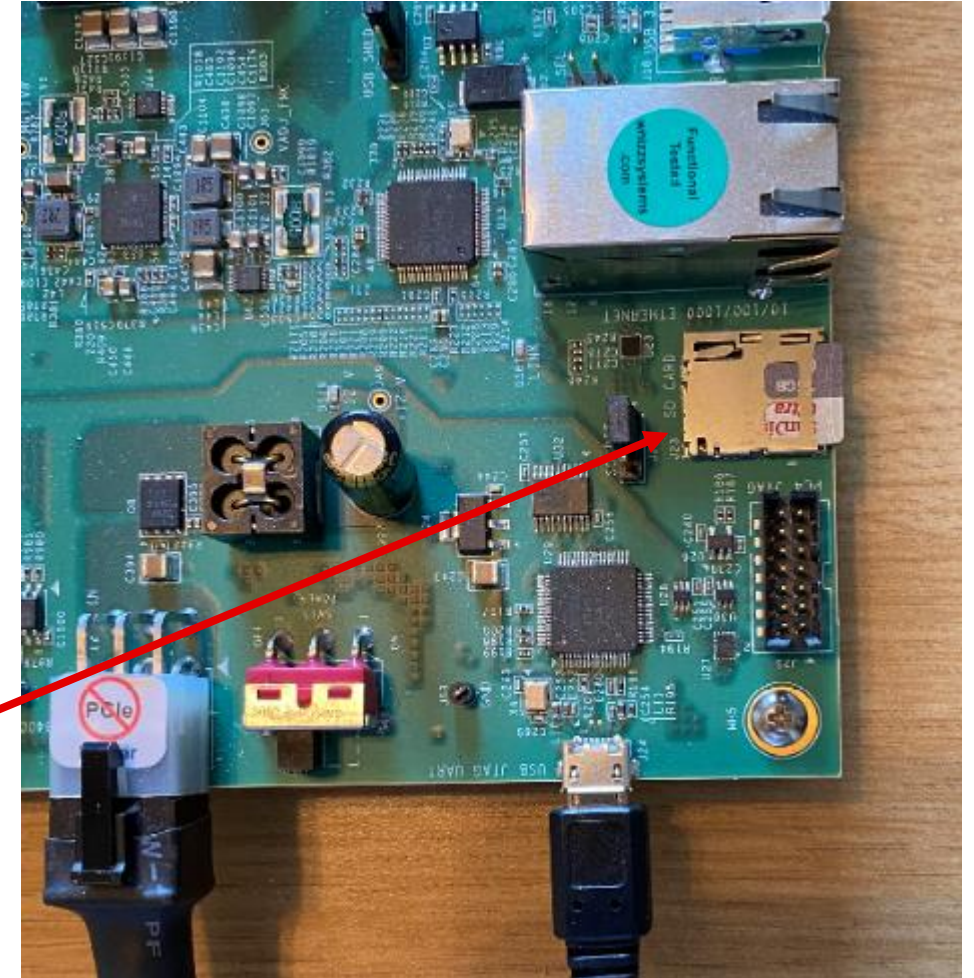
Note the location of the boot.bin file to put at the root level of the SD card.

Boot from SD Card

Set SW2 to on,off,off,off (SD Card boot mode).



Load boot.bin on the SD card, insert it into the board, and turn on the power.





Thank You

