

# Zynq® UltraScale+™ RFSoC Example Design: ZCU208

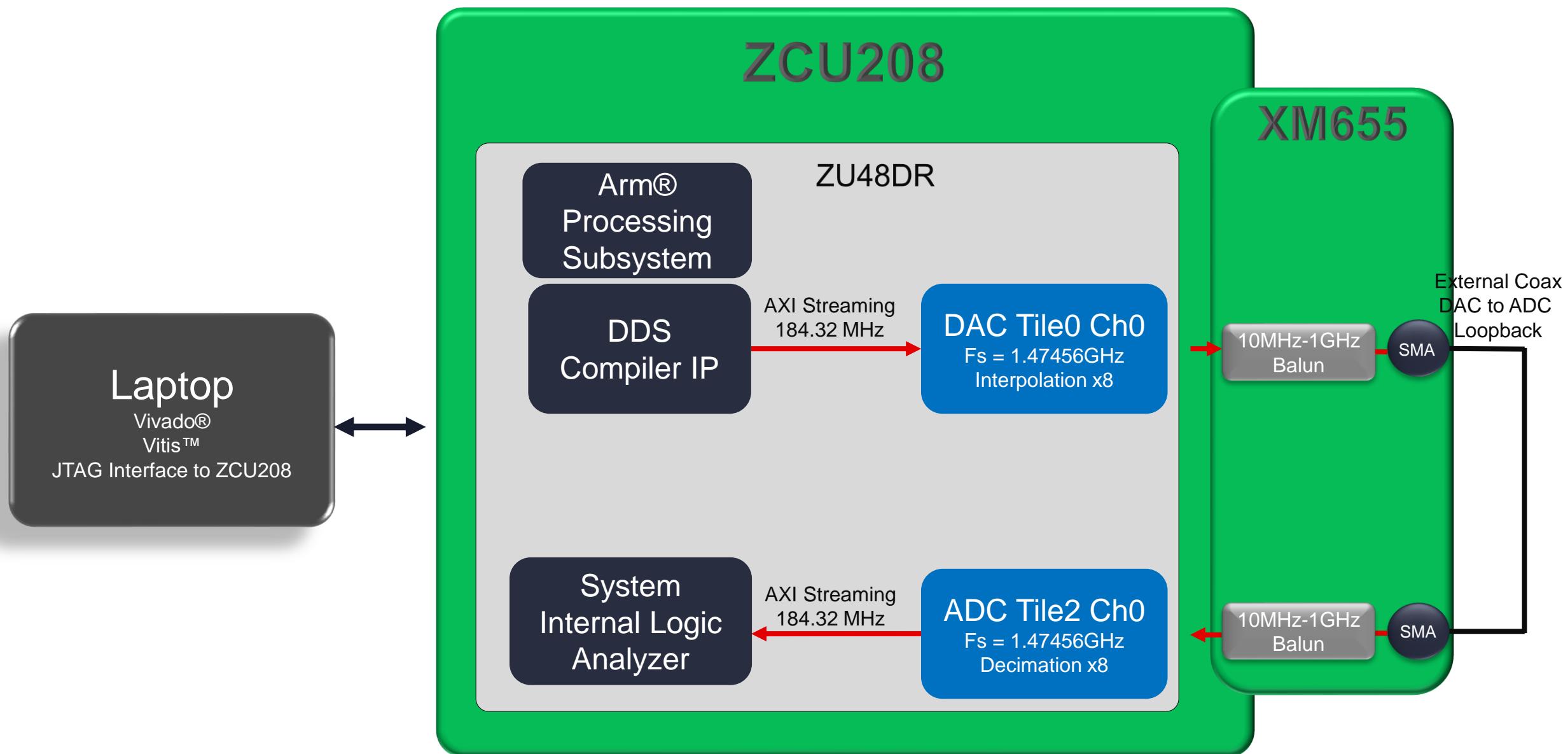
DDS Compiler for DAC and  
System ILA for ADC Capture – 2020.2



# Introduction

- ▶ This is an example starter design for the RFSoC.
- ▶ It uses the ZCU208 board.
- ▶ It uses a DAC and ADC sample rate of 1.47456GHz.
- ▶ The DAC will continuously play 10MHz sine wave from the DDS Compiler IP.
- ▶ The ADC output will be sent to a System ILA to be displayed in the Hardware Manager.
- ▶ DAC Tile228(0) Ch0 will be used (LF balun).
- ▶ ADC Tile226(2) Ch0 will be used (LF balun)
- ▶ 2020.2 Xilinx tools (Vivado® Design Suite and Vitis™ unified software platform).
- ▶ Design tested in the directory `c:\rfsoc\lex_des\zcu208\lv3\`.
- ▶ This kit comes with the Vivado HW project and SW source files.

# Demo Block Diagram

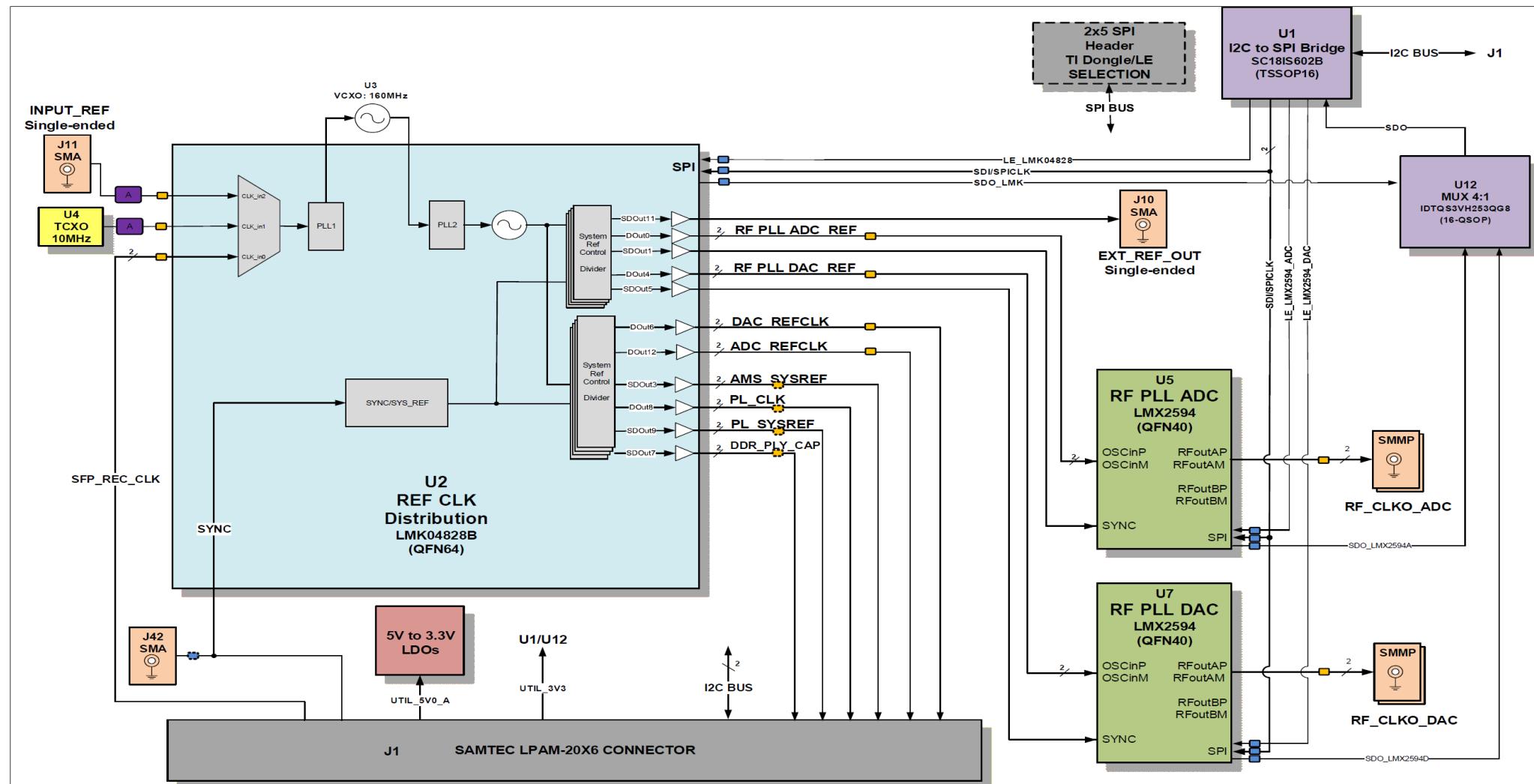


# CLK104 Block Diagram

Only the LMK04828B is used for this design; the LMX2594 outputs are powered down.

Clocking is configured via an I2C to SPI bridge.

## Block Diagram



# Data Converter Clocking

## CLK104/ZCU208



# DAC Setup

Basic   System Clocking   Advanced

DAC Tile 228   DAC Tile 229   DAC Tile 230   DAC Tile 231

Multi Tile Sync   Converter Band Mode   Variable Output Current

Enable Multi Tile Sync   Band: Single   Output Power: 20.0 [2.25 - 40.5]

Converter Configuration

DAC 0   DAC 1

Enable DAC

DUC Configuration

**DUC 0**

Invert Q Output  
 Inverse Sinc Filter  
Enable TDD Real Time Ports: Off

**Data Settings**

Analog Output Data: Real  
Interpolation Mode: 8x  
Samples per AXI4-Stream Cycle: 1  
Required AXI4-Stream clock: 184.320 MHz  
Datapath Mode: DUC 0 to Fs/2

**Mixer Settings**

Mixer Type: Coarse  
Mixer Mode: Real->Real  
Frequency: 0

**Analog Settings**

**DUC 1**

Invert Q Output  
 Inverse Sinc Filter  
Enable TDD Real Time Ports: Off

**Data Settings**

Analog Output Data: Real  
Interpolation Mode: Off  
Samples per AXI4-Stream Cycle: 16  
Datapath Mode: DUC 0 to Fs/2

**Mixer Settings**

Mixer Type: Off

**Analog Settings**

Nyquist Zone: Zone 1  
Decoder Mode: SNR Optimized

# ADC Setup

Component Name: usp\_rf\_data\_converter\_1

Basic System Clocking Advanced

Converter Setup

Converter Setup Advanced

Changing Converter Setup to Simple will cause current Advanced IP configuration to be lost.

RF-ADC RF-DAC

ADC Tile 224 ADC Tile 225 ADC Tile 226 ADC Tile 227

Multi Tile Sync Converter Band Mode Link Coupling

Enable Multi Tile Sync Band Single AC

Link Coupling

Converter Configuration

ADC 0 ADC 1

Enable ADC  Invert Q Output  Enable ADC  Invert Q Output

Dither  Enable ADC Observation Channel Ports  Dither  Enable ADC Observation C

Enable TDD Real Time Ports Off Off

Data Settings

Digital Output Data Real Real

Decimation Mode 8x Off

Samples per AXI4-Stream Cycle 1 8

Required AXI4-Stream clock: 184.320 MHz

Mixer Settings

Mixer Type Coarse Off

Mixer Mode Real->Real Real->Real

Frequency 0

Analog Settings

Nyquist Zone Zone 1 Zone 1

Calibration Mode Mode2 Mode2

# Data Converter Clocking

Component Name `usp_rf_data_converter_1`

Basic System Clocking Advanced

AXI4-Lite Interface Configuration

AXI4-Lite Clock (MHz) `100.0` 

Tile Clocking Settings

Tile	Sampling Rate (GSPS)	Max Fs (GSPS)	PLL	Reference Clock (MHz)	PLL Ref Clock (MHz)	Ref Clock Divider	Fabric Clock (MHz)	Clock Out (MHz)	Clock Source	Distribute Clock
ADC 224	4	5.000	<input type="checkbox"/>	4000.000	-	1	0.0	250.000	ADC224	Off
ADC 225	4	5.000	<input type="checkbox"/>	4000.000	-	1	0.0	250.000	ADC225	Off
ADC 226	1.47456 	5.000	<input checked="" type="checkbox"/>	184.320	184.32	1	184.320	11.520	ADC226	Off
ADC 227	4	5.000	<input type="checkbox"/>	4000.000	-	1	0.0	250.000	ADC227	Off
DAC 228	1.47456 	7.000	<input checked="" type="checkbox"/>	184.320	184.32	1	184.320	184.320	DAC228	Off
DAC 229	4	10.000	<input type="checkbox"/>	4000.000	-	1	0.0	500.000	DAC229	Off
DAC 230	4	10.000	<input type="checkbox"/>	4000.000	-	1	0.0	500.000	DAC230	Off
DAC 231	4	10.000	<input type="checkbox"/>	4000.000	-	1	0.0	500.000	DAC231	Off

ADC226 Warning: Current PLL reference clock may have negative impact on phase noise performance

DAC228 Warning: Current PLL reference clock may have negative impact on phase noise performance

PLL Summary Settings

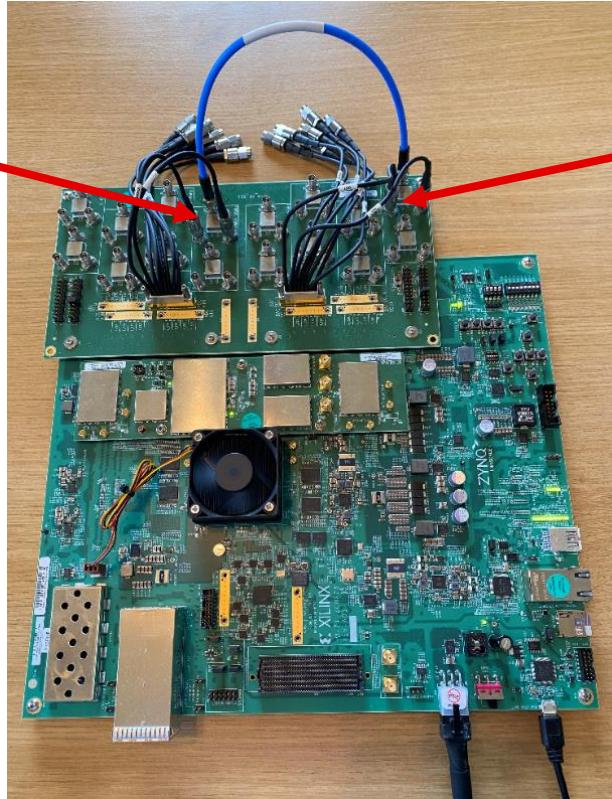
Tile	Vco (MHz)	Fb Div	M	R
ADC 224	-	-	-	-
ADC 225	-	-	-	-
ADC 226	8847.36	48	6	1
ADC 227	-	-	-	-
DAC 228	8847.36	48	6	1
DAC 229	-	-	-	-
DAC 230	-	-	-	-
DAC 231	-	-	-	-

# Board Setup for the Upcoming Designs

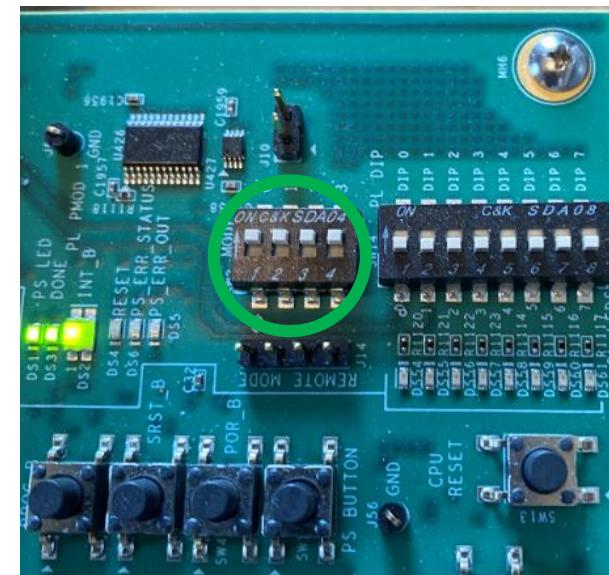
- ▶ Connect DAC Tile 228 Ch0 output to ADC Tile 226 Ch0 input on XM655 (low frequency balun connections).
- ▶ Set SW2 to on,on,on,on (JTAG boot mode).
- ▶ Connect USB to host for JTAG, PS UART, and System Controller UART access.

ADC Tile2 Ch0



DAC Tile0 Ch0

SW2



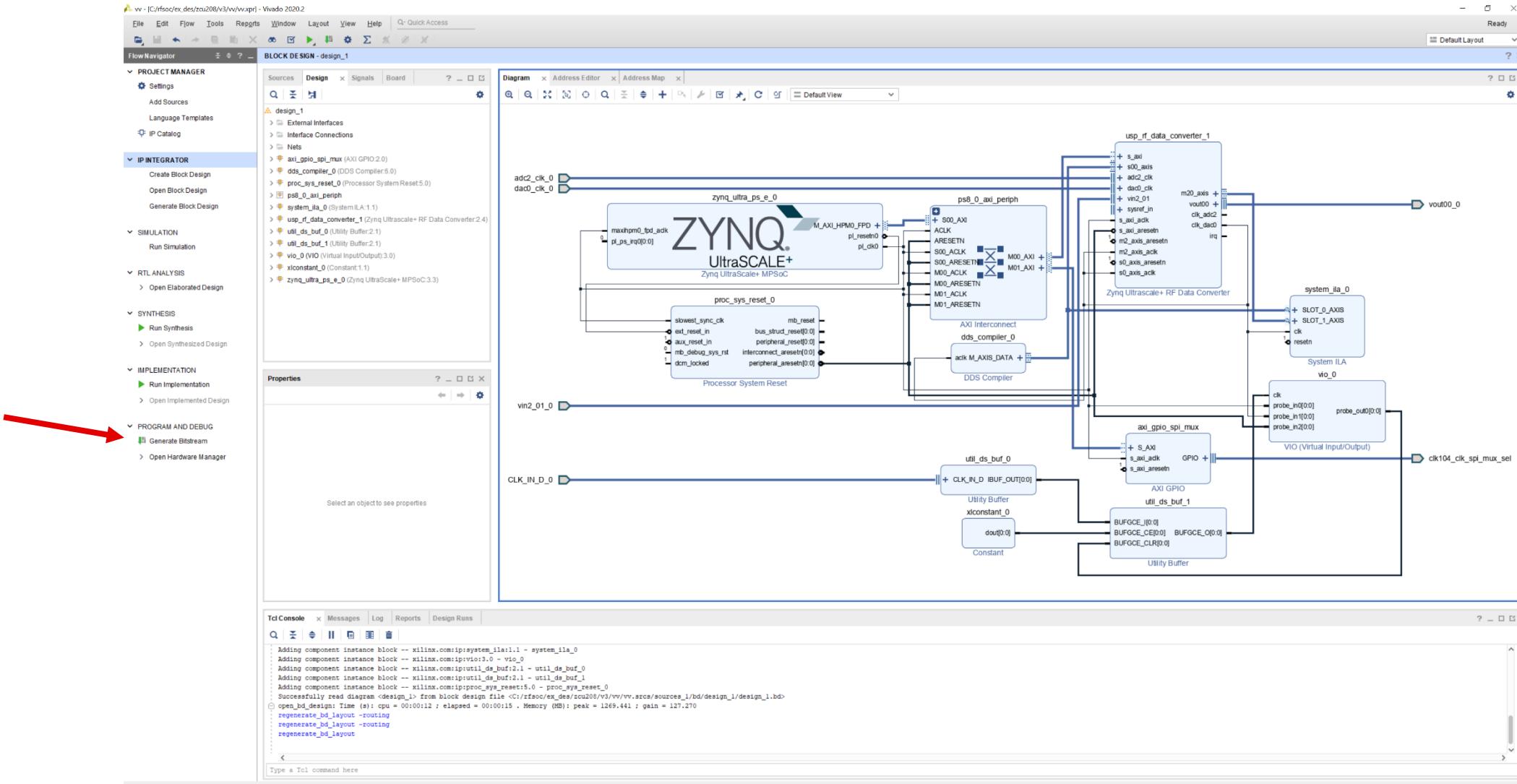
# Design Kit Contents

1. Extract the design kit to an appropriate folder—be mindful of the Windows path length requirement.
2. Extract `vv.xpr.zip`, which is the Vivado project.
3. Software source files in the “src” folder.
4. Design documentation in the `.pdf` file.

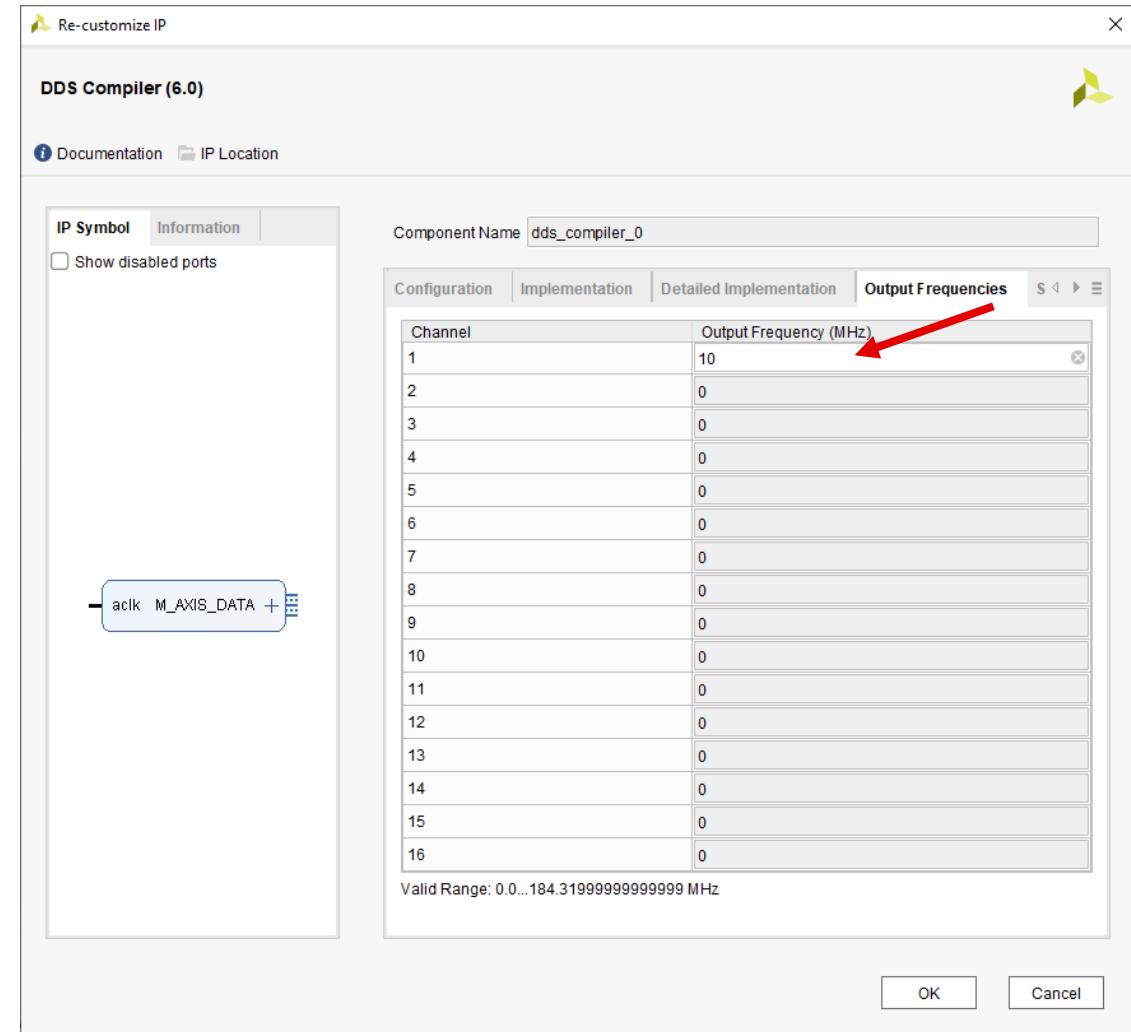
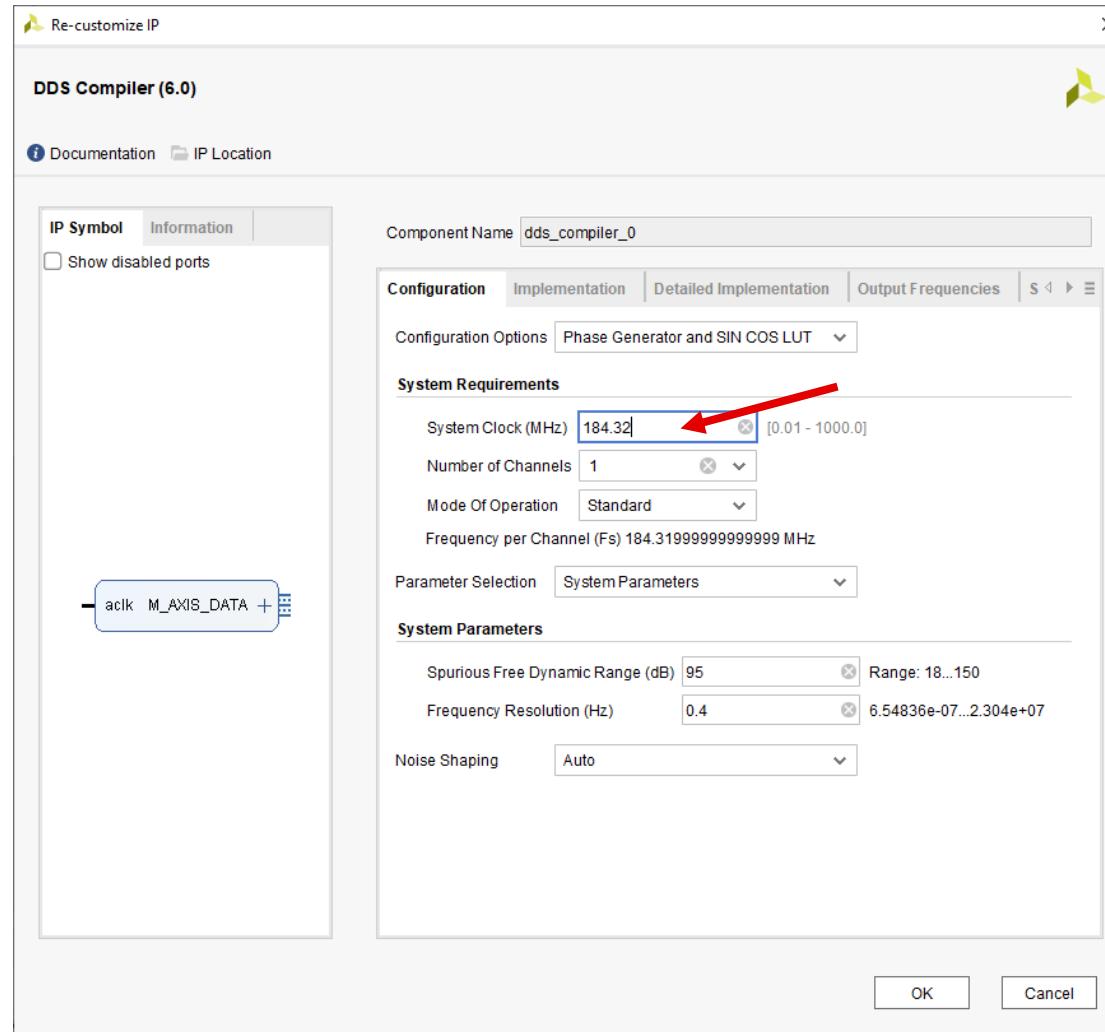
<input type="checkbox"/> Name	Date modified	Type	Size
src	7/10/2021 1:42 PM	File folder	
<code>vv.xpr.zip</code>	6/23/2021 1:54 PM	ZIP File	53,662 KB
<code>ZCU208_dds ila_2020p2_RevA.pdf</code>	7/10/2021 1:44 PM	Adobe Acrobat Docu...	4,465 KB

# Open Hardware Design and Generate the Bitstream

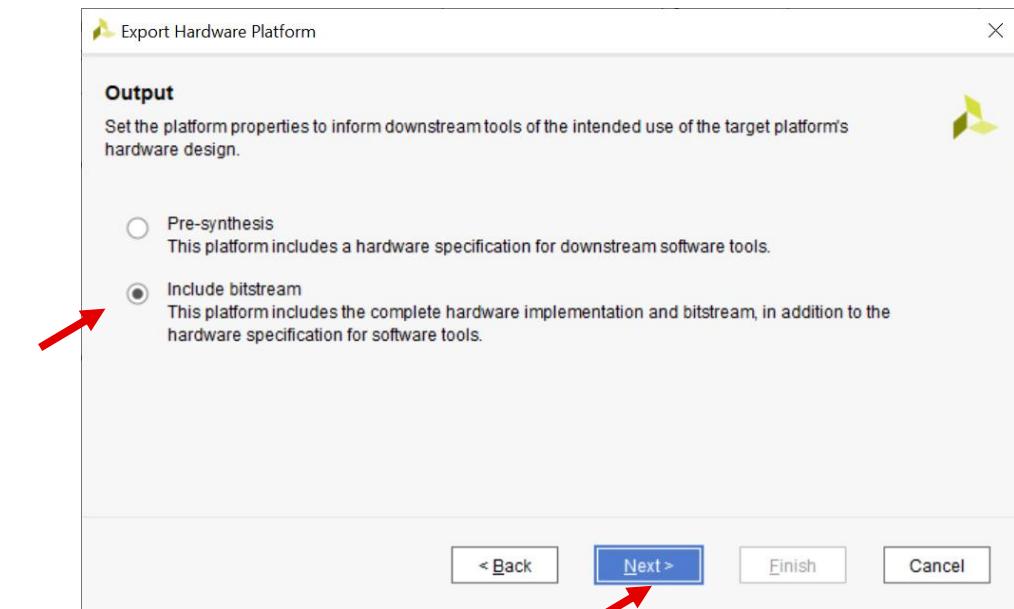
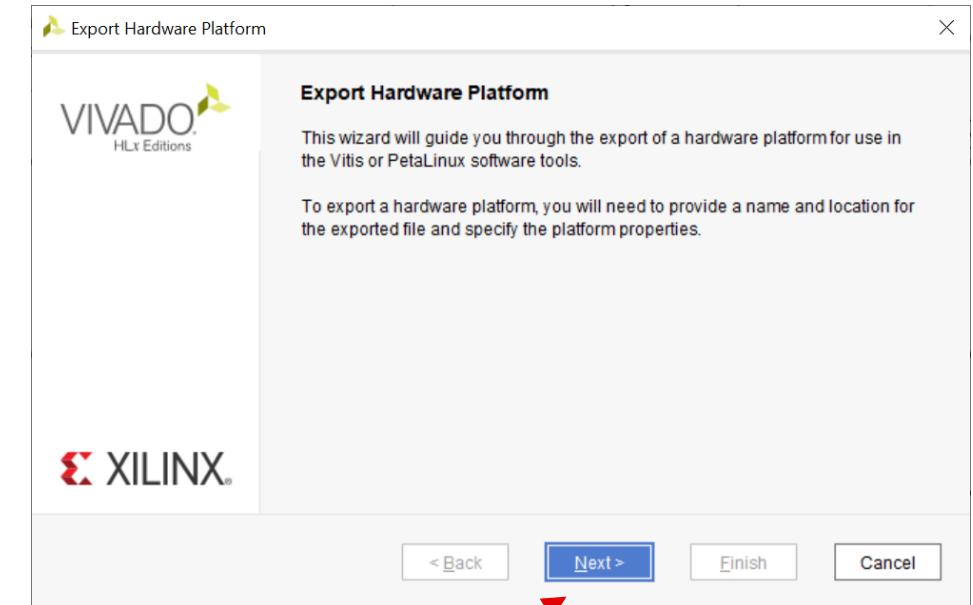
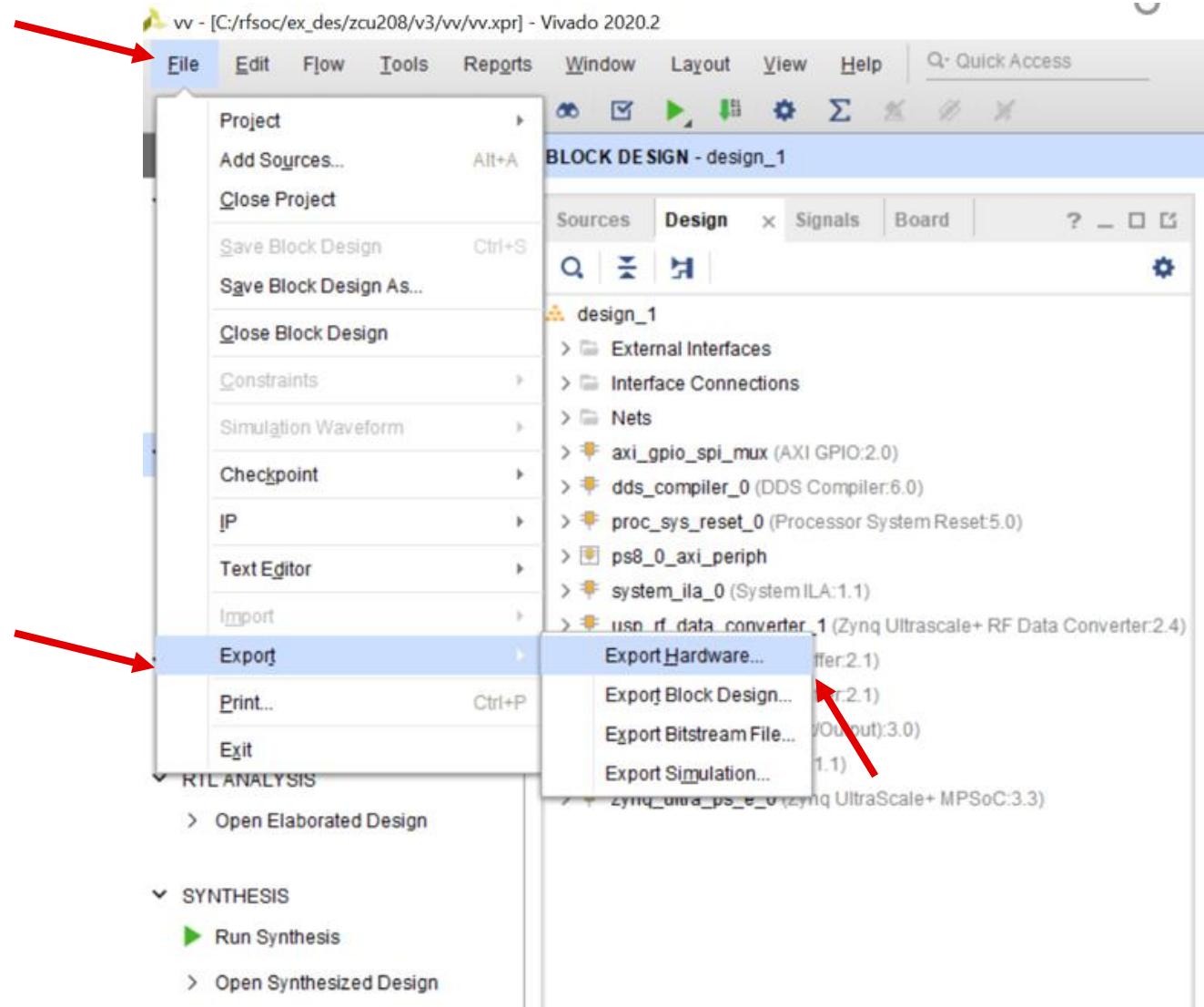
Extract vv.xpr.zip, open the design in Vivado®, and generate the bitstream.



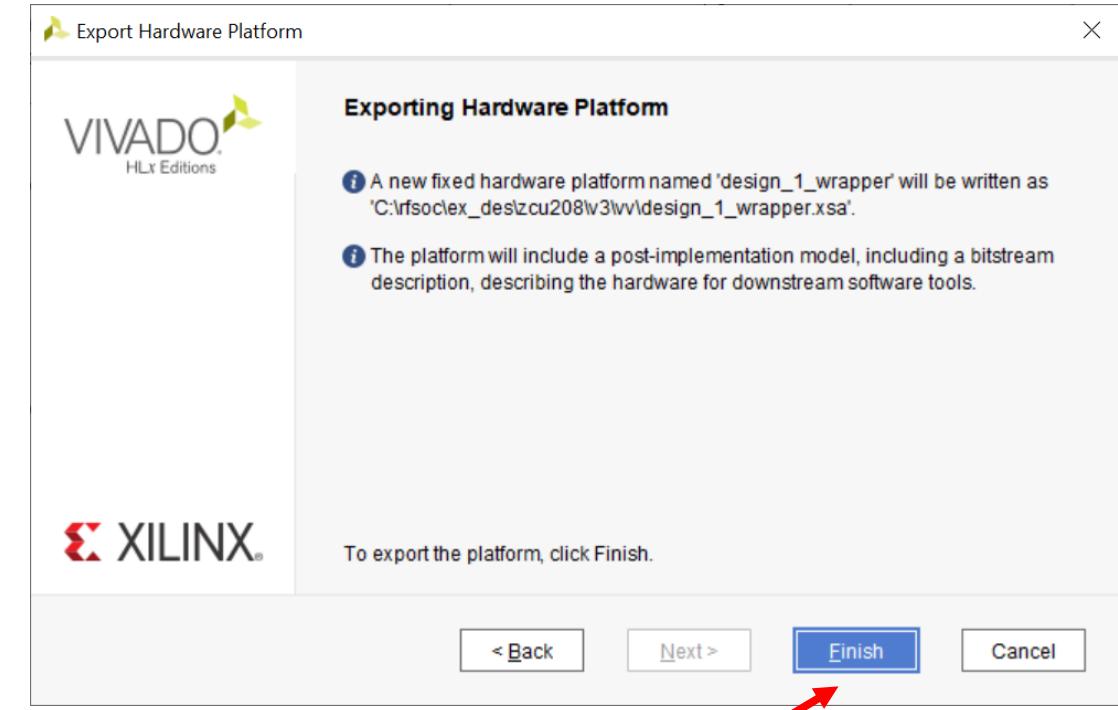
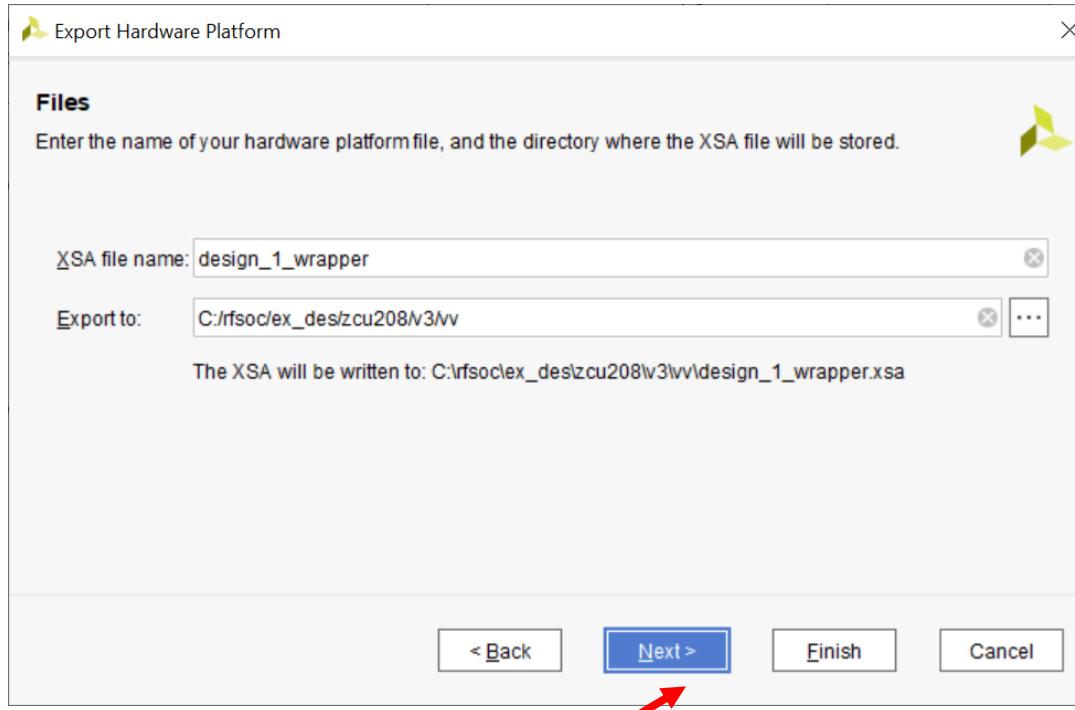
# DAC Sine Wave Generator (DDS Compiler IP)



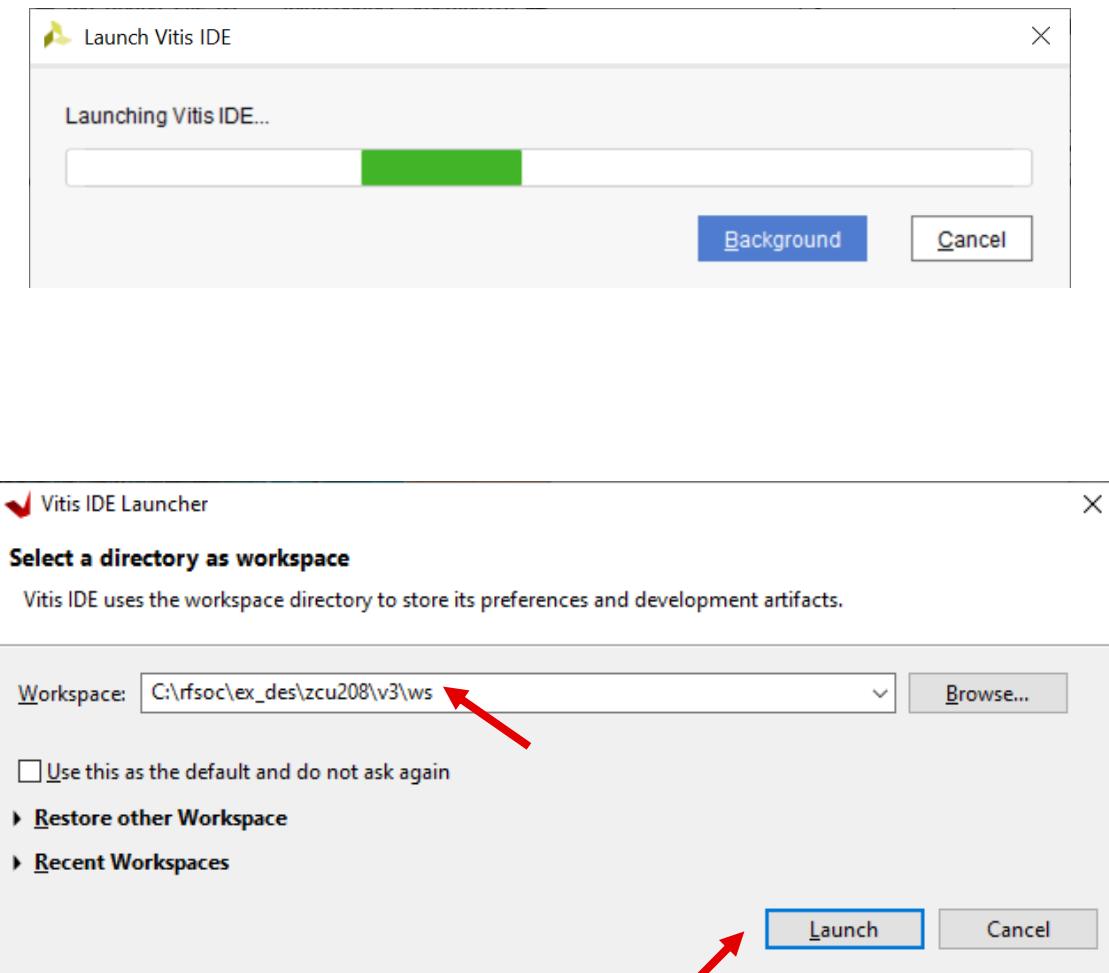
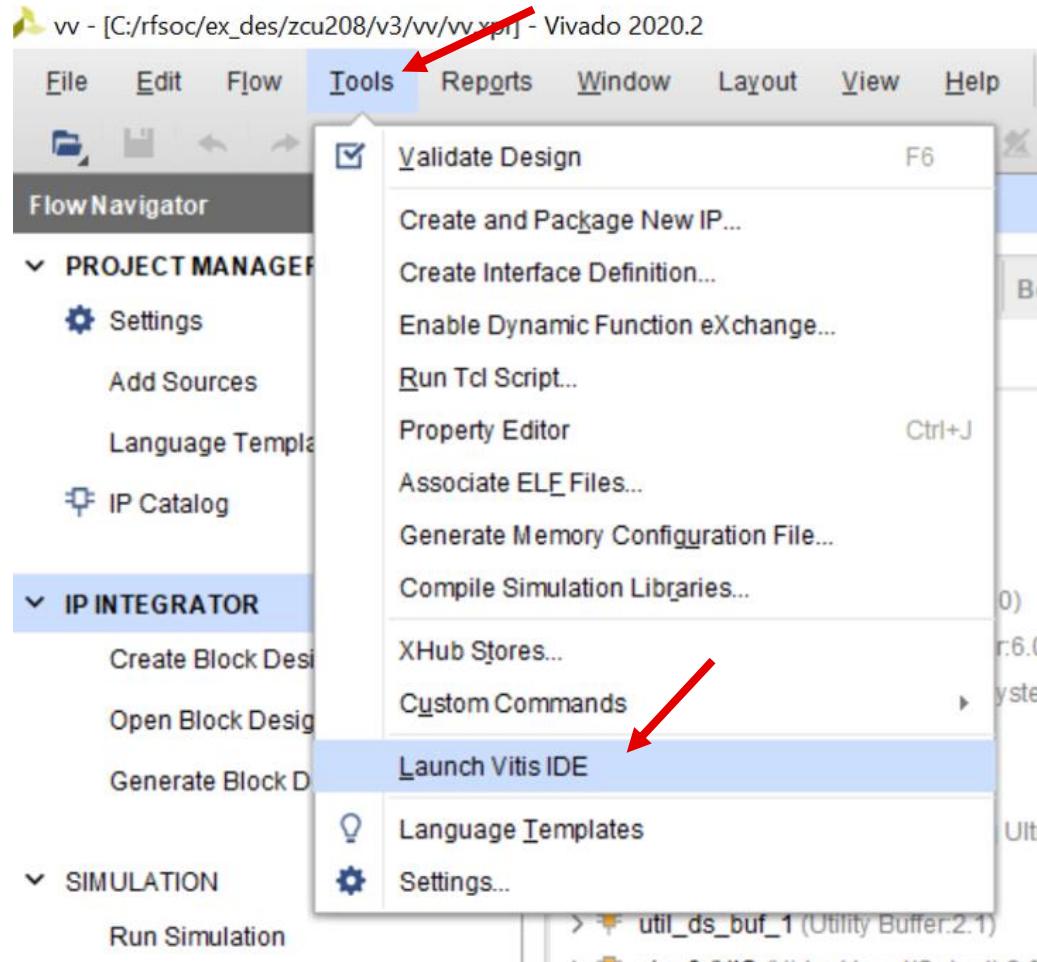
# Export Hardware



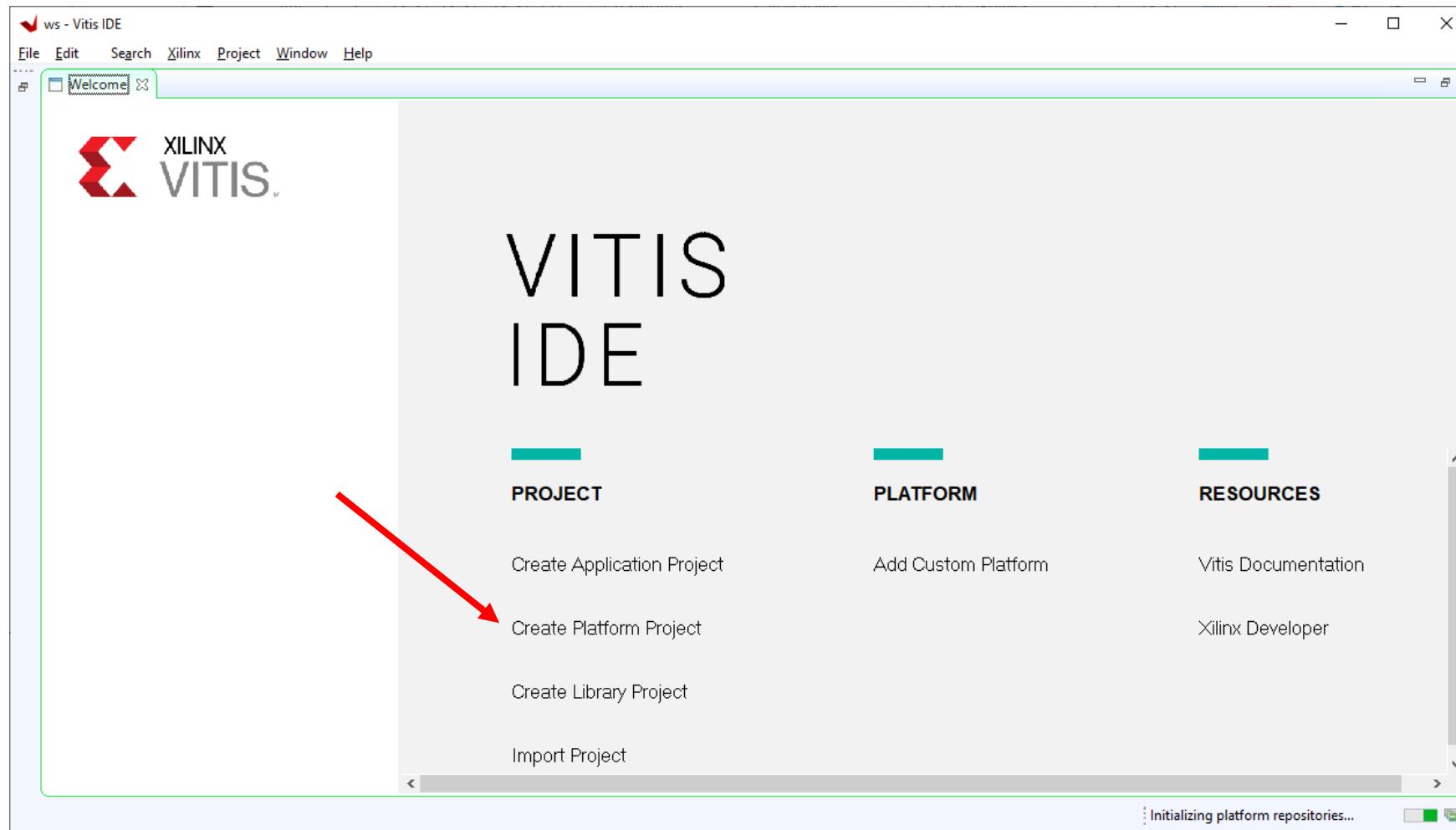
# Export Hardware Cont'd



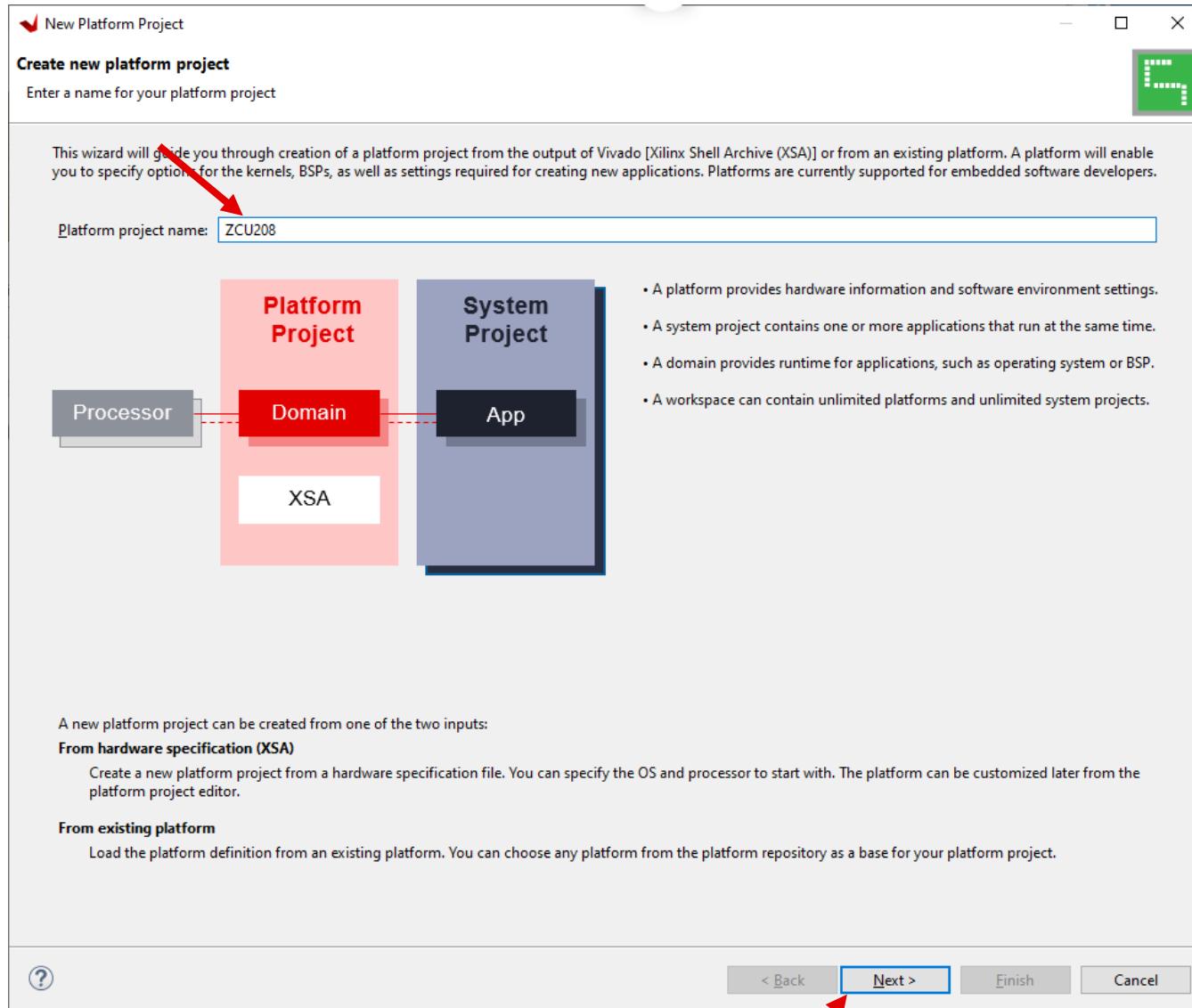
# Open Vitis™ Software Platform



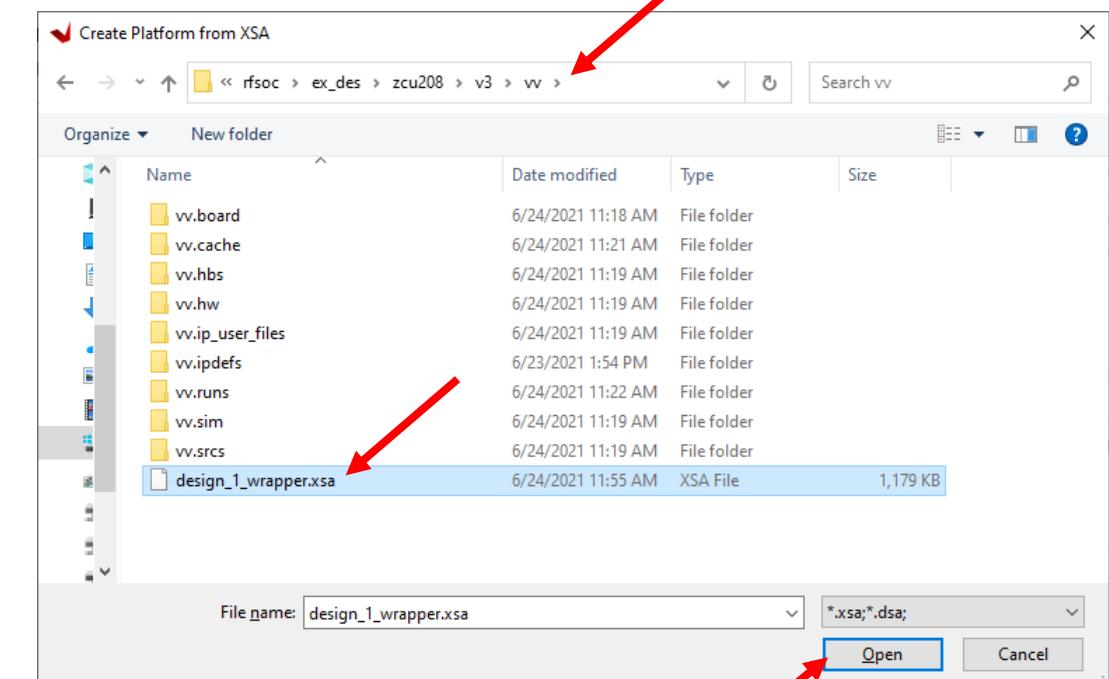
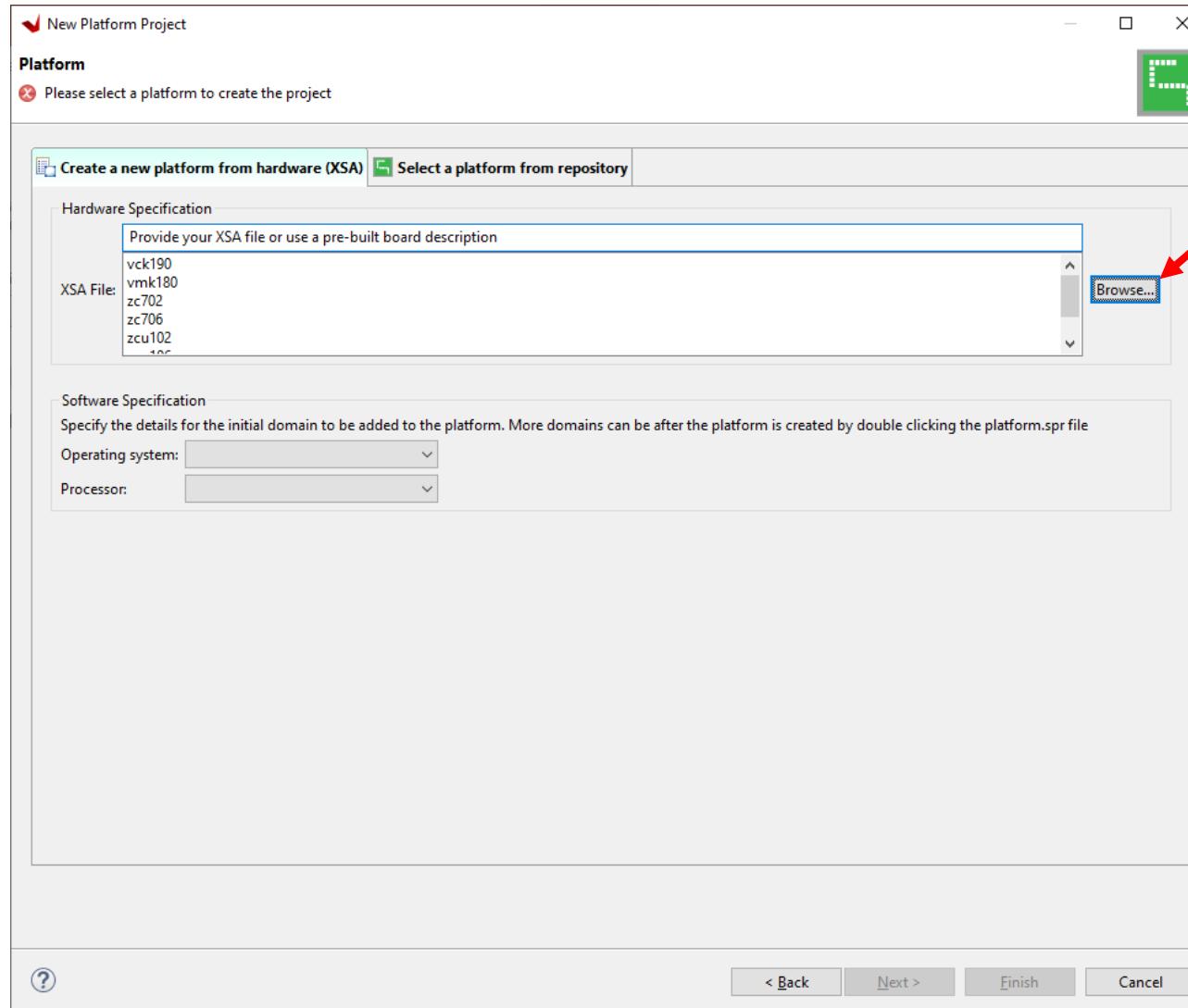
# Create Platform Project



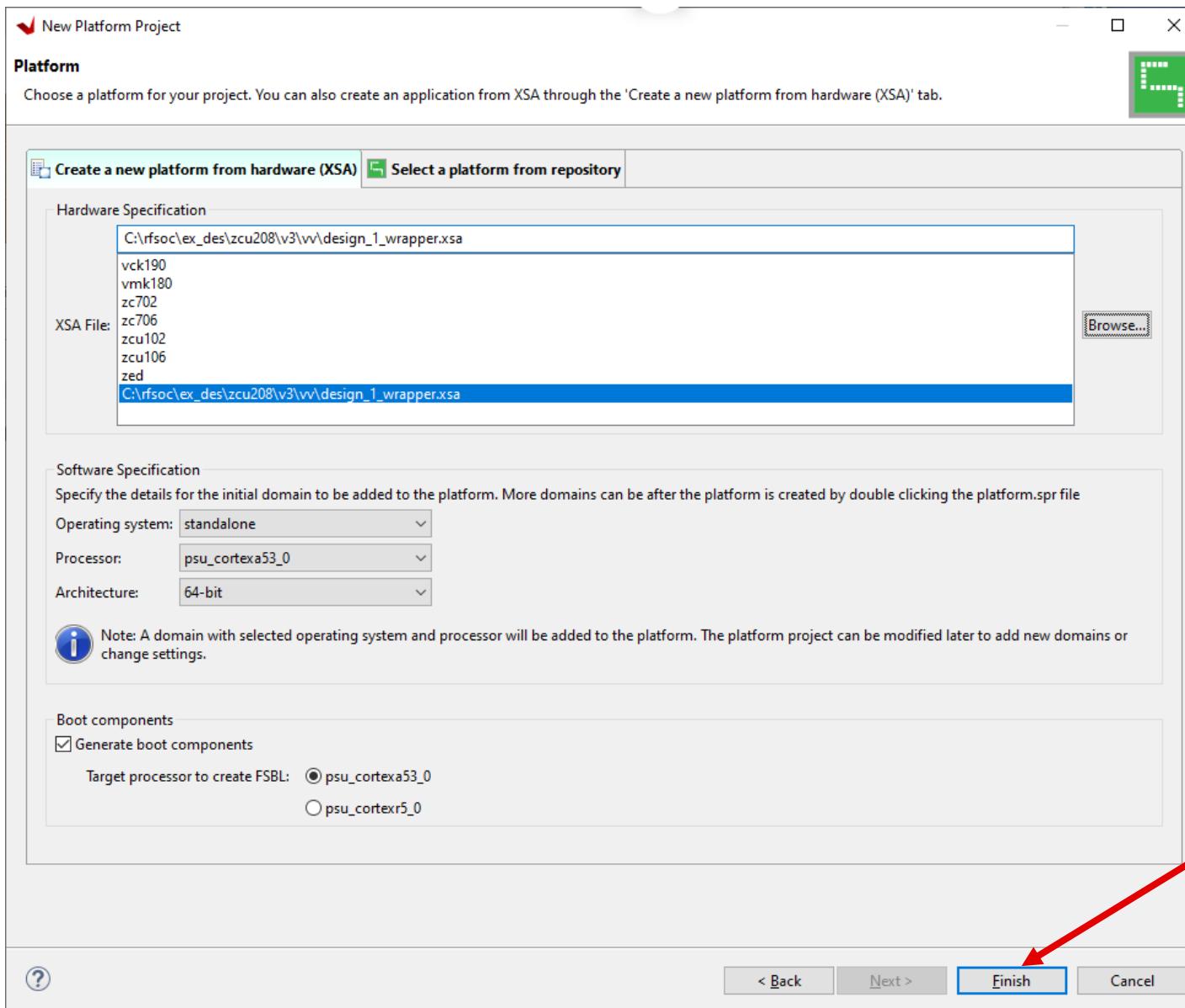
# Create Platform Project Cont'd



# Create Platform Project Cont'd

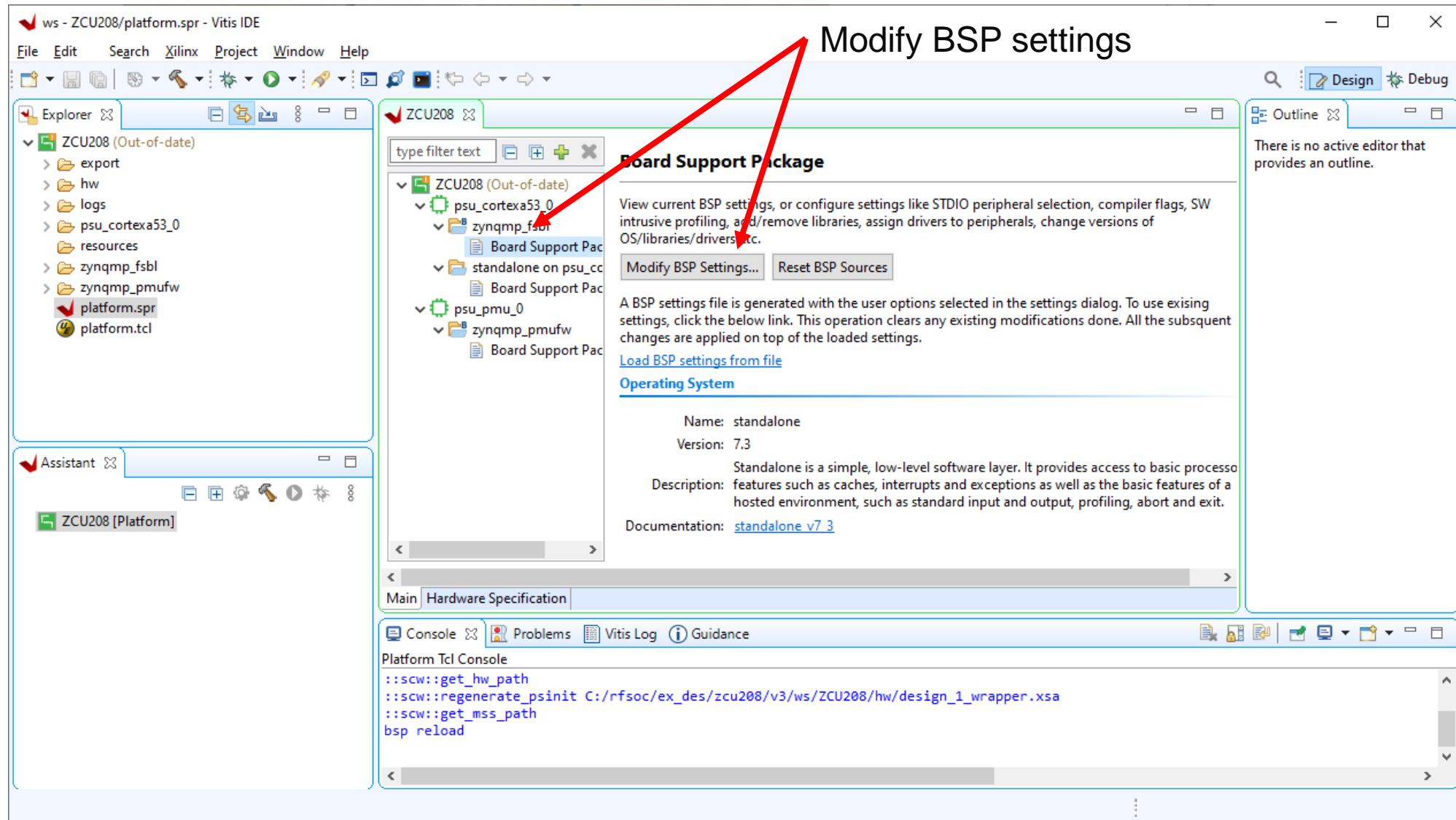


# Create Platform Project Cont'd

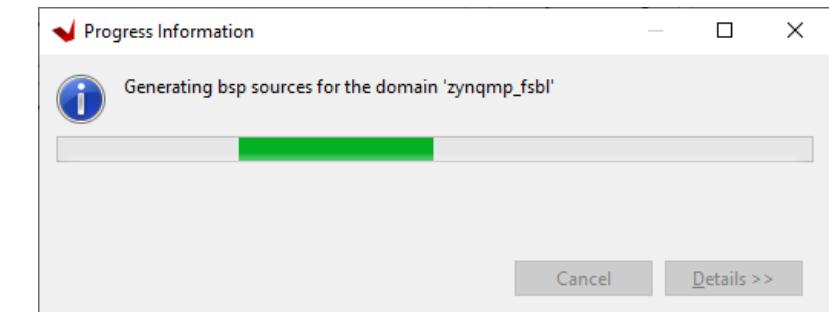
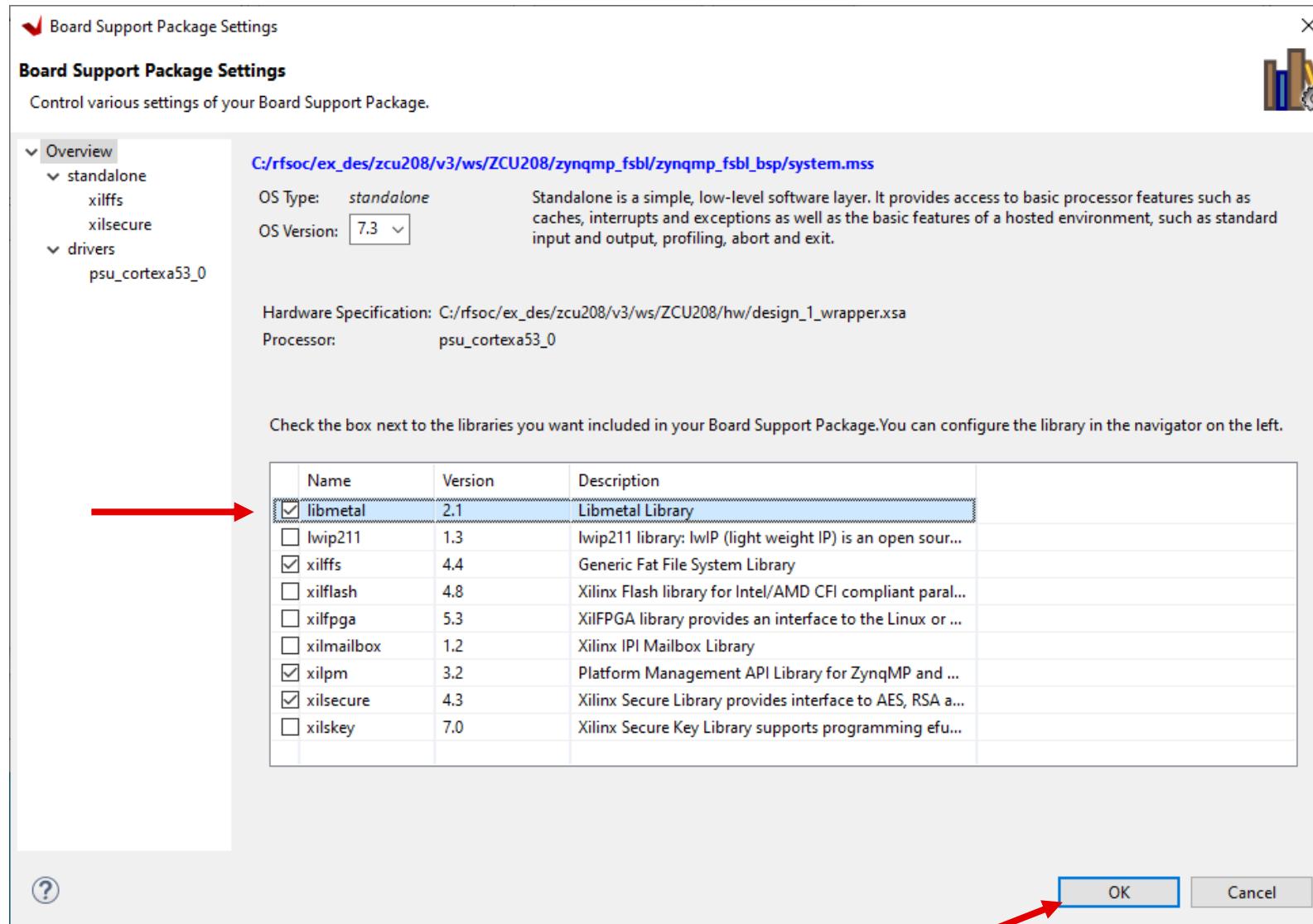


This may take  
a few minutes.

# Create Platform Project Cont'd

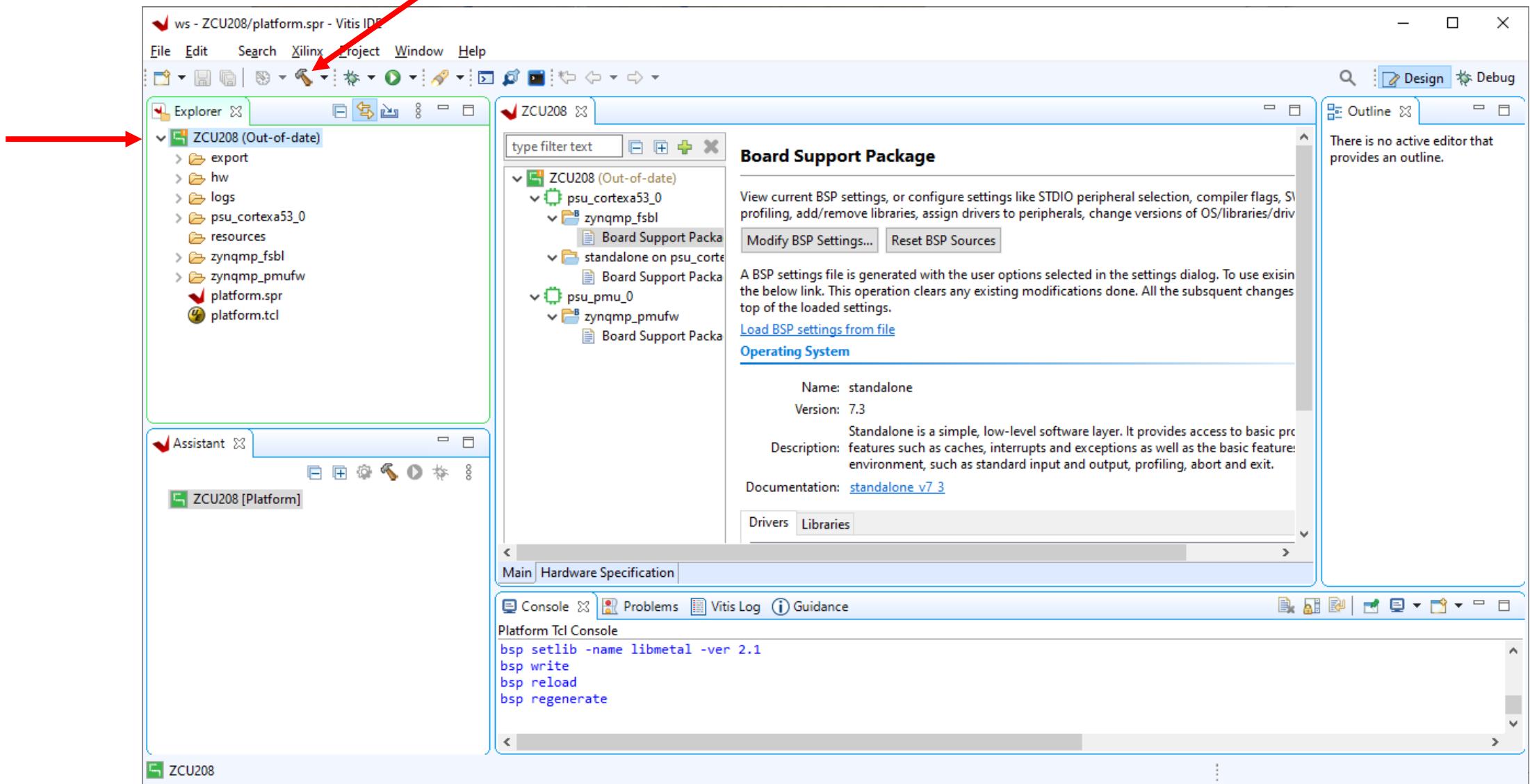


# Enable libmetal

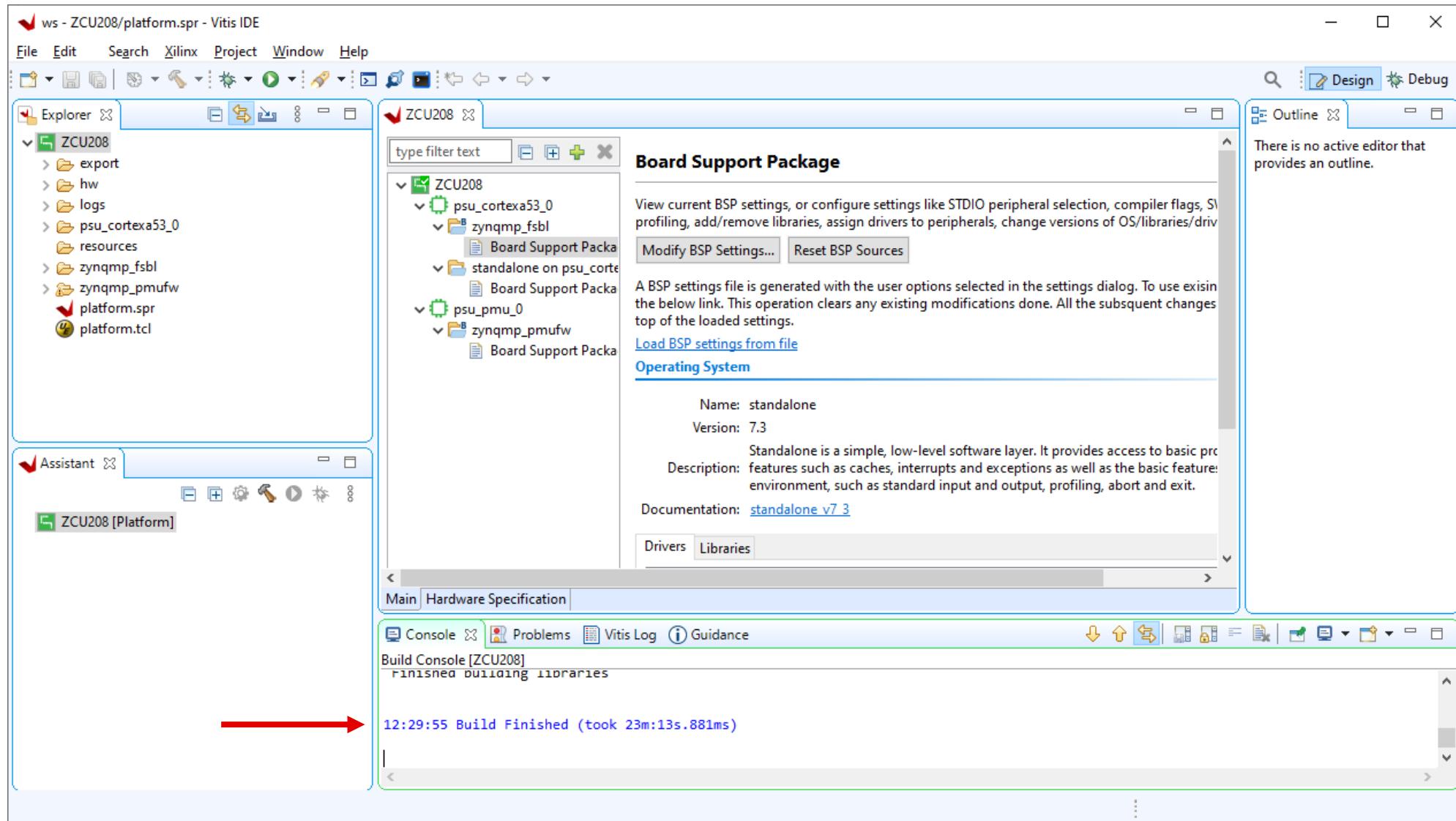


# Build Project

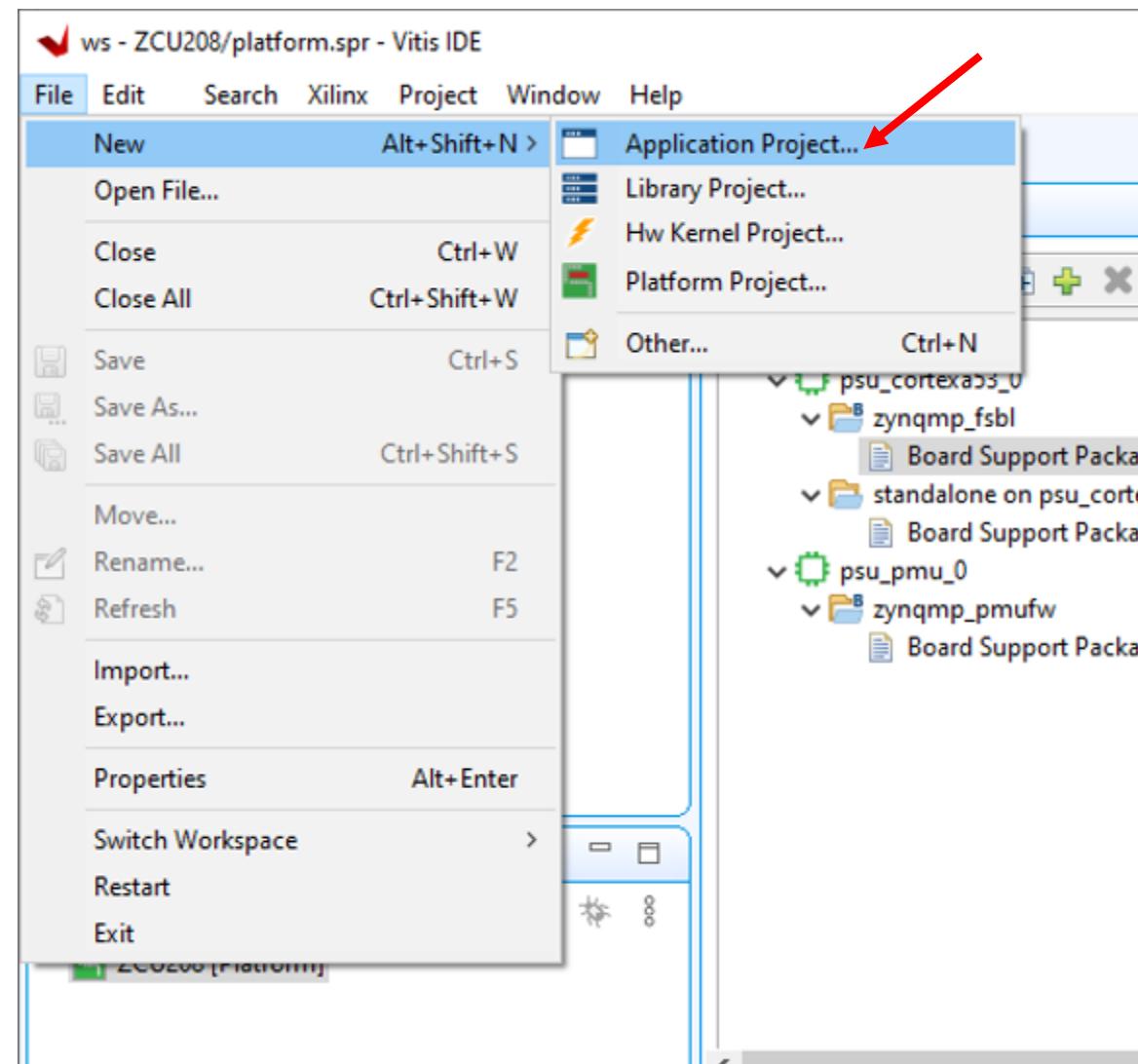
This may take  
a few minutes.



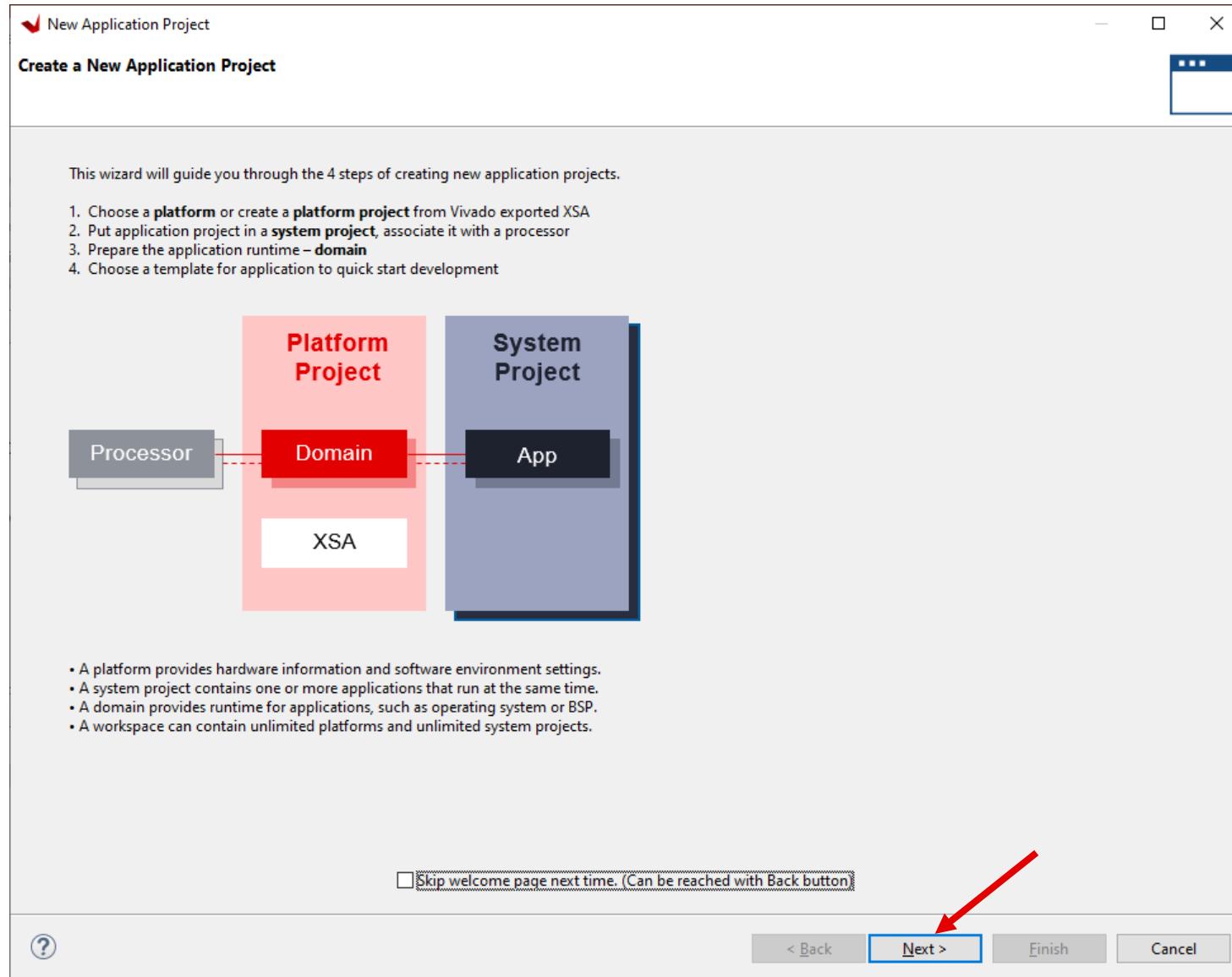
# Build Complete



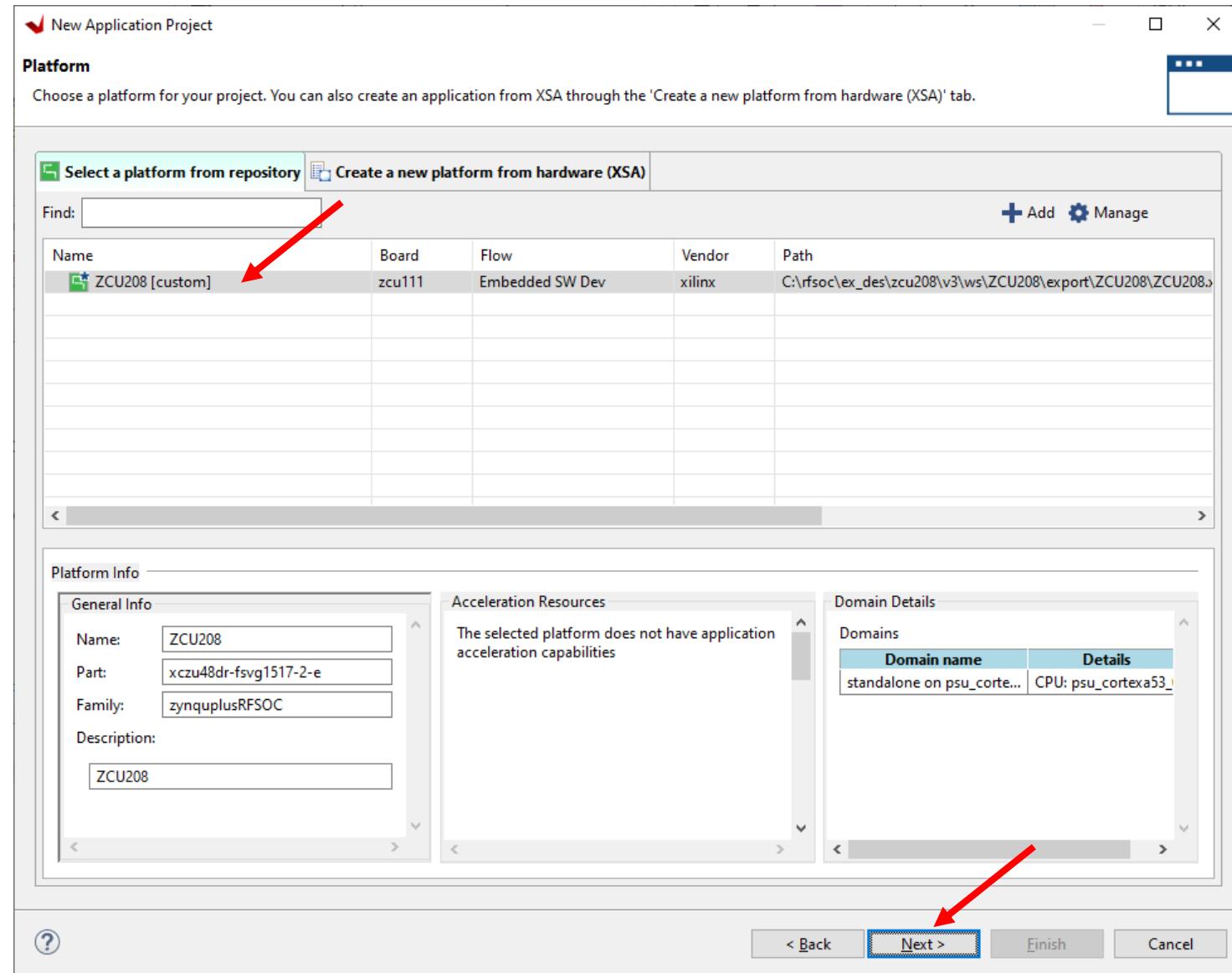
# Create Application



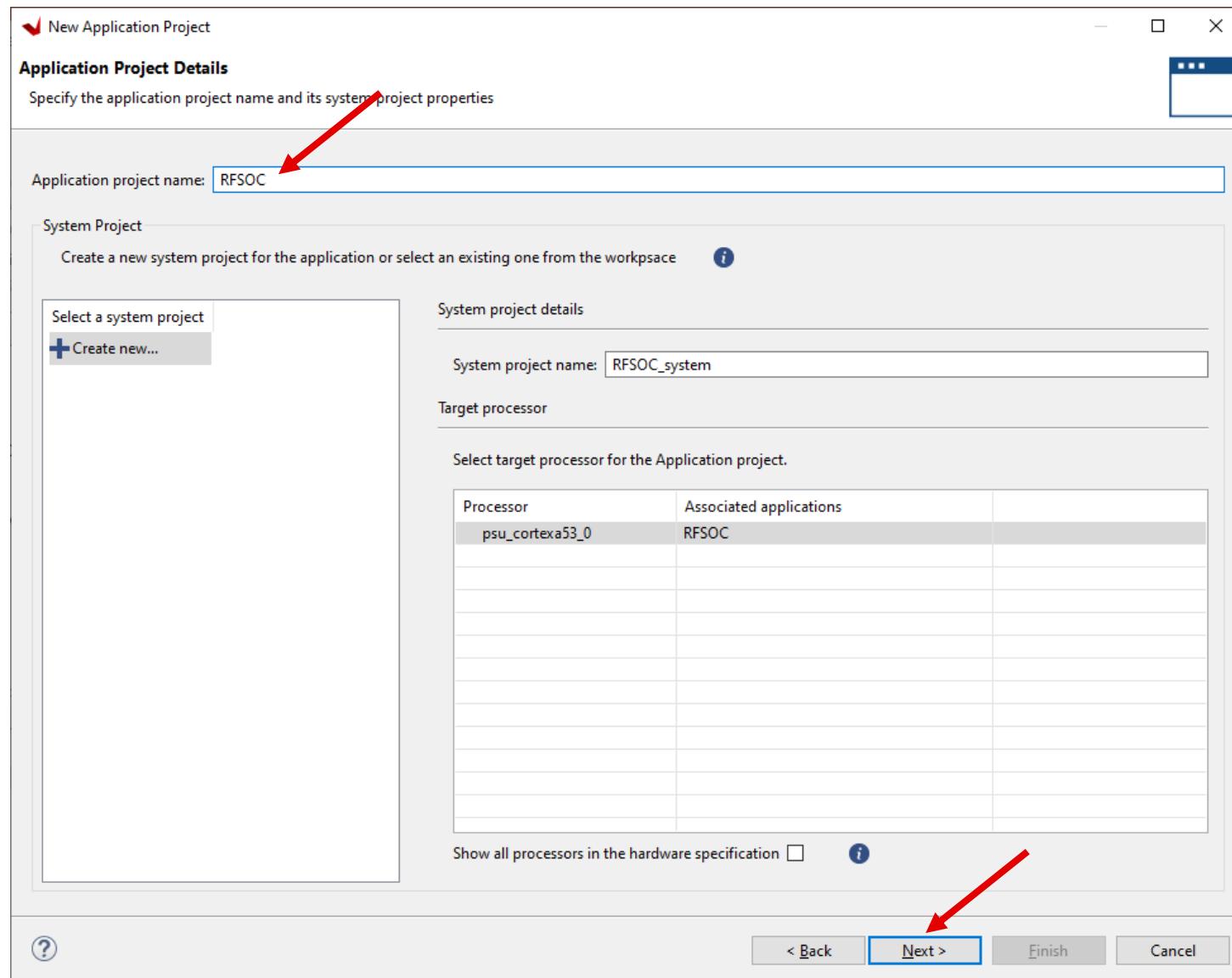
# Create Application Cont'd



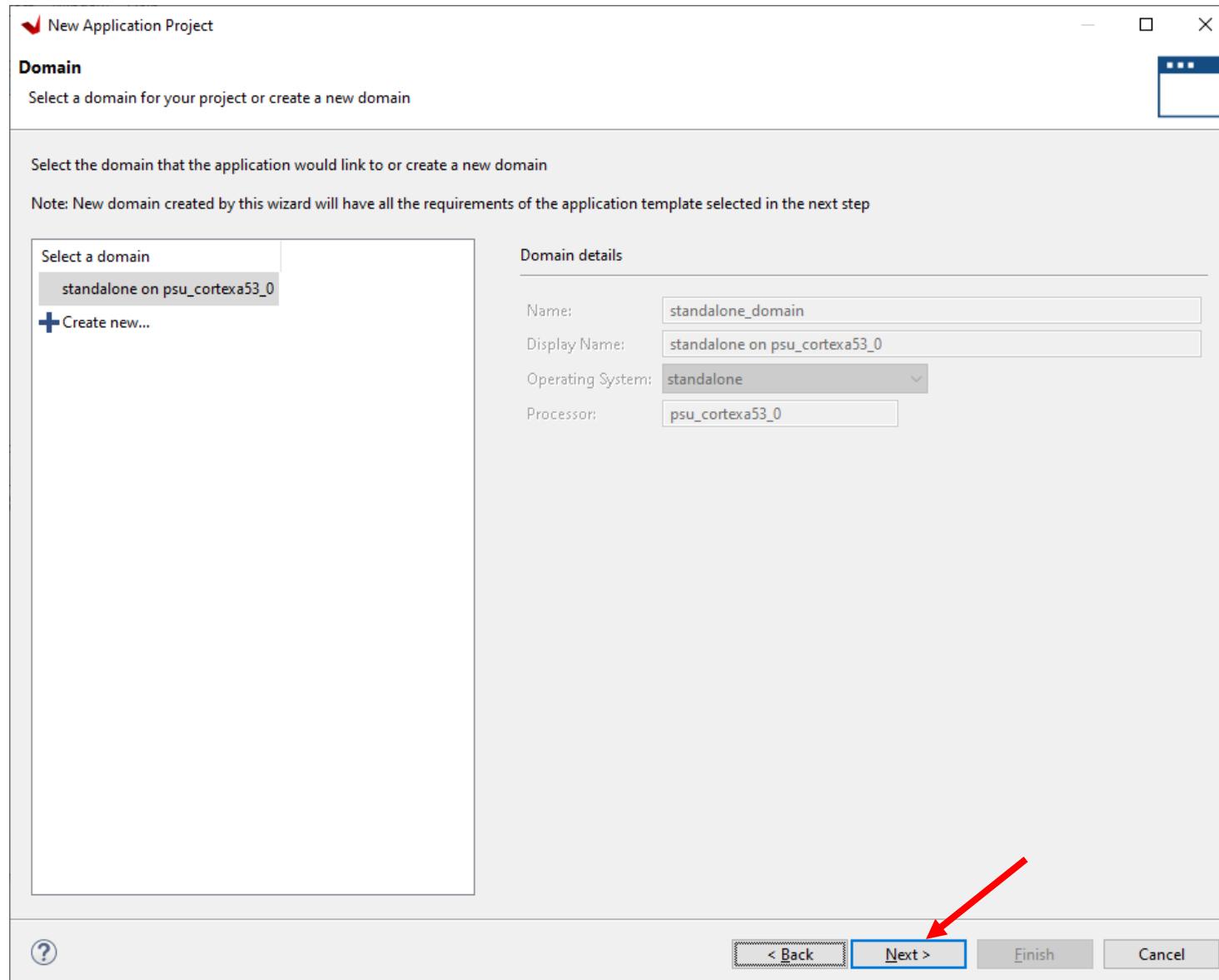
# Create Application Cont'd



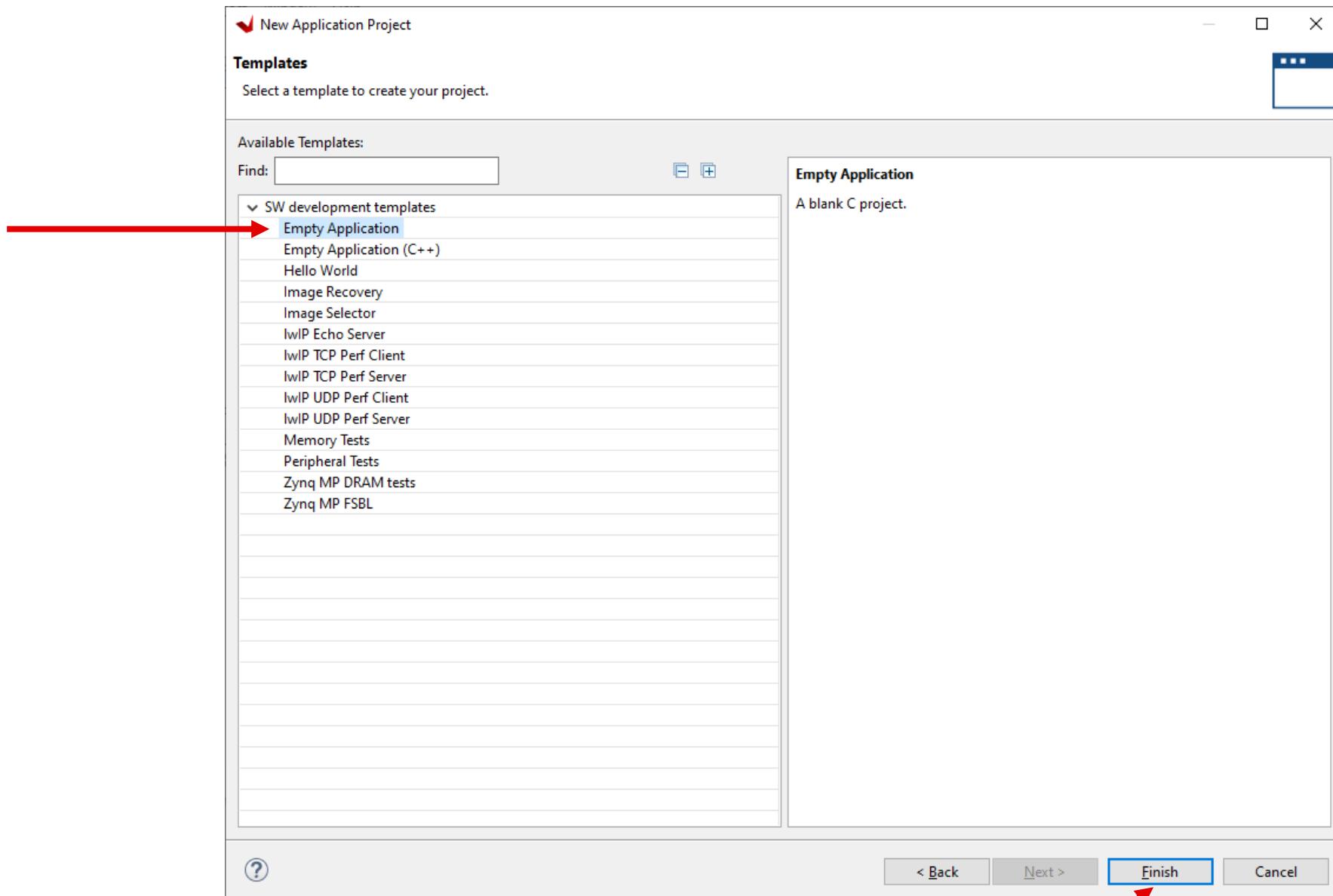
# Create Application Cont'd



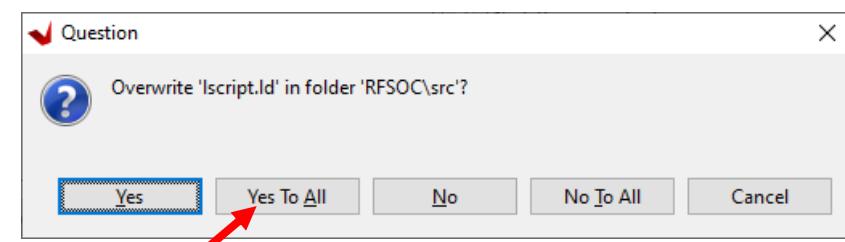
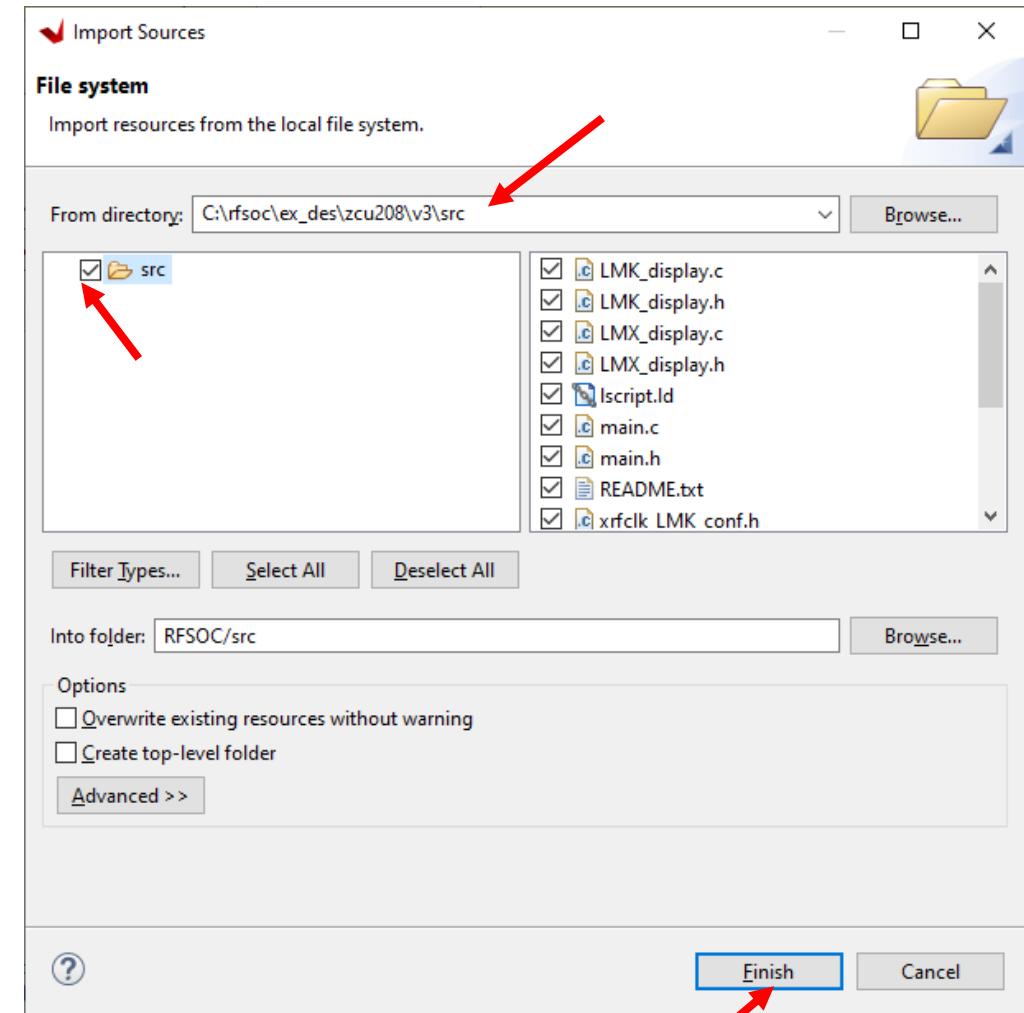
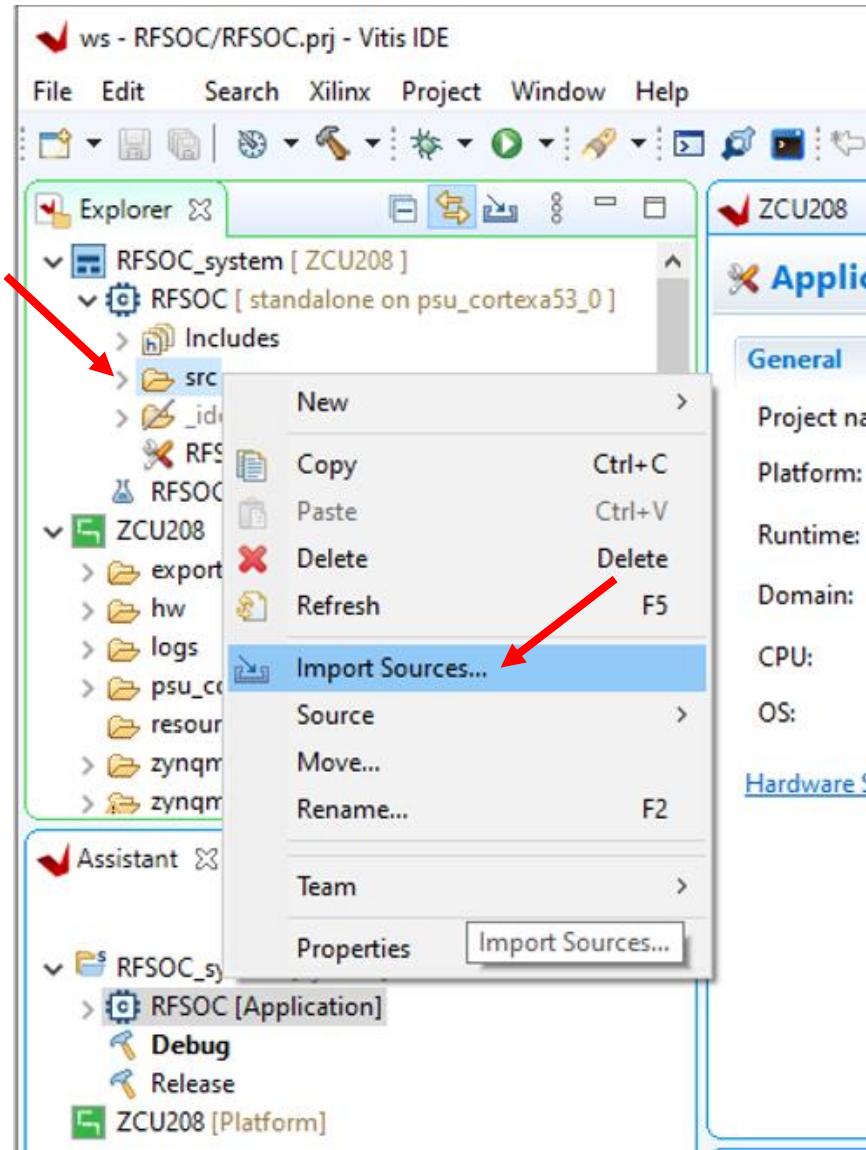
# Create Application Cont'd



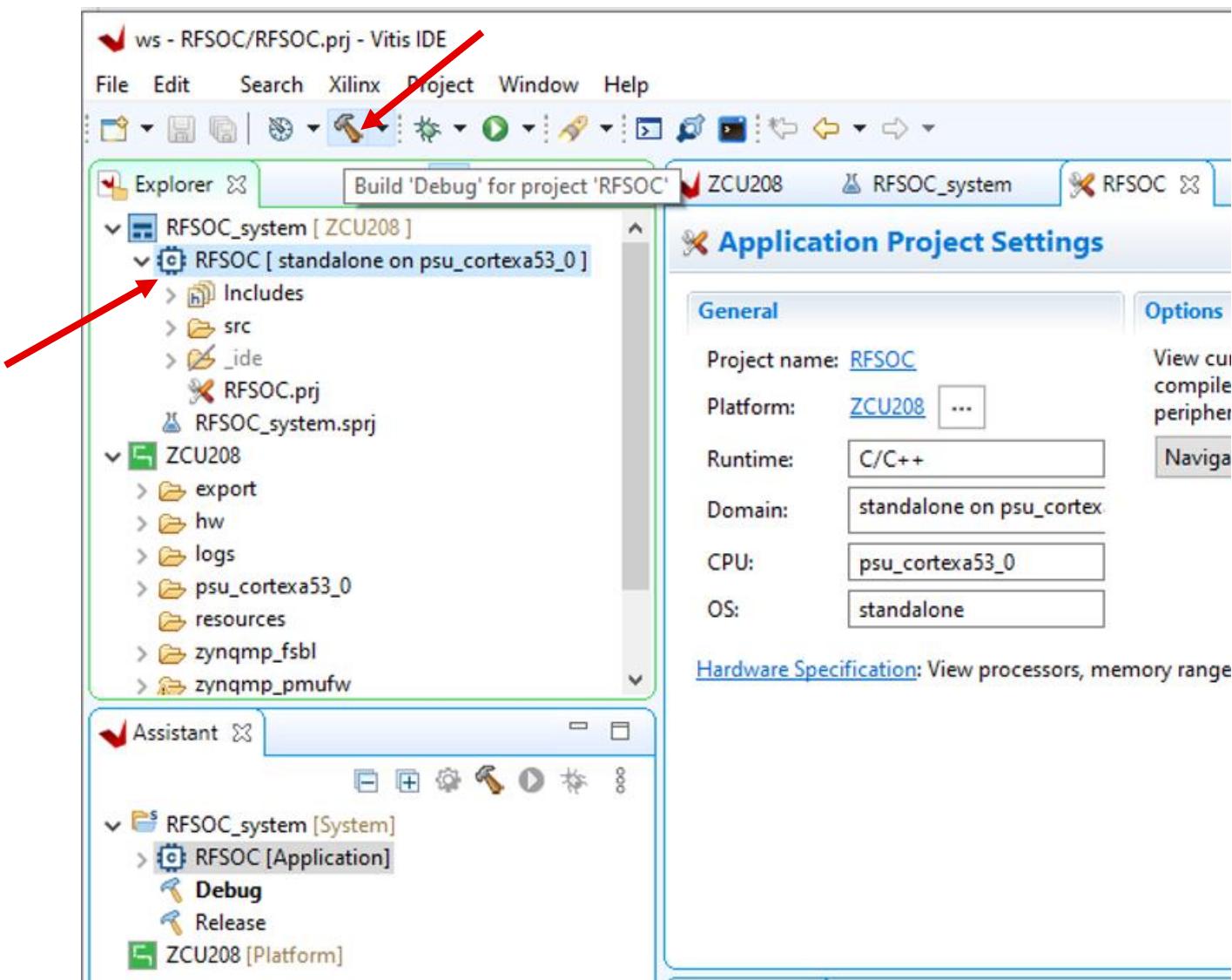
# Create Application Cont'd



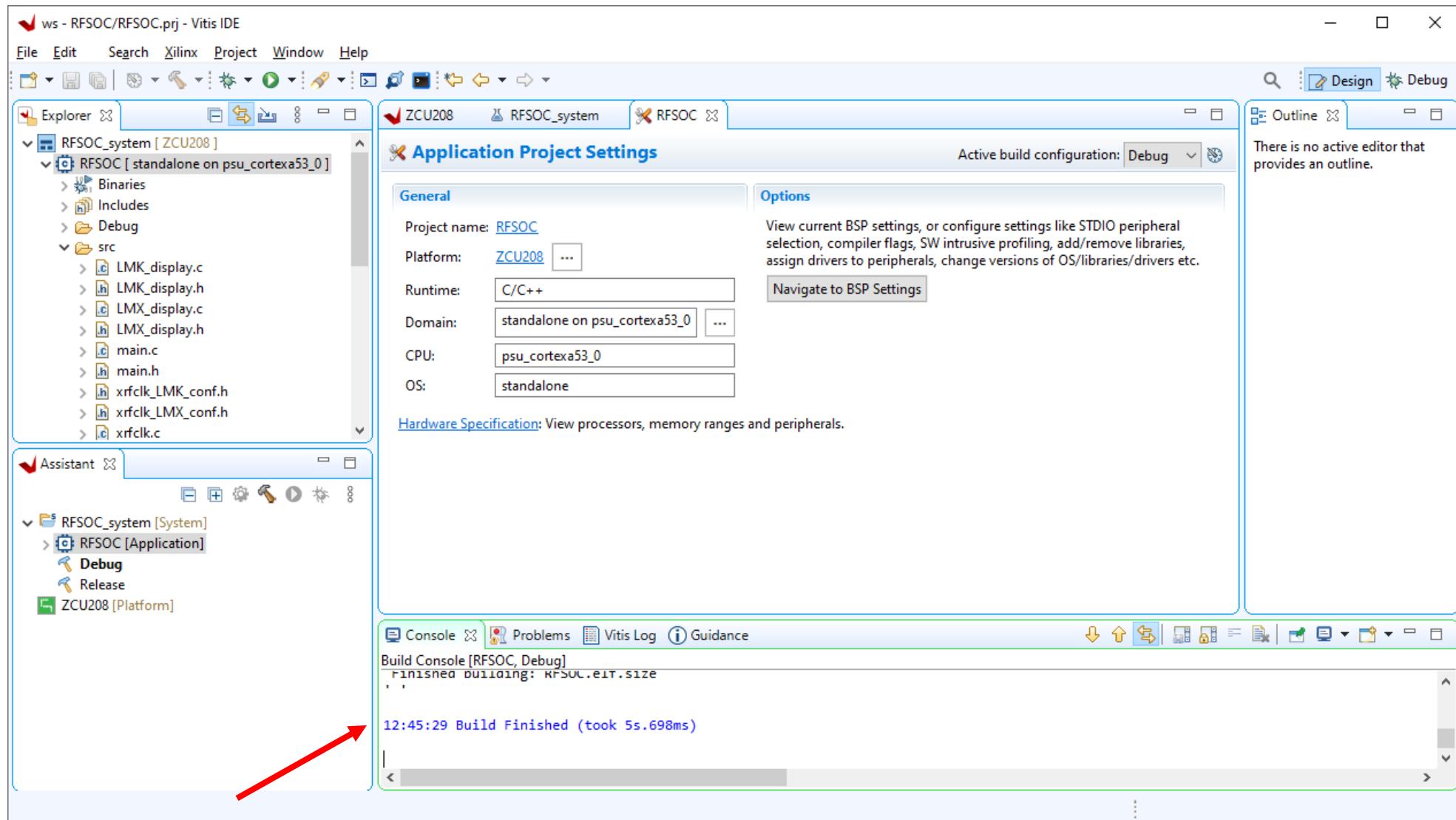
# Import Sources



# Build Application



# Build Complete



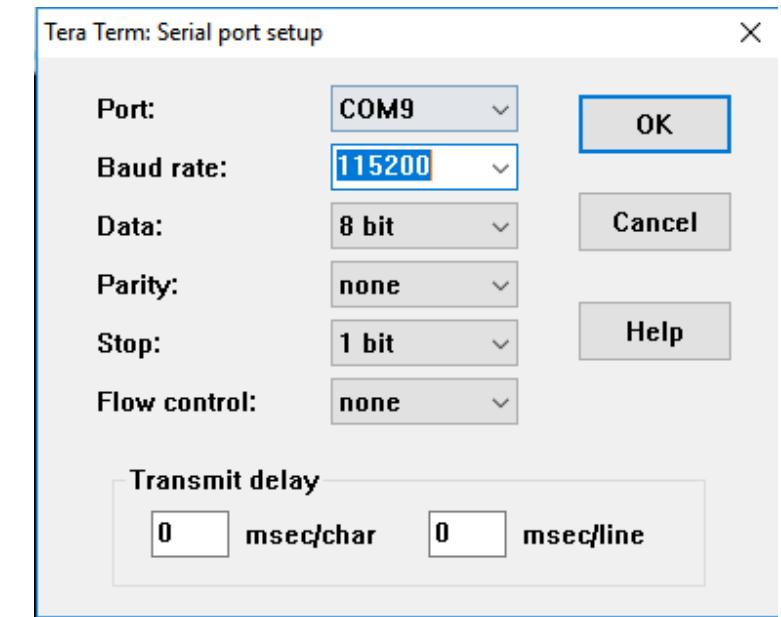
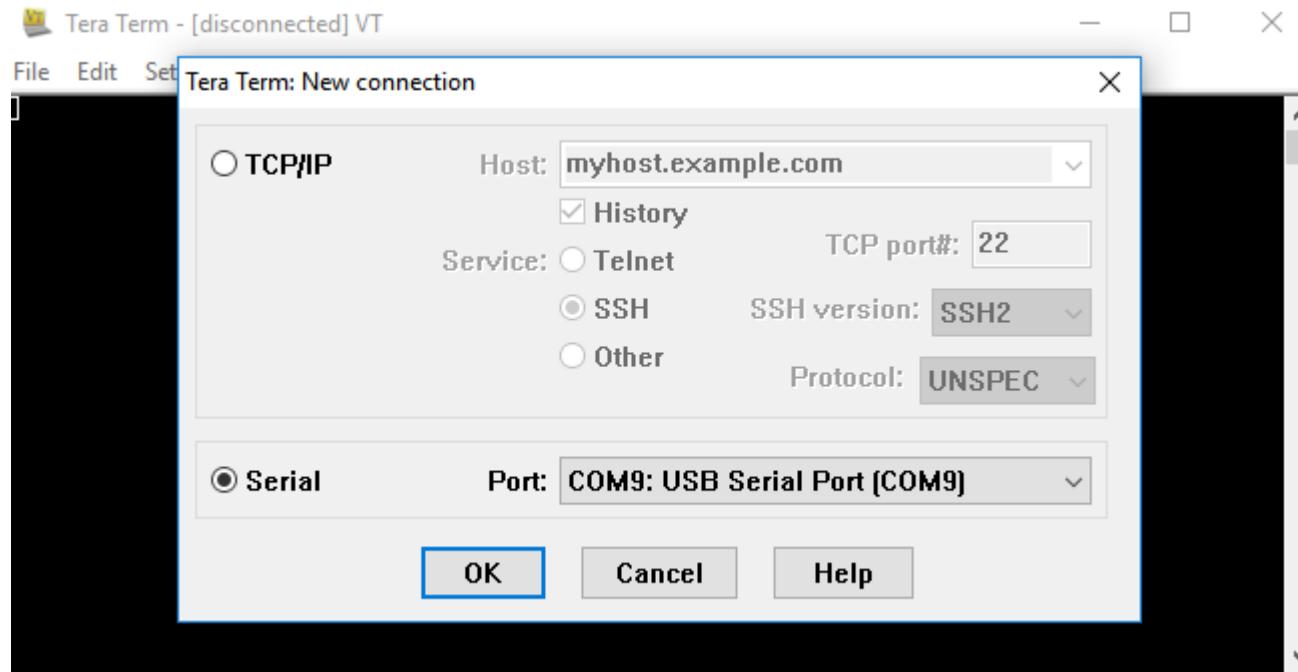


# Run Design

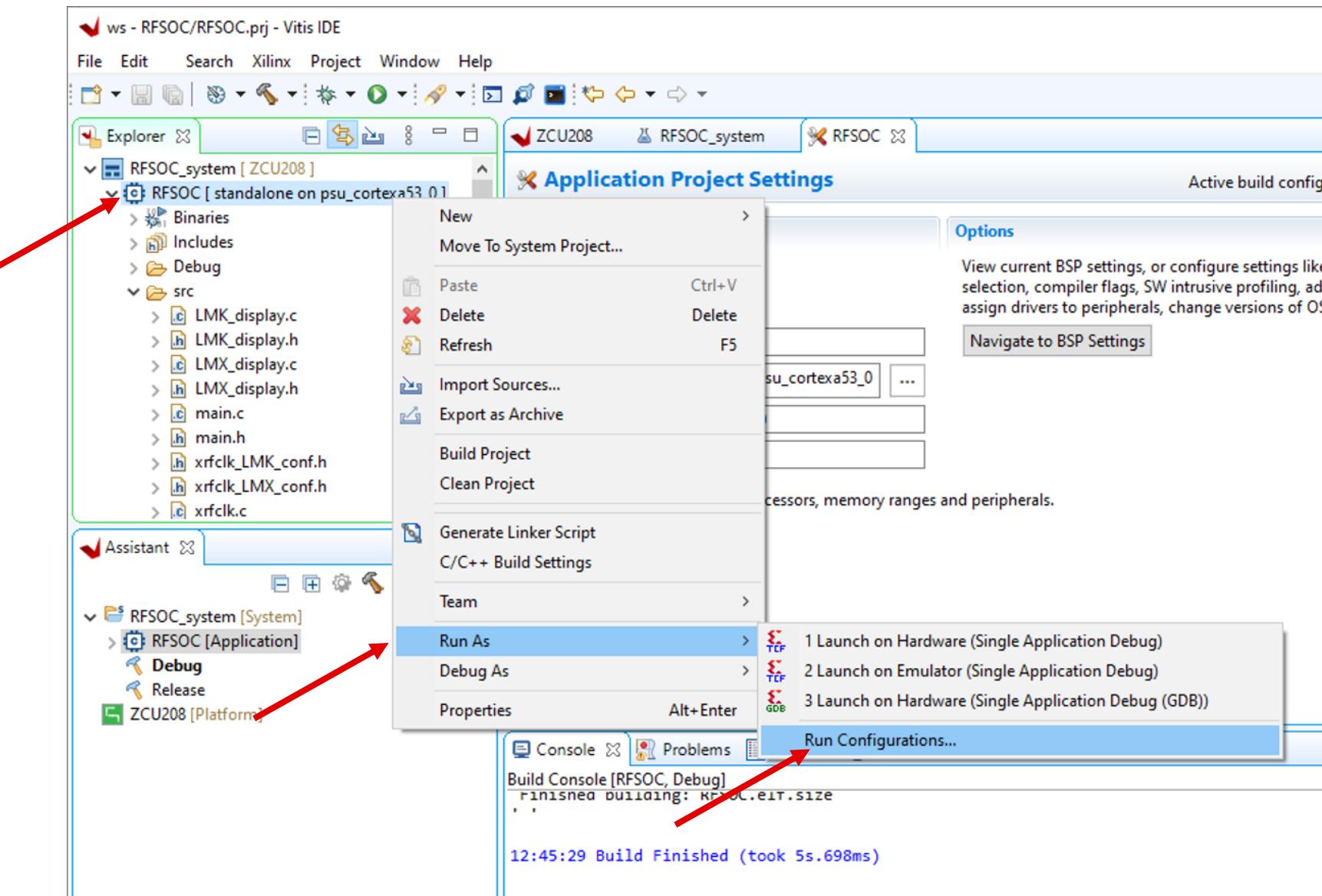
# Open a Terminal Window

Open the COM port on the compute and set the rate to 115200.

TeraTerm can be used. See [UG1036](#).

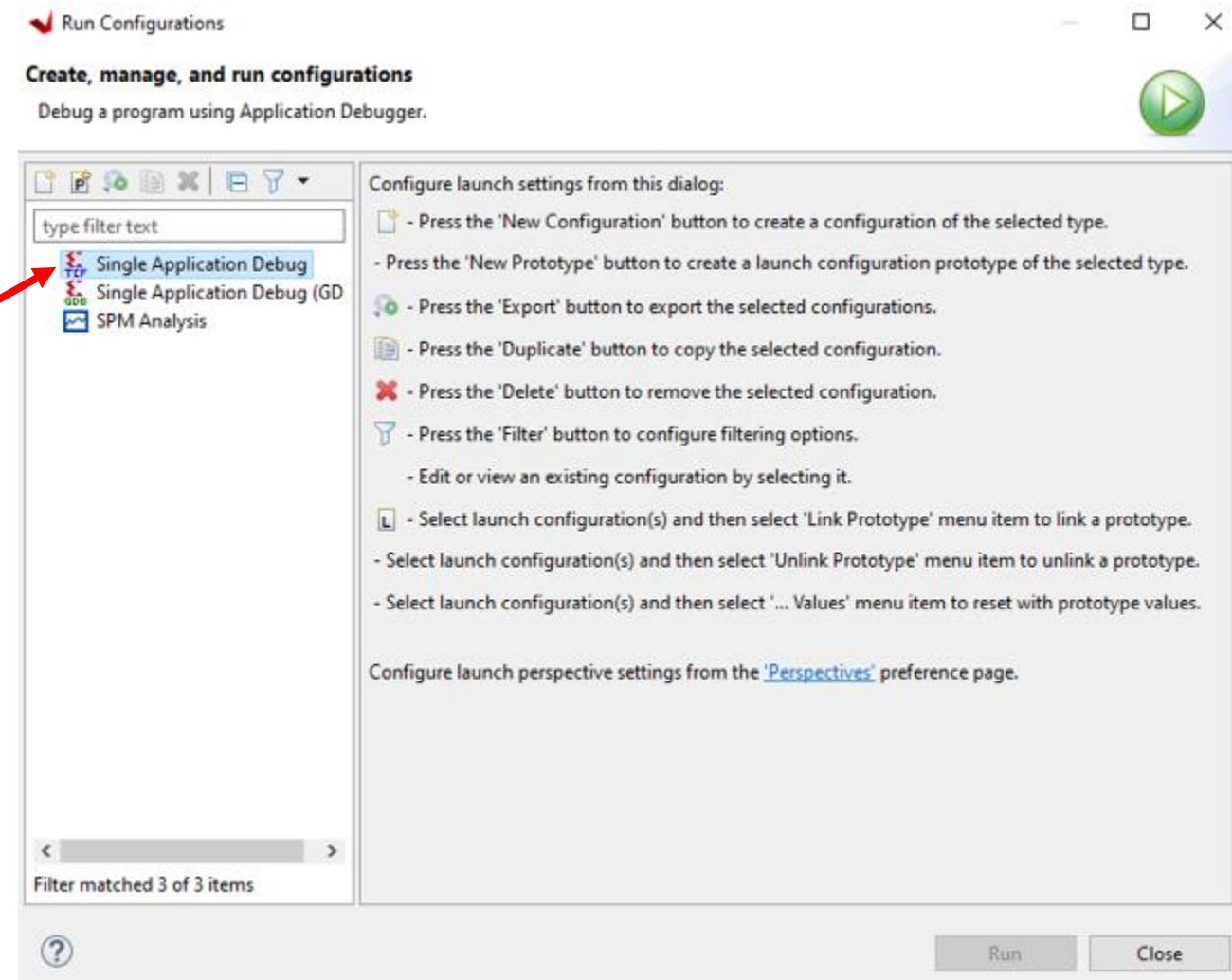


# Setup Run Configuration

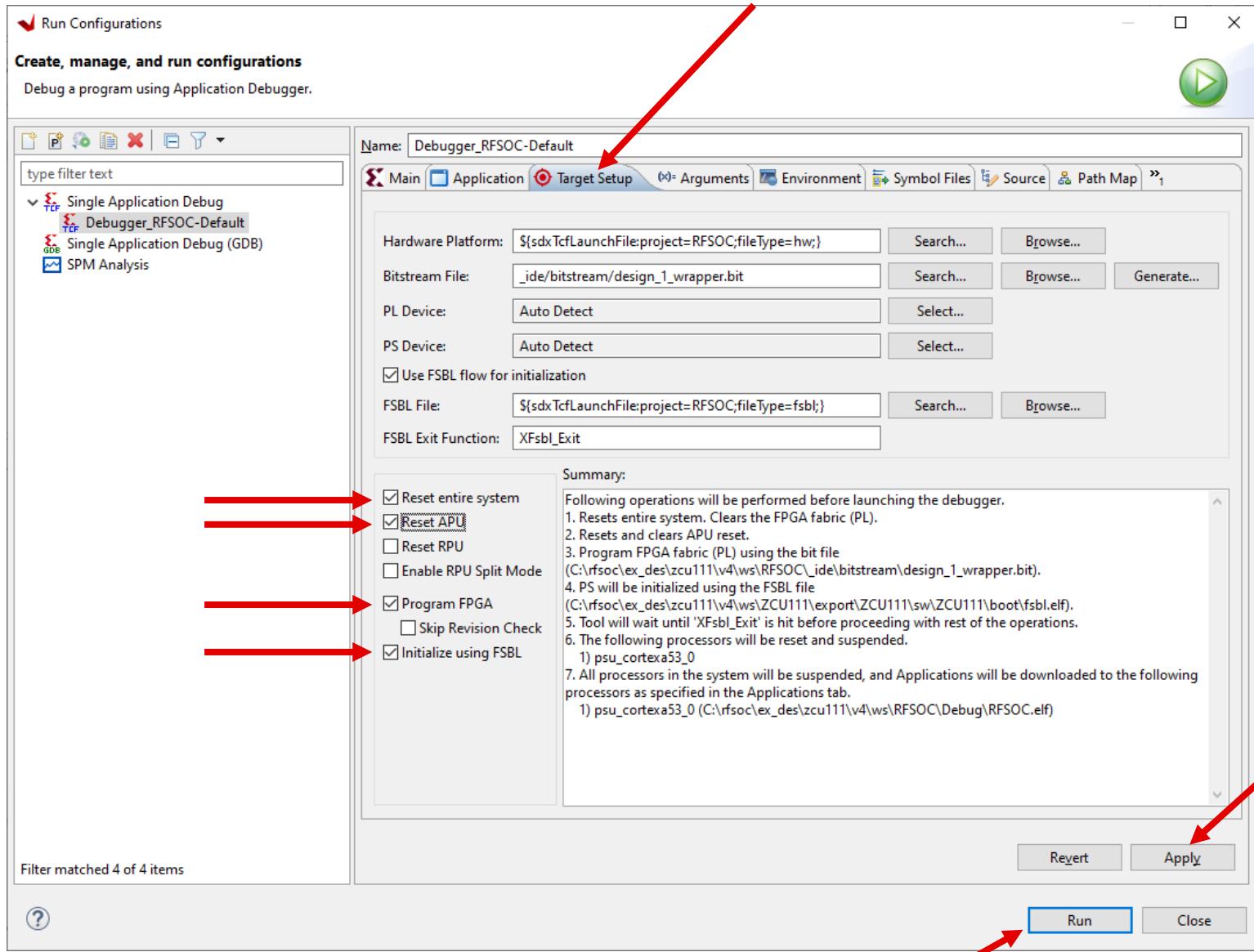


# Run Configuration Cont'd

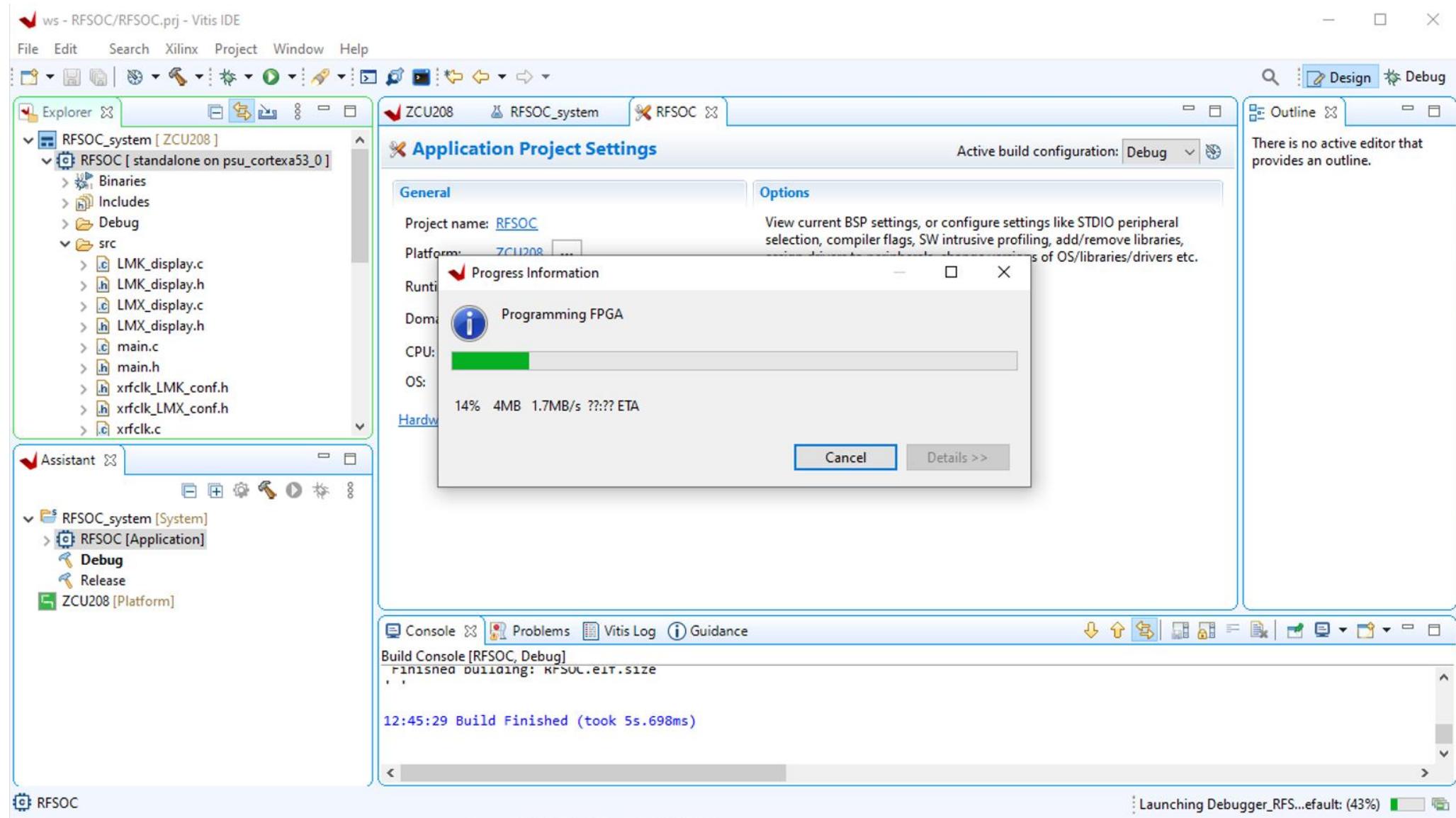
Double Click



# Run Configuration Cont'd



# Run Design



# Application Startup

The application...

1. Programs the clocks.
2. Issues the data converters master reset.
3. Displays the Power-on Sequence Step of the data converters.

```
COM41:115200baud - Tera Term VT
File Edit Setup Control Window Help

Xilinx Zynq MP First Stage Boot Loader
Release 2020.2 Jun 24 2021 - 12:14:38
PMU-FW is not running, certain applications may not be supported.

#####
Hello RFSoC World!

RFDC IP Version: 2.4

Configuring the data converter clocks...
Configuring CLK104 LMK and LMX devices
Clk settings read from LMK -----
CLKin1_freq: 10000KHz
DCLKout00(RFIN_RF1) : 184320KHz SDCLKout01(RF1_ADC_SYNC) : -----
DCLKout02(NC) : ----- SDCLKout03(AMS_SYSREF) : -----
DCLKout04(RFIN_RF2) : 184320KHz SDCLKout05(RF2_DAC_SYNC) : -----
DCLKout06(DAC_REFCLK) : 184320KHz SDCLKout07(DDR_PL_CAP_SYNC) : -----
DCLKout08(PL_CLK) : ----- SDCLKout09(PL_SYSREF) : -----
DCLKout10(NC) : ----- SDCLKout11(J10_SINGLE_END) : -----
DCLKout12(ADC_REFCLK) : 184320KHz SDCLKout13(NC) : -----


Clk settings read from LMX_RF1 -----
CLKin_freq: 184320KHz
RFoutA Freq: -----
RFoutB Freq: -----


Clk settings read from LMX_RF2 -----
CLKin_freq: 184320KHz
RFoutA Freq: -----
RFoutB Freq: -----

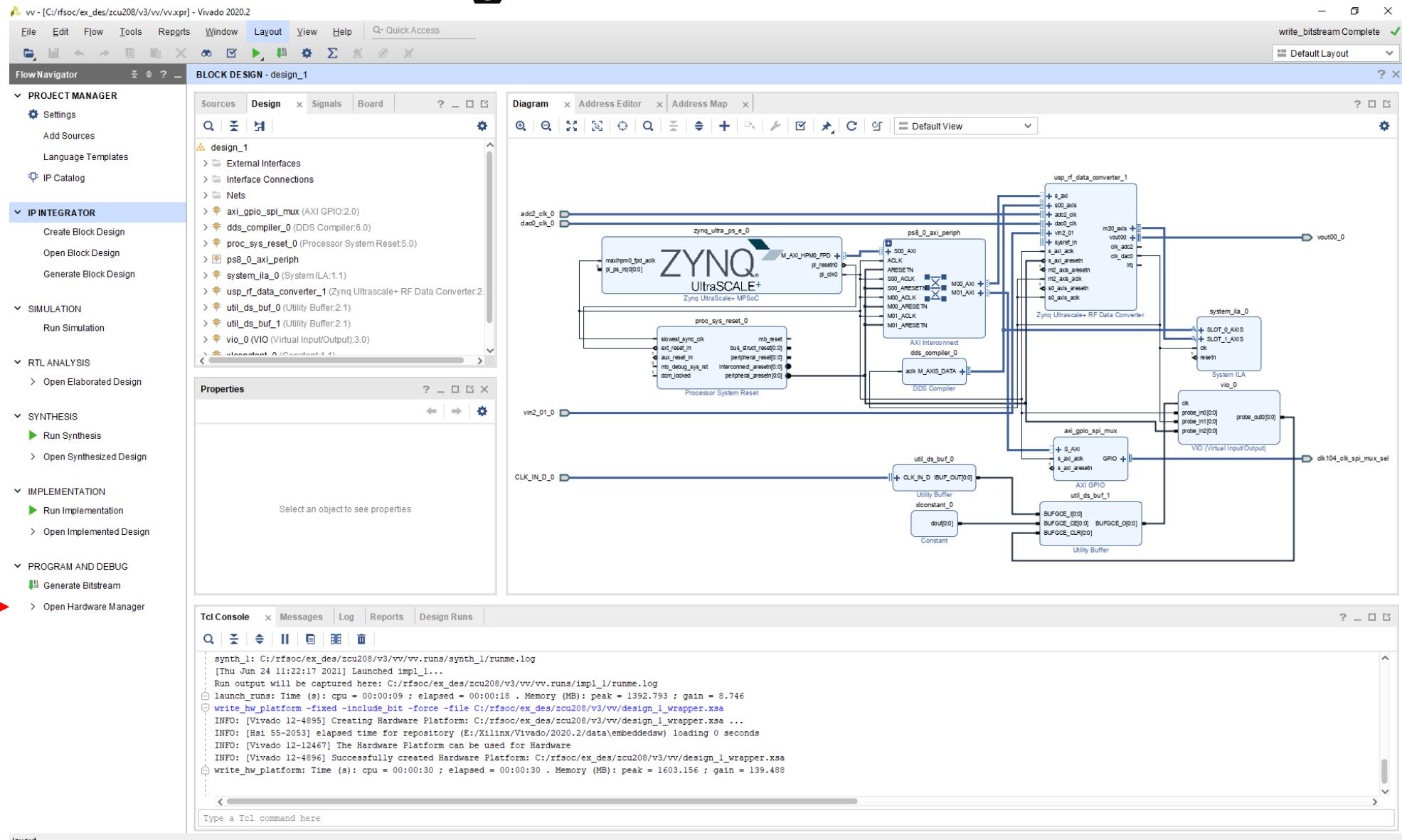

==== Metal log enabled ====
metal: debug: registered generic bus

DeviceID: 0
Silicon Revision: 1
The RFDC controller is initialized.
Data Converter startup up is in progress...

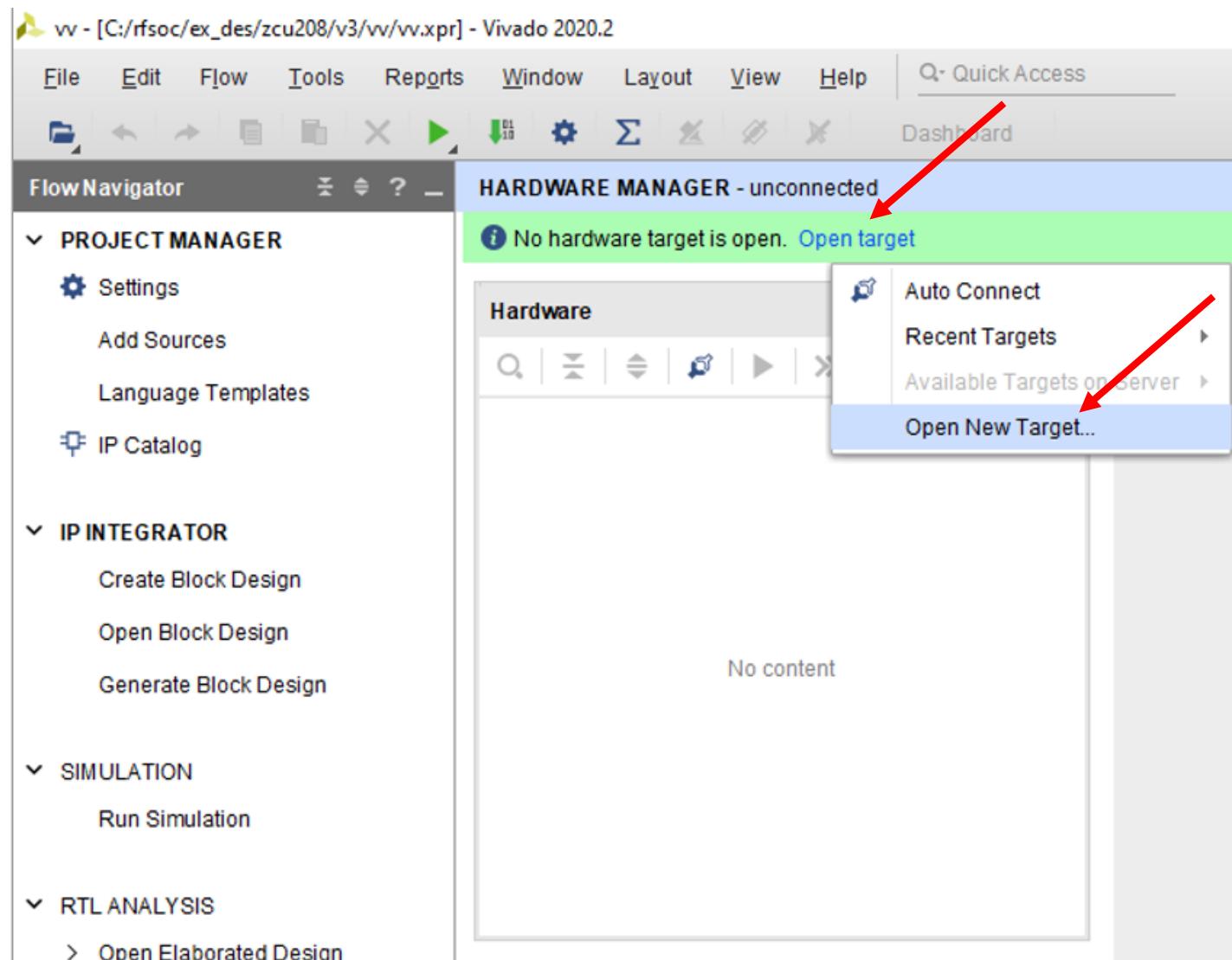
The Power-on sequence step. 0xF is complete.
  DAC Tile0 Power-on Sequence Step: 0x0000000F
  ADC Tile2 Power-on Sequence Step: 0x0000000F

Data Converter start up is complete!
----- Startup Complete -----
```

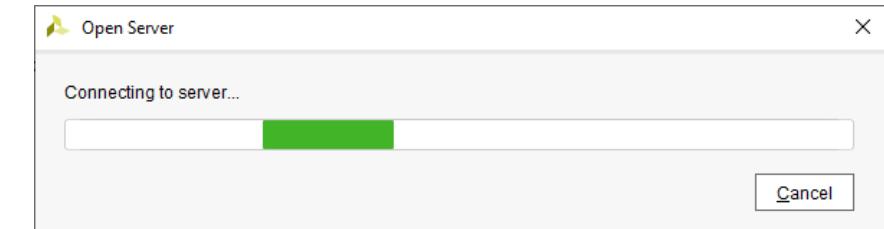
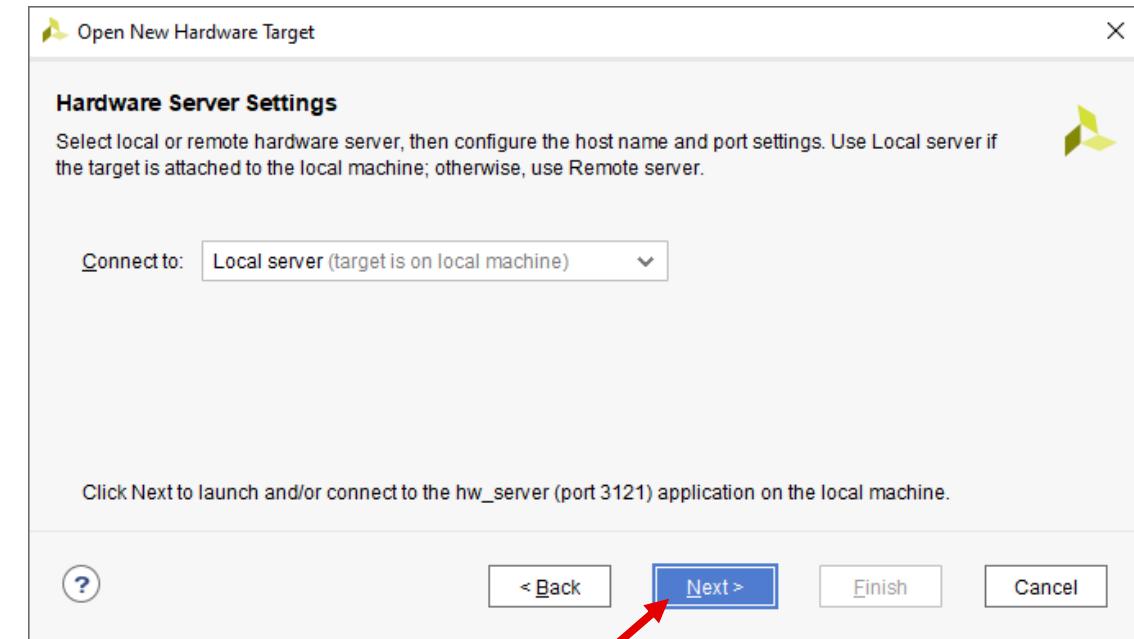
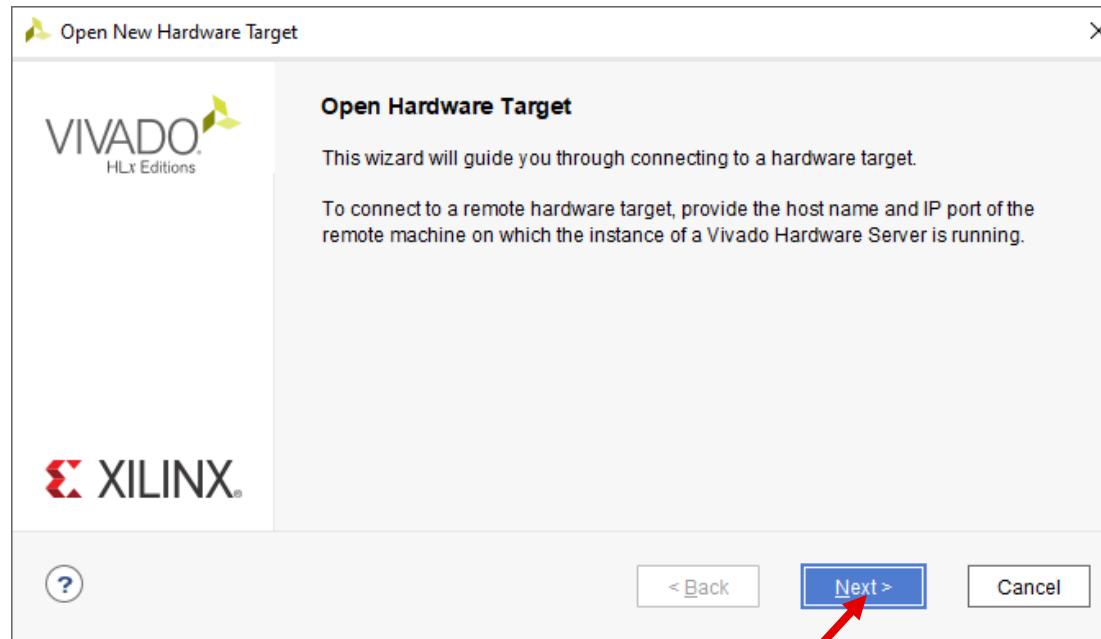
# Open Hardware Manager



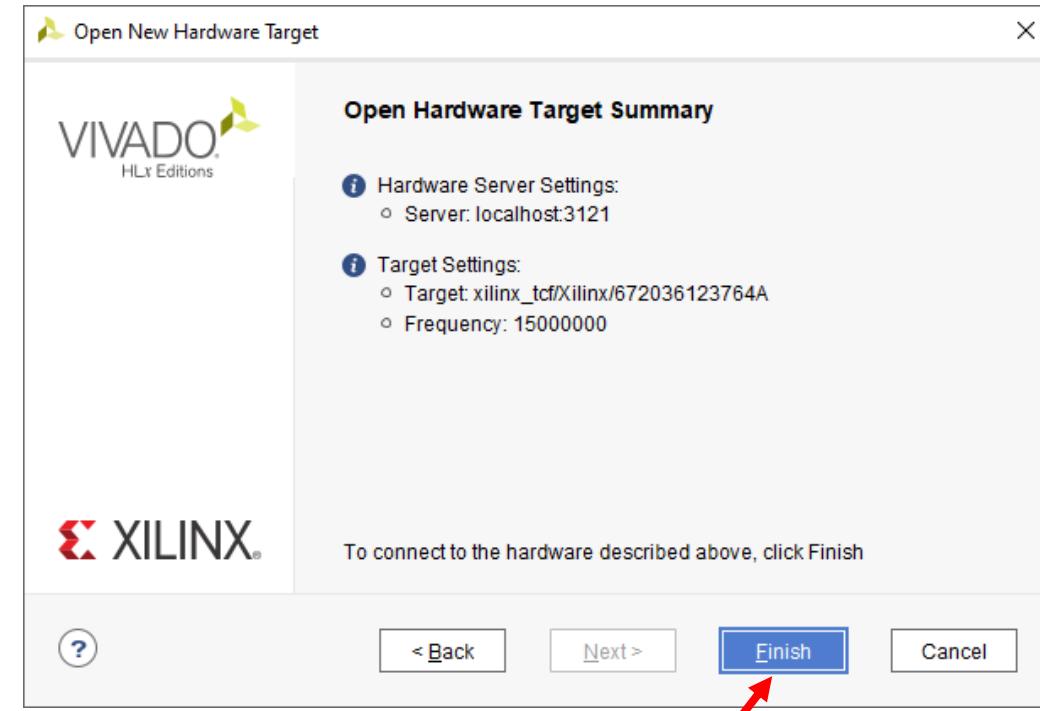
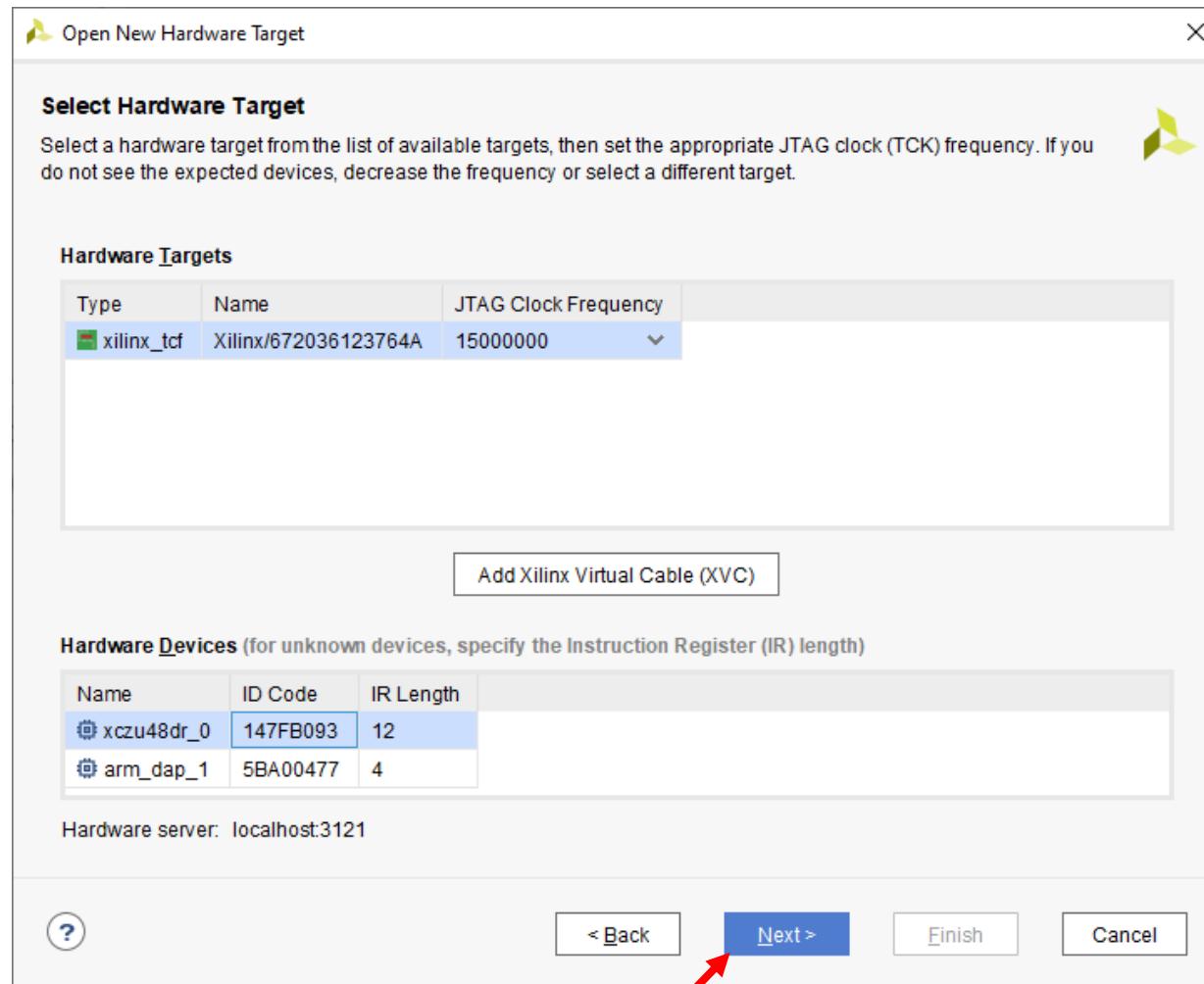
# Open New Target



# Open Hardware Target



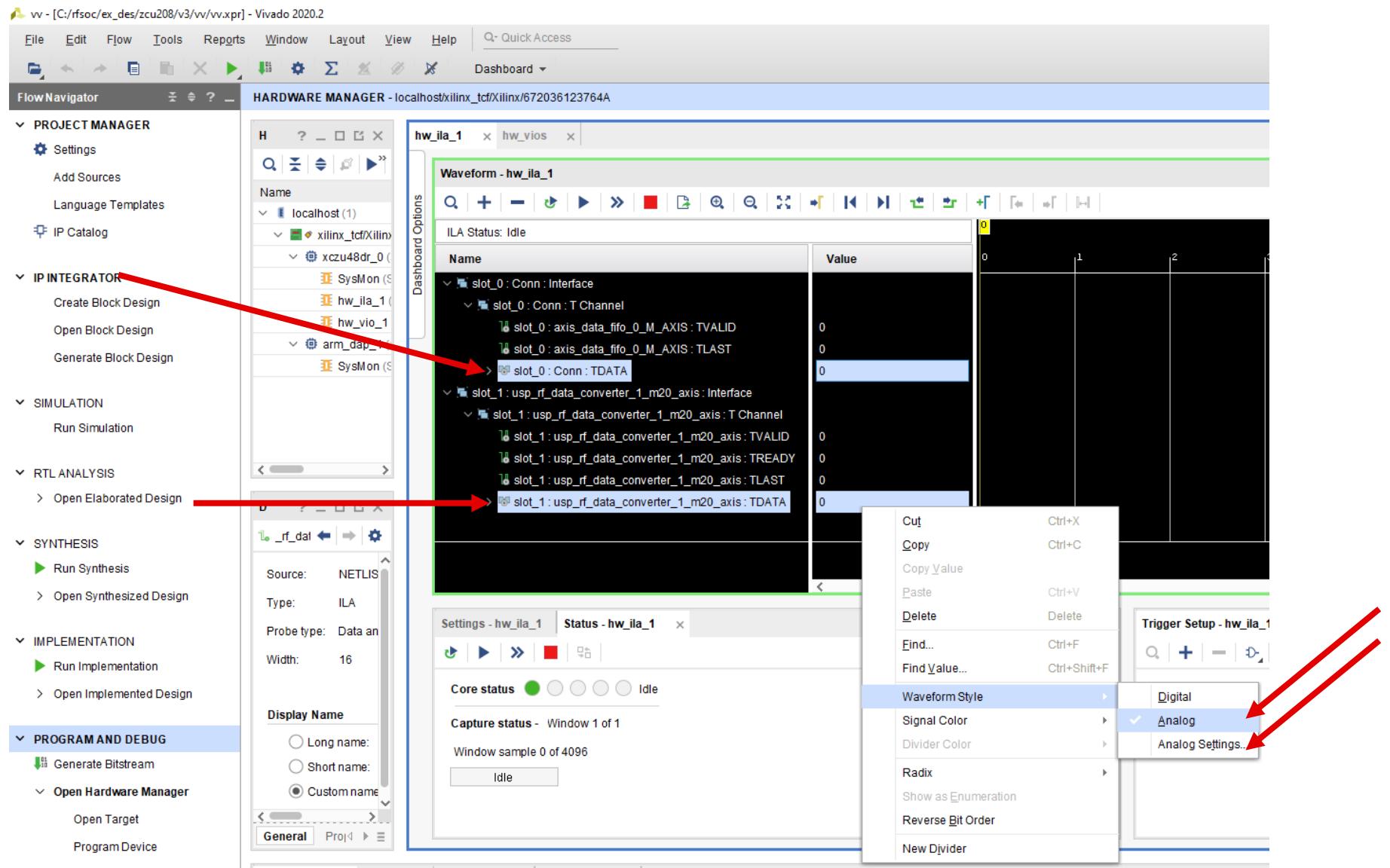
# Open Hardware Target Cont'd



# Convert Data to the Analog Waveform Style

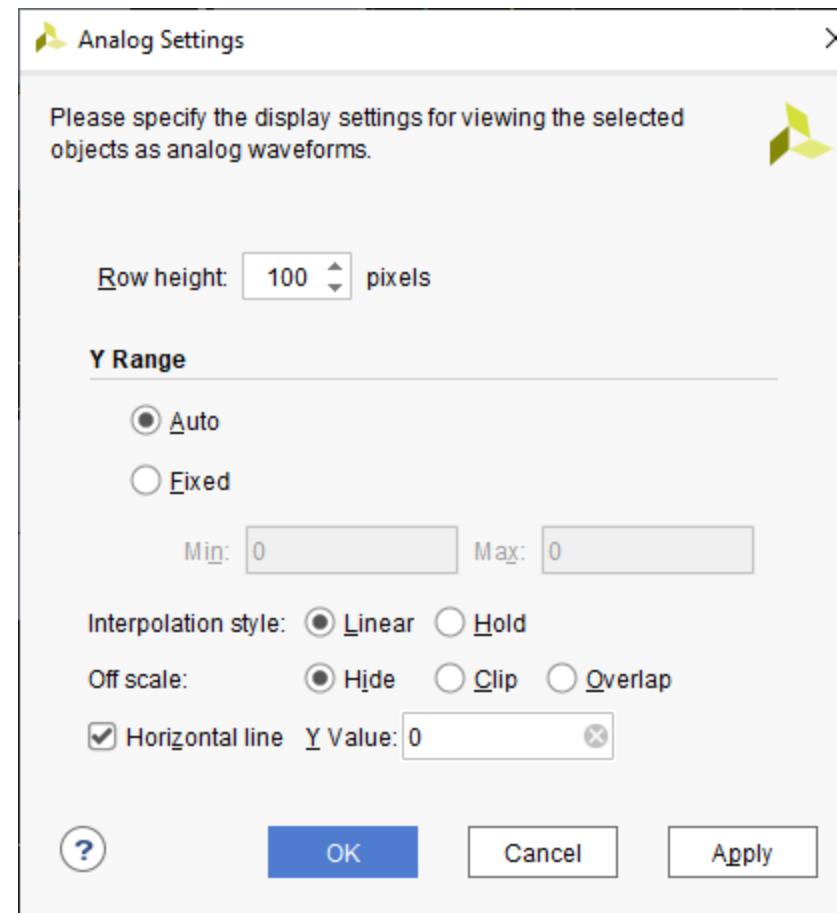
10MHz sine wave  
going from the DDS  
compiler to the DAC.

ADC capture to the  
System ILA.

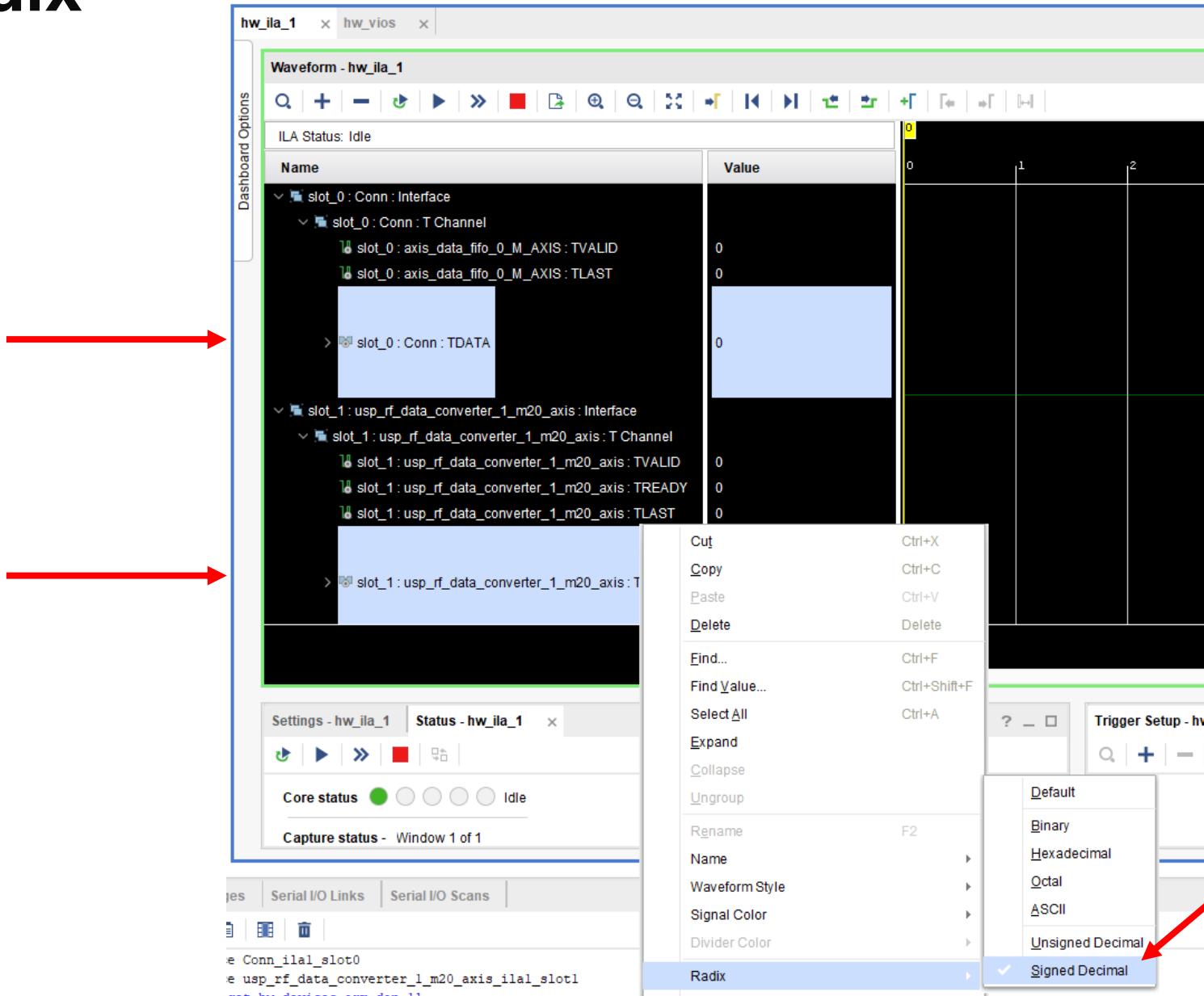


# Analog Settings

Set Row height to 100.



# Radix

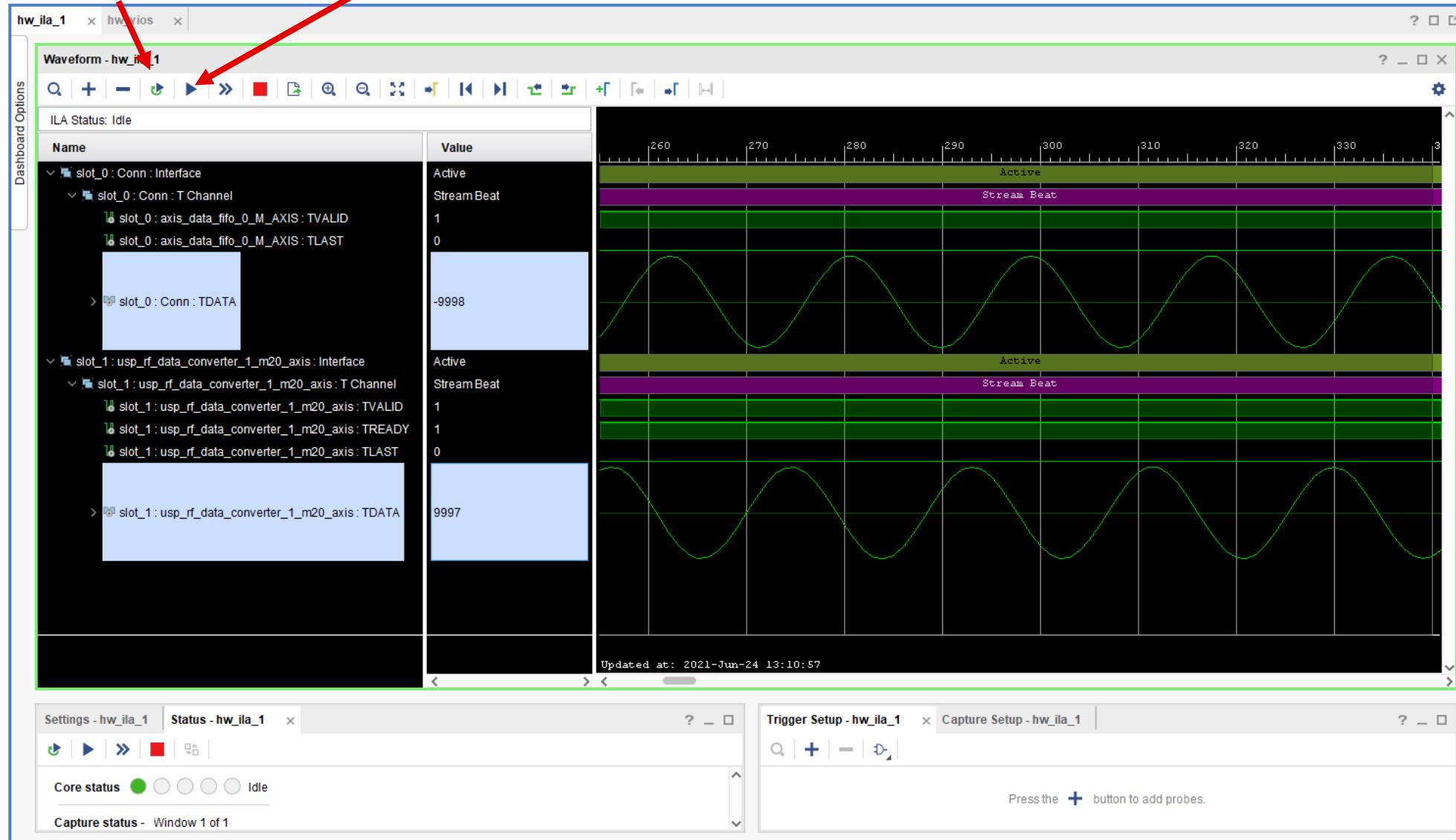


Use Radix of Signed Decimal.

# System ILA Capture

Automatically retrigger

Trigger ILA capture

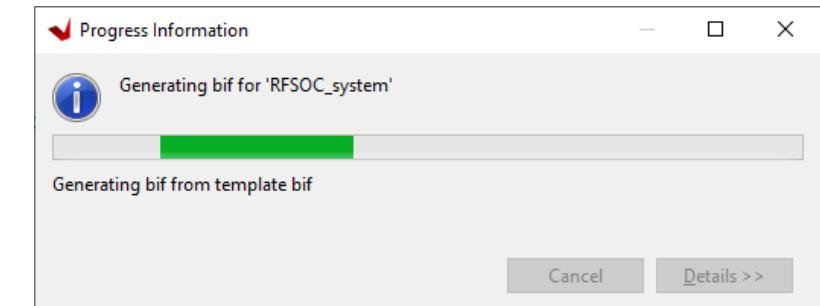
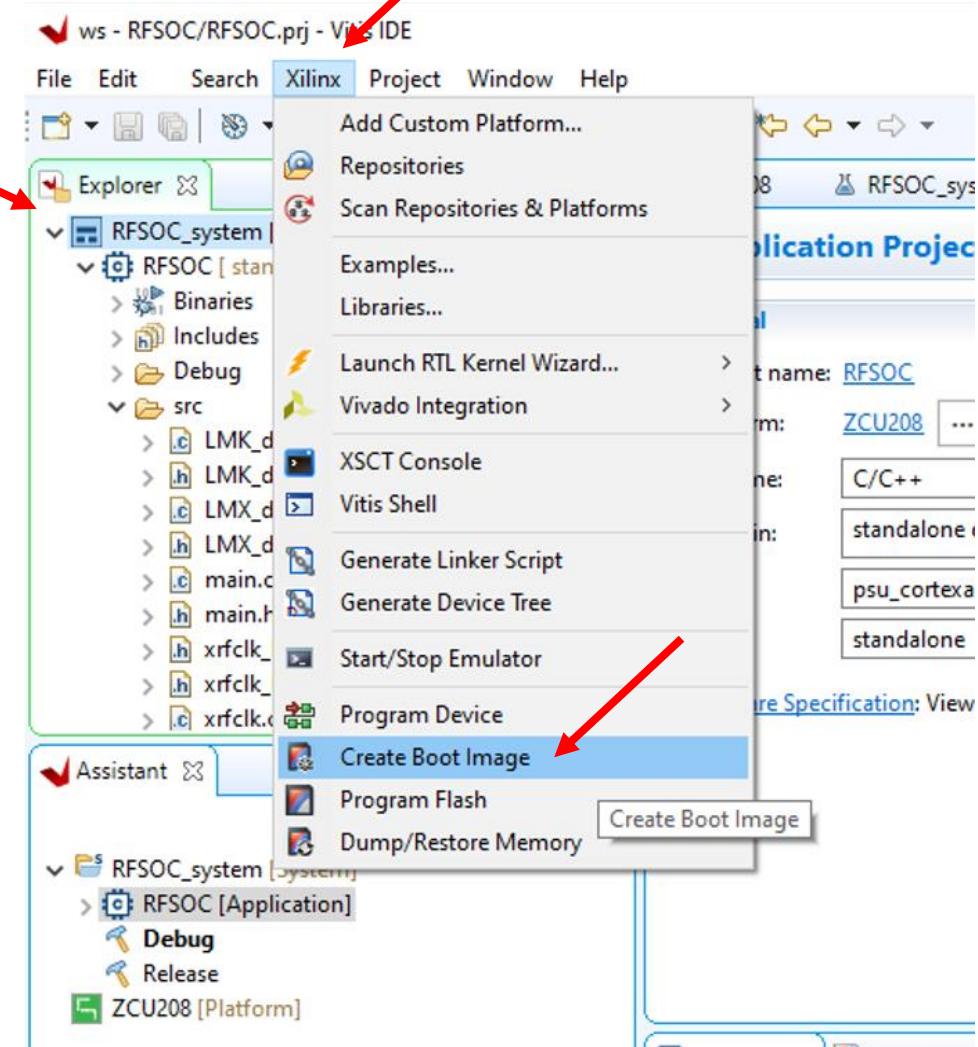




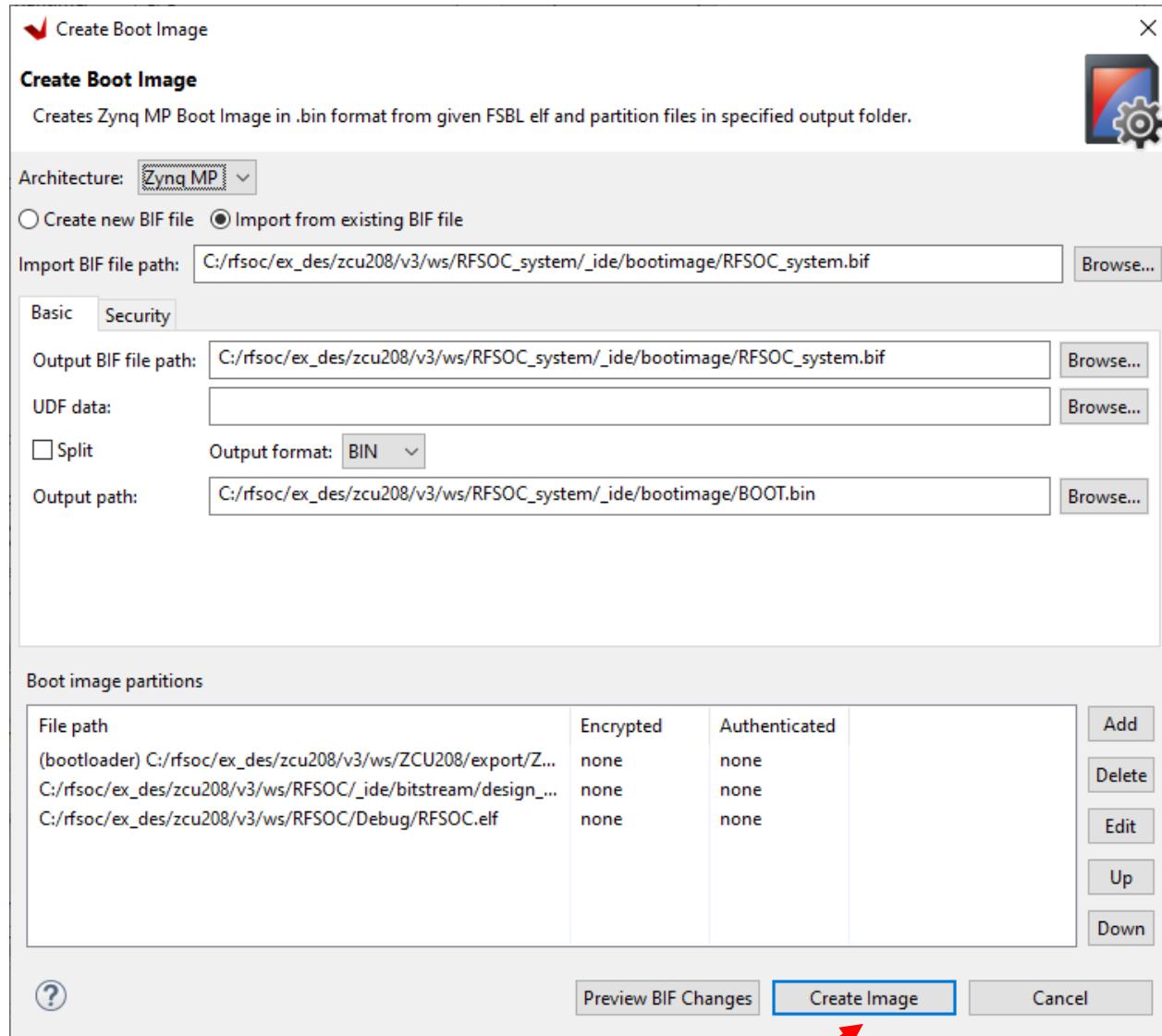
# Boot Image

# Create Boot Image

To run the application from the SD card rather than directly from Vitis™, create the boot.bin file.



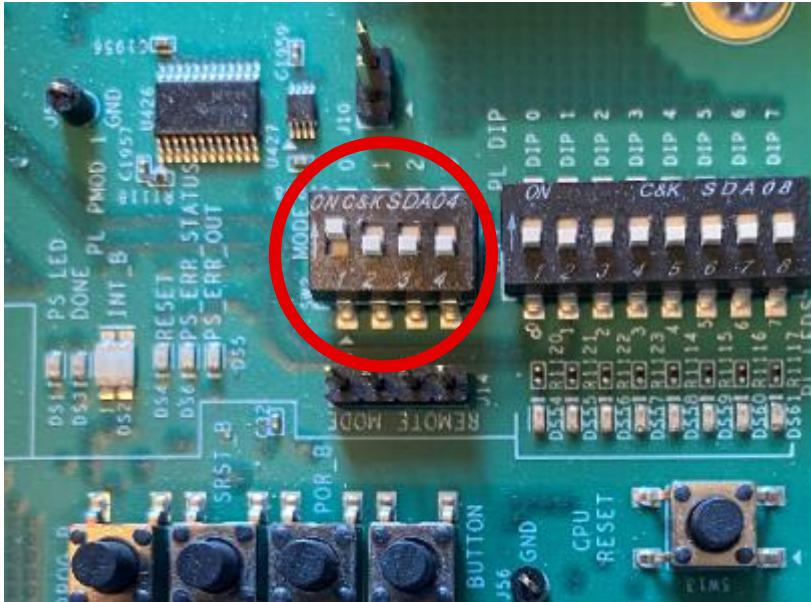
# Create boot.bin File



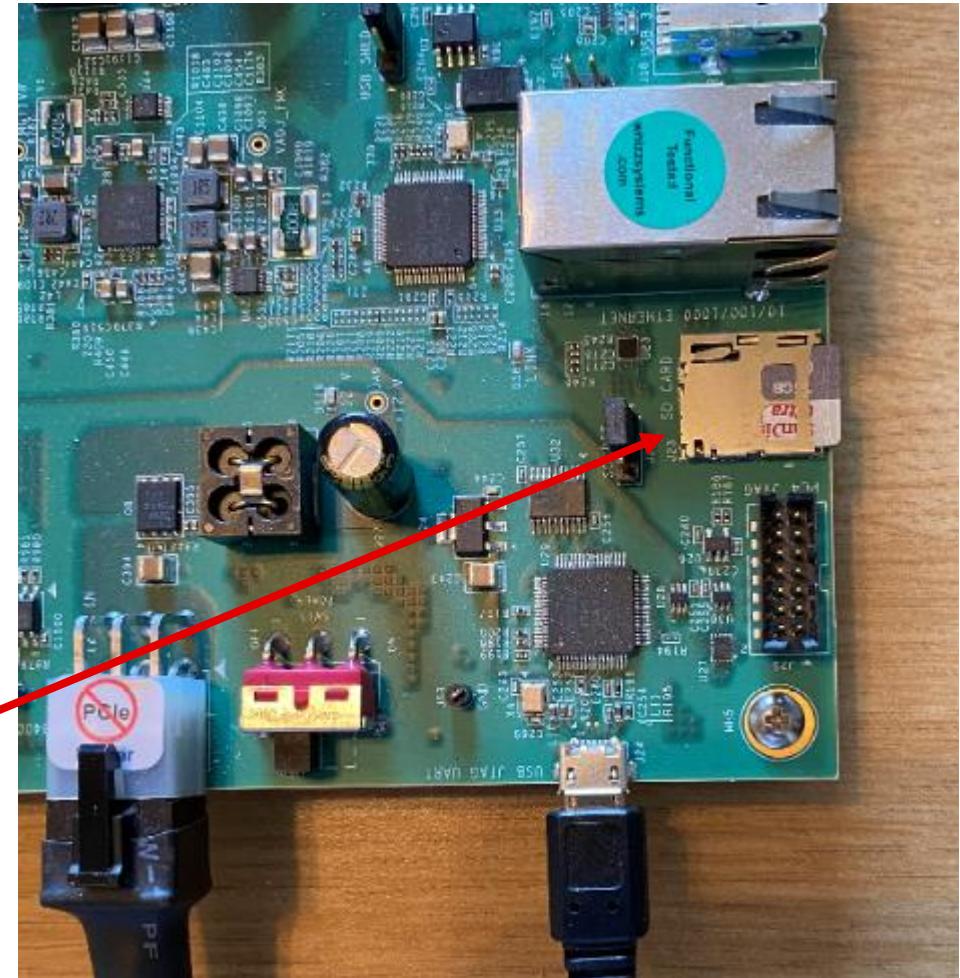
Note the location of the boot.bin file to put at the root level of the SD card.

# Boot from SD Card

Set SW2 to on,off,off,off (SD Card boot mode).



Load boot.bin on the SD card, insert it into the board, and turn on the power.





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Thank You

