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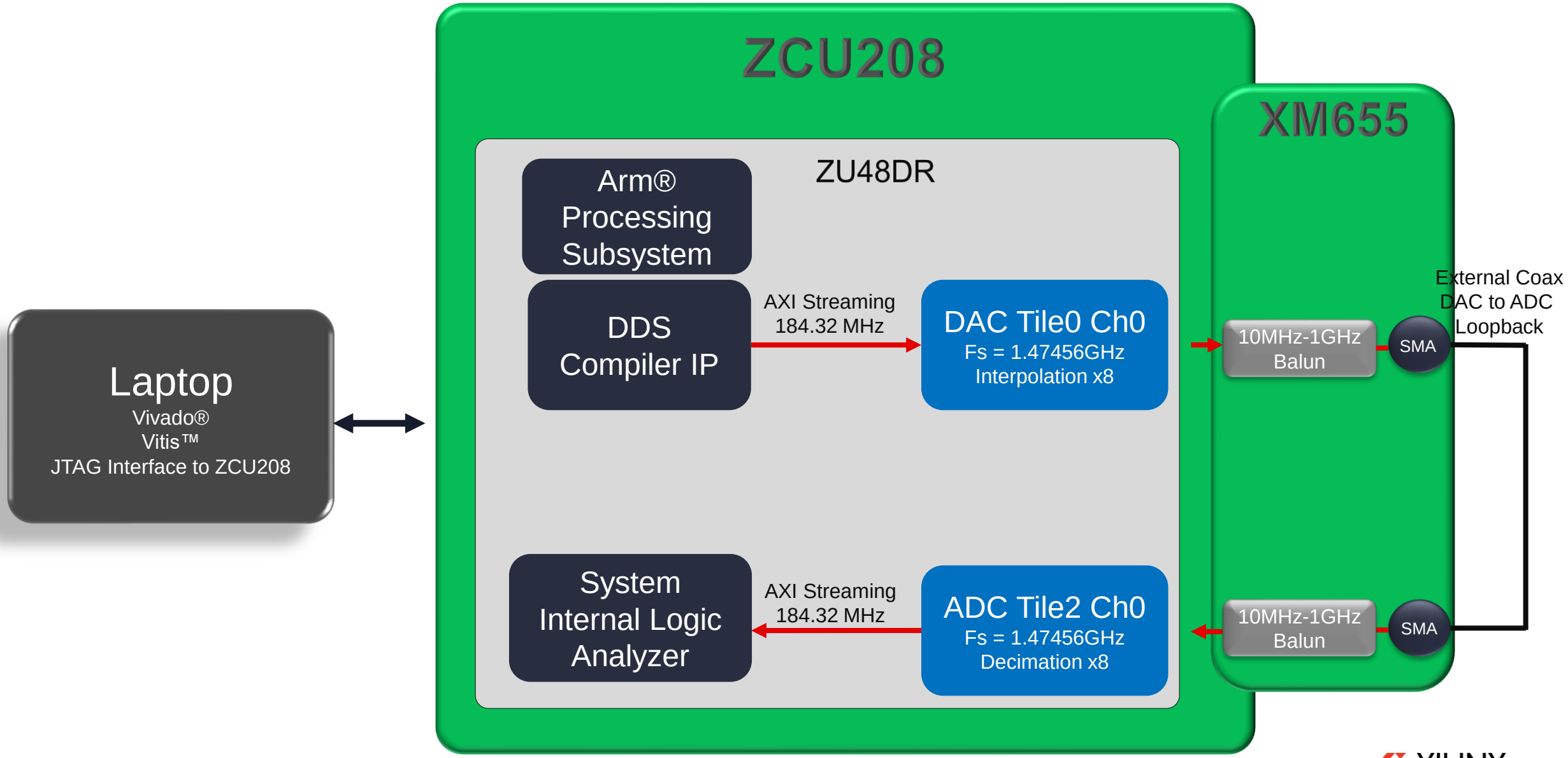
Zynq® UltraScale+™ RFSoC Example Design: ZCU208

DDS Compiler for DAC and System ILA for ADC Capture – 2020.2

Introduction

- This is an example starter design for the RFSoC.
- It uses the ZCU208 board.
- It uses a DAC and ADC sample rate of 1.47456GHz.
- The DAC will continuously play 10MHz sine wave from the DDS Compiler IP.
- The ADC output will be sent to a System ILA to be displayed in the Hardware Manager.
- DAC Tile228(0) Ch0 will be used (LF balun).
- ADC Tile226(2) Ch0 will be used (LF balun)
- 2020.2 Xilinx tools (Vivado® Design Suite and Vitis™ unified software platform).
- Design tested in the directory *c:\rfsoc\ex_des\zcu208\v3\.*
- This kit comes with the Vivado HW project and SW source files.

Demo Block Diagram



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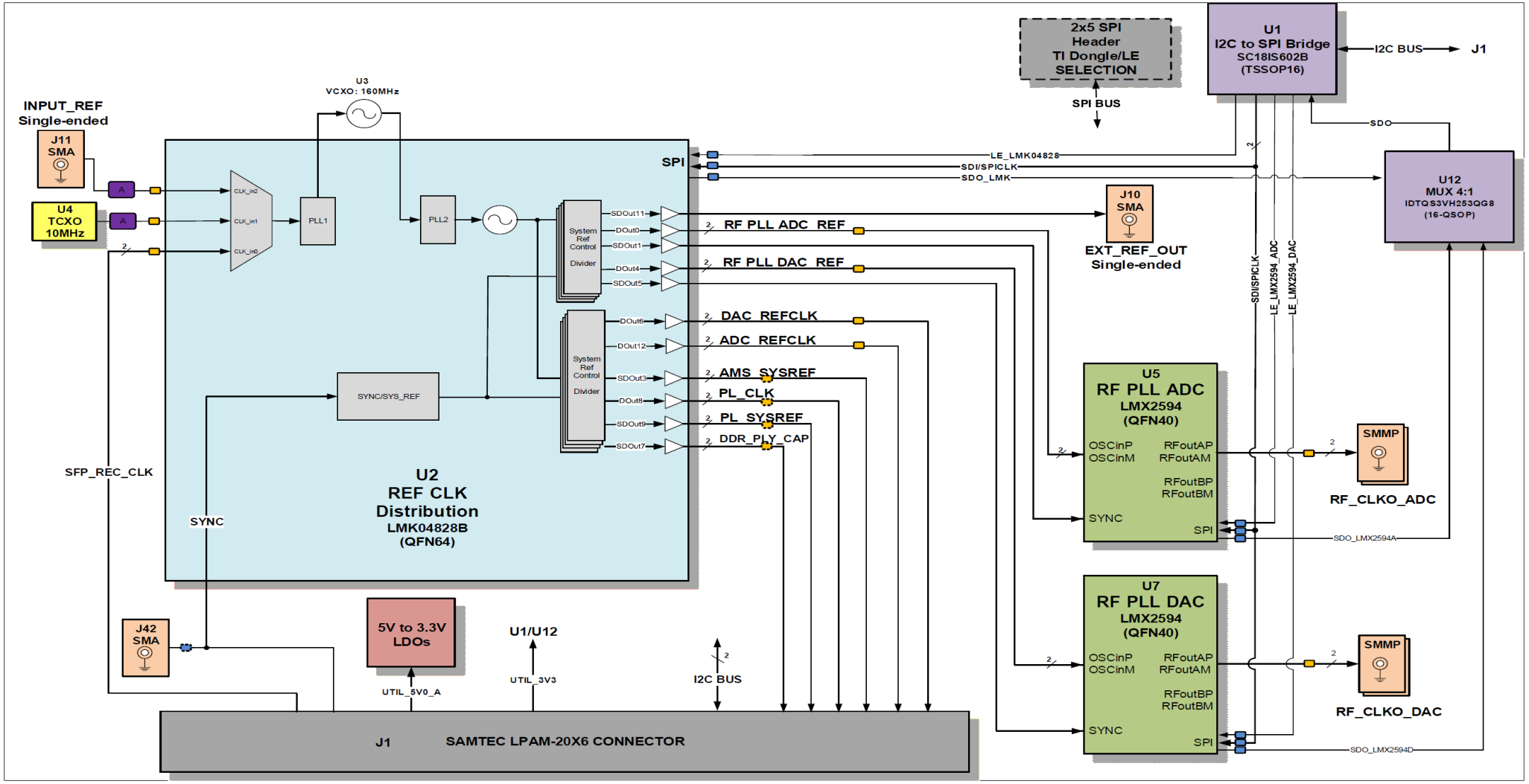
CLK104 Block Diagram

Only the LMK04828B is used for this design; the LMX2594 outputs are powered down.

Clocking is configured via an I2C to SPI bridge.

Block Diagram



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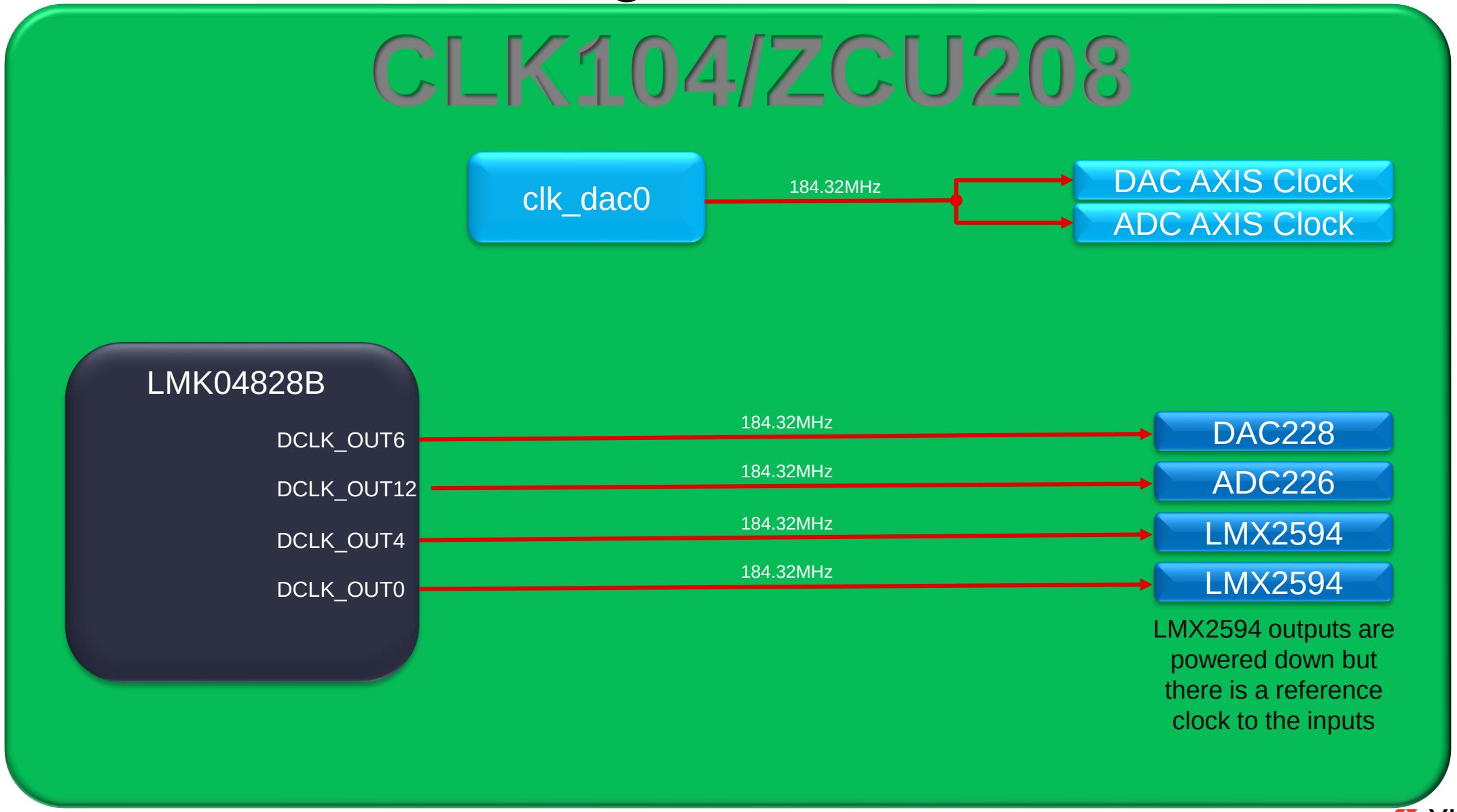
Data Converter Clocking



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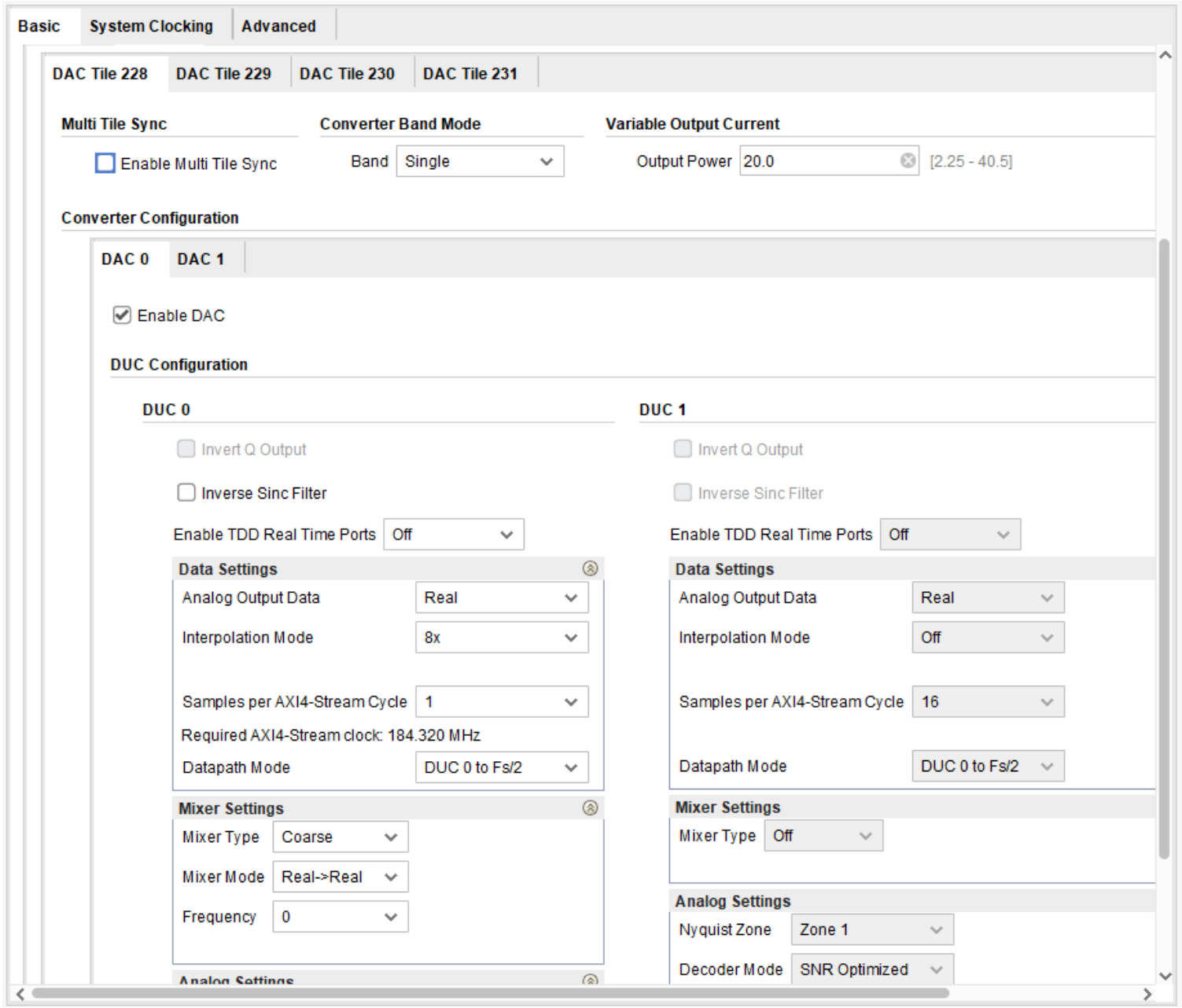
DAC Setup



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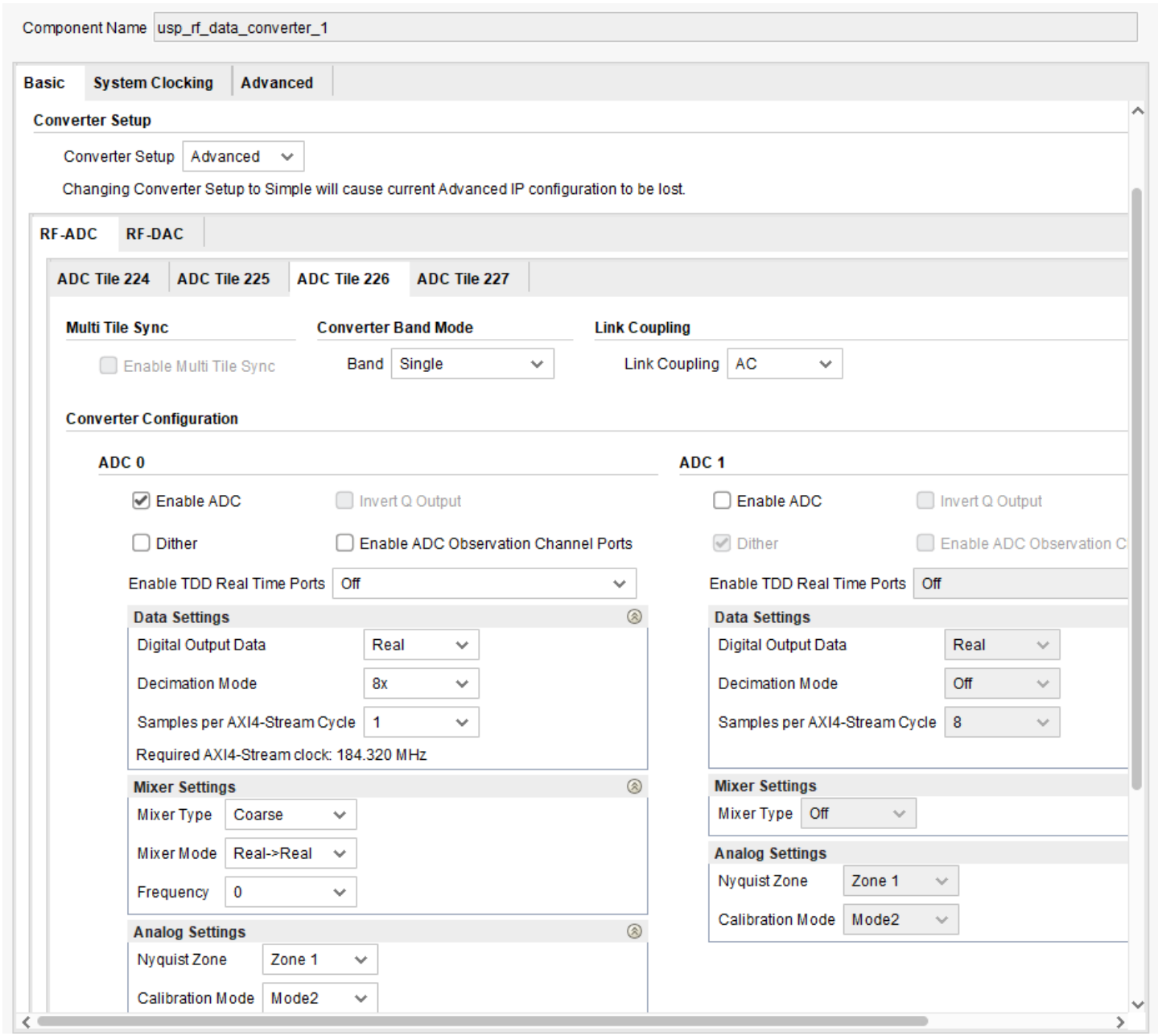
ADC Setup



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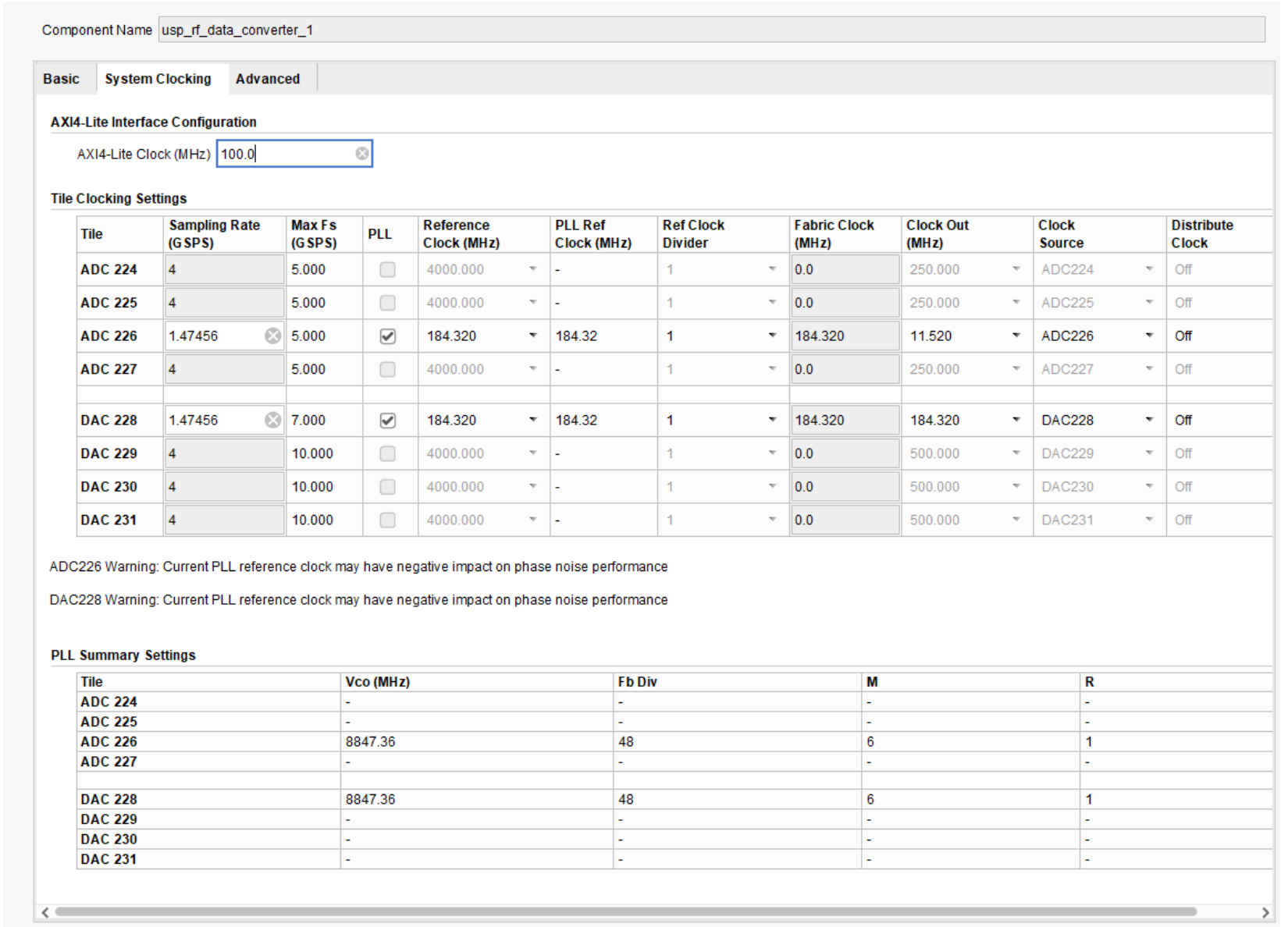
Data Converter Clocking



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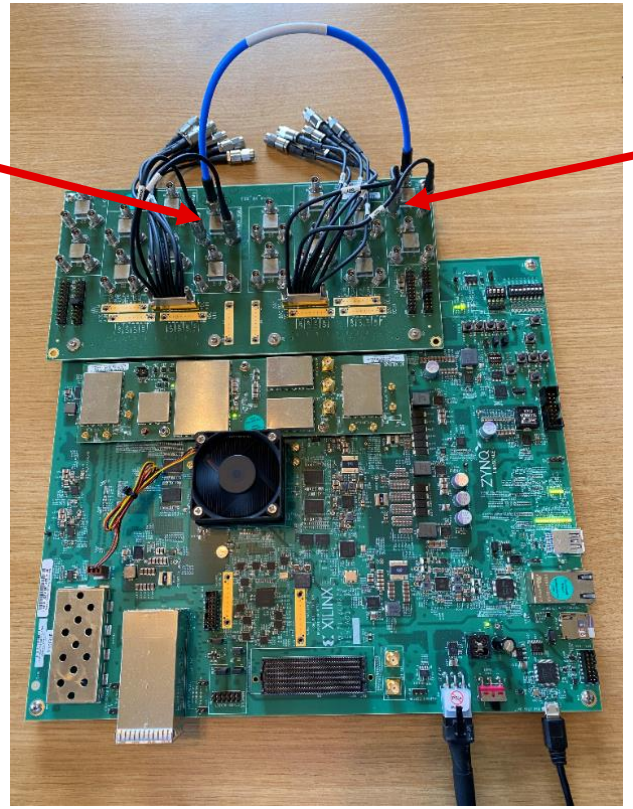
Board Setup for the Upcoming Designs

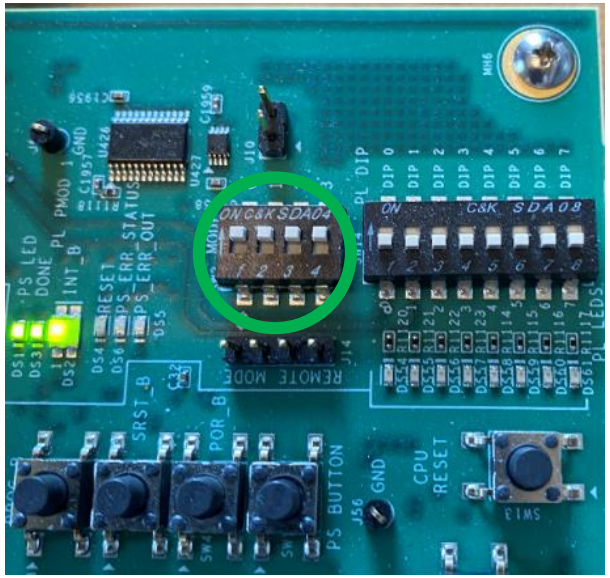
- Connect DAC Tile 228 Ch0 output to ADC Tile 226 Ch0 input on XM655 (low frequency balun connections).
- Set SW2 to on,on,on,on (JTAG boot mode).
- Connect USB to host for JTAG, PS UART, and System Controller UART access.

ADC Tile2 Ch0

DAC Tile0 Ch0



SW2



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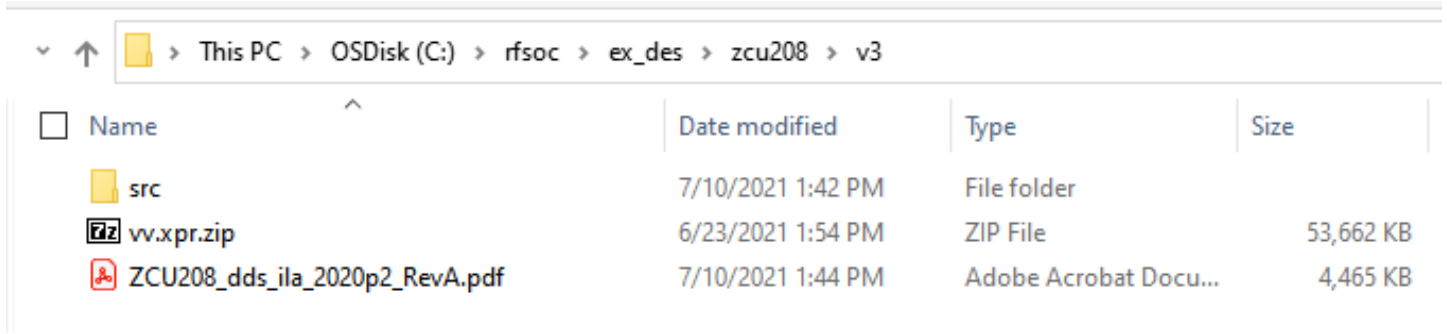
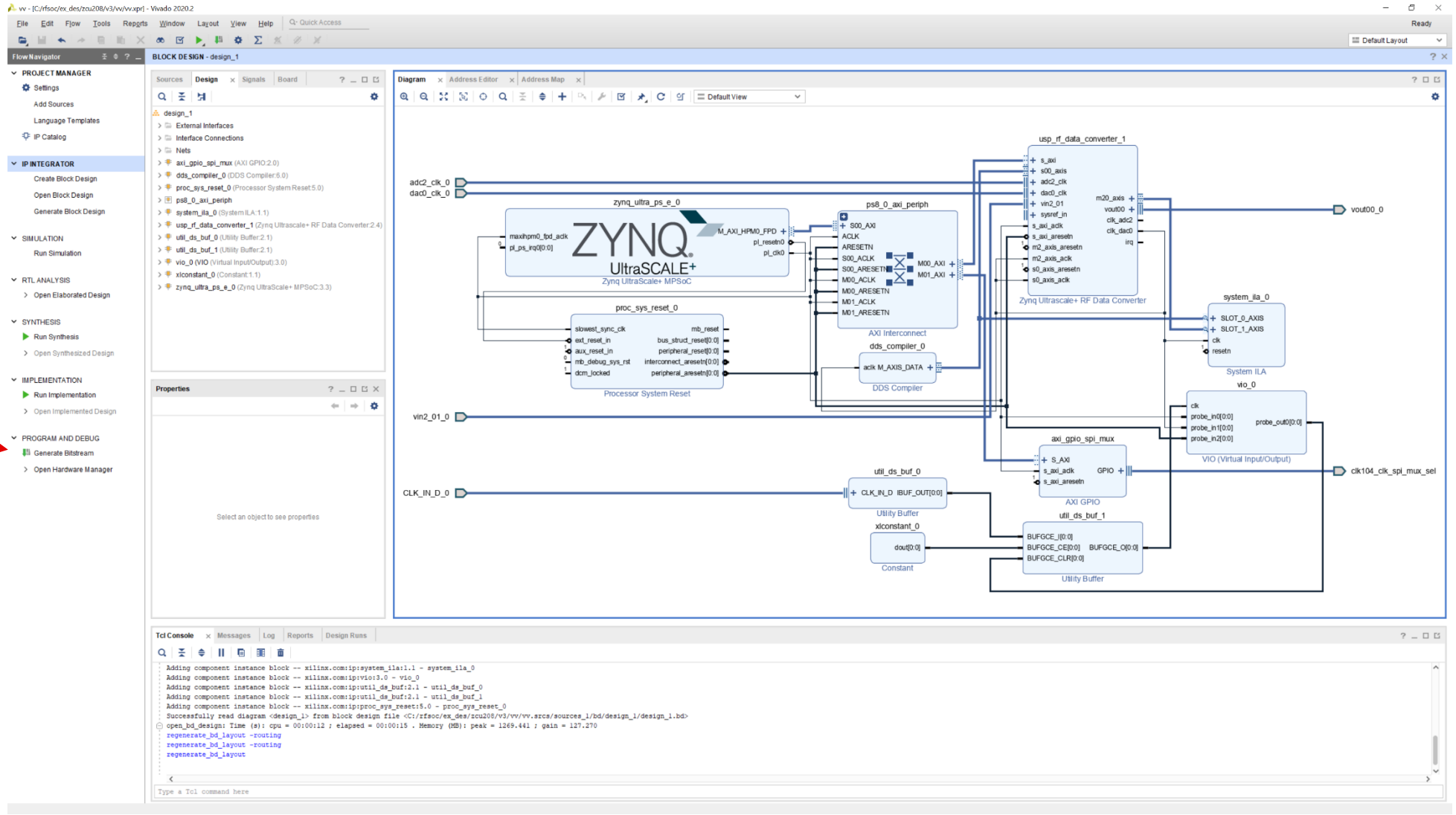
Design Kit Contents

1. Extract the design kit to an appropriate folder—be mindful of the Windows path length requirement.
2. Extract vv.xpr.zip, which is the Vivado project.
3. Software source files in the “src” folder.
4. Design documentation in the .pdf file.



Open Hardware Design and Generate the Bitstream

Extract vv.xpr.zip, open the design in Vivado®, and generate the bitstream.



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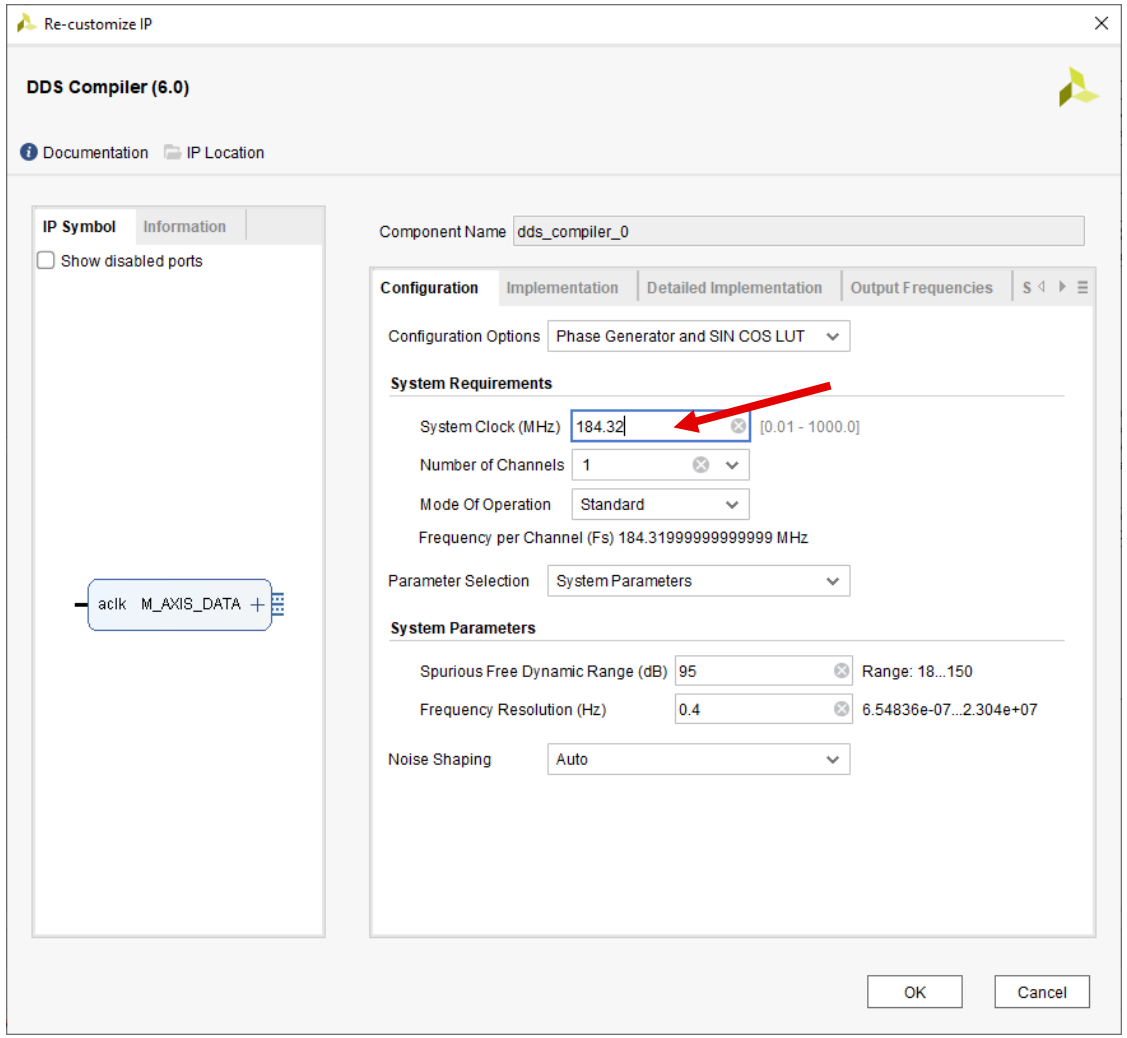
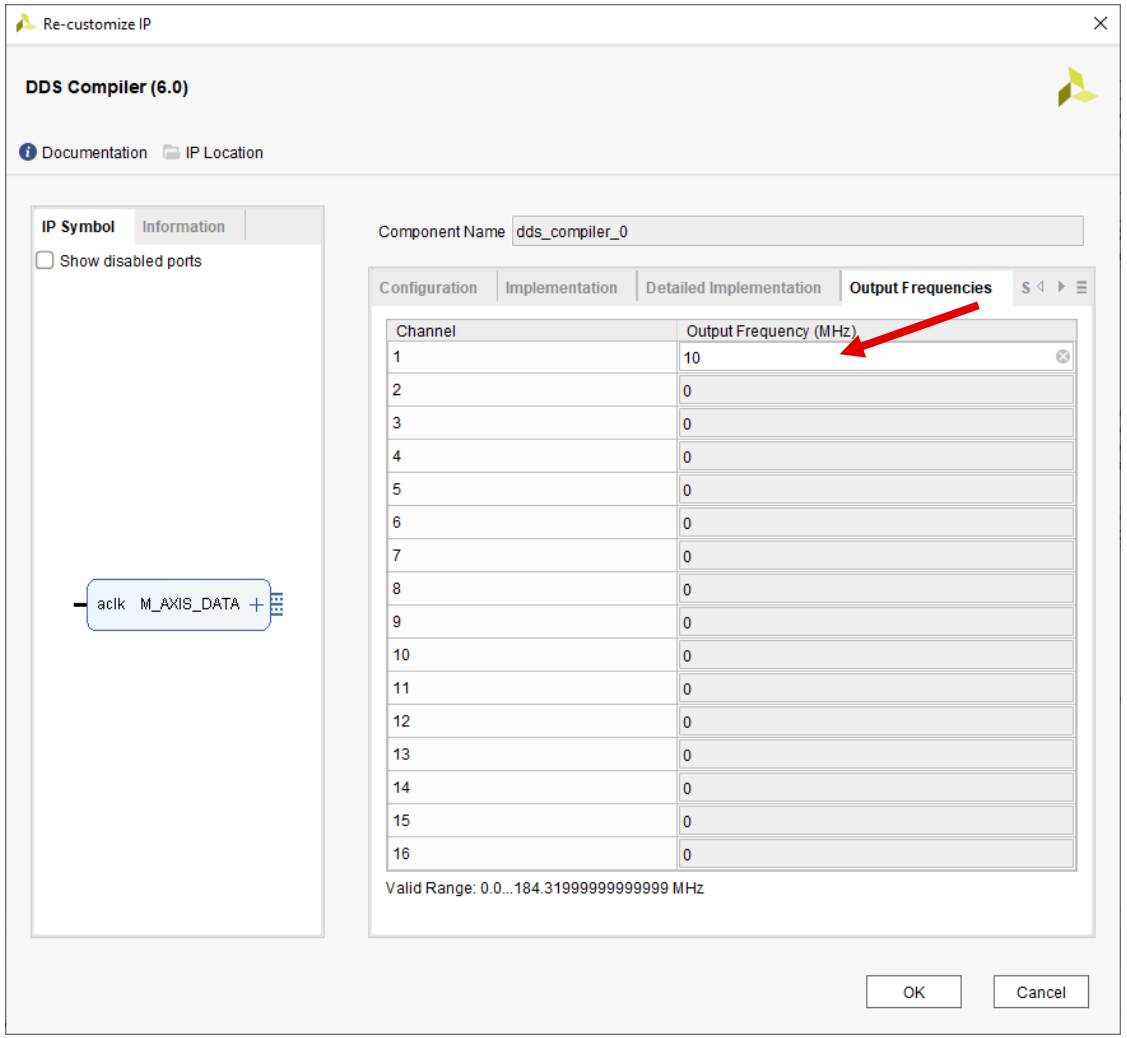
DAC Sine Wave Generator (DDS Compiler IP)





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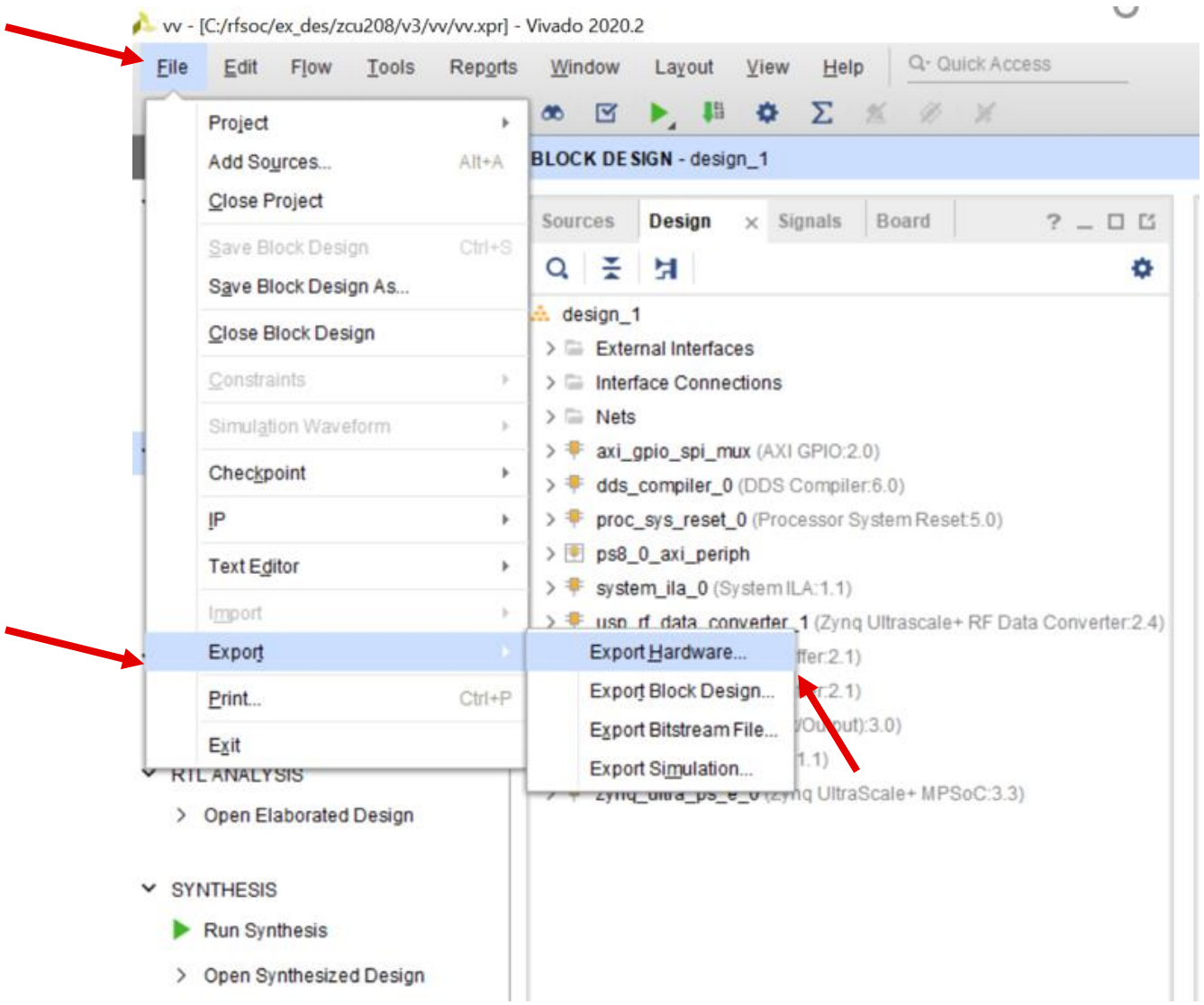
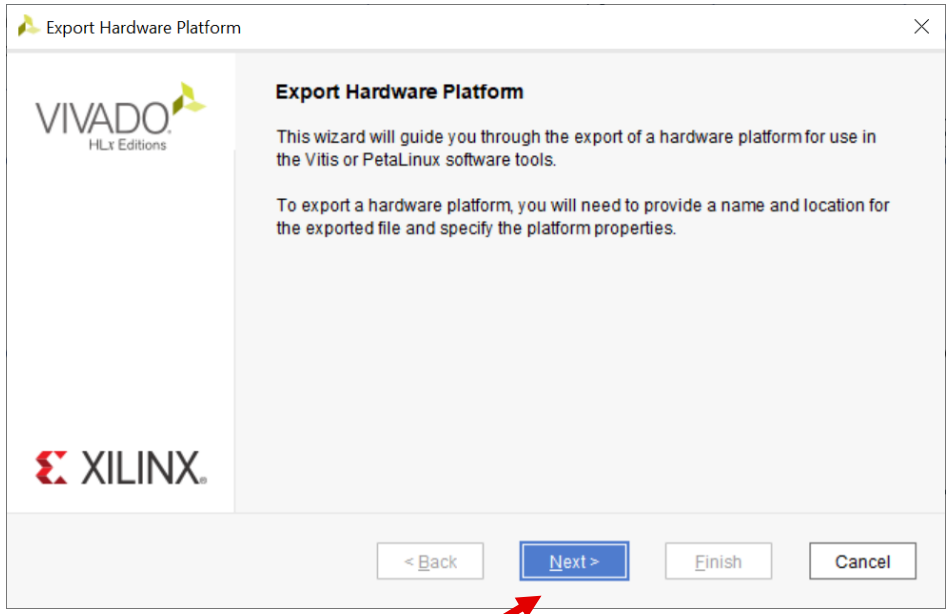
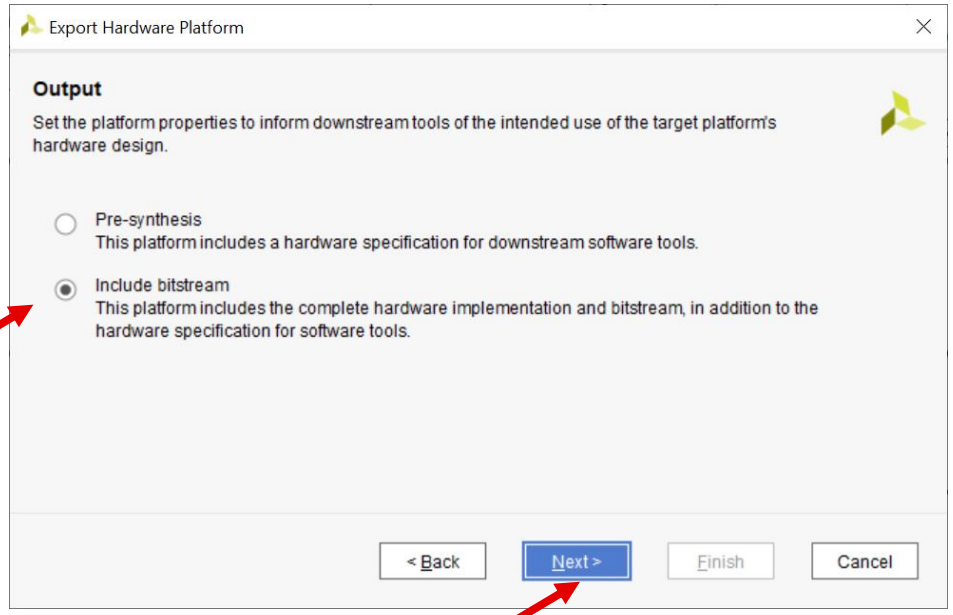
Export Hardware







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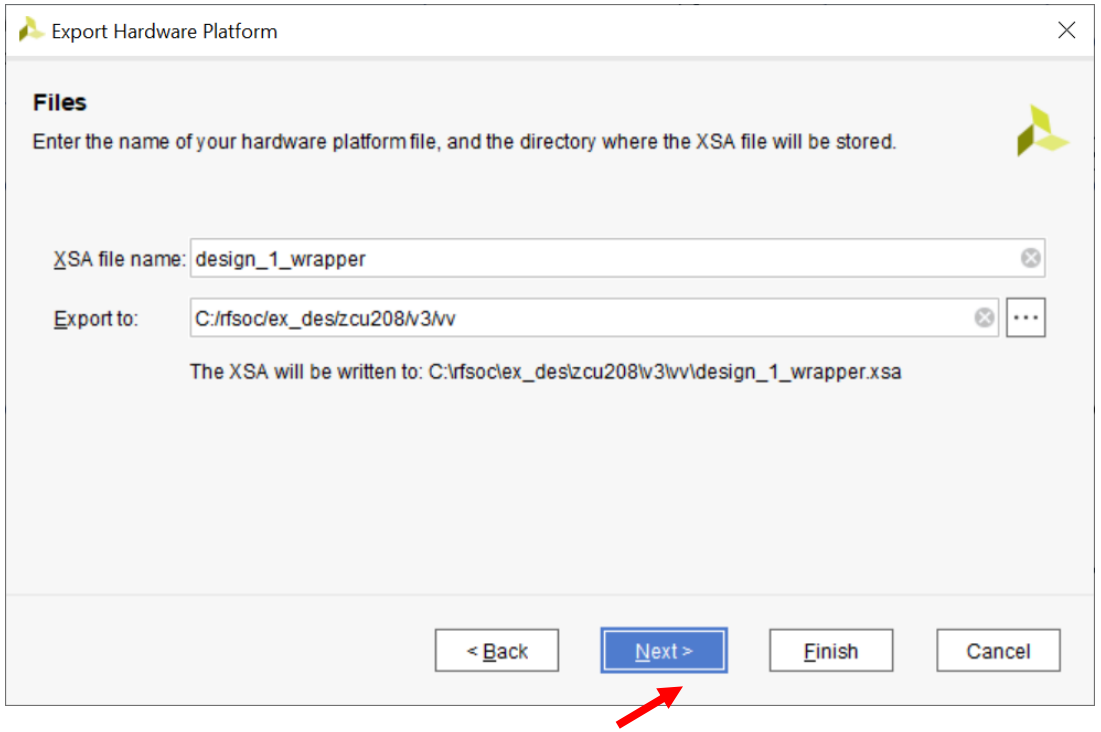
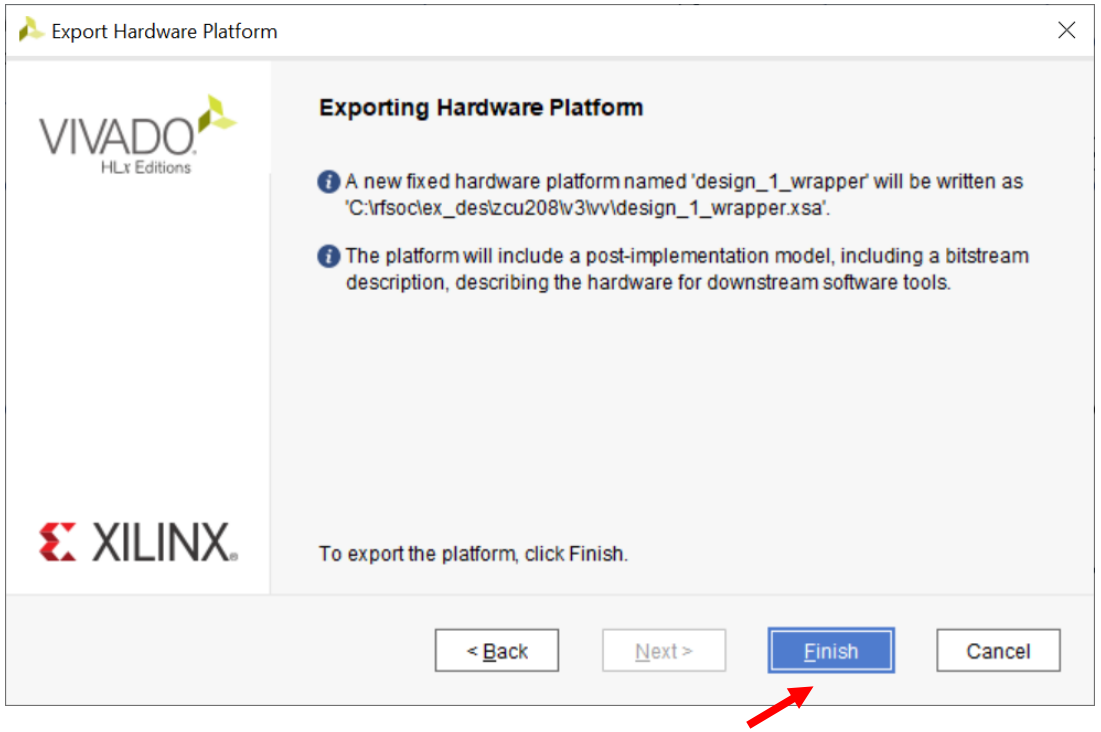
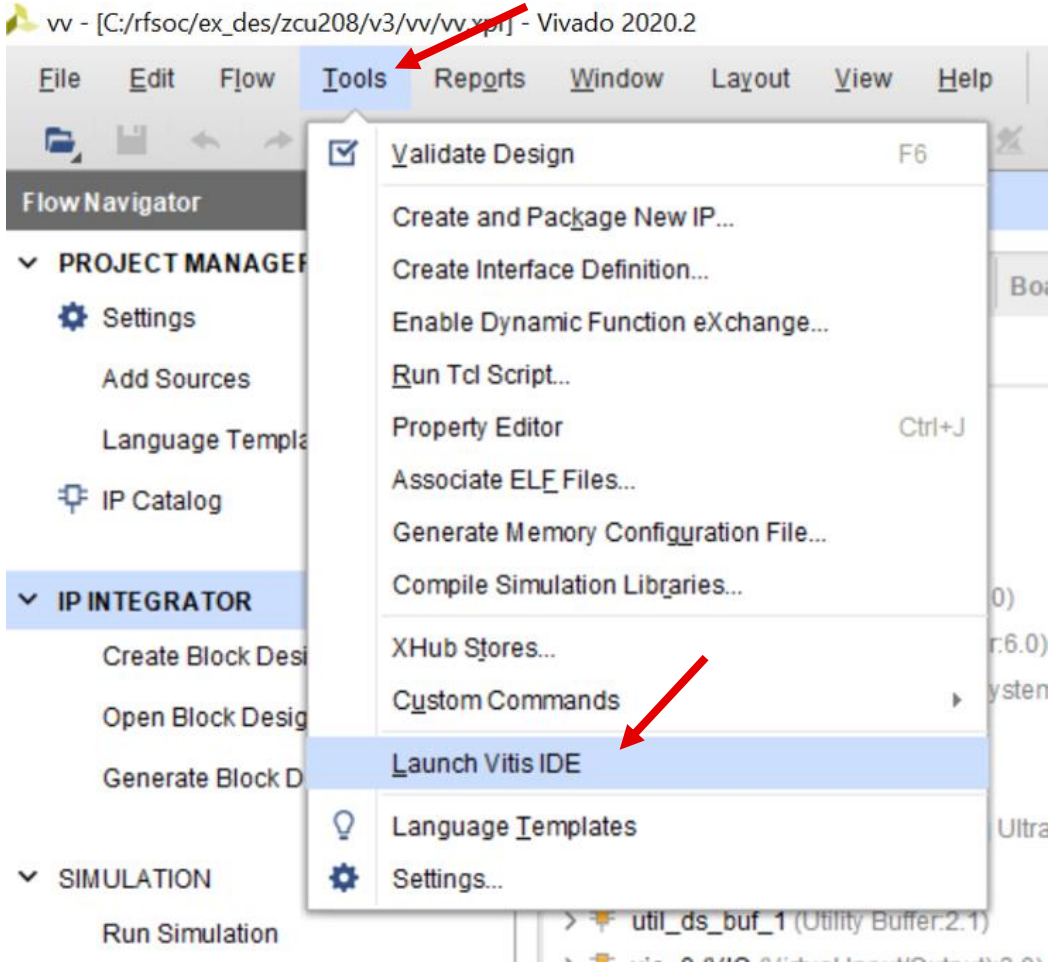
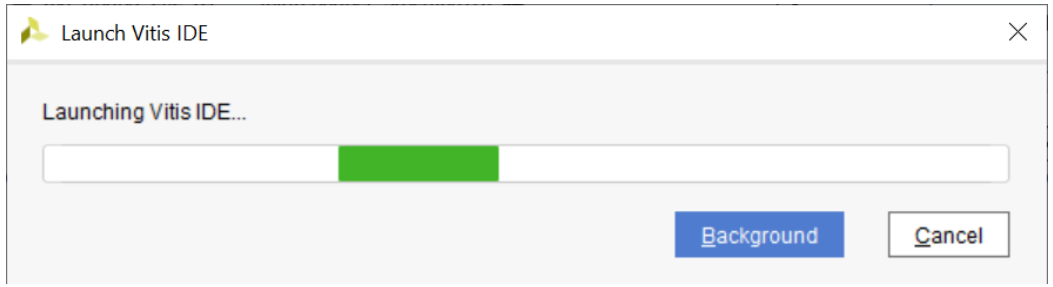
Export Hardware Cont'd

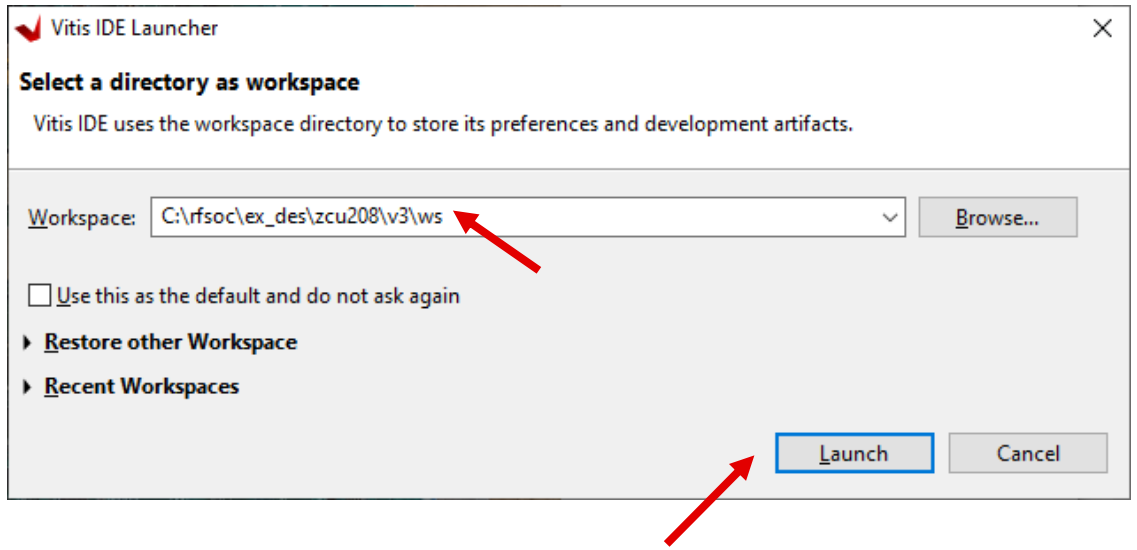




Open Vitis™ Software Platform







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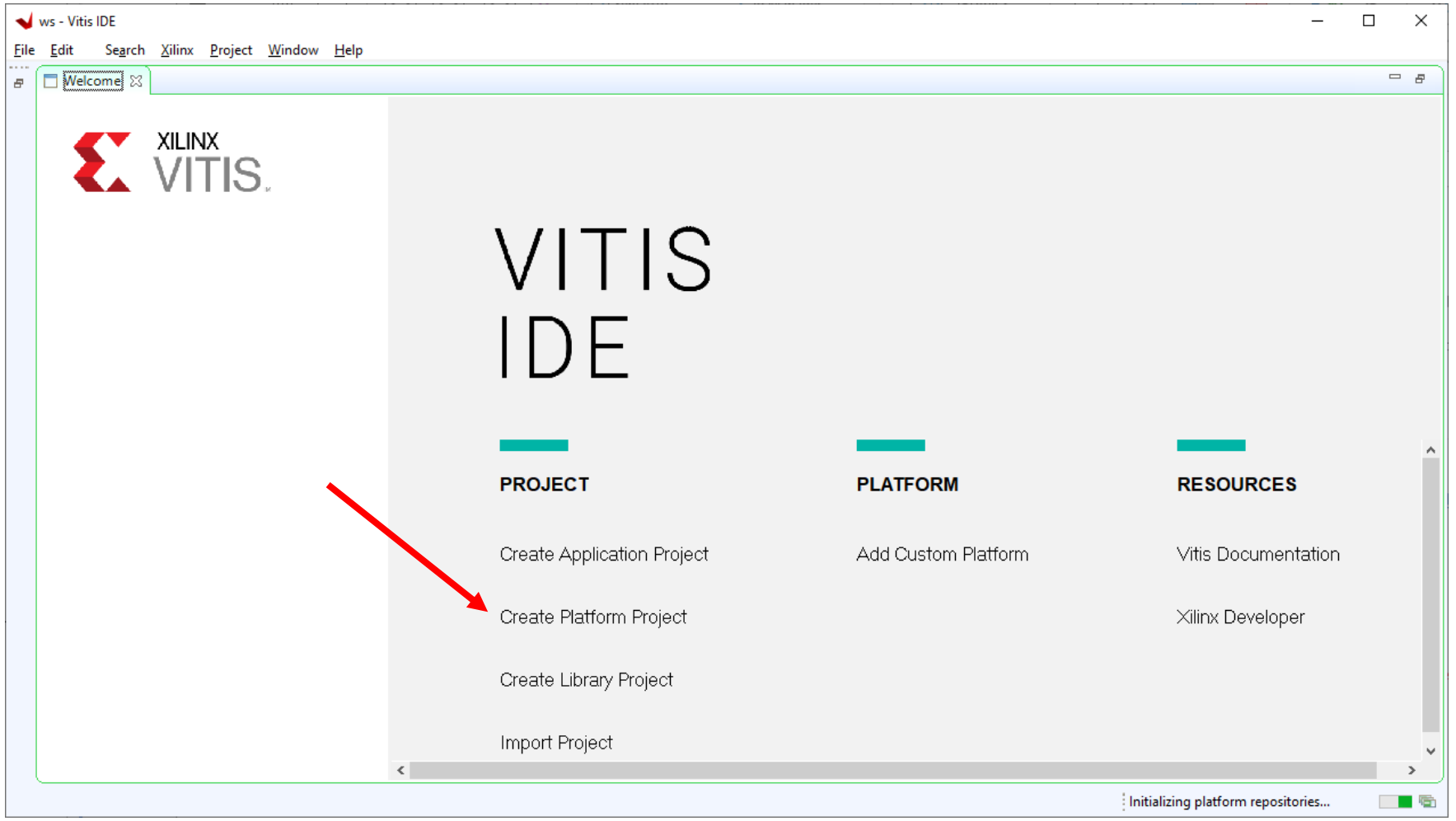
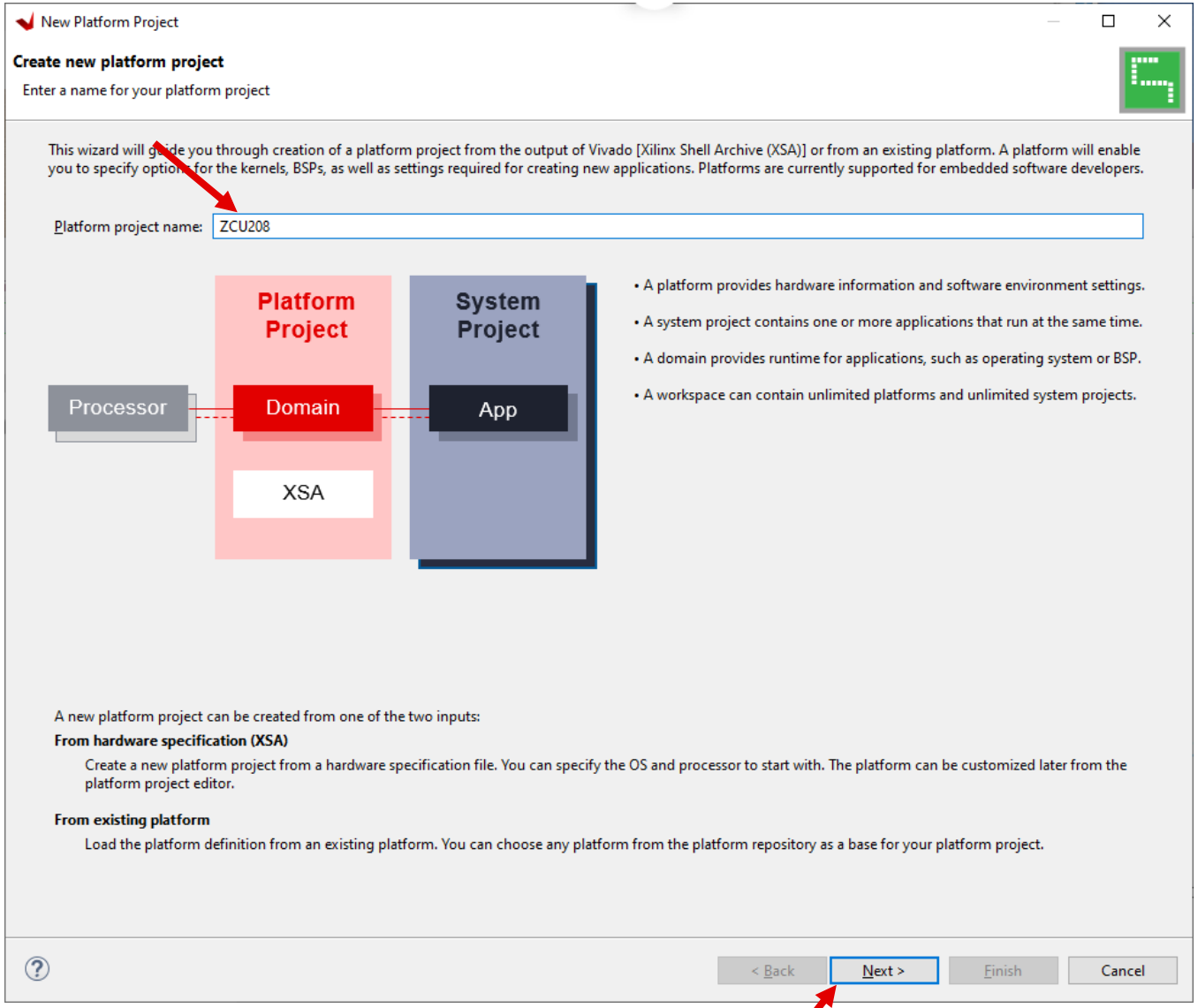
Create Platform Project



Create Platform Project Cont'd



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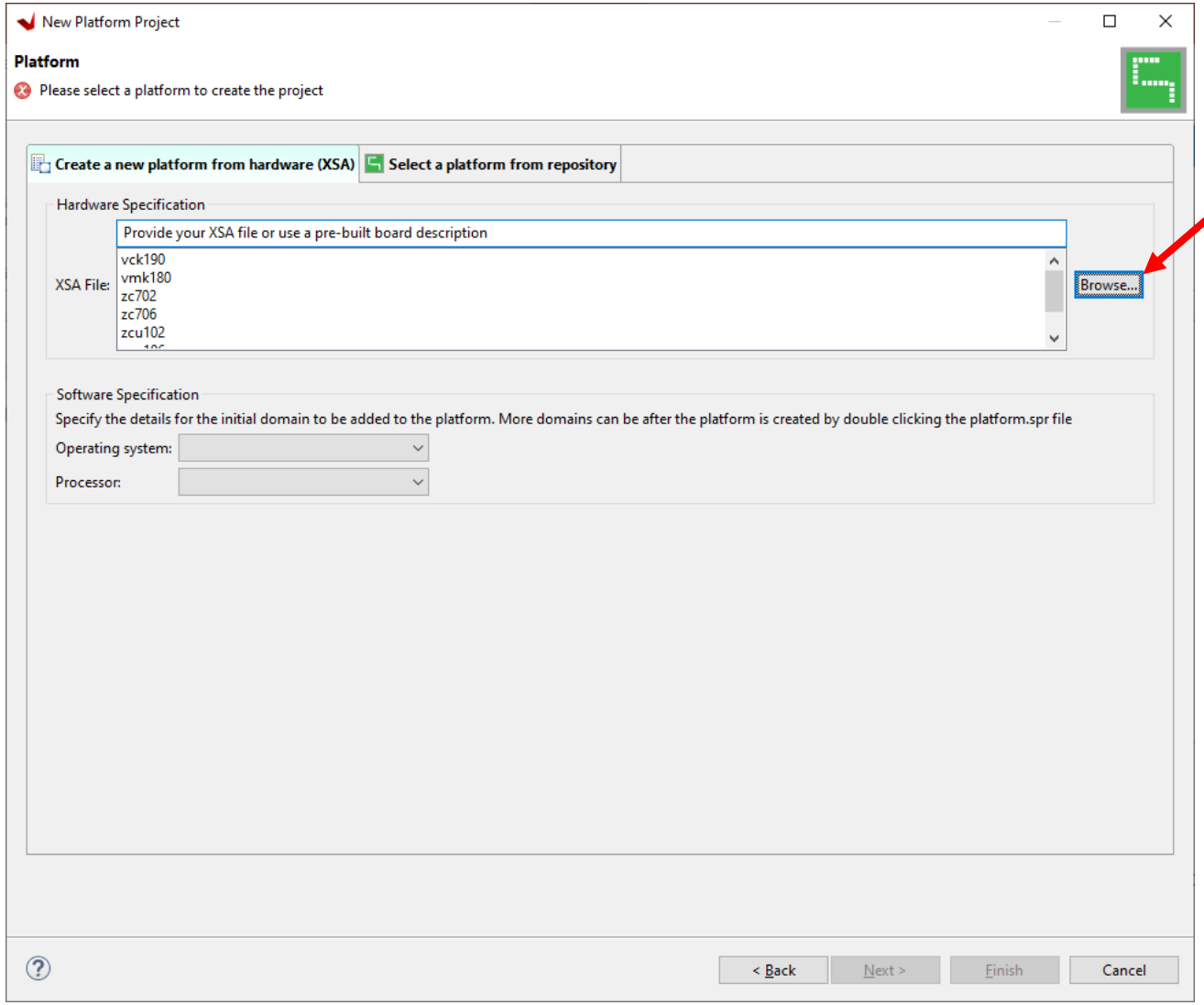
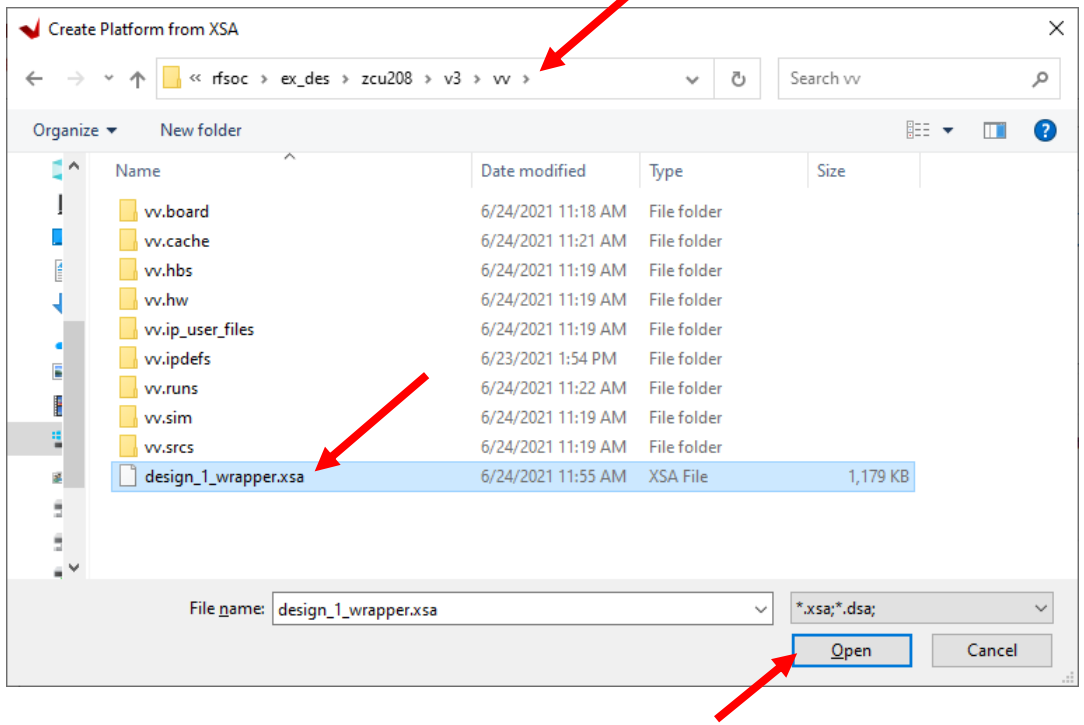
Create Platform Project Cont'd





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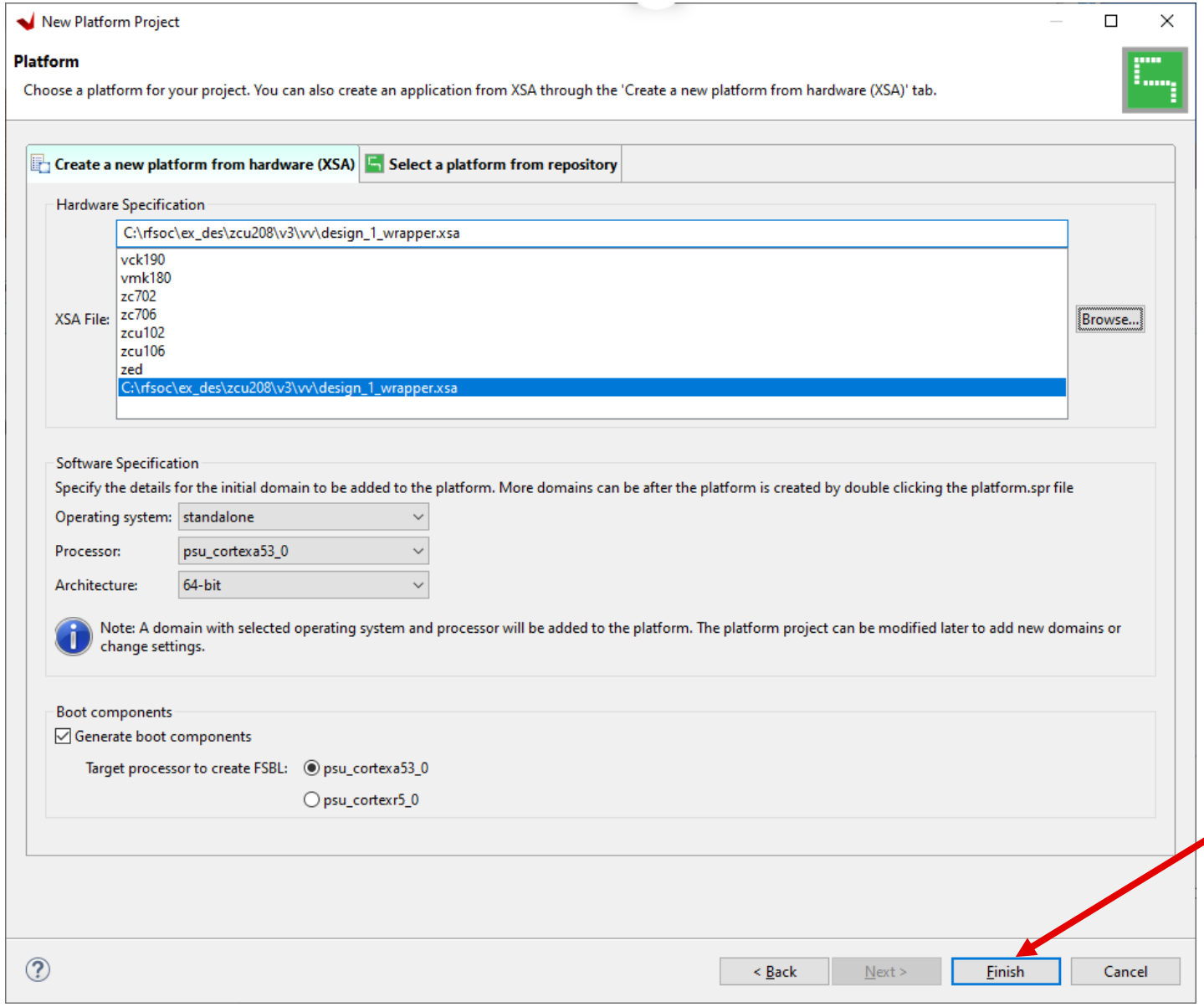
Create Platform Project Cont'd



This may take a few minutes.

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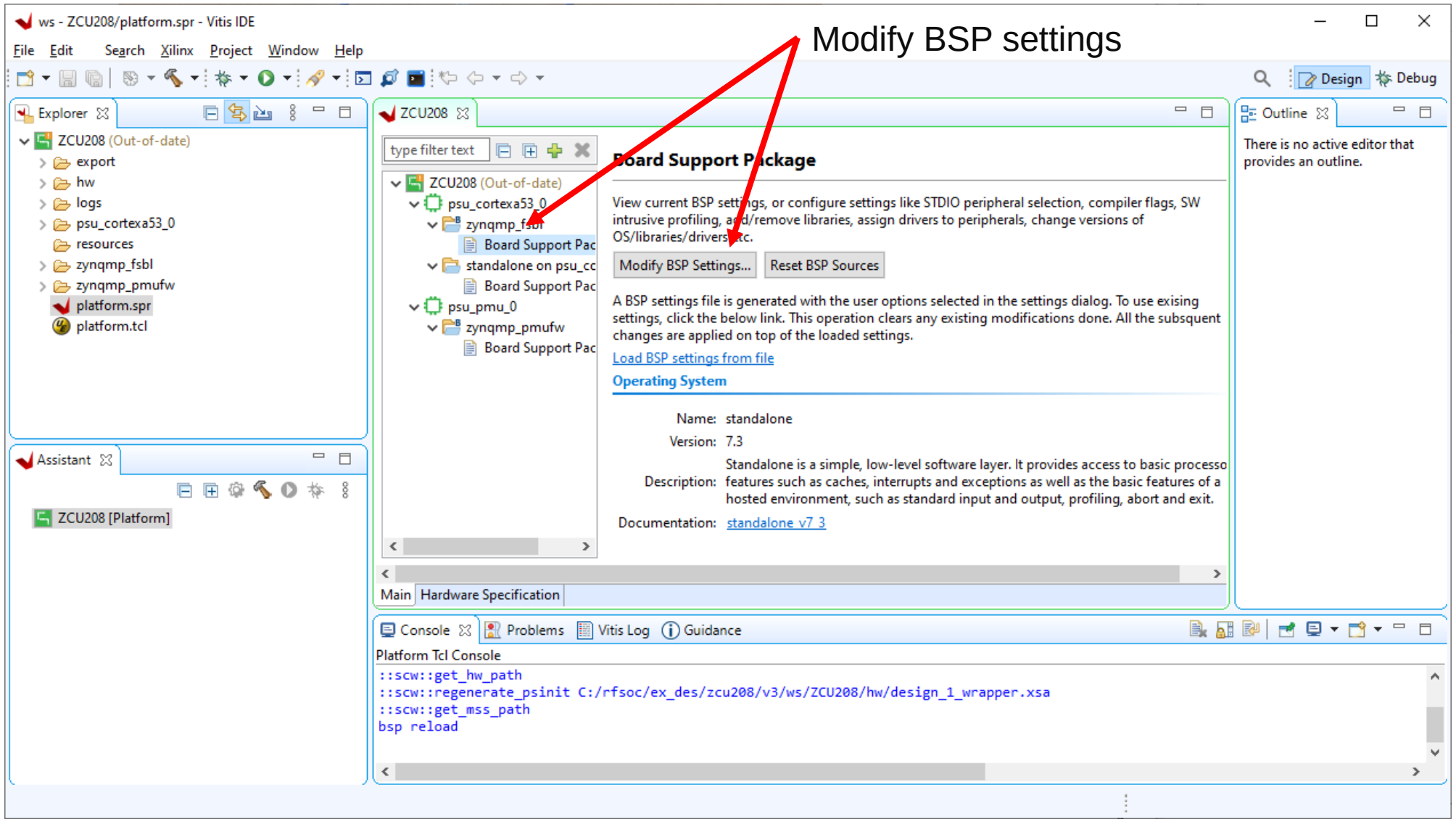
Create Platform Project Cont'd



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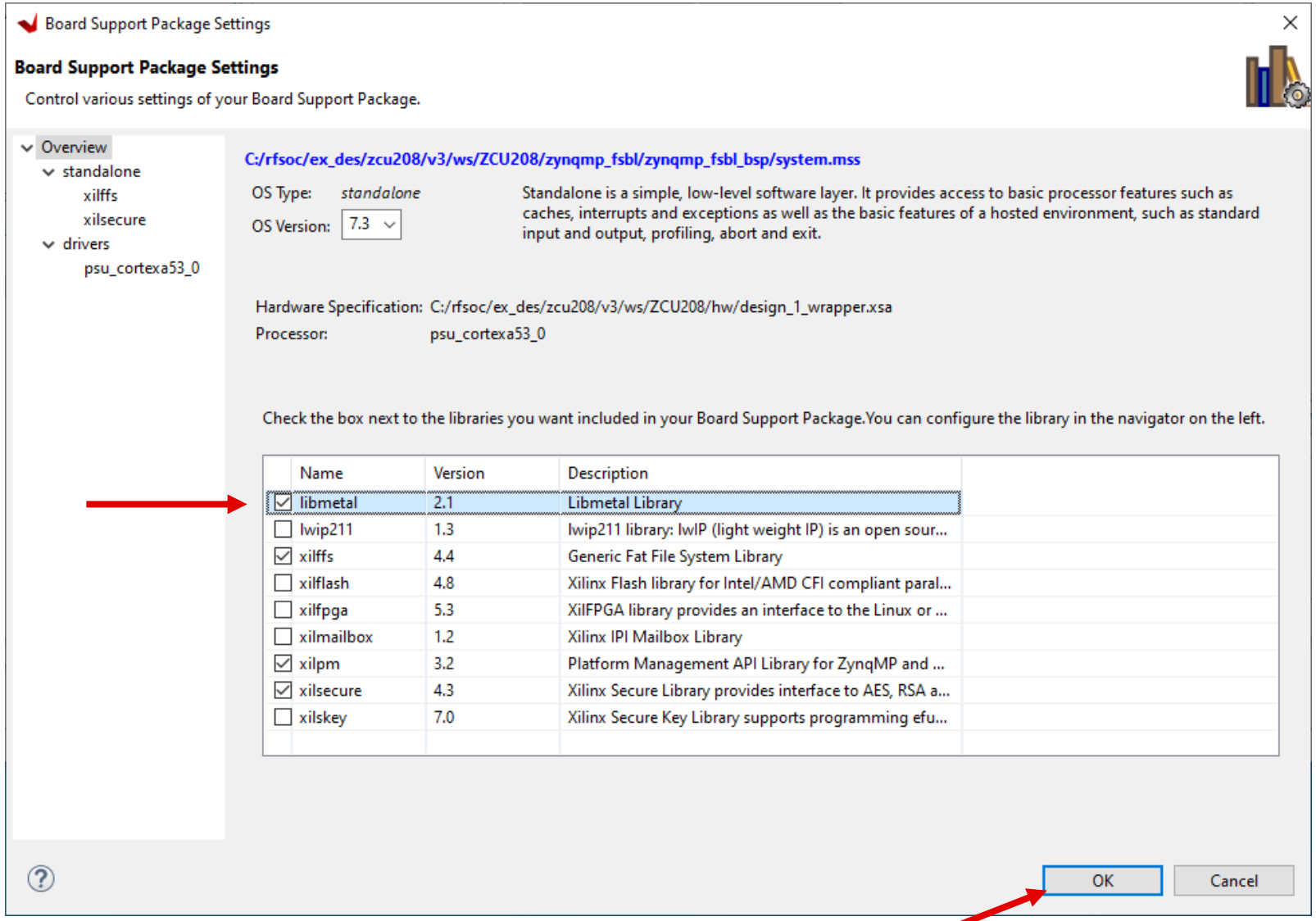
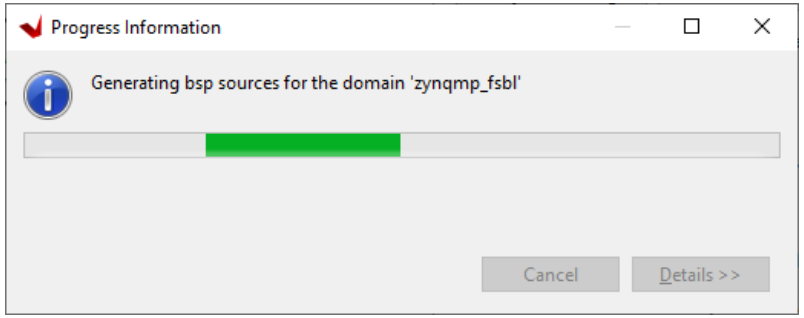
Enable libmetal





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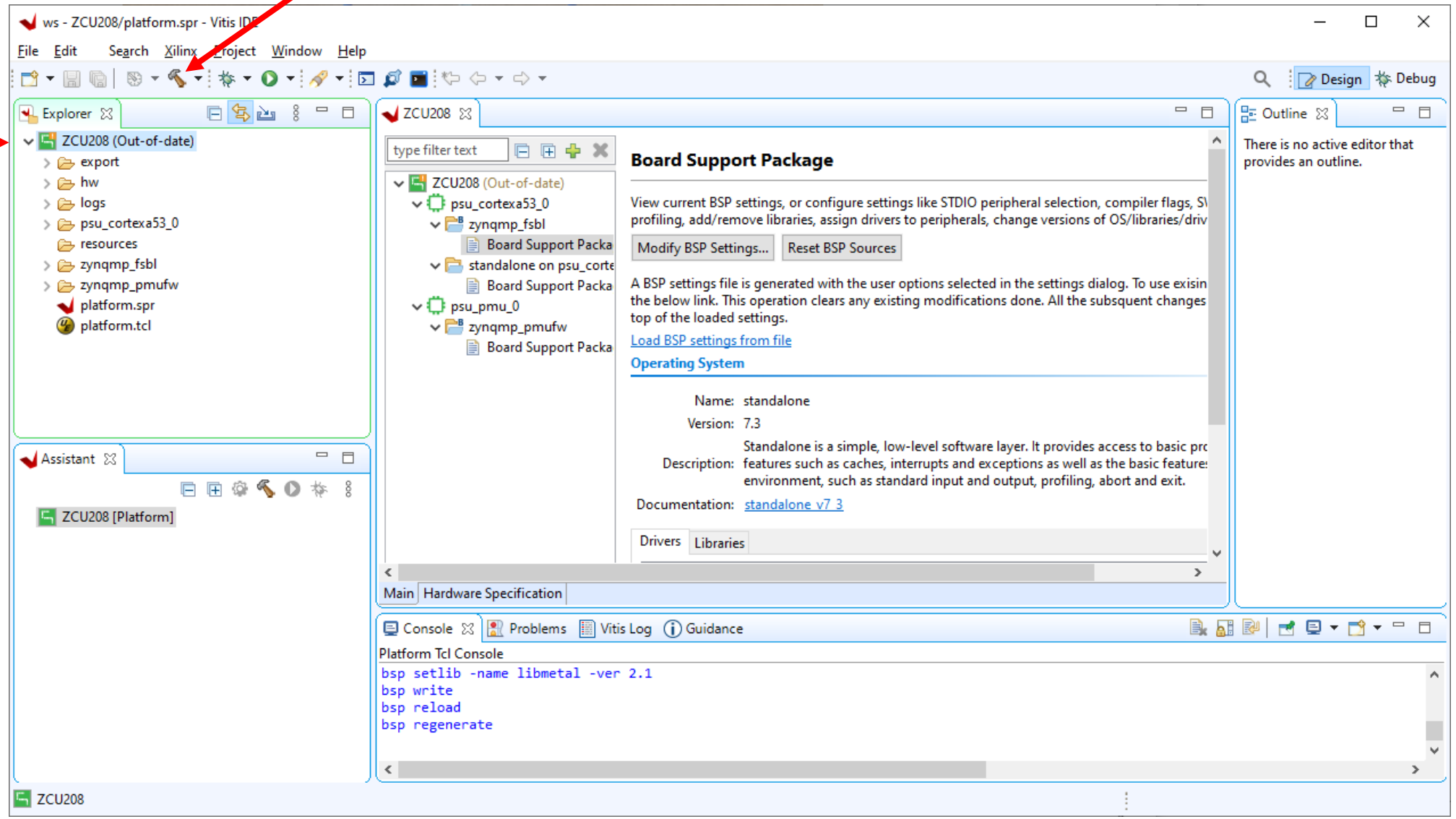
Build Project

This may take a few minutes.



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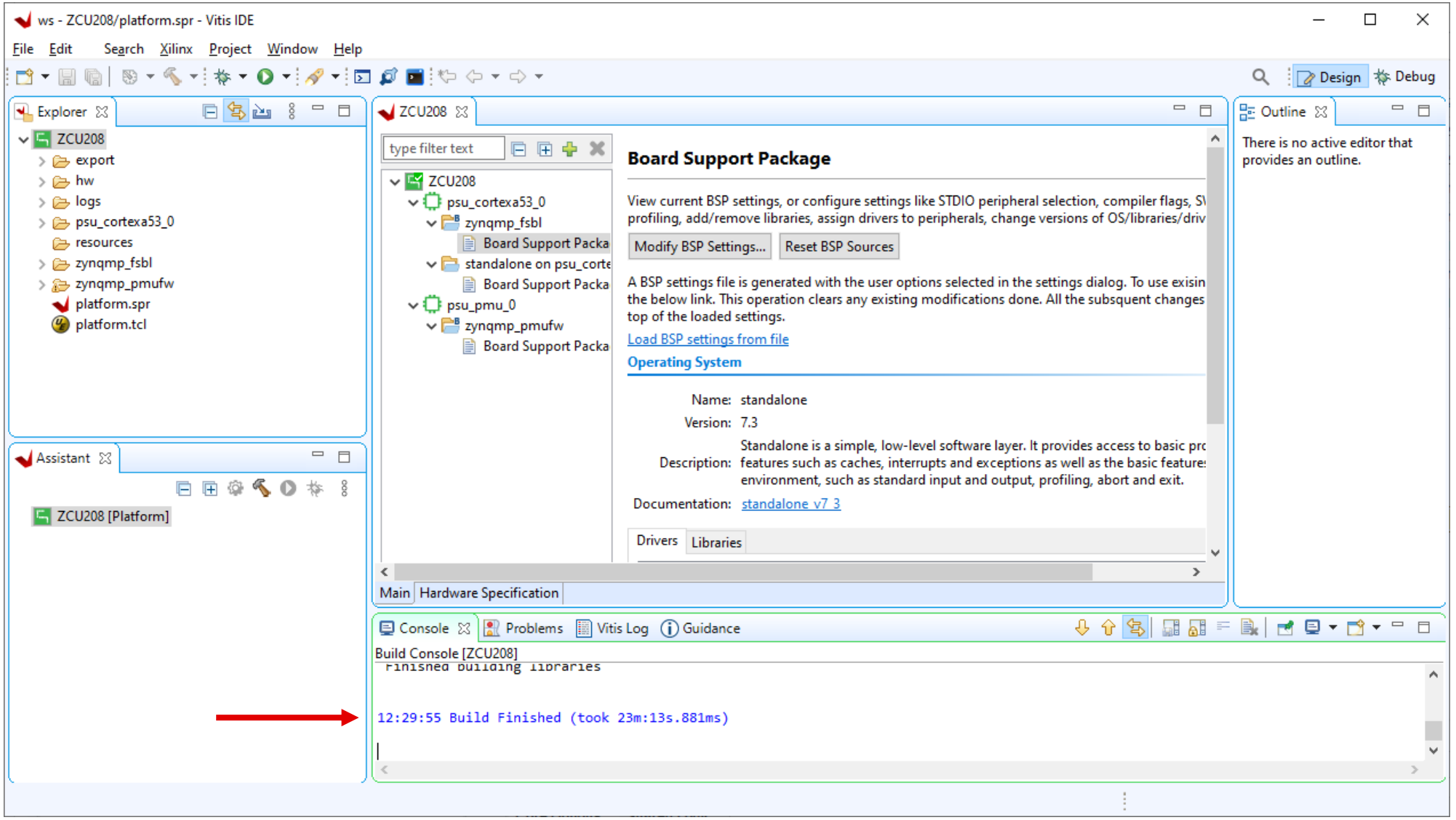
Build Complete



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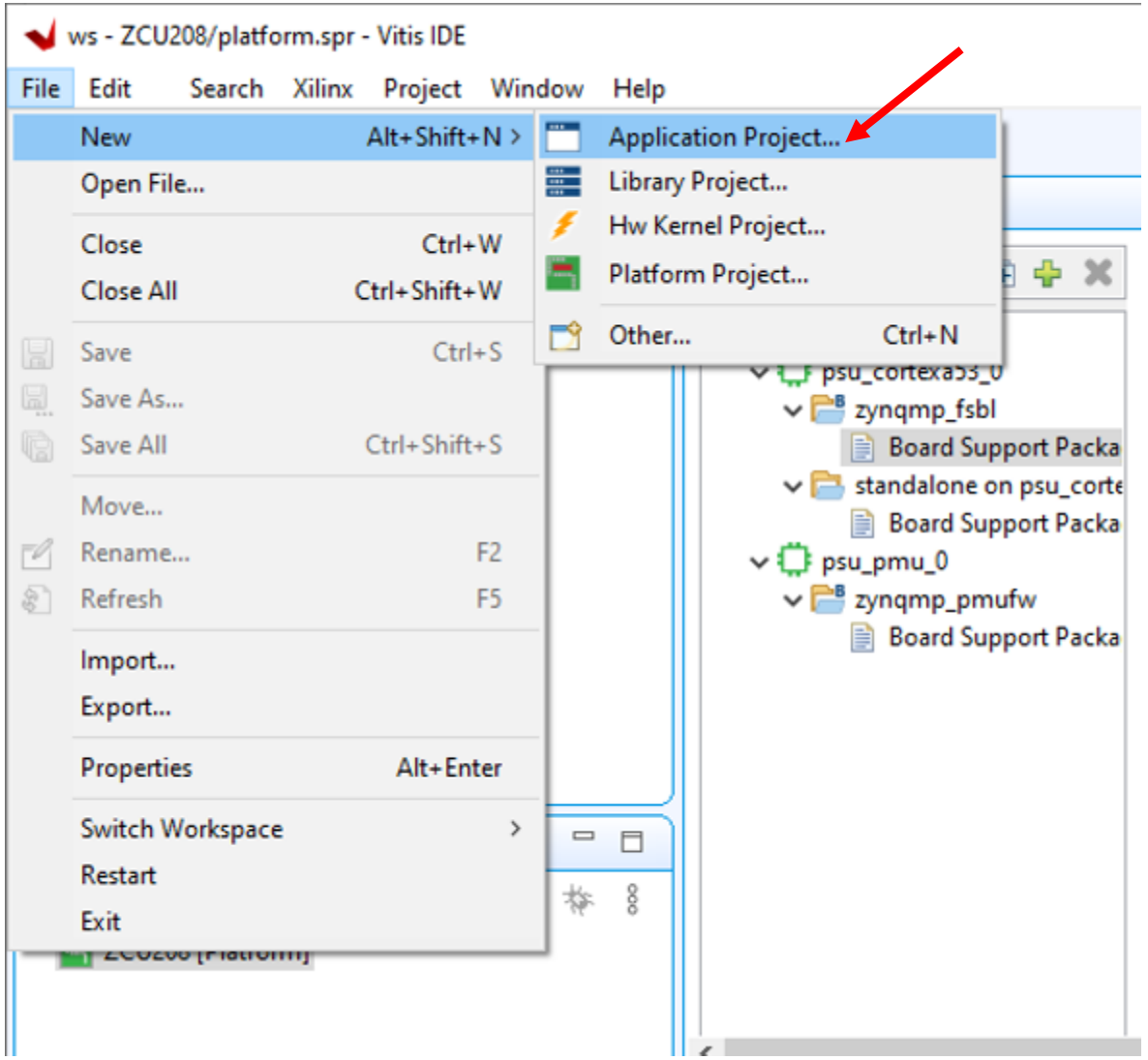
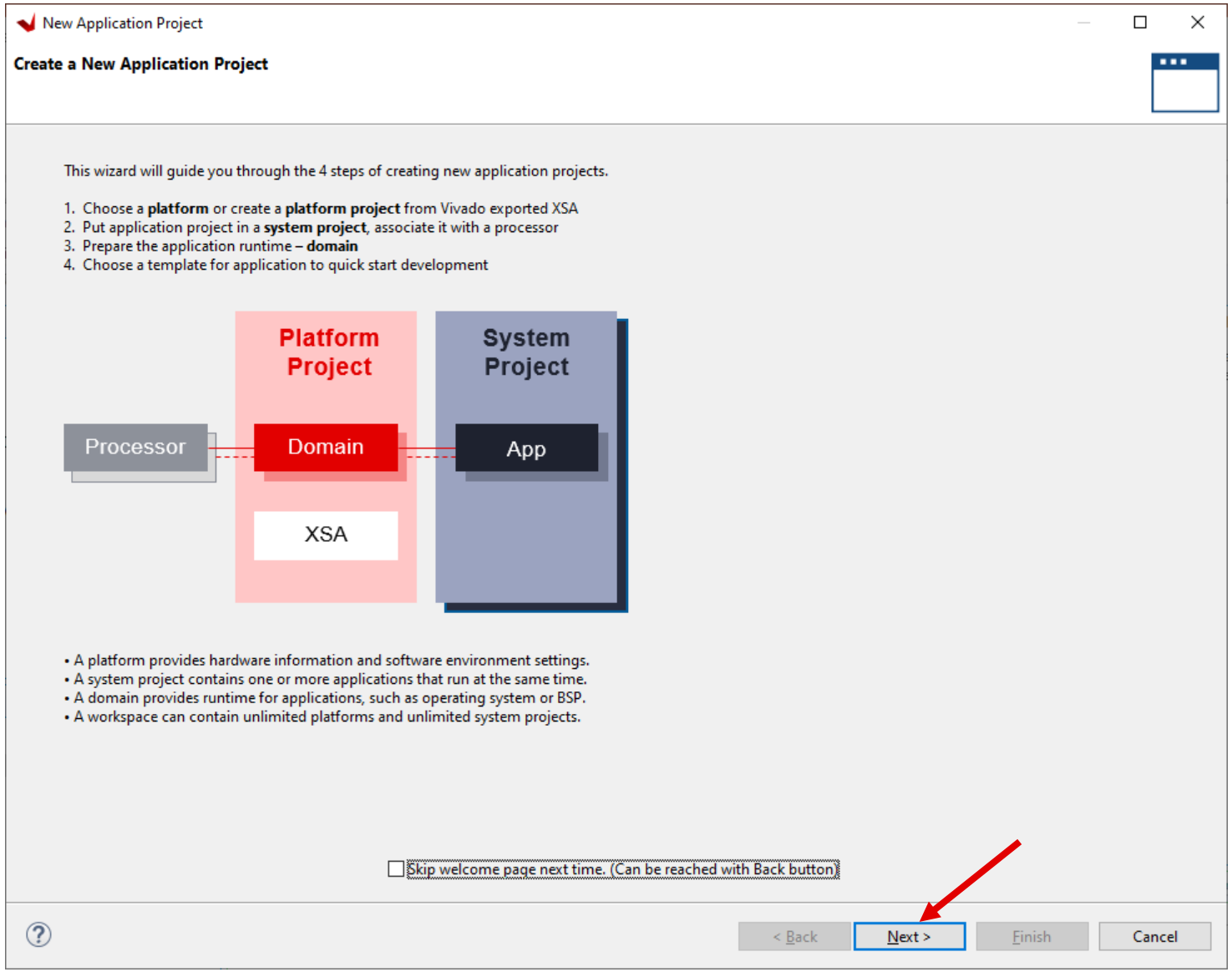
Create Application



Create Application Cont'd



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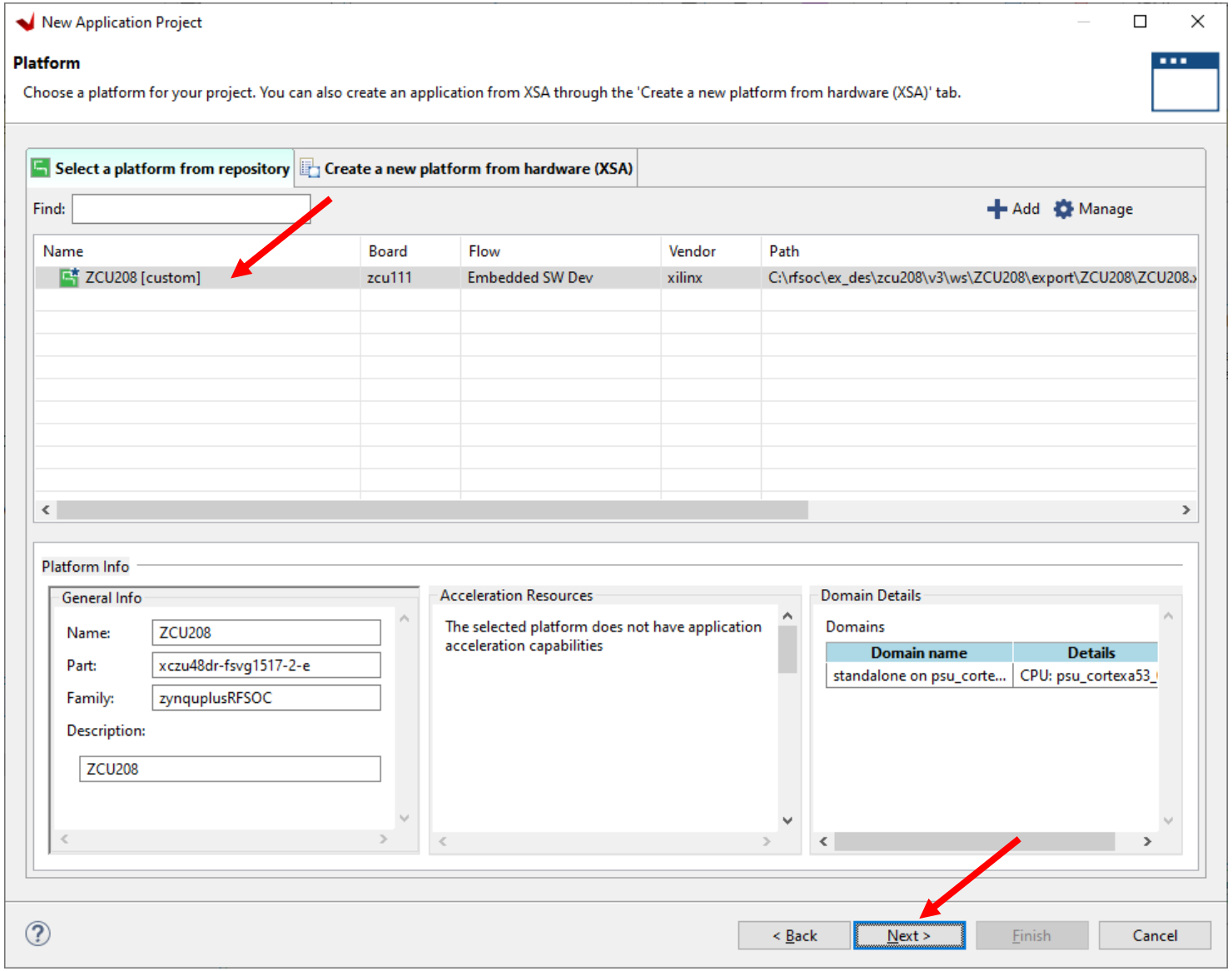
Create Application Cont'd



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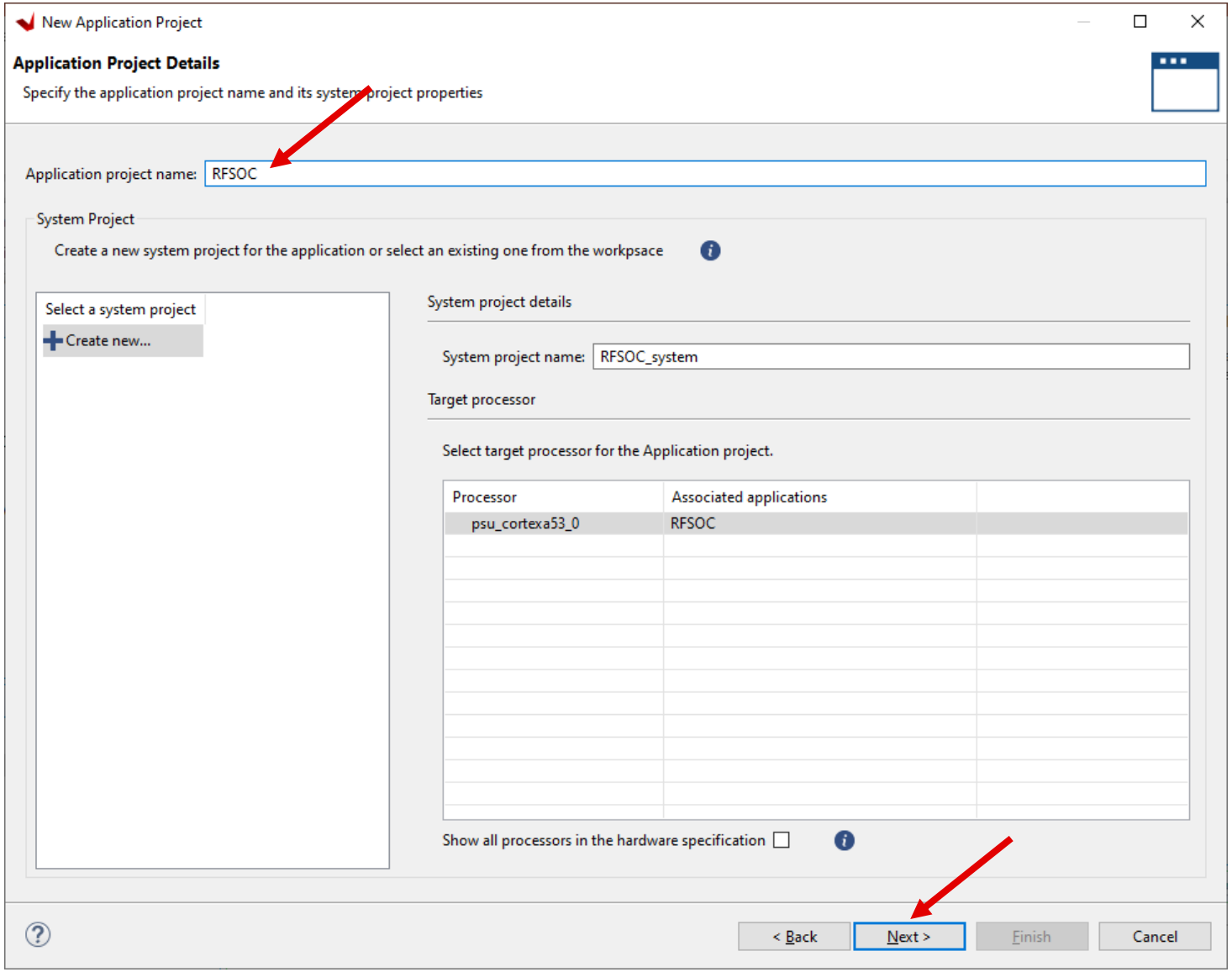

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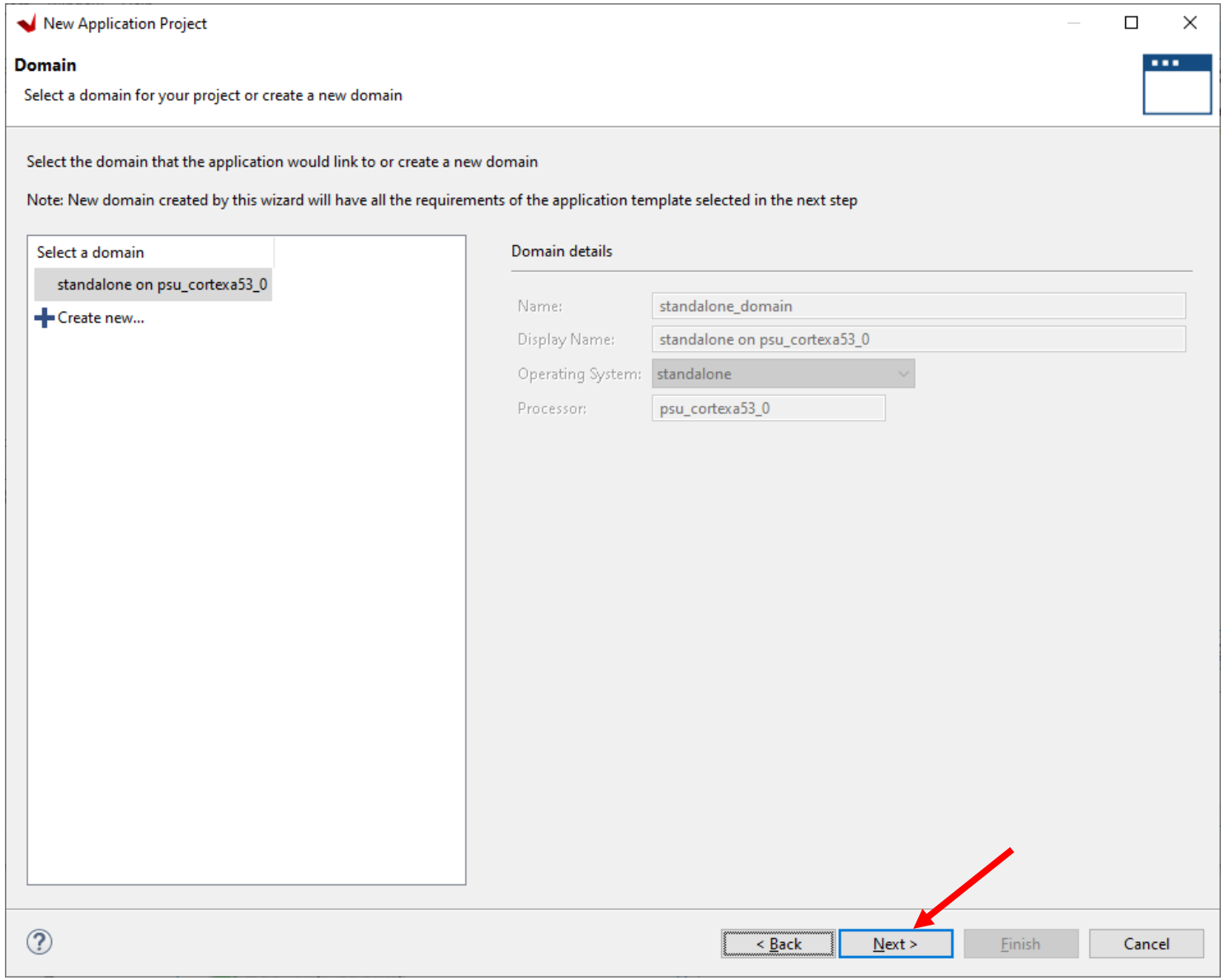

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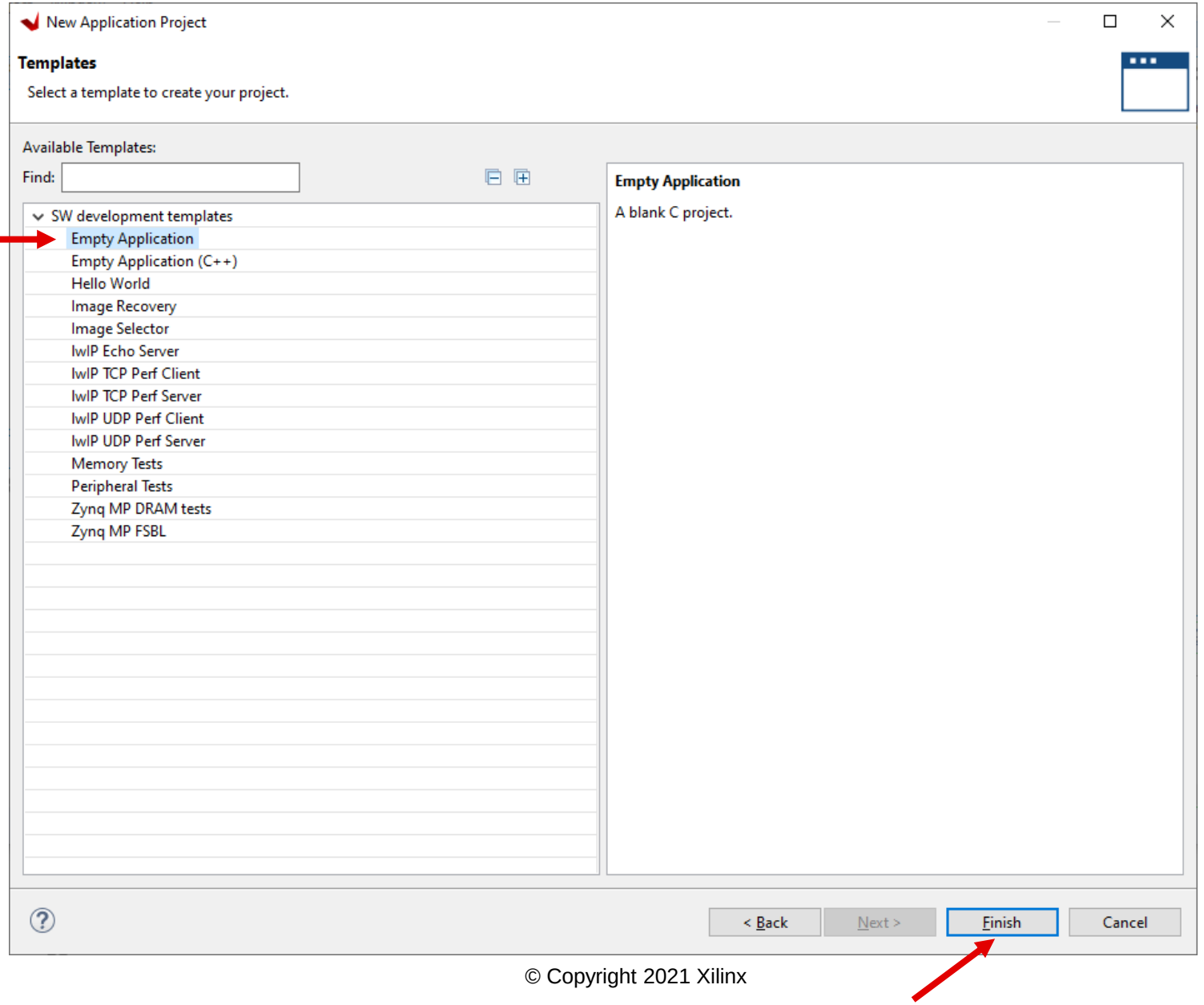

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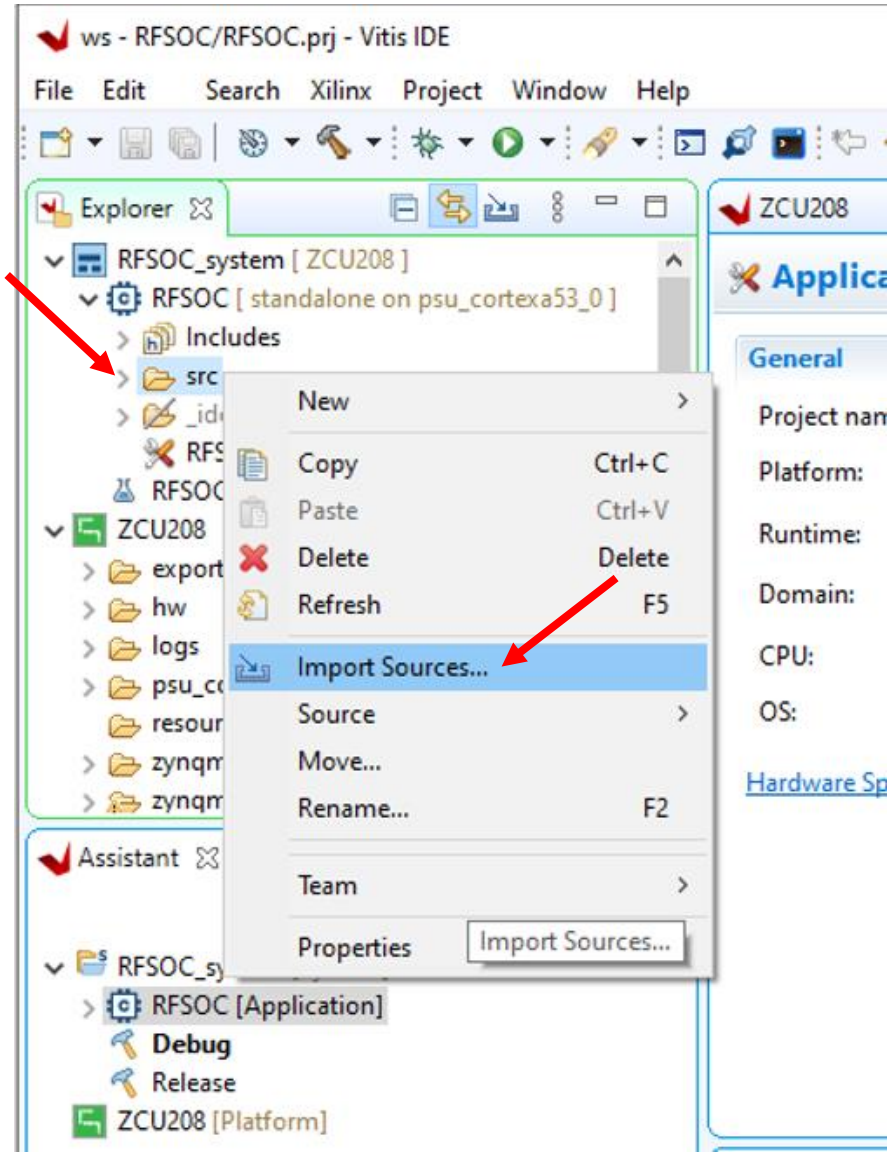
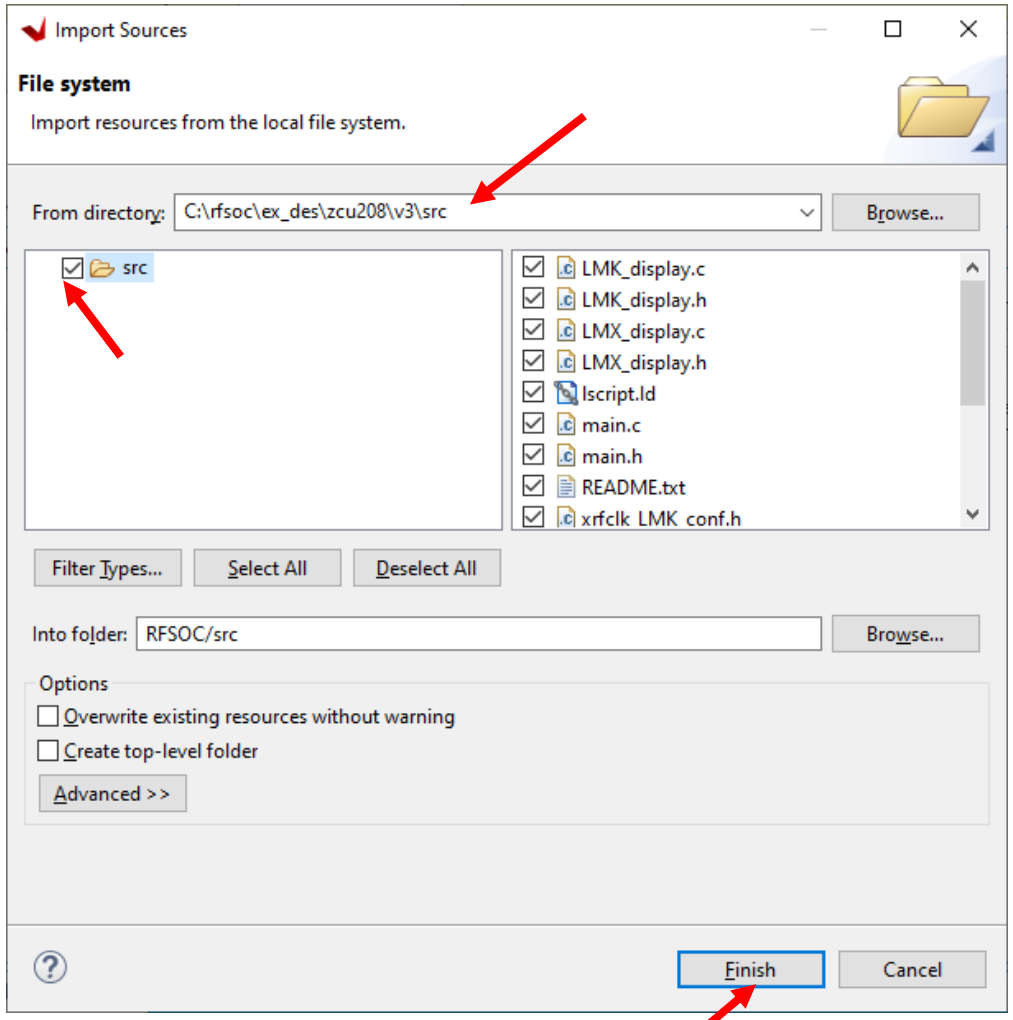
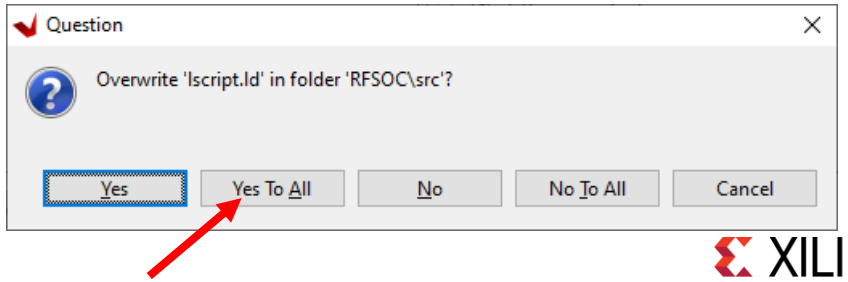
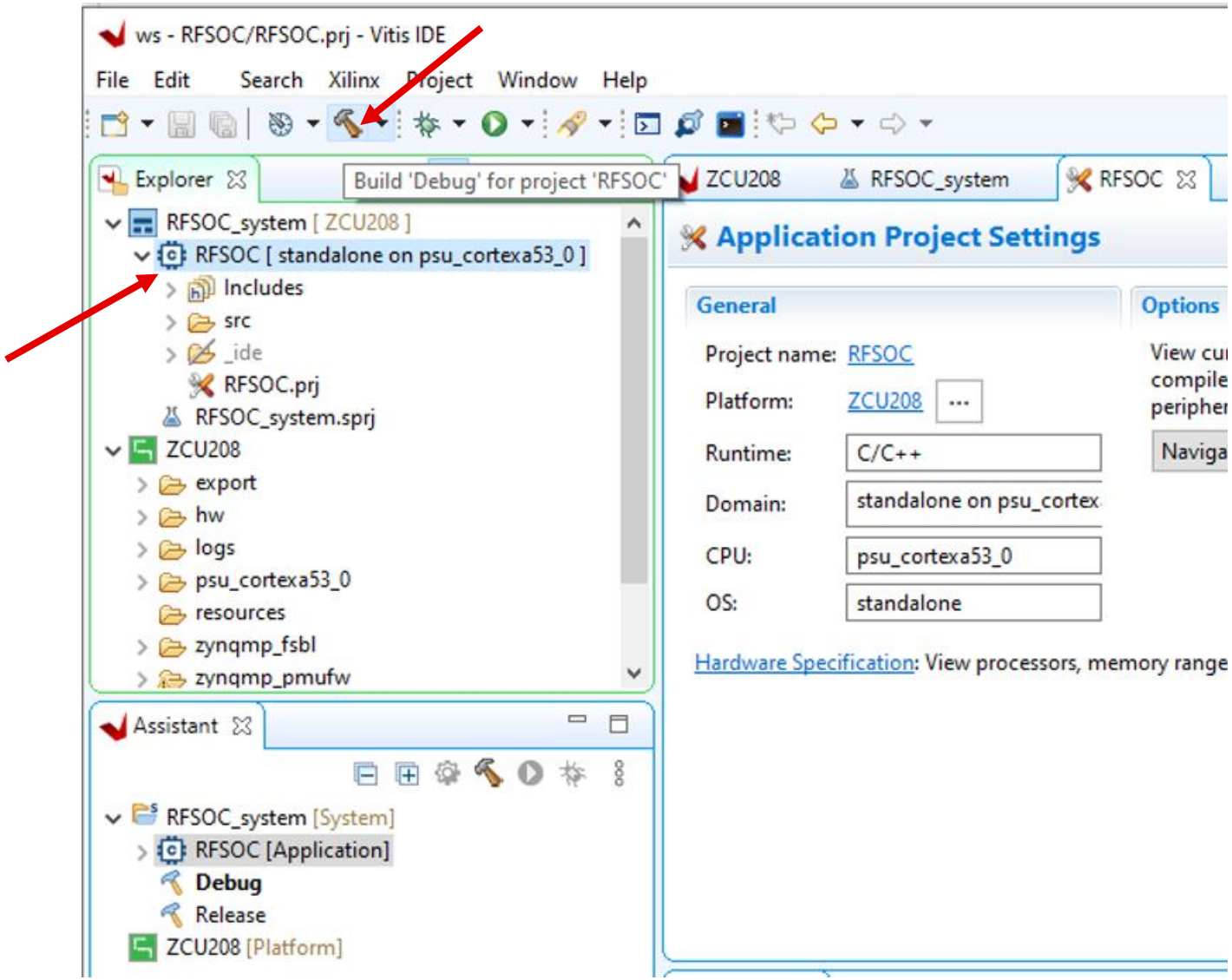
Import Sources



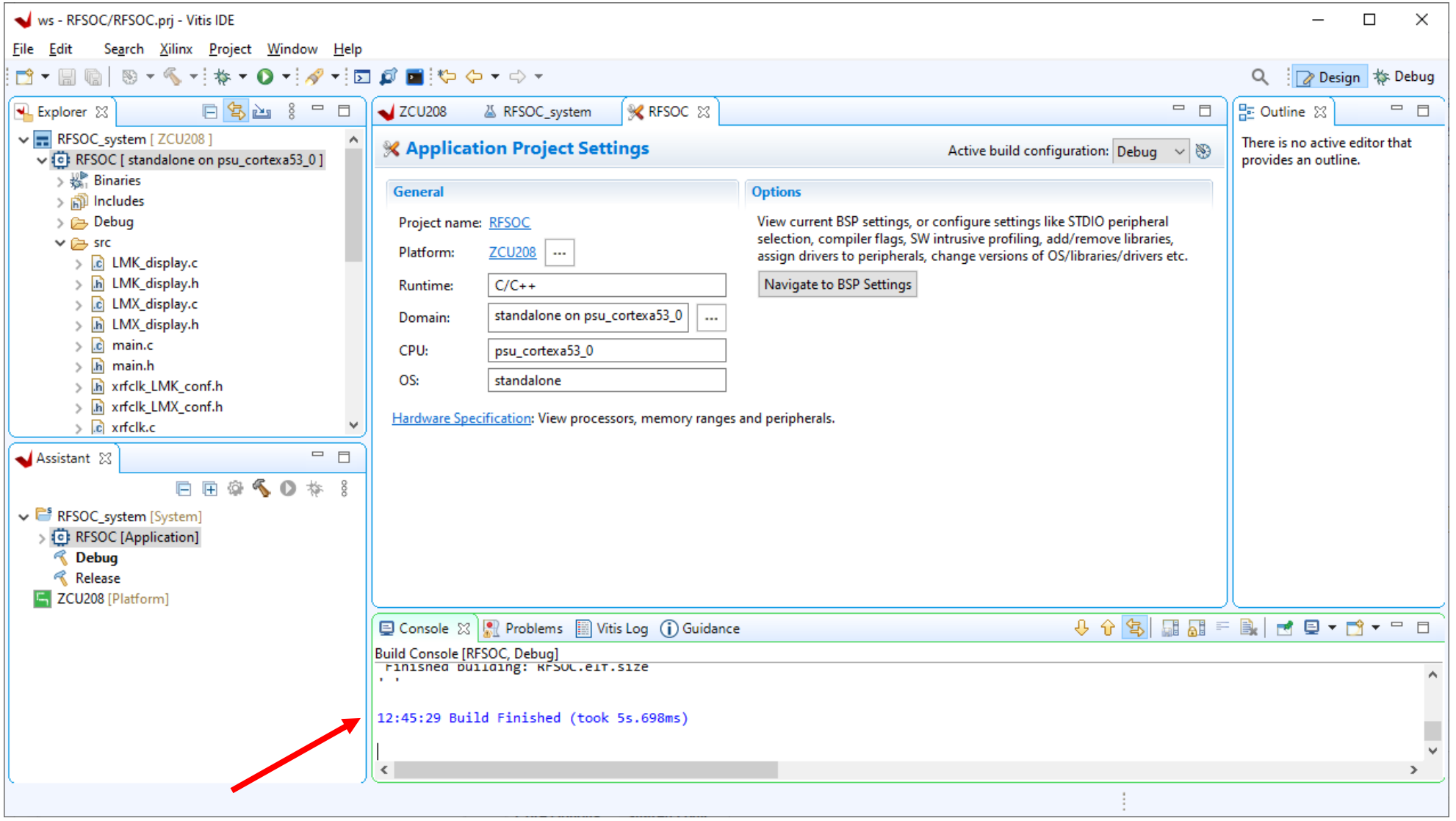




Build Application



Build Complete



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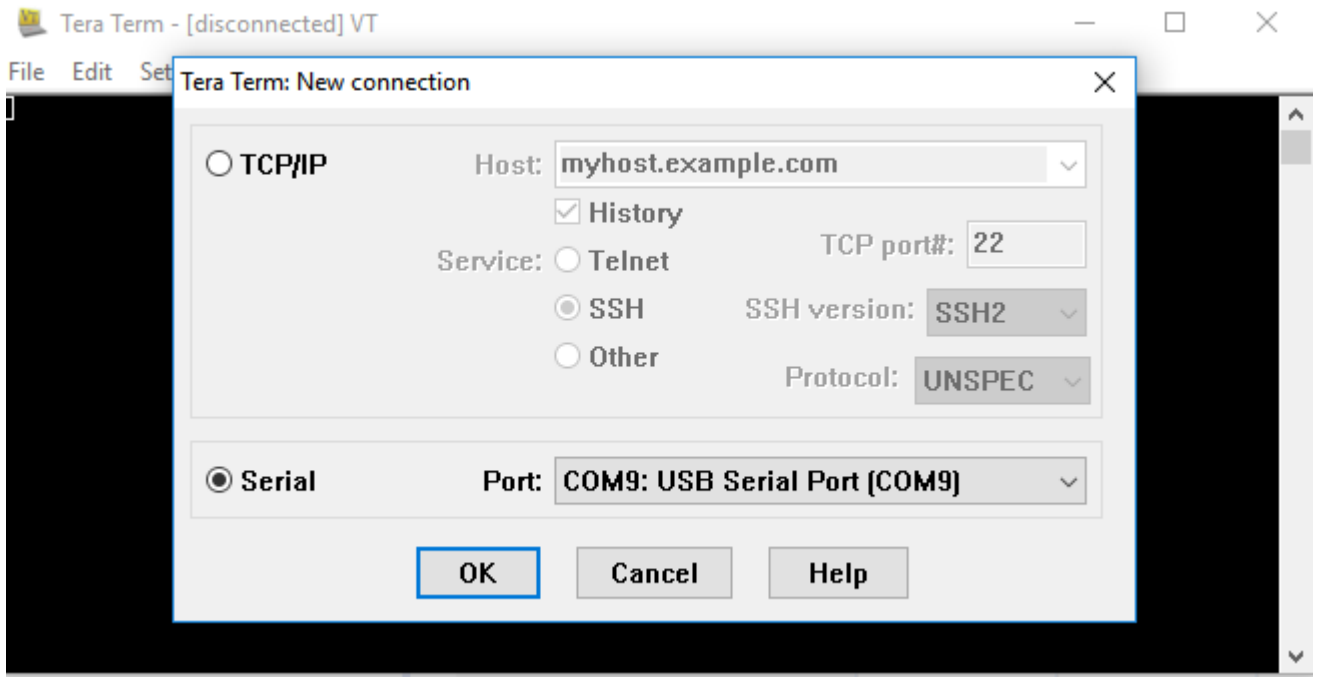
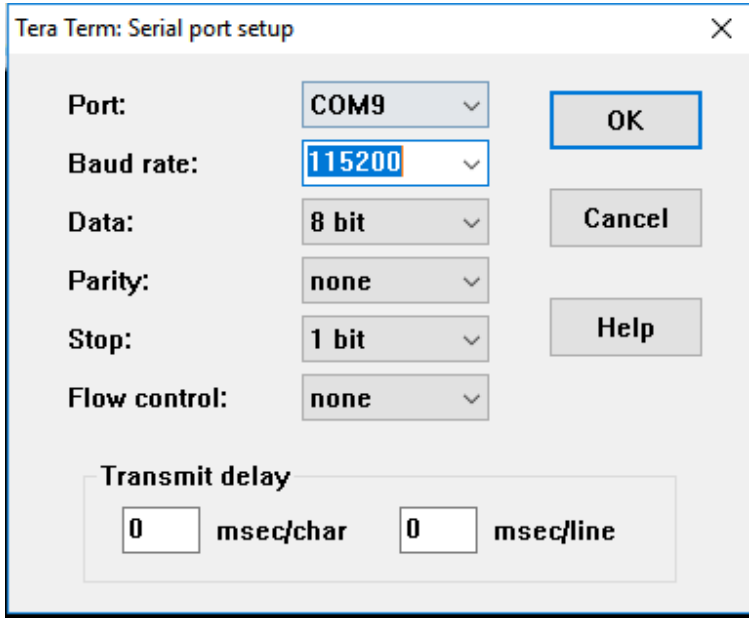
Run Design

Open a Terminal Window

Open the COM port on the compute and set the rate to 115200.

TeraTerm can be used. See UG1036.





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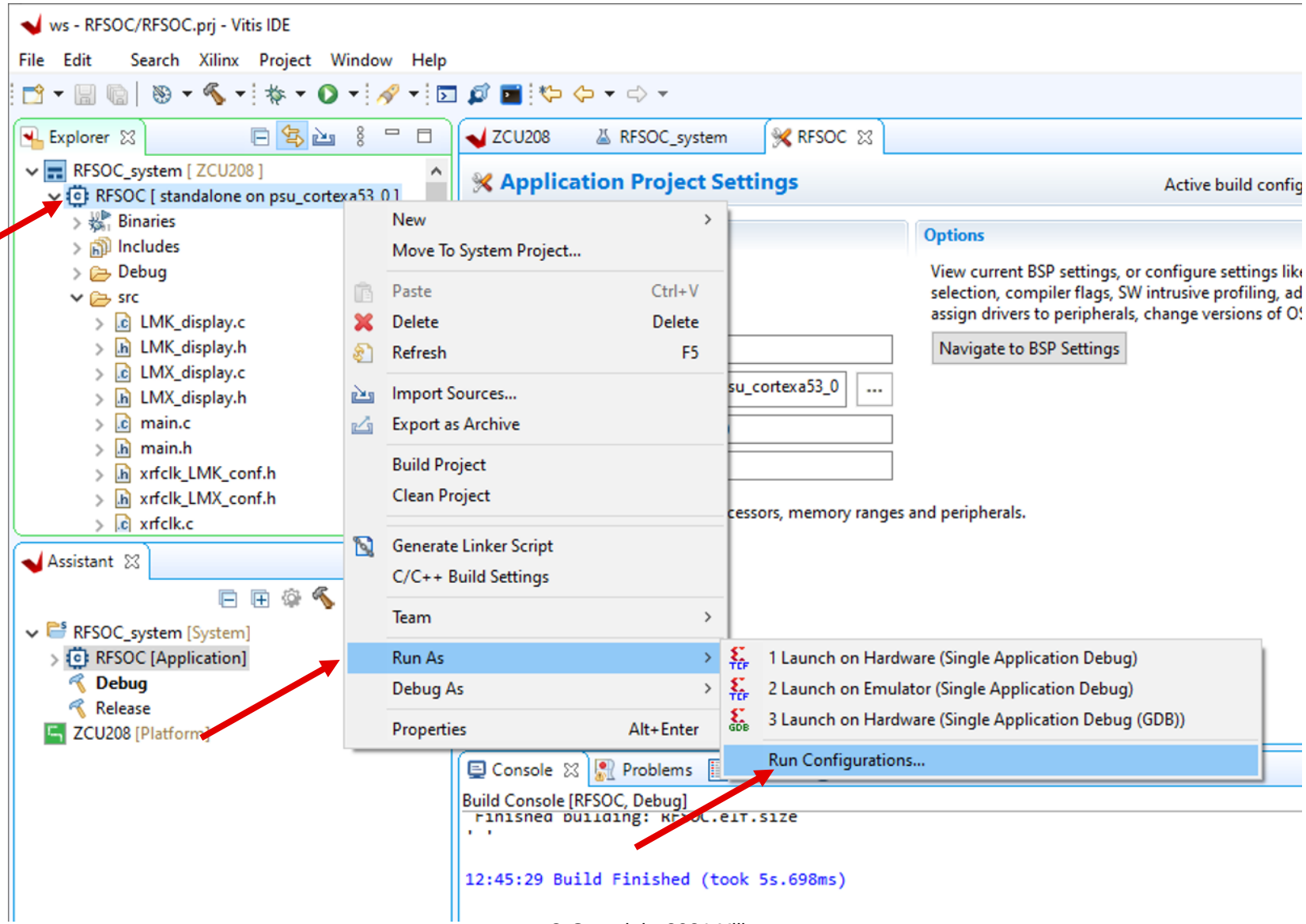
Setup Run Configuration



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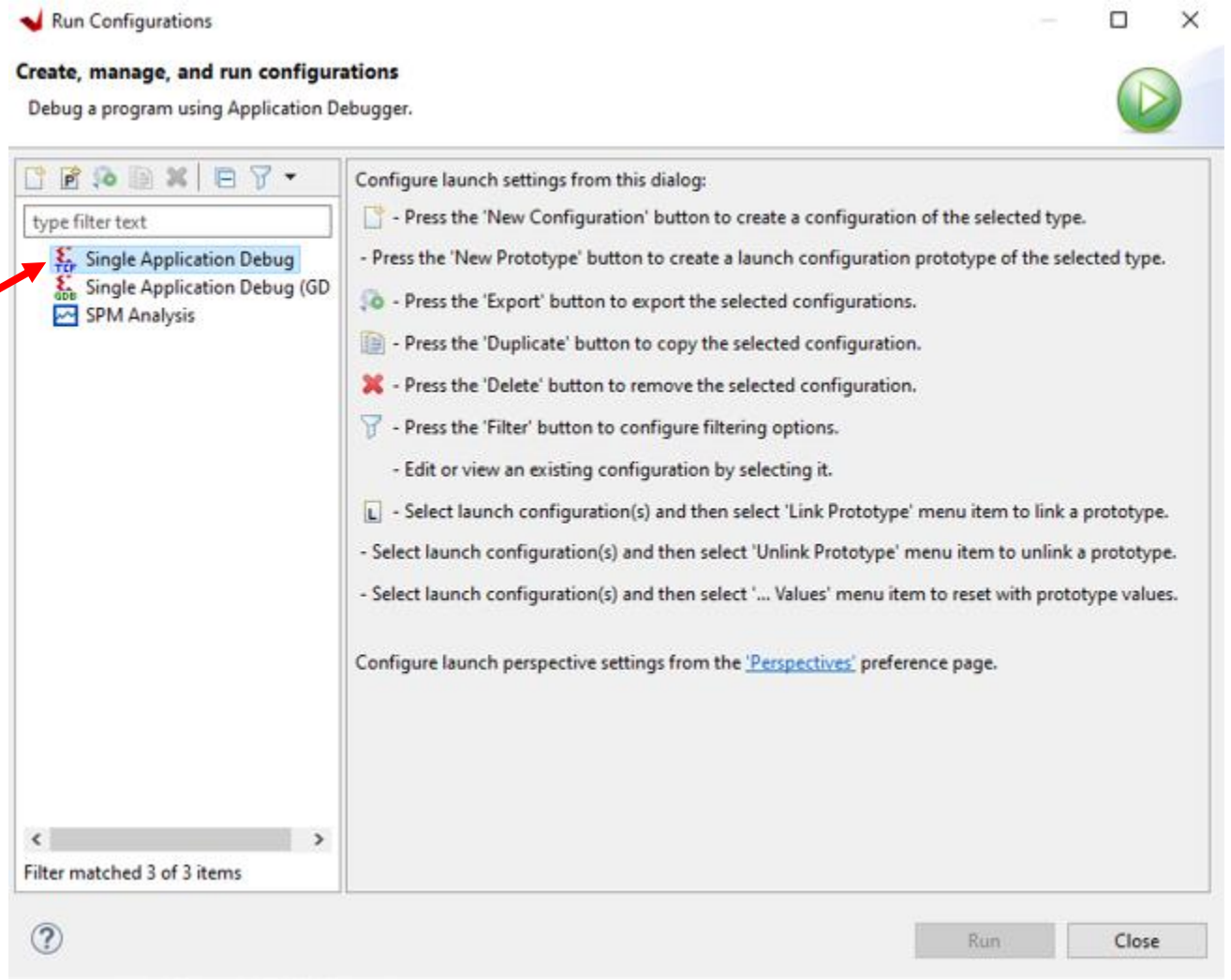
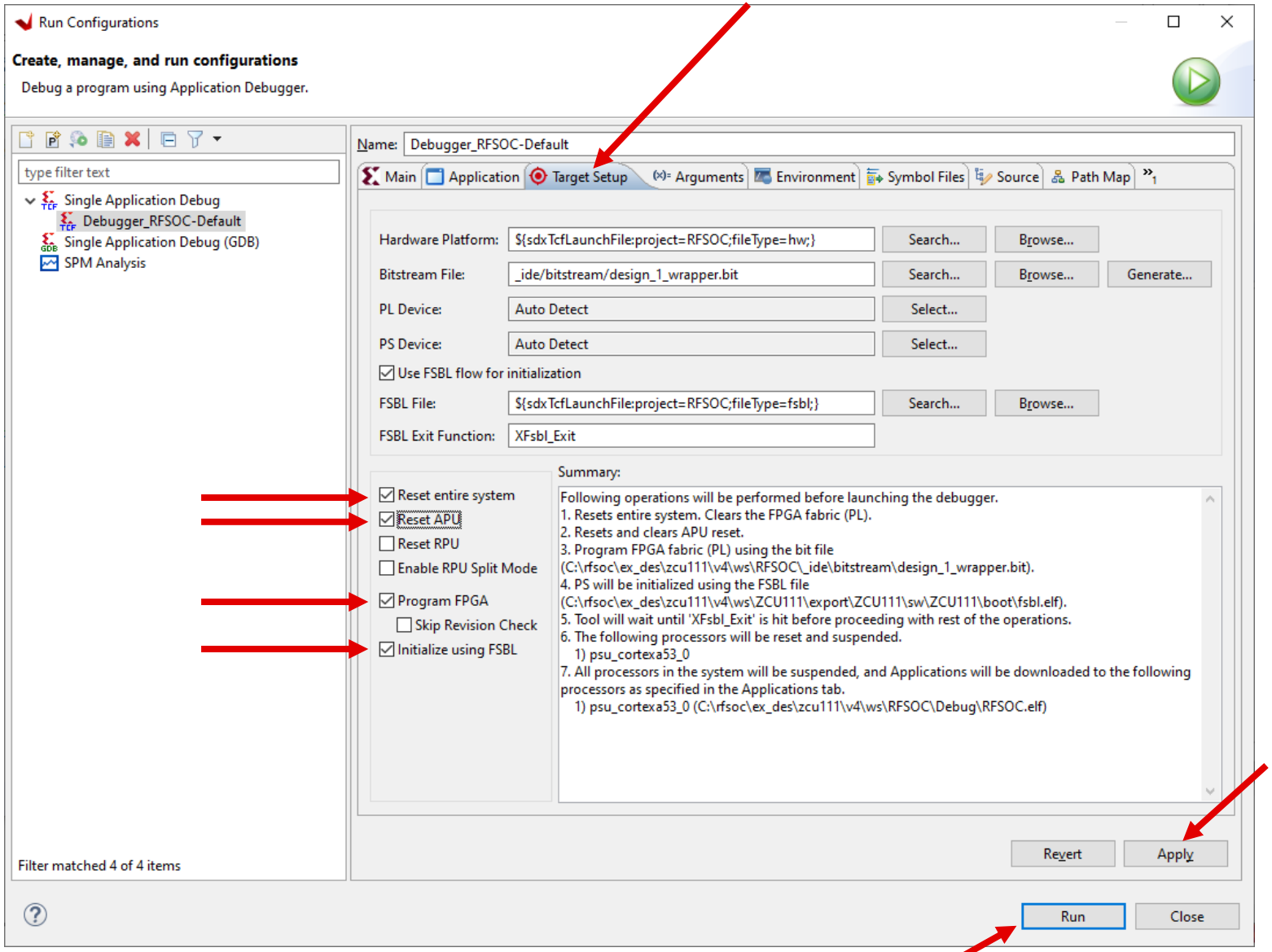
Run Configuration Cont'd

Double Click



Run Configuration Cont'd



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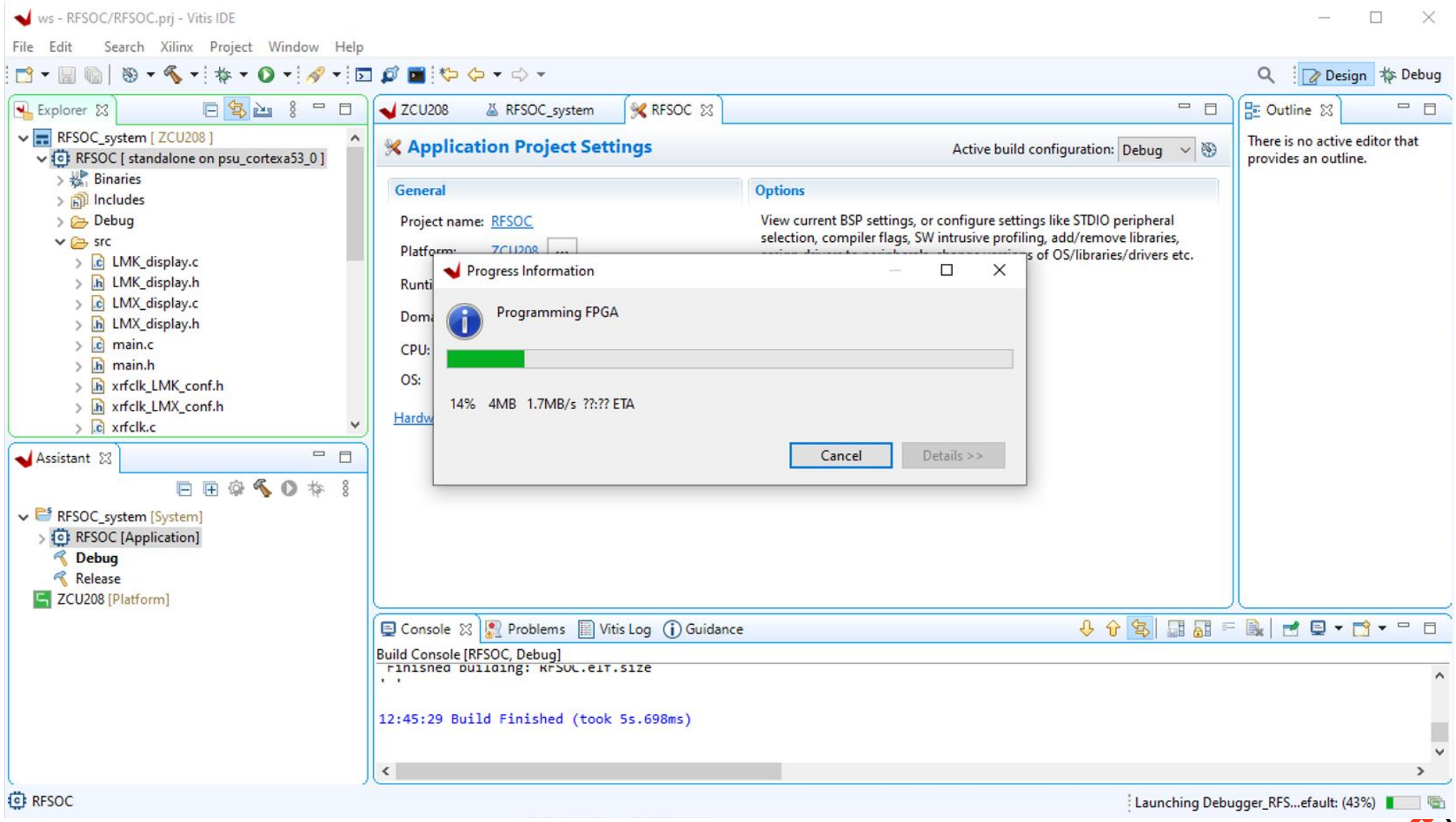
Run Design



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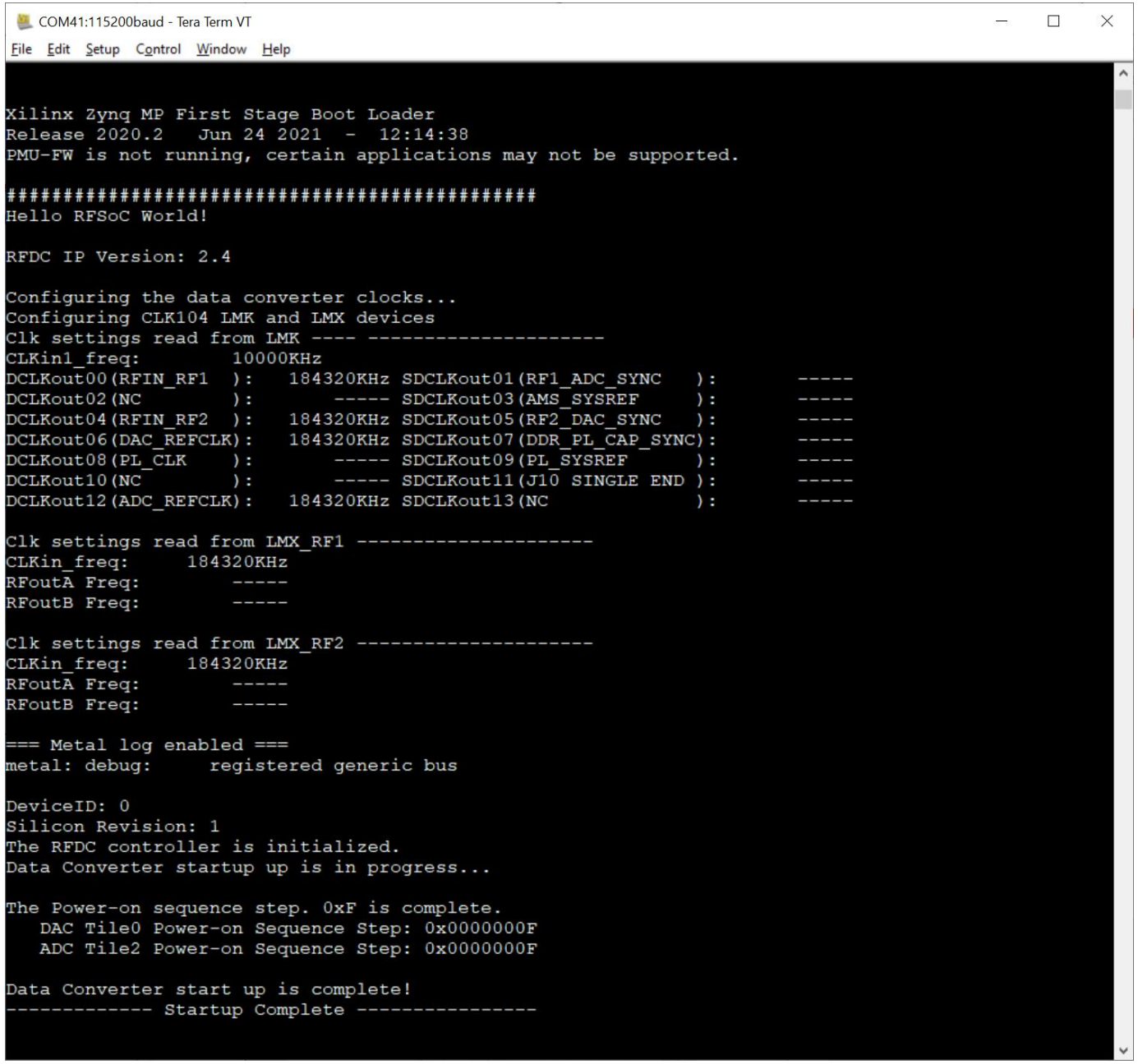
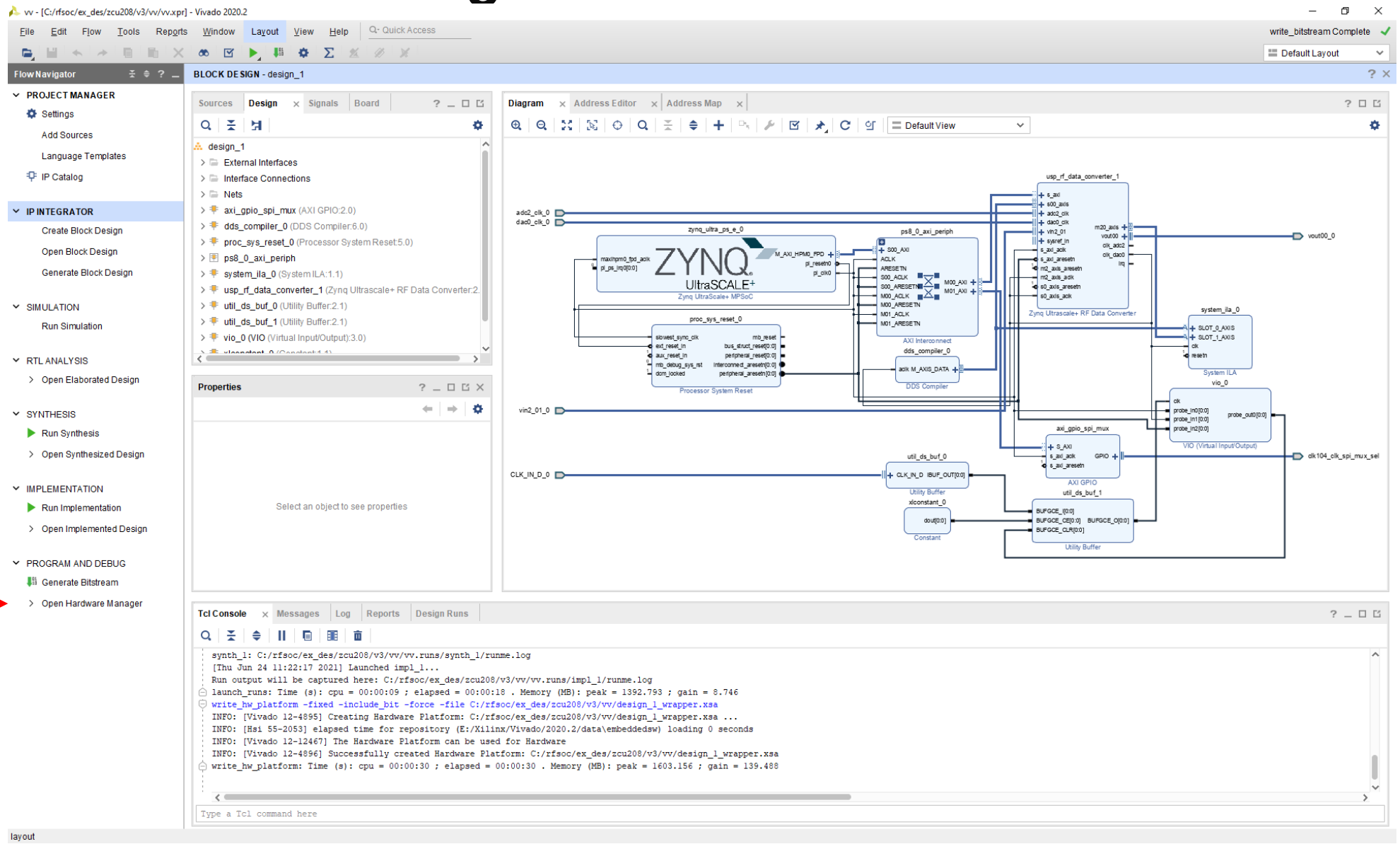
Application Startup

The application…

1. Programs the clocks.
2. Issues the data converters master reset.
3. Displays the Power-on Sequence Step of the data converters.



Open Hardware Manager



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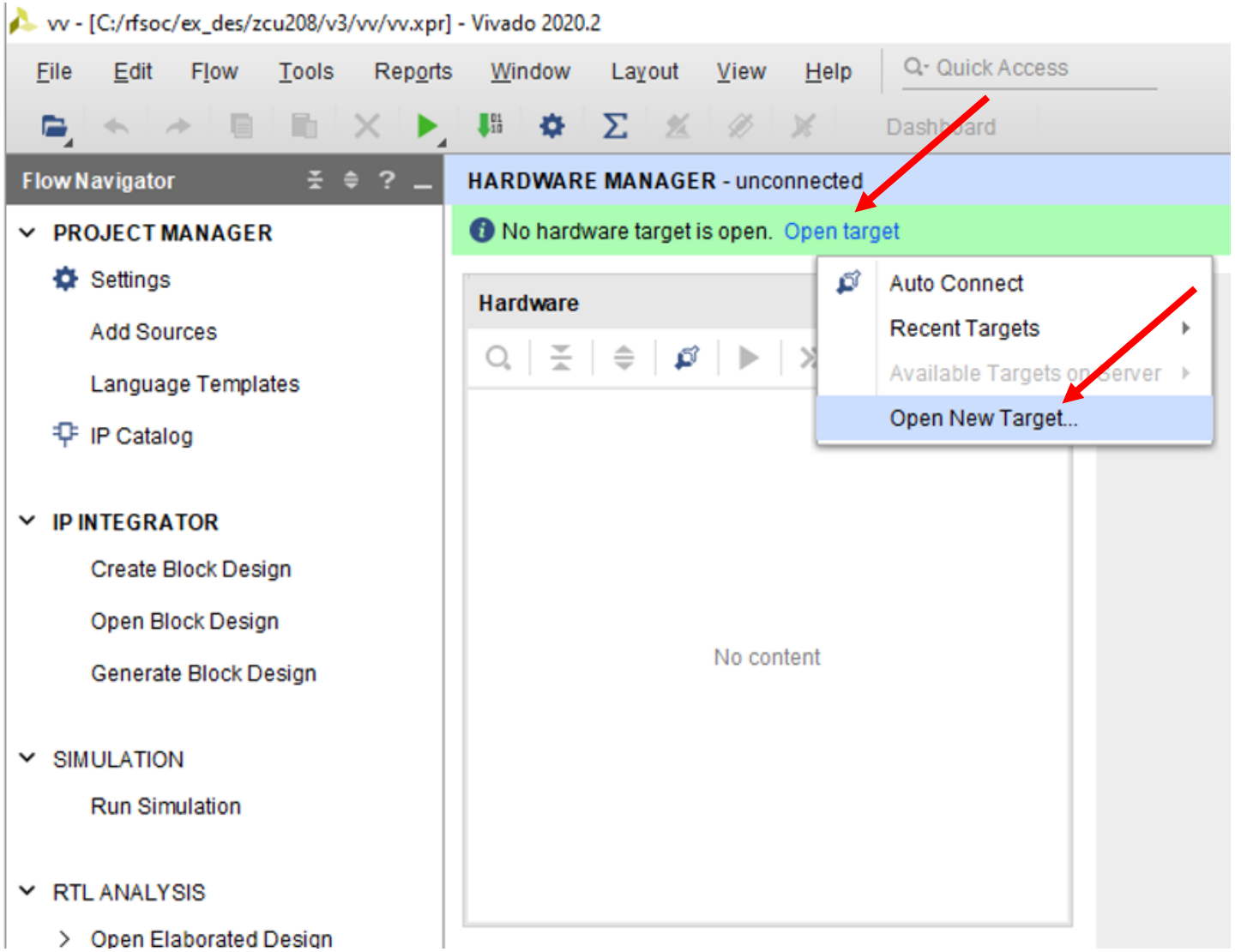
Open New Target



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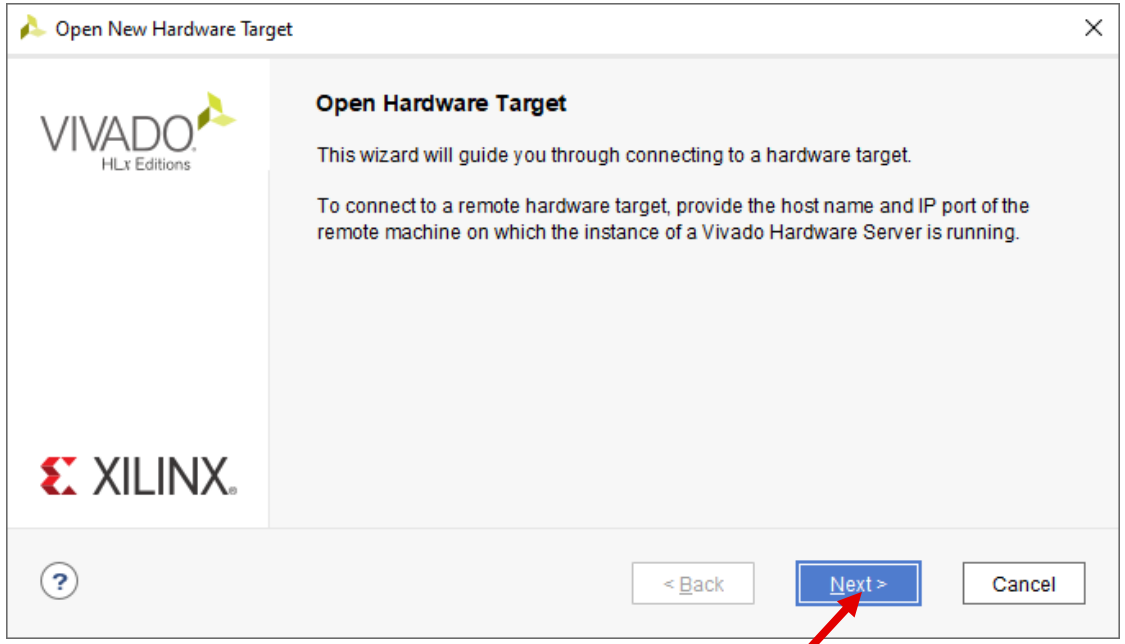
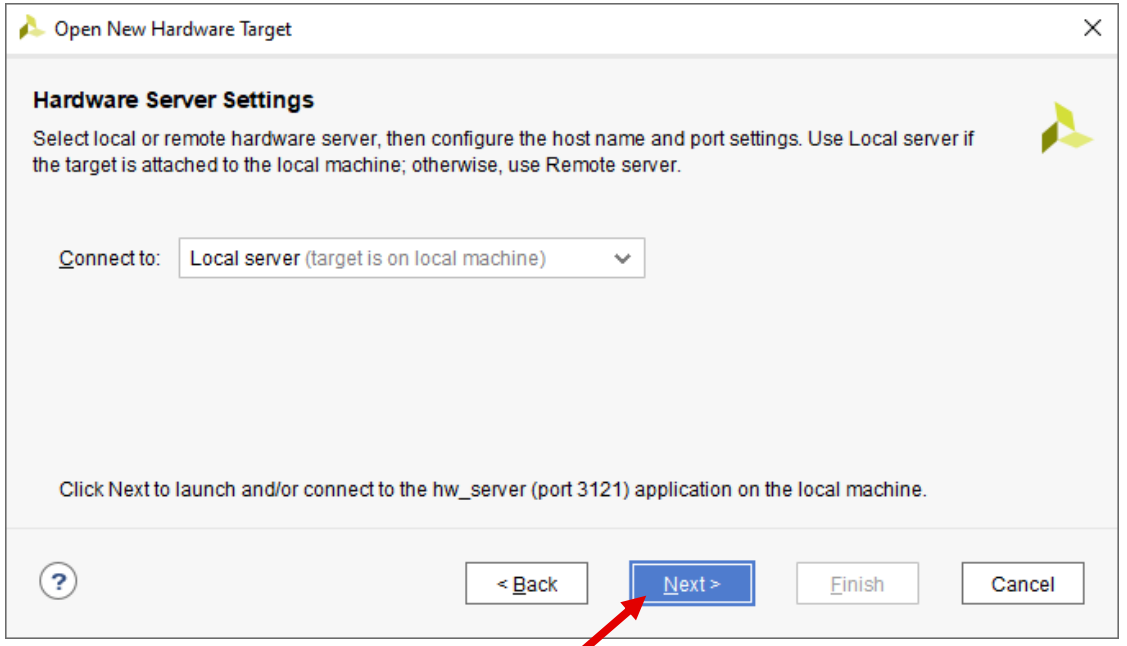
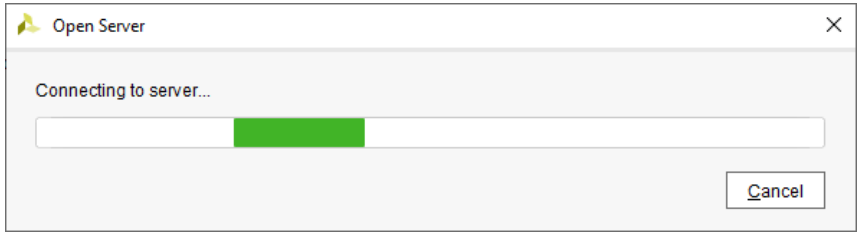
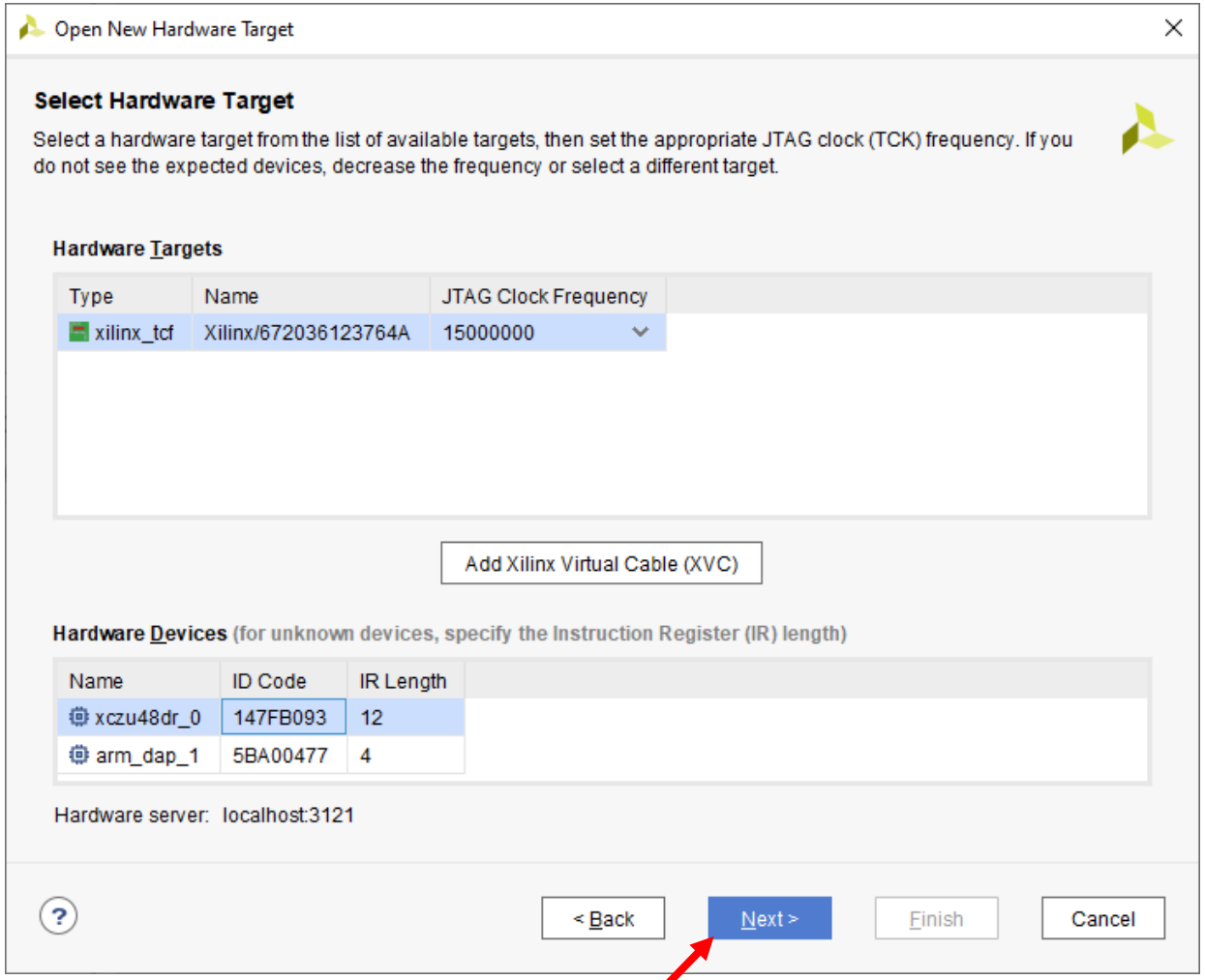
Open Hardware Target

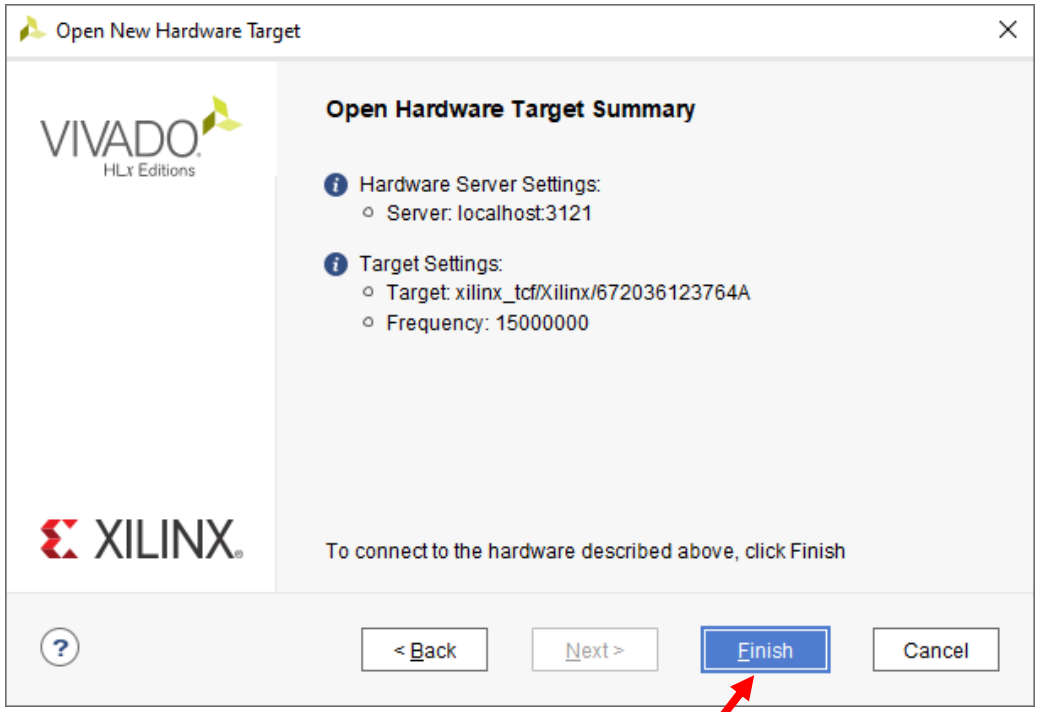


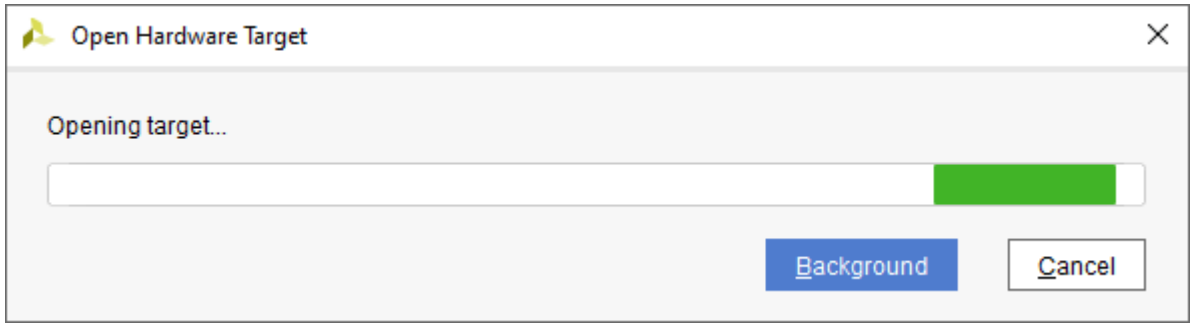




Open Hardware Target Cont'd





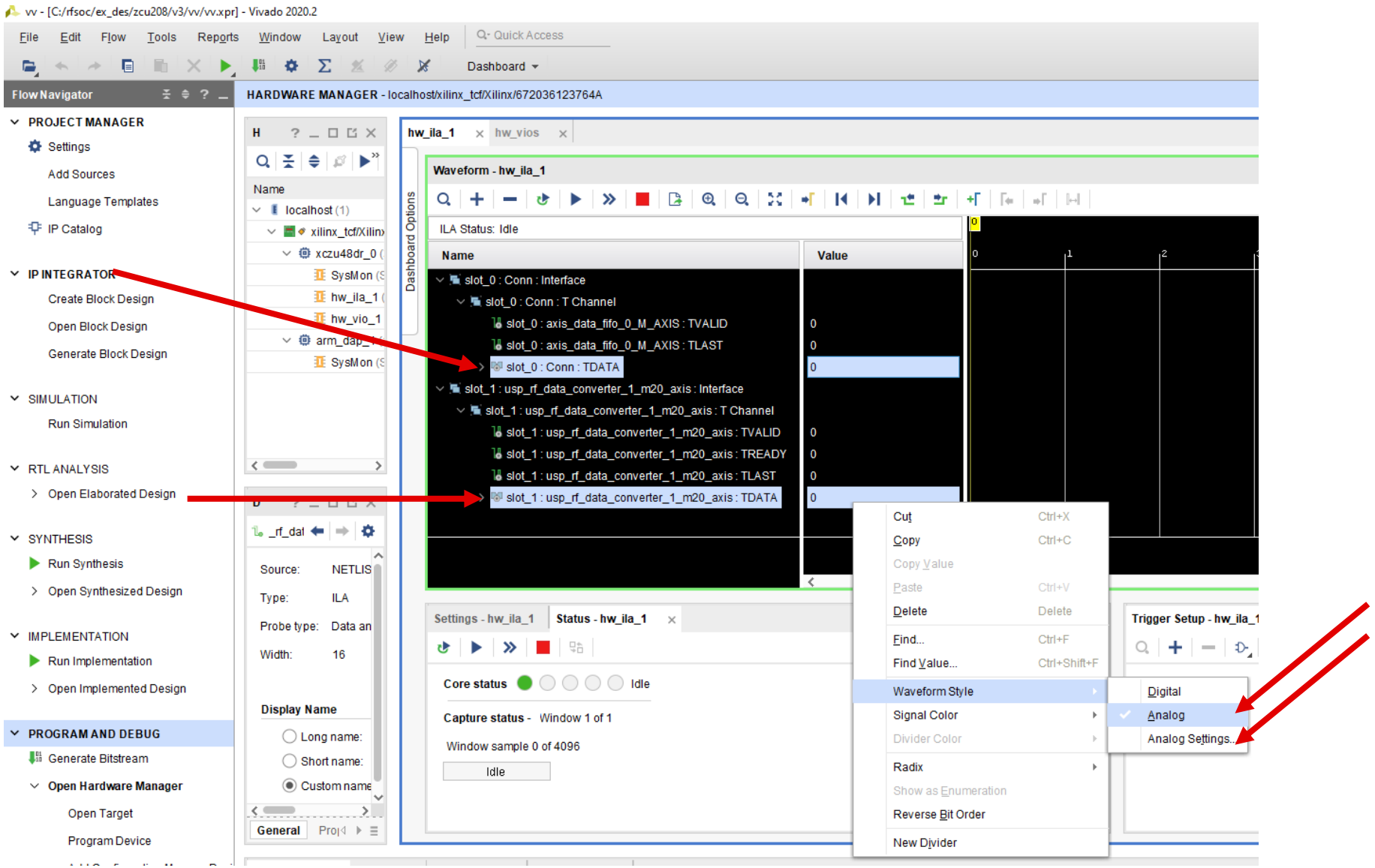


XILINX

Convert Data to the Analog Waveform Style

10MHz sine wave going from the DDS compiler to the DAC.

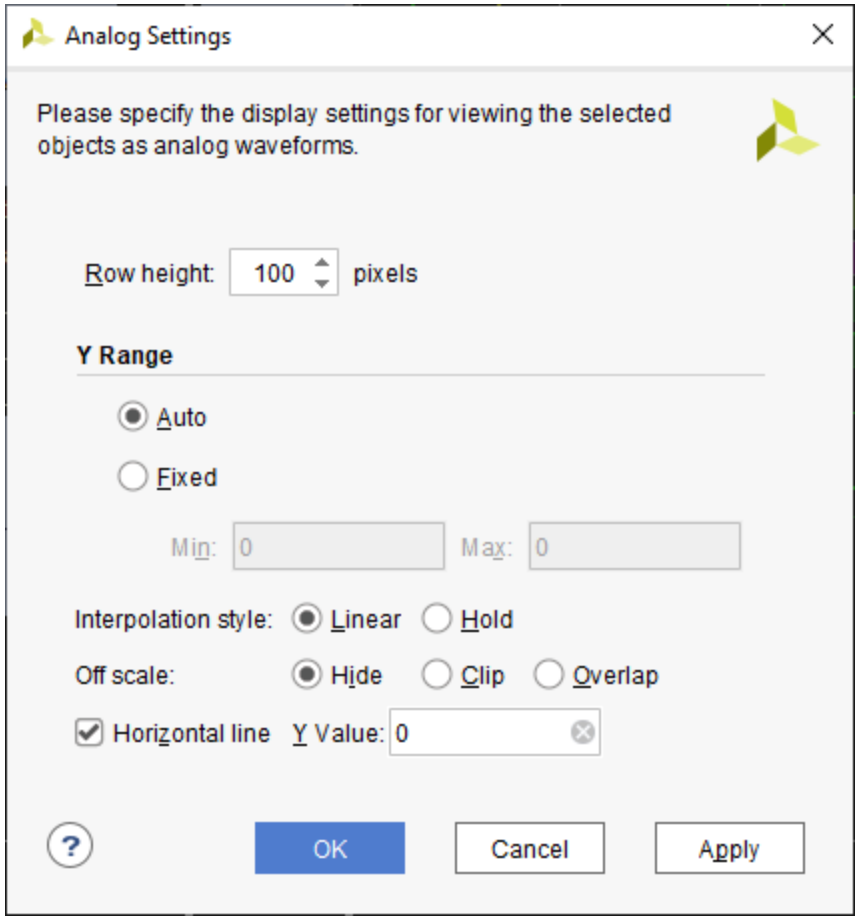
ADC capture to the System ILA.



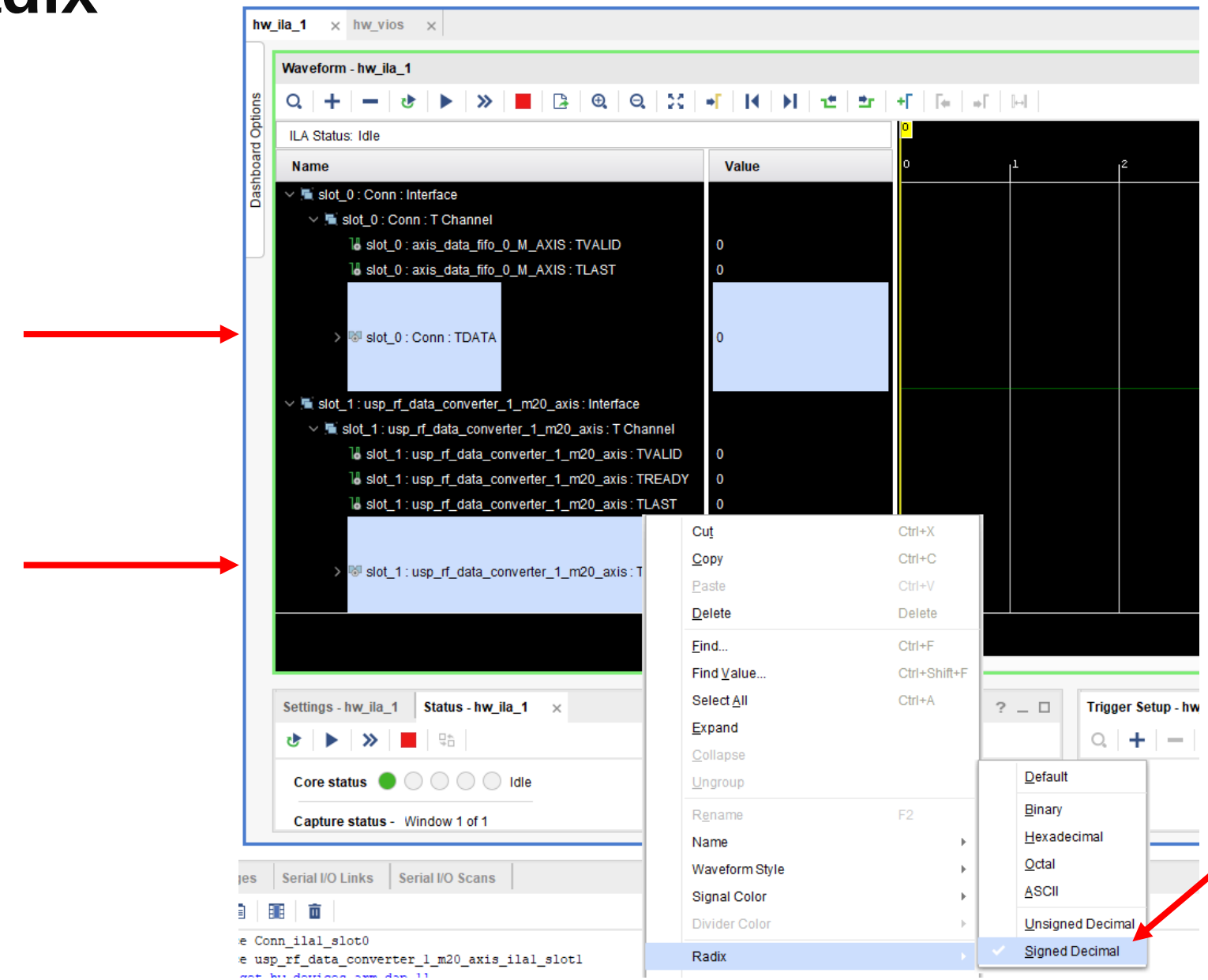
XILINX.

Analog Settings

Set Row height to 100.



Radix



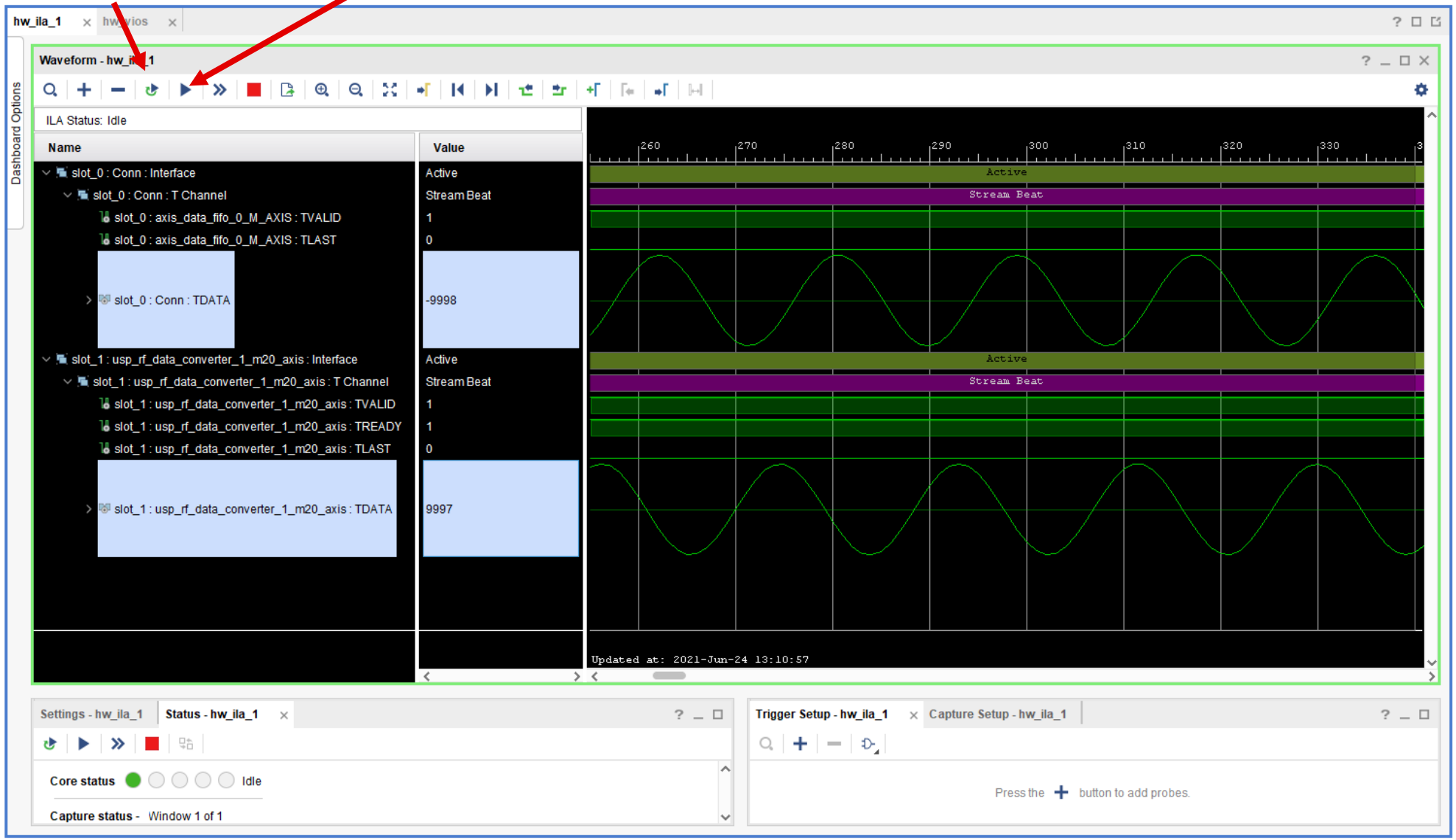
Use Radix of Signed Decimal.

XILINX.

System ILA Capture

Automatically retrigger

Trigger ILA capture

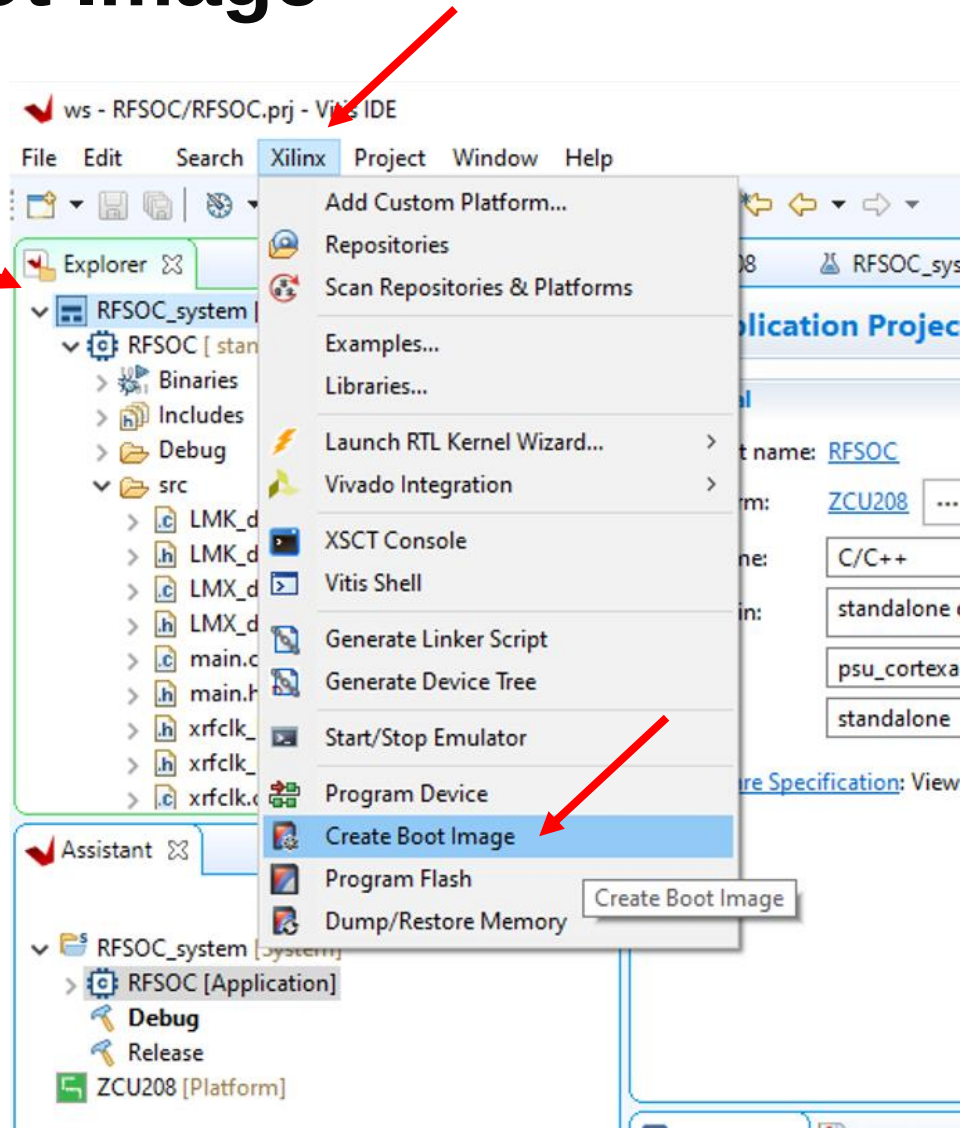


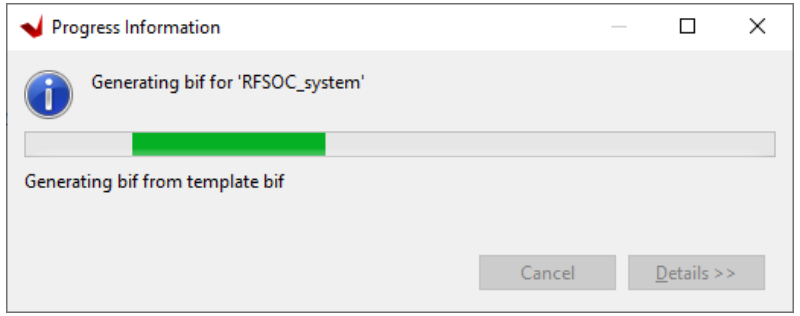
XILINX.

Boot Image

Create Boot Image

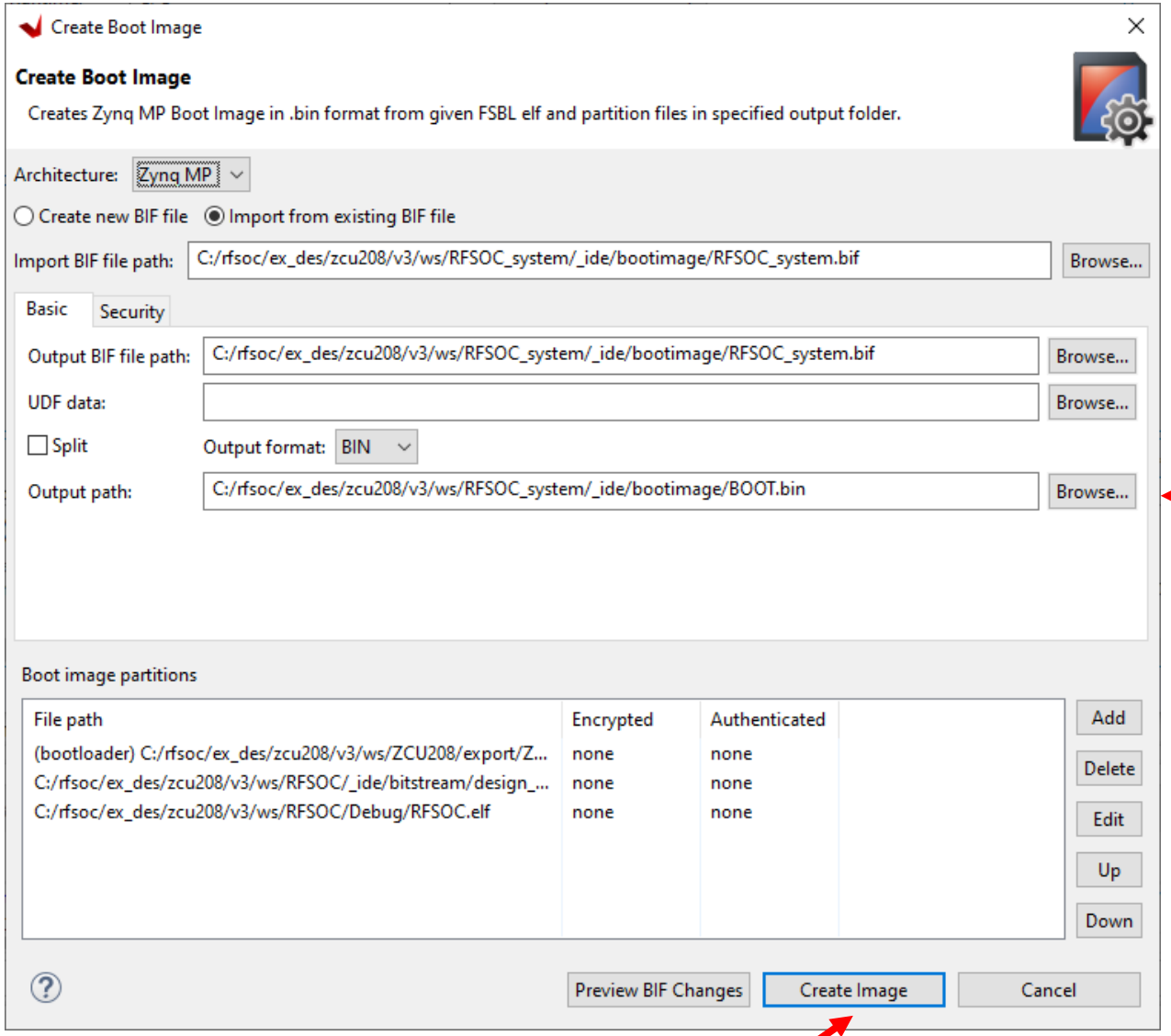
To run the application from the SD card rather than directly from Vitis™, create the boot.bin file.





XILINX.

Create boot.bin File

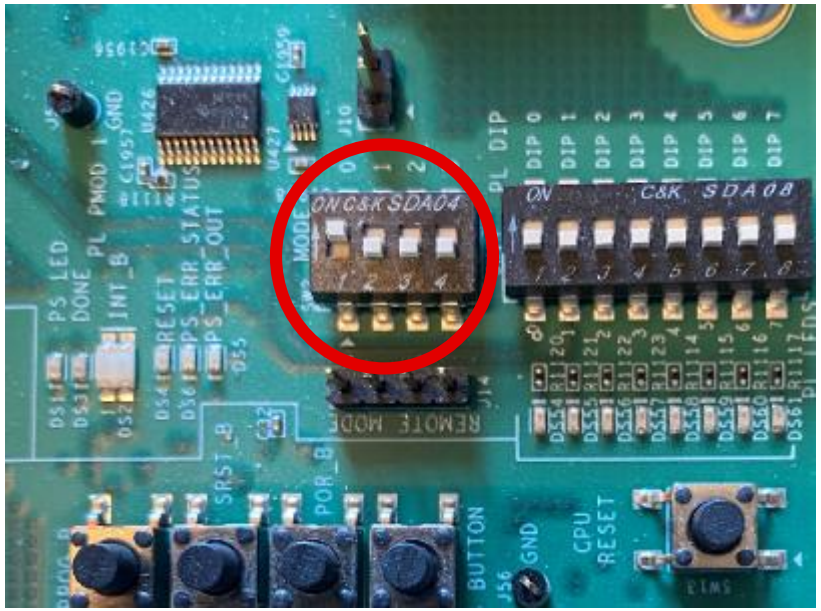


Note the location of the boot.bin file to put at the root level of the SD card.

XILINX.

Boot from SD Card

Set SW2 to on,off,off,off (SD Card boot mode).



Load boot.bin on the SD card, insert it into the board, and turn on the power.

XILINX.

Thank You