

# CoolRunner-II™

## ENABLING PRODUCT DIFFERENTIATION IN THE DIGITAL CONSUMER MARKET



*Product Differentiation: Separating your product from the competition.*

*Enhancing Technology: Adding innovation to existing chipset features.*

*Enabling Technology: Add entirely new features to open new markets.*

# XILINX. THE LEADER IN PROGRAMMABLE LOGIC.

## DESIGNERS PREFER COOLRUNNER-II CPLDs.

Based upon both supplier and component criteria, designers choose Xilinx as a preferred vendor for low-power CPLD products. Weighing competitors not only by price, but by reputation of product, delivery, quality, and attention to special needs, Xilinx comes out on top.

According to HTC, the device features were what tipped the scale. Not only did the base power consumption meet or exceed power budgets, but key low-power enhancements played a large role in part selection. "HTC has received a substantial amount of performance capabilities in Xilinx products," said Peter Chou, HTC's president. "Their combination of leading-edge technologies, complete programmable system design, and full technical service support are essential to the success of HTC."

## TOC

<b>The Benefits of CPLDs</b>	3
<b>Handsets</b>	
Pocket PC/Phone with Keyboard	4
DataGATE Blocking	4
Cell Phone with Camera Zoom	5
PocketPC/Phone	5
Handset Application Note Support	6
<b>Portable Consumer</b>	
GPS Unit	7
PDA Device	7
Portable Satellite Radio and MP3 Player	8
Alcohol Analyzer	8
<b>Wired Consumer</b>	
Digital Music Box	9
Digital Wireless Interface	9
Photo Printer	10
Logic Consolidator	11
<b>Documented Xilinx CPLD Applications</b>	
Digital Media Player	12
Digital Camera	12
<b>Memory Control</b>	
Compact Flash Card Interface and Control	13
SD Card Interface	13
SDRAM Controller	13
<b>Display Interface</b>	
LED Driver Block	14
LCD Module	14
Level Shifting	15
Microcontroller Interface	15
Serial Peripheral Interface Master	15
<b>CoolRunner-II Advance Features</b>	16
<b>Industry's Lowest Power CPLD</b>	17
<b>CoolRunner-II CPLD Selection Guide</b>	18
<b>Take the Next Step</b>	19

# WHY DESIGNERS ARE USING COOLRUNNER-II CPLDs

## THE BENEFITS OF XILINX COOLRUNNER-II CPLDs

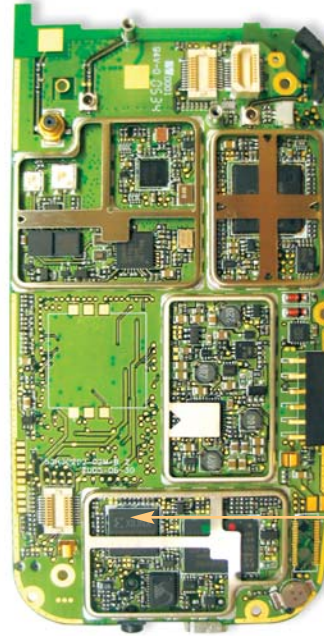
### Much more than logic and flip-flops

- **Product Differentiation.** Separating your product from the competition
  - Enhancing technology: adding an innovation to existing chipset features
  - Enabling technology: adding entirely new features to open up new markets
  - Increase brand awareness: give your product something memorable
- **Low Power RealDigital Advantage**
  - DataGATE: lower power; requires no external devices
- **Flexibility**
  - Easily integrate the components that best meet your needs
  - Support modular configurations
  - Easy System Customization
- **Time-to-Market Advantage**
  - Free efficient and proven development tools (WebPACK)
  - Standard off-the-shelf components
  - Free Reference Designs
- **Fully Programmable and Re-Programmable**
  - Reduced exposure to risk, bugs, component shortages, evolving standards
  - Field upgradeable hardware
- **System Cost Management**
  - Logic consolidation: reduce the number of devices in your design
- **Efficient Life-Cycle Product Management**
  - Extremely effective at enabling derivative designs
  - Exploit market opportunities before your competition
  - Expand the market base of your ROI
- **Combine Functionality**
  - Level Shifting and I/O Pin Expansion and Logic Consolidation
  - Keypad scanner and other features in one device

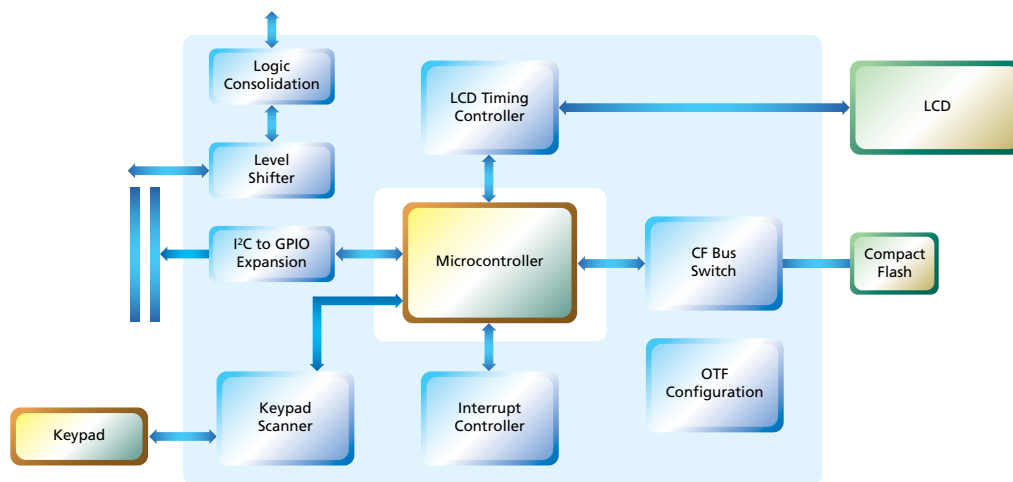
# HANDSETS

## POCKET PC PHONE

- DataGATE
- Level Shifter
- I<sup>2</sup>C to GPIO Expansion
- OTF Configuration
- Interrupt Controller
- CF Bus Switch
- Keypad Scanner
- LCD Timing Controller
- Logic Consolidation

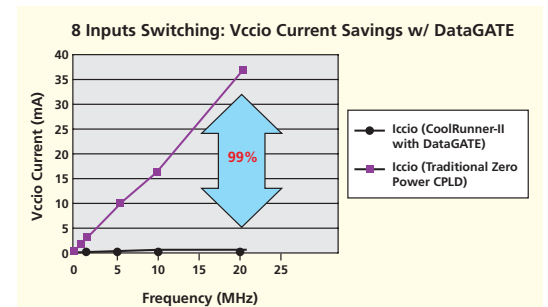
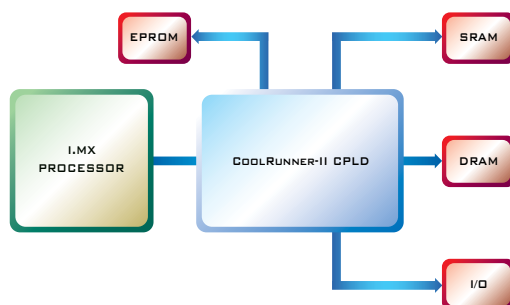


CoolRunner-II  
XC2C128  
CP132



## DATAGATE BLOCKING

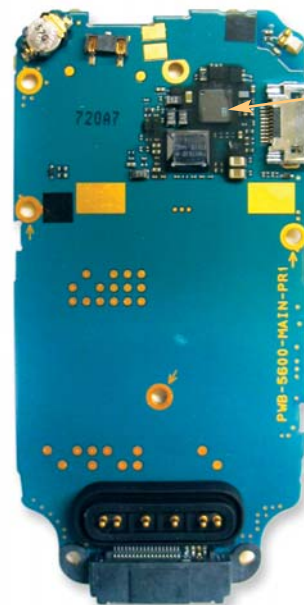
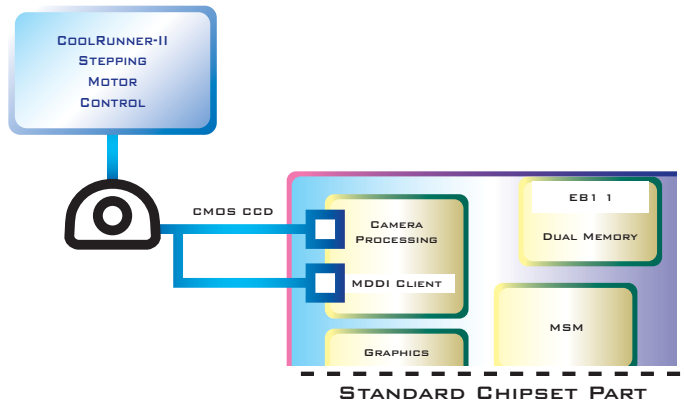
- XAPP395 Using DataGATE in CoolRunner-II CPLDs
- WP227 The Real Value of CoolRunner-II DataGATE





## CELL PHONE WITH CAMERA ZOOM

- Focus Control for Stepping Motor.
- Chipset Differentiation.



CoolRunner-II  
XC2C32  
QF32

## POCKET PC/PHONE

- Keypad Scanner
- Logic Consolidation

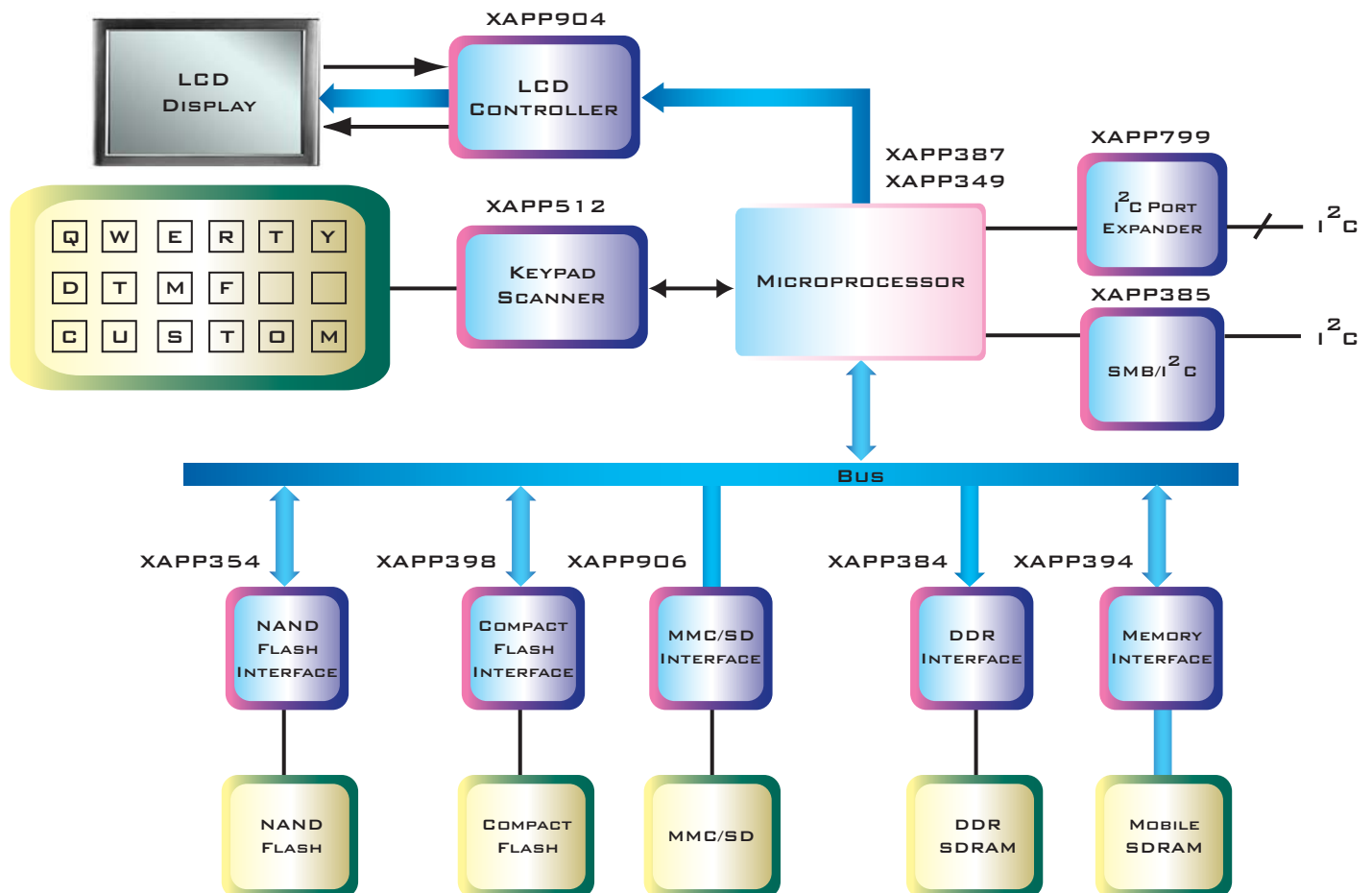


CoolRunner-II  
XC2C128  
CP132



# HANDSET APPLICATION NOTE SUPPORT

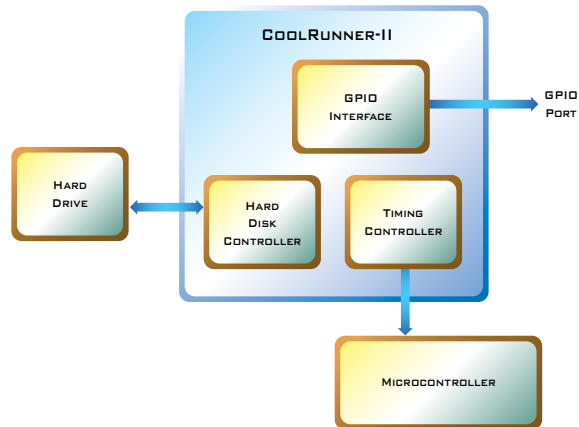
- Free HDL Design Files Accompany Application Notes
- Proven Customer Design Use and Support
- [www.xilinx.com/support/library.htm](http://www.xilinx.com/support/library.htm)



# PORTABLE CONSUMER

## GPS UNIT

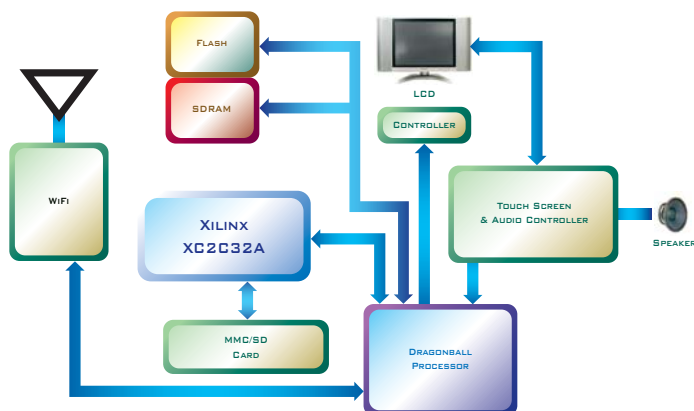
- Hard Disk Control
- GPIO Interface
- Timing Controller



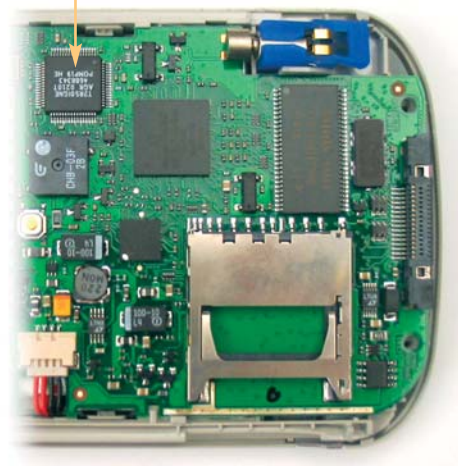
CoolRunner-II  
XC2C128  
CP132

## PDA DEVICE

- SD Card Interface

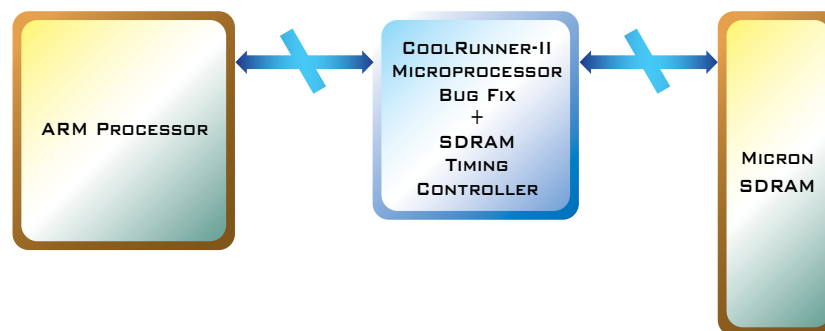
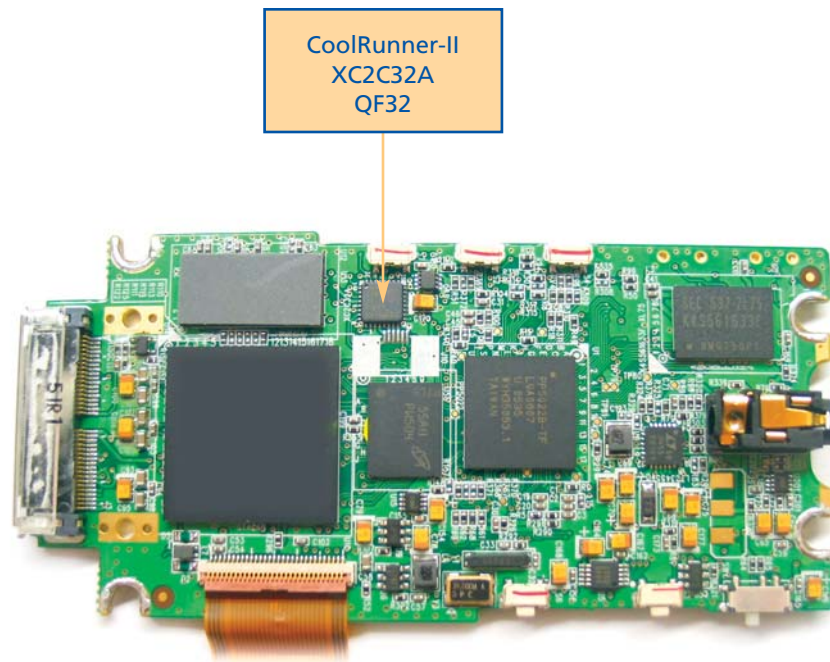


CoolRunner XPLA3  
XCR3032XL  
3.3 Volt



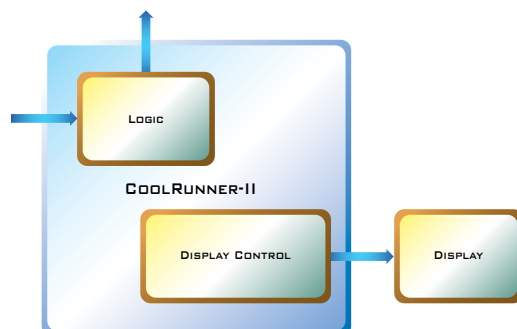
# PORTABLE SATELLITE RADIO AND MP3 PLAYER

- Microprocessor Bug Fix
- SDRAM Timing Controller

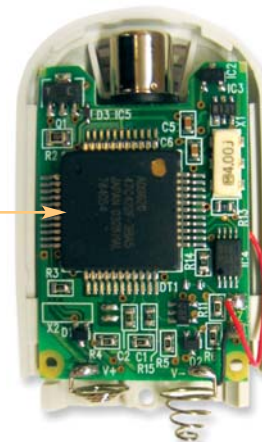


# ALCOHOL ANALYZER

- Display Control
- Logic Consolidation



CoolRunner XPLA3  
CPLD  
Under  
Piggyback  
Device

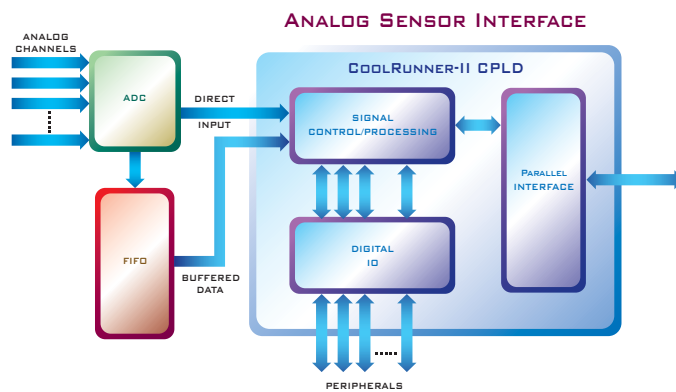
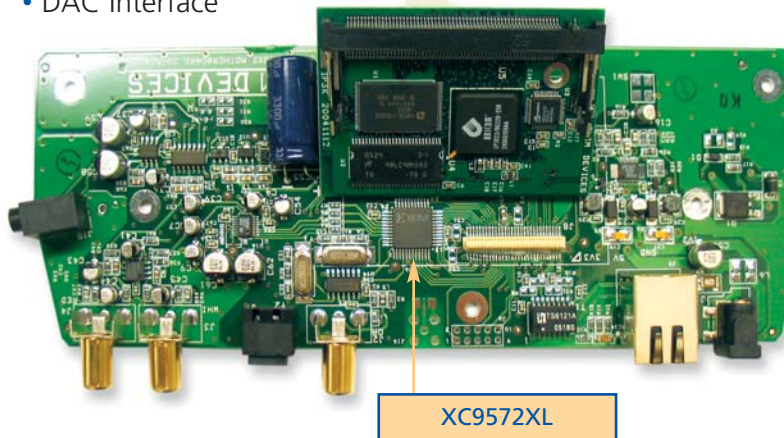




# WIRED CONSUMER

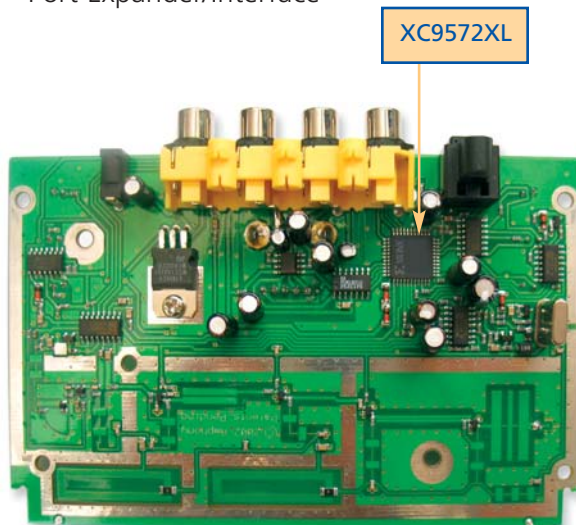
## DIGITAL MUSIC BOX

- Port Expander/Interface
- DAC Interface



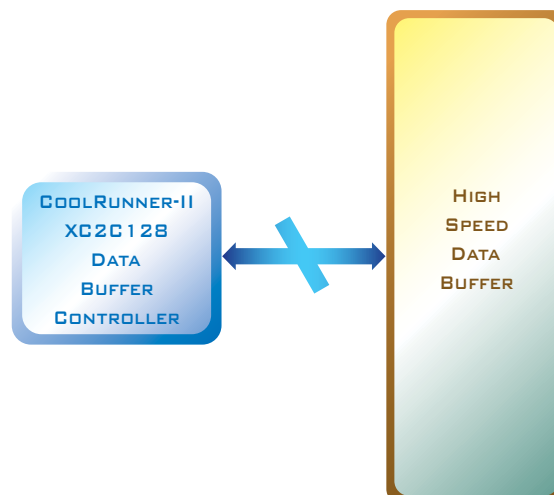
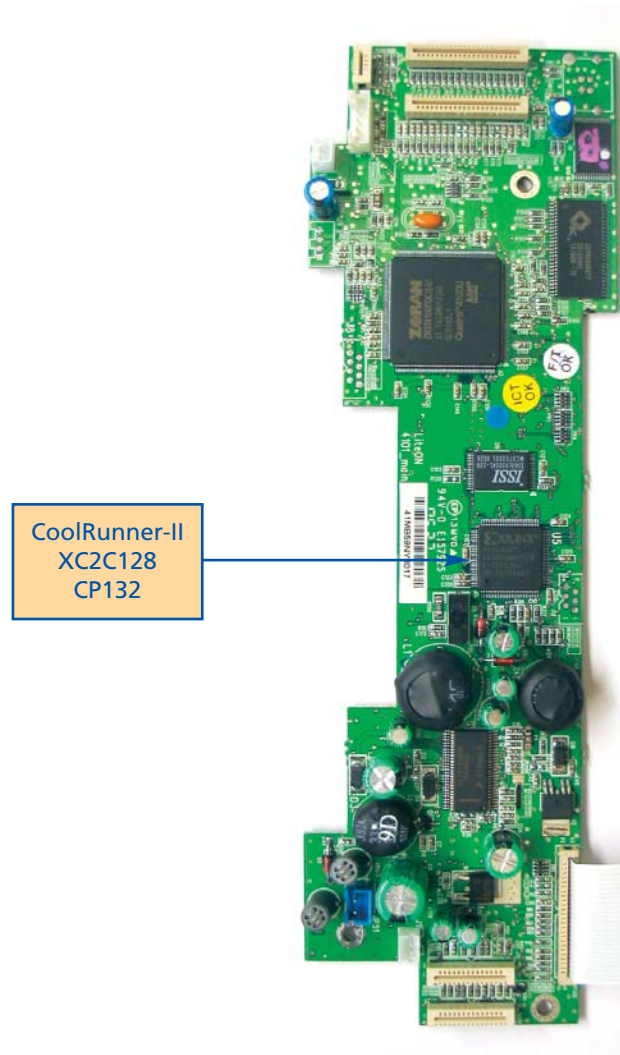
## DIGITAL WIRELESS INTERFACE

- Port Expander/Interface



# PHOTO PRINTER

- High Speed SRAM Controller



# LOGIC CONSOLIDATOR

## Xilinx CPLDs Offer More for Less



### Get More

- Logic
- Features and Performance
- Security
- Flexibility

### For Less

- Price
- Board area
- Power
- EMI

### The Logic Consolidator demonstrates how Xilinx CPLDs can:

- Reduce component cost and manufacturing cost
- Reduce component count and PC board space
- Decrease time-to-market
- Increase reliability

### Documentation

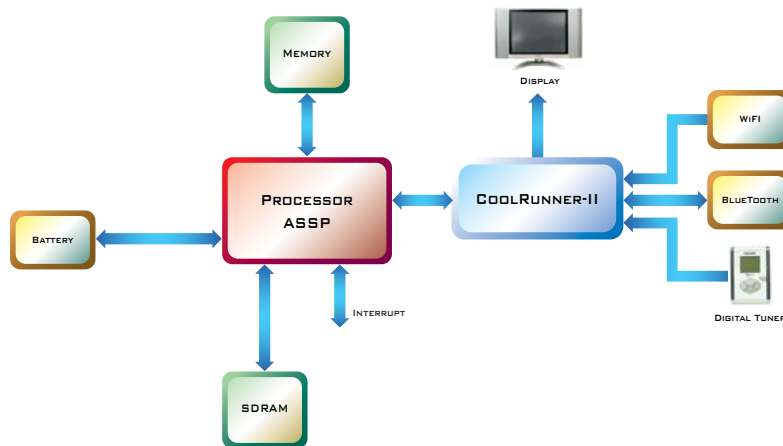
- **WP202:** The Advantages of Migrating from Discrete Logic Devices to CPLDs (PDF)
- **WP214:** TTL Burn Rate for Xilinx CPLDs (PDF)

Download the latest version of the CPLD Logic Consolidator now!  
[www.xilinx.com/products/silicon\\_solutions/cplds/cpld\\_logic\\_consolidator.htm](http://www.xilinx.com/products/silicon_solutions/cplds/cpld_logic_consolidator.htm)

# DOCUMENTED XILINX CPLD APPLICATIONS

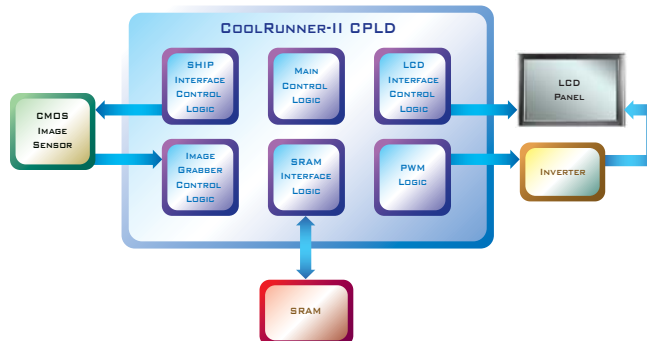
## DIGITAL MEDIA PLAYER

- XAPP328 Design of an MP3 Player Using a CoolRunner CPLD



## DIGITAL CAMERA

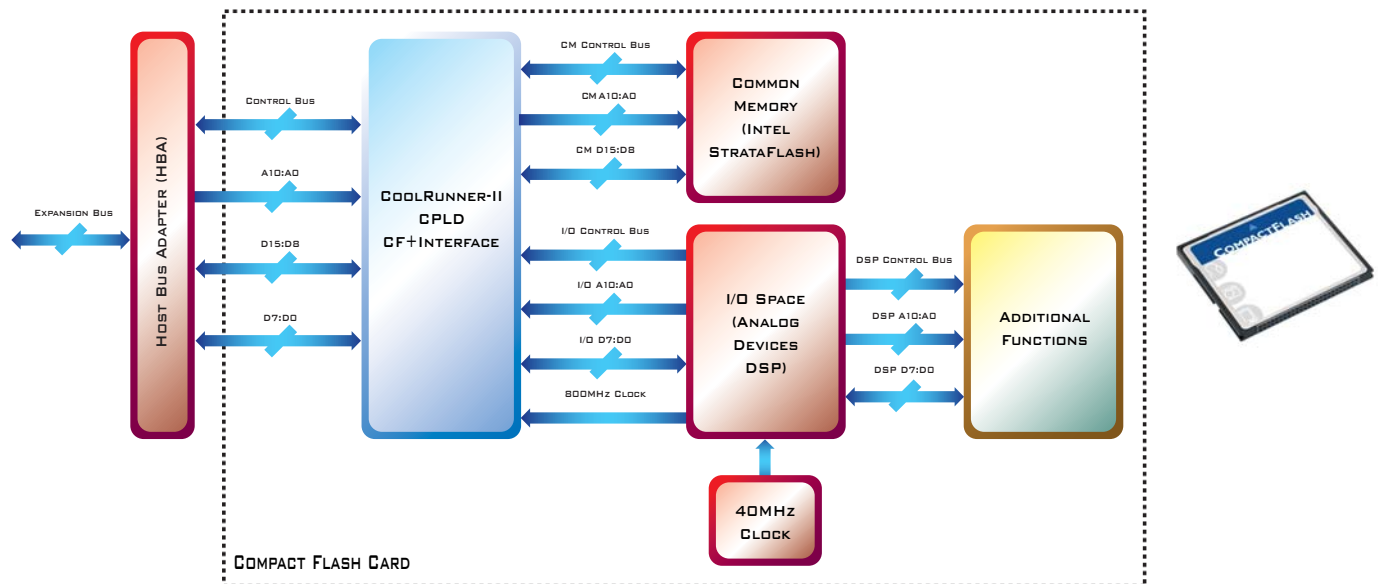
- XAPP390 Design of a Digital Camera with CoolRunner-II CPLDs



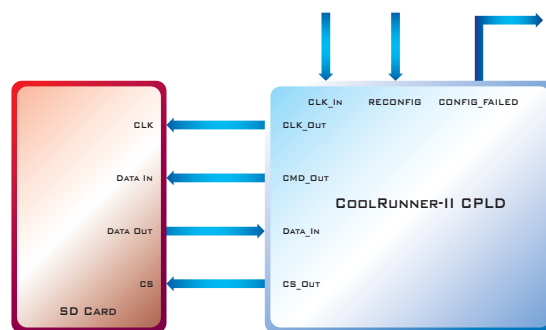
# MEMORY CONTROL

## COMPACT FLASH CARD INTERFACE AND CONTROL

- XAPP398 Compact Flash Interface for CoolRunner-II CPLDs

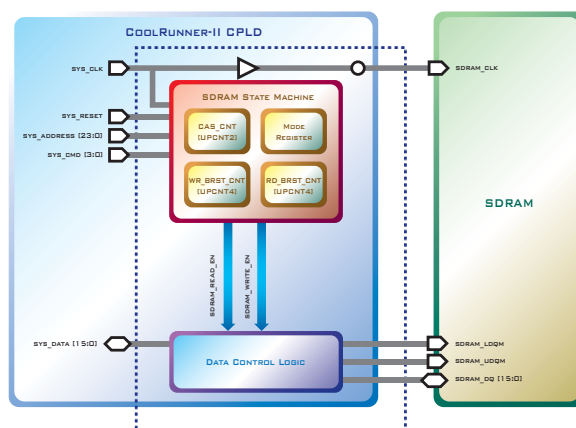


## SD CARD INTERFACE



- XAPP906 Interfacing to Secure Digital Cards with CoolRunner-II CPLDs

## SDRAM CONTROLLER



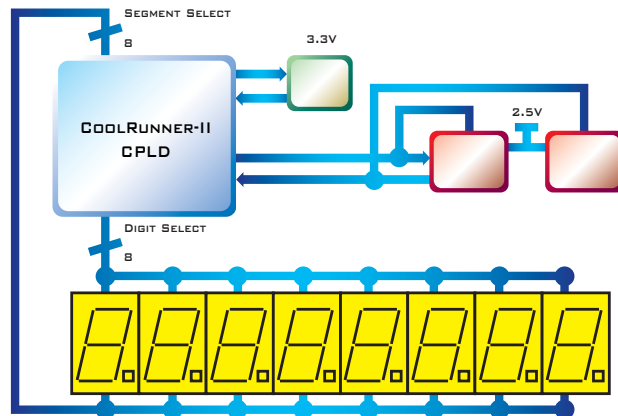
- XAPP384 Interfacing to DDR SDRAM with CoolRunner-II CPLDs
- XAPP394 Interfacing to Mobile SDRAM with CoolRunner-II CPLDs



# DISPLAY INTERFACE

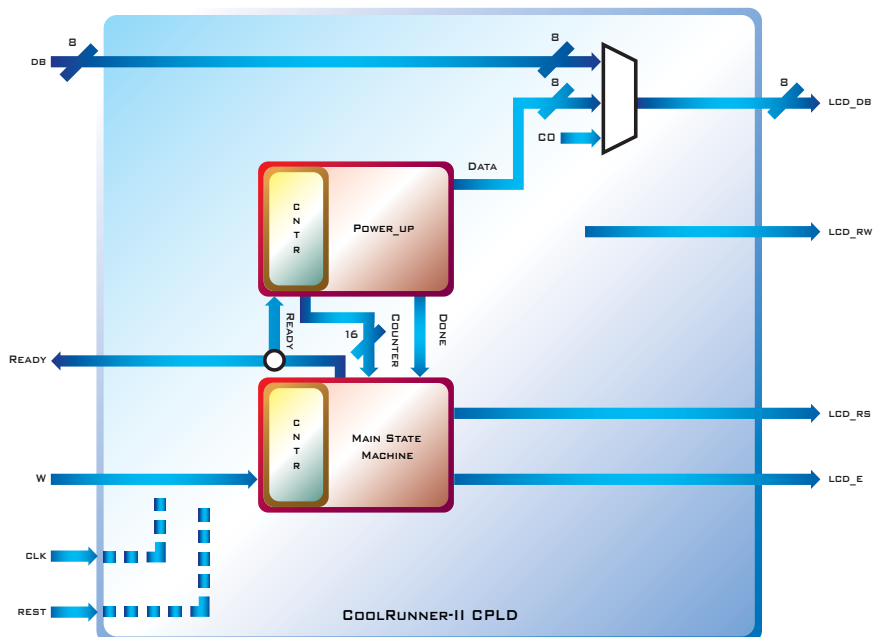
## LED DRIVER BLOCK

- XAPP805 Driving LEDs with Xilinx CPLDs



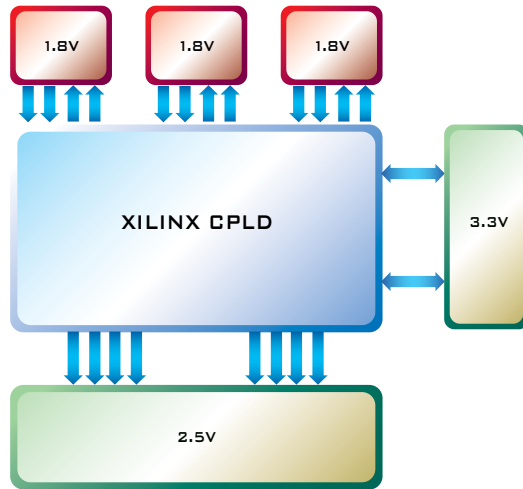
## LCD MODULE

- XAPP904 CoolRunner-II Character LCD Module Interface



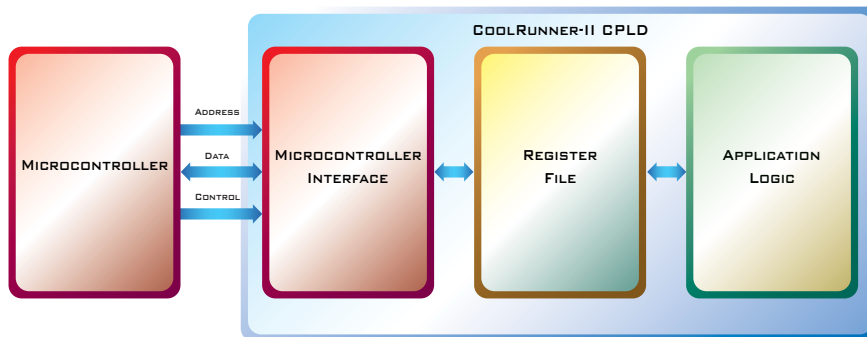
## LEVEL SHIFTING

- XAPP785 Level Translation Using Xilinx CPLDs



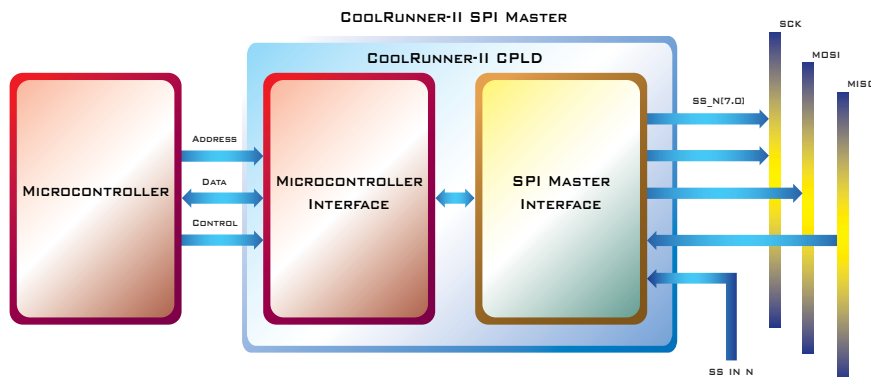
## MICROCONTROLLER INTERFACE

- XAPP393 CoolRunner-II CPLD 8051 Microcontroller Interface



## SERIAL PERIPHERAL INTERFACE MASTER

- XAPP386 CoolRunner-II Serial Peripheral Interface Master
- XAPP800 Configuring Xilinx FPGAs with SPI Flash Memories Using CoolRunner-II CPLDs



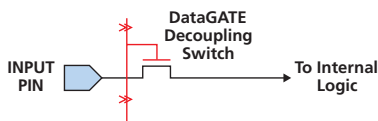
# COOLRUNNER-II

## ADVANCED FEATURES

### DataGATE

Series switches on the inputs allow decoupling of internal logic from external "don't care" transitions. Outputs are held at the last valid state when DataGATE is enabled.

- Reduces power consumption by eliminating 'don't care' internal switching
- Supports hot plugging
- Reduces EMI
- Simplifies system debug



### Advanced Security

Four levels of design security

- Prevents design theft or accidental overwrite
- Ideal for mobile phones and PDAs and other wireless applications

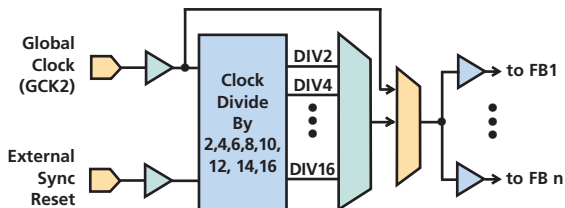
### I/O Banking

Multiple I/O banks, each with independently selectable voltage levels

- System voltage interfacing
- Bridging standards
- Bus multiplexing

### Clock Division

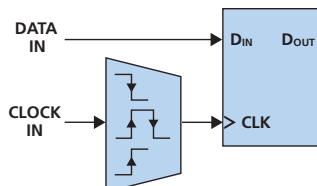
- Even/Odd clock generation
- Duty cycle correction
- Multiple clock nets



### DualEDGE Flip Flops

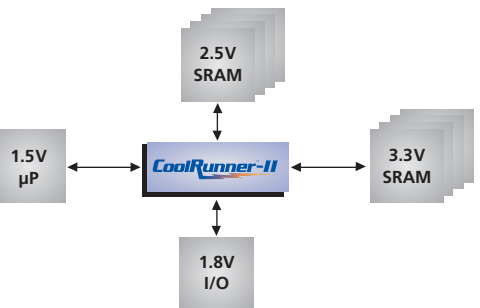
Each flip-flop can switch on the rising, falling or both edges of the clock

- Higher-resolution PWM
  - Motor control
  - LCD contrast
  - Power conversion
  - Position indication
- Increased timer resolution



### In System Programming and On The Fly Reconfiguration

- Reprogram the design post-deployment
- Reprogram the CPLD with a new pattern while the existing pattern is operational
- Multiple design patterns from a single CPLD



### 500mV Input Hysteresis

- Improved noise immunity
- Reduced power consumption (fewer false transitions)
- Superior signal integrity



# INDUSTRY'S LOWEST POWER CPLDs.

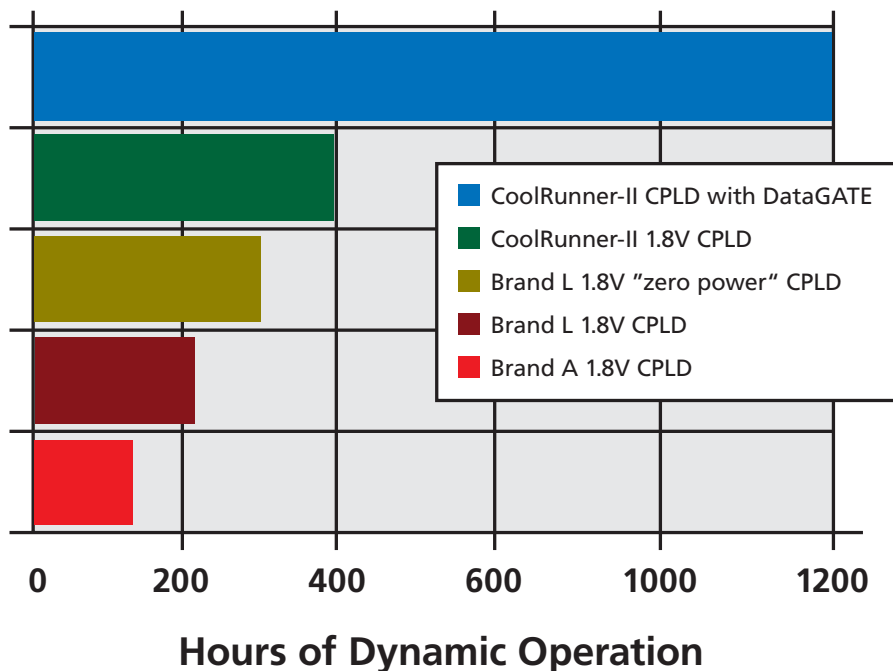
SO LOW-POWER, COOLRUNNER-II CPLDs EVEN RUN ON APPLES!



- XAPP381 CoolRunner-II Demo Board

## CPLD BATTERY LIFE COMPARISON

- CoolRunner-II CPLDs with DataGATE dramatically extends battery life



**Note:** 256 macrocell devices at 100% duty cycle with 2 AA batteries, populated with 16 bit counters at 20 MHz.

# COOLRUNNER-II CPLD SELECTION GUIDE

Device		XC2C32A	XC2C64A	XC2C128	XC2C256	XC2C384	XC2C512
System Gates		750	1500	3000	6000	9000	12000
Macrocells		32	64	128	256	384	512
Product Terms per Macrocell		56	56	56	56	56	56
Maximum I/O		33	64	100	184	240	270
Minimum Pin-to-Pin Logic Delay (ns)		3.8	4.6	5.7	5.7	7.1	7.1
DualEDGE Registers		Yes	Yes	Yes	Yes	Yes	Yes
Input Hysteresis		Yes	Yes	Yes	Yes	Yes	Yes
DataGATE and Clock Divide		—	—	Yes	Yes	Yes	Yes
Global Clocks		3	3	3	3	3	3
Product Term Clocks per Function Block		16	16	16	16	16	16
Packages	Size	Maximum User I/O					
QFG32	5x5 mm	21	—	—	—	—	—
VQ44	12x12 mm	33	33	—	—	—	—
PC44	17.5x17.5 mm	33	33	—	—	—	—
QFG48	7x7 mm	—	37	—	—	—	—
CP56	6x6 mm	33	45	—	—	—	—
VQ100	16x16 mm	—	64	80	80	—	—
CP132	8x8 mm	—	—	100	106	—	—
TQ144	22x22 mm	—	—	100	118	118	—
PQ208	30.6x30.6 mm	—	—	—	173	173	173
FT256	17x17 mm	—	—	—	184	212	212
FG324	23x23 mm	—	—	—	—	240	270

## LOW-COST SMALL FORM-FACTOR PACKAGING

					
Package Type:	QF32	CP56	QF48	CP132	FT256
Dimensions:	5x5mm	6x6mm	7x7mm	8x8mm	17x17mm
Board Area:	25mm <sup>2</sup>	36mm <sup>2</sup>	49mm <sup>2</sup>	64mm <sup>2</sup>	289mm <sup>2</sup>
Max. I/O:	21	45	37	106	212
(Actual Size)					



# TAKE THE NEXT STEP

The Xilinx CPLD Design Kit contains everything you need to design and debug your next CPLD design, including:

- ISE WebPACK software
- Prototype board with pre-programmed CoolRunner-II and XC9500XL CPLDs
- Download cable
- Training material
- Resource CD

[www.xilinx.com](http://www.xilinx.com)



## Design Faster with CoolRunner Reference Designs.

Xilinx CPLD reference designs make designing much easier than with other solutions. These drop-in, ready-to-use functions are comprised of HDL design code and application notes that allow to finish your design faster. You can also increase product flexibility and user advantages with our comprehensive reference designs.

[www.xilinx.com/cpld/ref-designs](http://www.xilinx.com/cpld/ref-designs)

## CPLD QuickStart Applications.

Xilinx CoolRunner-II CPLDs are shown in a wide range of design examples, with presentations and demonstrations to show how you can complete your design faster, with lower power and lower cost.

[www.xilinx.com/cpld/quickstart](http://www.xilinx.com/cpld/quickstart)

**Corporate Headquarters**

Xilinx, Inc.  
2100 Logic Drive  
San Jose, CA 95124  
Tel: (408) 559-7778  
Fax: (408) 559-7114  
Web: [www.xilinx.com](http://www.xilinx.com)

**European Headquarters**

Xilinx  
Citywest Business Campus  
Saggart,  
Co. Dublin  
Ireland  
Tel: +353-1-464-0311  
Fax: +353-1-464-0324  
Web: [www.xilinx.com](http://www.xilinx.com)

**Japan**

Xilinx, K.K.  
Shinjuku Square Tower 18F  
6-22-1 Nishi-Shinjuku  
Shinjuku-ku, Tokyo  
163-1118, Japan  
Tel: 81-3-5321-7711  
Fax: 81-3-5321-7765  
Web: [www.xilinx.co.jp](http://www.xilinx.co.jp)

**Asia Pacific**

Xilinx, Asia Pacific Pte. Ltd.  
No. 3 Changi Business Park Vista, #04-01  
Singapore 486051  
Tel: (65) 6544-8999  
Fax: (65) 6789-8886  
RCB no. 20-0312557-M  
Web: [www.xilinx.com](http://www.xilinx.com)

**Distributed By:**