

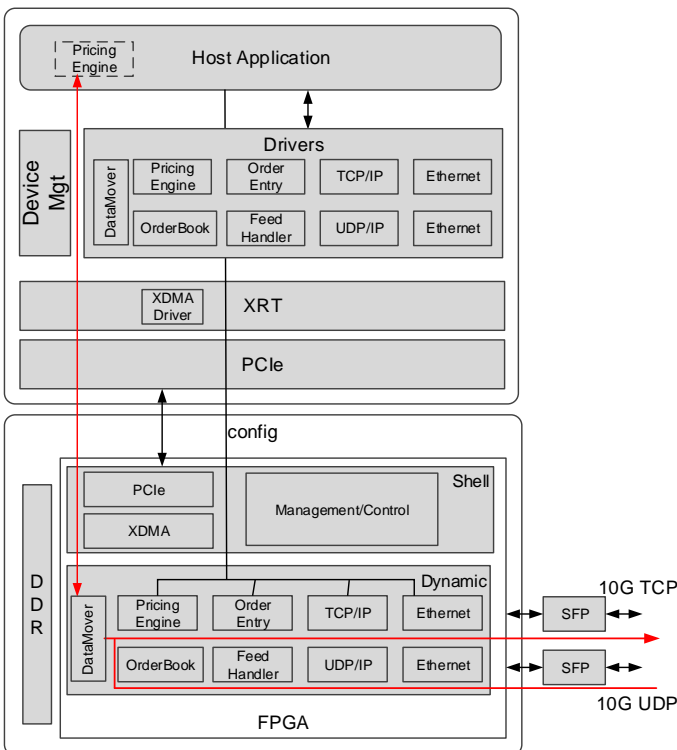
# XILINX ALGORITHMIC TRADING REFERENCE DESIGN

## INTRODUCTION

A fully featured open source and license free HLS hardware & software trading solution reference design. Give your developers a head start to create their own hardware-accelerated algorithmic trading platform

## PRODUCT OVERVIEW

- > Alveo U50,U250 boards with Vitis tools and libraries
- > Migration from software algorithms to hardware
- Dataplane entirely in hardware
- Dataplane in hardware with pricing algorithm on host
- > Baseline from which users can develop solutions



## Features and Benefits

- > CME “Market by Price” scheme:
  - CME Feedhandler, Orderbook
  - Two Pricing Algorithms
  - Order Entry templated trades
- > 10GbE UDP, TCP, IP(v4) in FPGA
- > Data Transfer to host CPU
- > Debug and diagnostic features

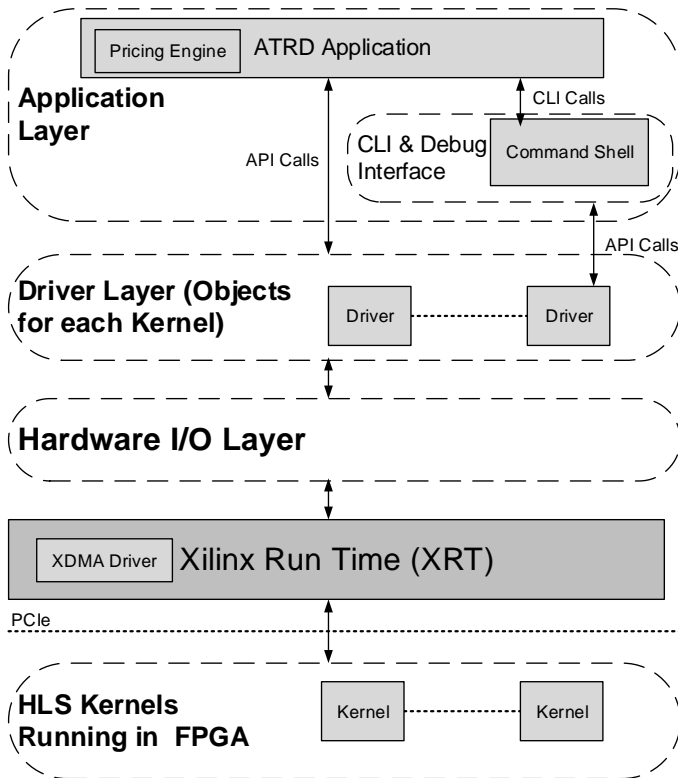
### Quick Start Package provides:

- > All HLS,C++ source code
- > FPGA image (XCLBIN)
- > PCAP input and output files
- > Build automation tool
- > Comprehensive user guide

## DATA TRANSFER WITH HOST

- > Supports trading algorithm on host CPU
  - Order Book pushed from FPGA to host
  - Trading request pushed from host to FPGA
  - XDMA transfer of data

- > Data mover kernel
  - Ring buffers in Alveo Memory.
  - Data source updates tail pointer of buffer
  - Data receiver monitors tail pointer to detect new data available



## SOFTWARE OVERVIEW

- > Algorithmic Trading Ref. Design application
  - Configuration of trading and IP address parameters
  - Software Trading application (if required)
  - Calls APIs on driver layer
  - Recovers diagnostic and debug information
- > User Interface (Command line shell)
  - Command shell provides easy interface with help functionality.
- > Driver layer (User space)
  - API Control of each hardware block
  - Exposes functionality of hardware
- > Hardware I/O Layer
  - All communication with hardware
  - Download image XCLBIN to FPGA
- > XRT (Xilinx Run Time)
  - XRT is a combination of userspace and linux kernel driver components
  - XRT provides a standardized software interface to the FPGA

## TAKE THE NEXT STEP

Get Started with Vitis <https://www.xilinx.com/products/design-tools/vitis/vitis-platform.html>  
 Alveo U50: <https://www.xilinx.com/products/boards-and-kits/alveo/u50.html#gettingStarted>  
 Alveo U250: <https://www.xilinx.com/products/boards-and-kits/alveo/u250.html#gettingStarted>  
 Request Lounge Access: <https://www.xilinx.com/member/forms/registration/fintech.html>  
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