

Products, Profits Proliferate on Zynq SoC Platforms

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Customers find they can maximize revenue by building their product portfolios around Xilinx's Zynq SoC.



Ever since Xilinx® shipped the Zynq®-7000 All Programmable SoC in late 2011, a bounty of products has been arriving. Today the Zynq SoC is at the heart of many of the world's newest and most innovative automotive, medical and security vision products, as well as advanced motor-control systems that make factories safer, greener and more efficient. The Zynq SoC has also won sockets in next-generation wired and wireless communications infrastructure equipment as well as a wealth of emerging Internet of Things applications.

Having experienced firsthand the unmatched versatility of a device that integrates a dual-core ARM® Cortex™-A9 MPCore processor with programmable logic and key peripherals all on the same chip, a growing number of customers are expanding their use of the Zynq SoC from the processor of choice for one socket to the platform choice for entire product lines. By deploying a platform strategy leveraging the Zynq SoC and hardware/software reuse, they are able to quickly create many derivatives or variations of their products. The result is higher levels of design productivity and an improvement in the bottom line.

Let's look at what practices top platform-electronics companies employ to improve profitability; why the Zynq SoC is far superior to ASIC, standalone ASSP and even two-chip ASSP+FPGA platform implementations; and how you can put the Zynq SoC to good use to drive prolific profitability at your company.

To many, the word "platform" has become an overused marketing term. But in the electronics industry, many companies such as Apple, Intel and Cisco Systems have effectively executed platform business strategies to become highly profitable electronics leaders. In deploying platform strategies, companies make a relatively substantial upfront investment in creating and documenting the blocks they designed for the initial version of their electronics product platform. They then turn those design blocks into intellectual-property (IP) blocks, which they reuse to quickly and easily expand into derivative product lines and

models along with next-generation products, delivering each of those derivative products faster and with less effort, less design cost and fewer resources.

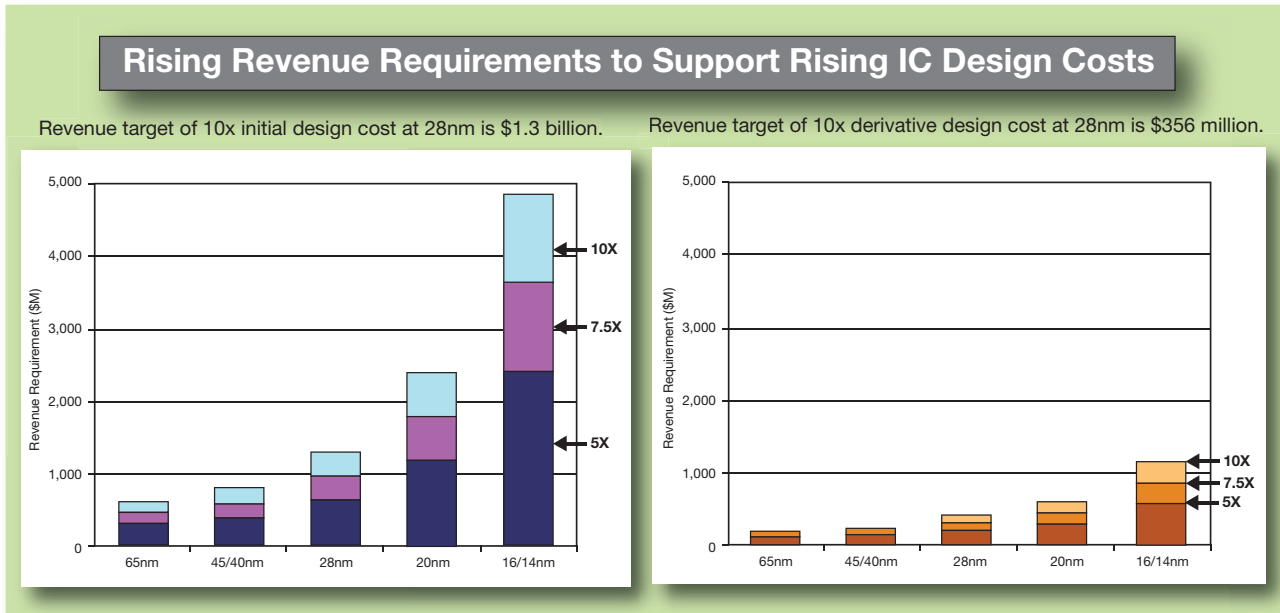
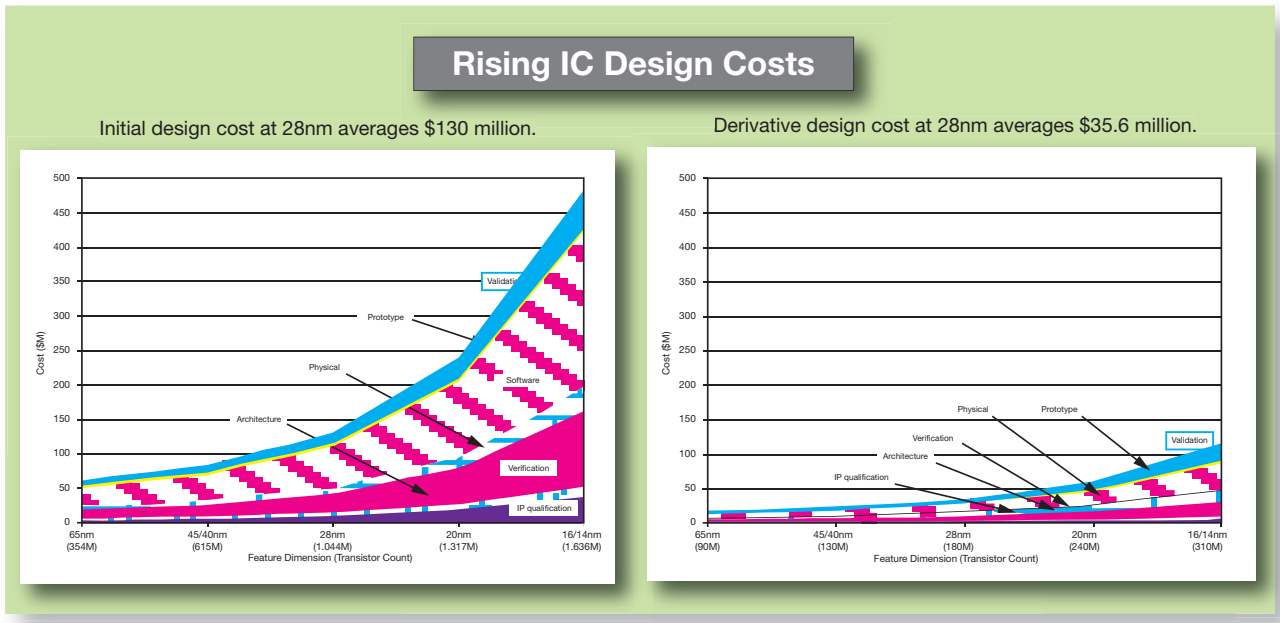
CHALLENGES TO ACHIEVING PROFITABILITY

Research firm International Business Strategies (IBS) in its 2013 report “Fac-

tors for Success in System IC Business” concludes that as the cost of producing an ASIC or ASSP device using the latest silicon processes continues to rise from the 28-nanometer manufacturing node to 20 nm, 16 nm and 10 nm, companies producing their own chips will increasingly struggle to achieve the traditional end-product revenue goal:

revenue 10 times larger than their initial R&D investment. Many make great strides toward achieving this 10x goal by creating multiple derivative products on each node.

“Derivative designs can cost 20 percent of the initial design cost, which means that if a commitment is made to a new product family that has very



Source: International Business Strategies, Inc. (IBS) (2013/2014)

Figure 1 – The initial cost of developing an IC rises with the introduction of each new silicon process technology. In comparison, the cost of developing subsequent derivative products on the same node is much lower, making it far easier to achieve the end-product revenue target of 10x design cost. Platform design allows companies to rapidly develop derivative designs and increase profitability.

‘New design concepts that reduce the cost of implementing new products have the potential to change the structure of the semiconductor industry dramatically.’

high development costs, then derivative designs can be implemented at a much lower cost. To optimize revenues and profits, it is advantageous for companies to implement multiple [derivative] designs in a technology node,” the report said. “Implementing only one or two designs in a technology node can result in very high up-front costs and high risks associated with getting good financial returns.

“New design concepts that reduce the cost of implementing new prod-

ucts have the potential to change the structure of the semiconductor industry dramatically,” the report went on. “However, until a new design methodology emerges, semiconductor companies need to adapt their business models to the reality of the changing financial metrics in the semiconductor industry as feature dimensions are reduced” [Source: *International Business Strategies, Inc. (IBS) (2013/2014)*].

In the study, IBS shows that the design cost of a 28-nm ASIC or ASSP (the

first or initial product) is \$130 million (Figure 1). Meanwhile, the design cost of a derivative is significantly lower: \$35.6 million. Thus, to achieve the 10x revenue goal for both types of devices requires an investment of \$1.3 billion for complex devices but only \$356 million for derivatives [Source: *International Business Strategies, Inc. (IBS) (2013/2014)*].

The IBS study shows that companies must spend 650 engineering years to design a complex ASIC at 28 nm. In com-

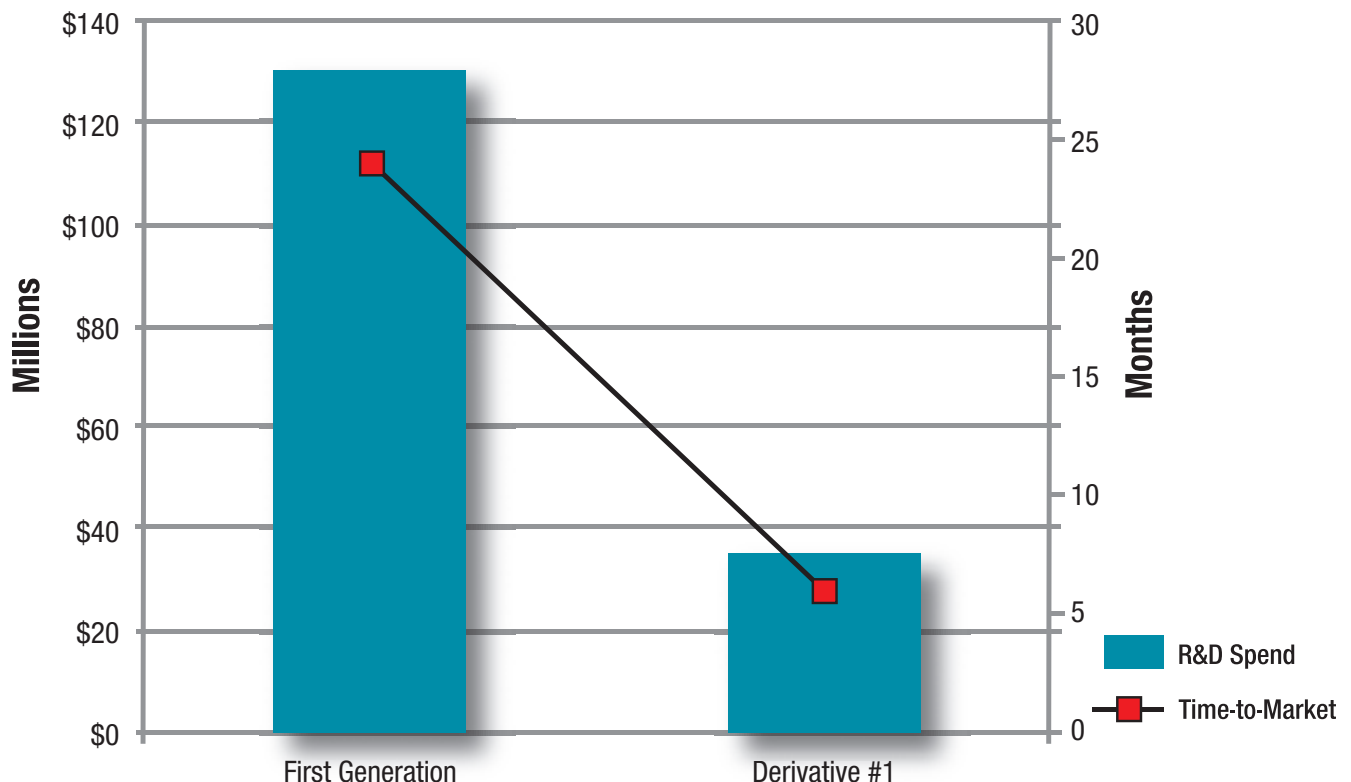


Figure 2 – Derivative designs reduce time-to-market, development time and costs, making profitability goals easier to achieve.

Developing multiple derivatives on the same node using a platform strategy allows a company to optimize revenue and profit.

parison, a derivative 28-nm ASIC design requires only 169 engineering years to develop, a 3.8x reduction.

Assuming ASIC teams are developing new designs in step with Moore's Law and are working on a two-year development cycle, it would take 325 engineers to complete a complex 28-nm ASIC in those two years. However, it would take only 85 engineers to complete a derivative 28-nm ASIC in two years. Or if a company were to use all 325 of engineers to develop the derivative as well, they could complete the job in six months (Figure 2).

Further, as illustrated in Table 1, if we assume that the initial complex design achieved its 10x revenue payback of \$1.3 billion using 325 engineers, a derivative design with a smaller addressable market that is only 80 percent (\$1.04 billion) the revenue size of the initial ASIC's market would require just 85 engineers over two years to develop a product that would garner a net present value (NPV) that is much better than the NPV of the initial ASIC design. (NPV is defined as the difference between the present value of cash inflows and cash

outflows. The concept is used in capital budgeting to analyze the profitability of an investment or project.)

What's more, the derivative would have a much more favorable "profitability index" or PI (NPV divided by R&D money spent) than the initial ASIC. Even if that derivative addressed a market half the size (\$650 million) of the initial design, it would have an NPV better than the initial ASIC, with essentially the same PI.

PLATFORMS: THE BEST STRATEGY FOR PROFITABLE DERIVATIVES

Increasingly semiconductor companies, as well as electronics system companies, are turning to platform strategies as a way to quickly create derivative products and maximize profitability in the face of rising R&D costs, increased competition and customer demand for better everything. Platform strategies further reduce product development time, time-to-market and engineering-hour costs while simultaneously increasing the profitability of each derivative or next-gen product.

As the IBS study shows, developing

derivative designs is a way for companies to "optimize revenues and profits." And developing multiple derivatives on the same node (in other words, derivatives of derivatives) using a platform approach allows companies to further optimize revenue and profit, as each subsequent design can benefit from lessons learned in the prior design, reuse and a more precise understanding of customer requirements.

PROCESSING CHOICE IS KEY TO SUCCESS OF THE PLATFORM

Two of the biggest business decisions a company can make when deploying a platform strategy are actually vital technical decisions: Which one of the many processing systems will be at the heart of your product platform? And which silicon implementation of that processing system is the best for improving profitability?

In a platform strategy, a processing system must meet or exceed application software and system requirements. It must be scalable and easily extendable; must have a large, established and growing ecosystem; and

	Lifetime Revenue* (\$M)	R&D Spend (\$M)	Lifetime Net Profit** (\$M)	NPV*** (\$M)	Profitability Index
Initial Complex ASIC	\$1300	\$130	\$260	\$12.85	0.1
Derivative #1 (80% size market)	\$1040	\$35	\$208	\$74.78	2.14
Derivative #2 (50% size market)	\$650	\$35	\$130	\$34.47	0.98

* Assumes 7 years

** Assumes profit margin 20%

*** Assumes 15% discount rate

Table 1 – Creating derivative designs has an impressive net present value (NPV) but even more impressive profitability index.

must allow architects and engineers to leverage prior design work. Finally, it must come from an established, stable supplier with a road map and a track record of not deviating from that road map or of issuing endless errata. While there are candidates that fit some of these qualifications, the one that meets or exceeds all of them is the ARM microprocessor architecture.

ARM has become the de-facto-standard embedded processing architecture for just about anything that isn't a PC. A vast majority of electronics systems today that use advanced embedded processing, from mobile phones to cars to medical equipment, employ ARM processor cores. In particular, ARM's Cortex-A9 processor architecture is at the heart of many types of systems-on-chip (SoCs). It can be found in ASIC designs typically created for highest-volume, value-added products like bleeding-edge smartphones and tablets, as well as in many ASSP designs for companies wishing to enter established low- to moderate-volume markets that typically compete on pricing for lack of feature differentiation.

To add differentiation to their products, many companies create product platforms that pair an FPGA with an off-the-shelf ASSP based on an ARM processing system. In this configuration, they can differentiate in hardware as well as in software, creating a broader feature set or a higher-performing end product that's flexible and upgradable—one that helps them outshine competitors offering me-too software-programmable-only ASSP implementations. Adding Xilinx FPGAs to these ASSPs has helped a plethora of companies differentiate their products in the marketplace.

THE IDEAL PLATFORM SOLUTION: ZYNQ SOC

With the Zynq-7000 All Programmable SoC, Xilinx is fielding a platform implementation of the stalwart ARM Cortex-A9 that suits the vast majority of embedded applications. As illustrated in Table 2, the Zynq SoC offers many advantages over ASIC, ASSP and even ASSP+FPGA combos as a silicon platform. In comparison to other hardware implementations of the ARM processing

system, the Zynq SoC has the best feature set in terms of NRE, flexibility, differentiation, productivity/time-to-market, lowest cost of derivatives and best overall risk mitigation (Table 3).

What's more, the Zynq-SoC has vast cost advantages over other platform implementations. Let's look at the numbers.

The average cost of designing a 28-nm ASIC is \$130 million, and thus the 10x revenue goal amounts to \$1.3 billion for ASIC designs, said Barrie Mullins, director of All Programmable SoC product marketing and management at Xilinx. But typical design projects based on the Zynq SoC inherently have a much lower overall design cost and faster time-to-market than ASIC implementations, he said. That's because Zynq SoCs supply a pre-designed, tested, characterized, verified and manufactured SoC that provides software, hardware, I/O performance and flexibility for differentiation. What's more, the Zynq SoC benefits from the fact that Xilinx hardware and software design tools are inexpensive and are highly integrated, whereas ASIC tool flows are

	Total System Cost	Flexibility	Differentiation	Time-to-Market	Cost of Derivatives	Risk
Zynq SoC	Low + best value	Most flexible: HW and SW programmable + programmable I/O	Highest degree of programmability, HW/SW co-design	Fastest for integrated HW & SW differentiation	Lowest due to HW & SW programmability	Predictably low risk
ASSP + FPGA	Higher than Zynq SoC (system dependent)	Highly flexible but ASSP I/O limited compared to Zynq SoC	HW and SW programmable, ASSP-dependent	Fastest if ASSP requires HW differentiation	Low to high depending on FPGA vendor	Low to high depending on FPGA vendor
ASSP	Lowest if SW-only programmability is sufficient	Good but SW-programmable only	Limited to SW programmable only - easy cloning	Fastest if SW-only differentiation required	Lowest if SW-only derivatives needed	Can be Lowest if SW-only programmability is sufficient
ASIC	High to prohibitive	Once manufactured only limited SW flexibility	Best HW differentiation but limited SW differentiation	Lowest & riskiest	Highest	Terrible (respins)

- Best platform attributes
- Good platform attributes
- Passable platform attributes
- Worst platform attributes

Table 2 – The Zynq-7000 All Programmable SoC offers an ideal mix of attributes for customers looking to implement a platform strategy.

Lowest NRE, Best Risk Mitigation	Greatest Flexibility & Differentiation	Streamlined Productivity & Fast TTM	Lowest Cost of Derivatives & Highest Profitability
<ul style="list-style-type: none"> ✓ Already manufactured silicon ✓ Negligible development & design tool costs ✓ Xilinx IP library + third-party IP ✓ Extensive development boards 	<ul style="list-style-type: none"> ✓ All Programmable HW, SW & I/O ✓ Anytime field programmable ✓ Partial reconfiguration ✓ System Secure (encryption) 	<ul style="list-style-type: none"> ✓ Instant HW/SW co-development ✓ All Programmable Abstractions (C, C++, OpenCV, OpenCL, HDL, model-based entry) ✓ Vivado Design Suite, Vivado HLS, IP Integrator & UltraFast Methodology ✓ Broad and open OS & IDE support (Open-source Linux & Android, FreeRTOS, Windows Embedded, Wind River, Green Hills, & many others) 	<ul style="list-style-type: none"> ✓ IP standardized on ARM AMBA AXI4 ✓ Reuse precertified code (ISO, FCC, etc.) ✓ Reuse & refine code & testbenches ✓ Volume silicon, power circuitry, PCBs & IP licensing

Table 3 – Factors like low NRE charges and flexibility make the Zynq SoC the ideal processing choice for a platform strategy.

complex, have significant interoperability and compatibility issues, and entail complex licensing with costs running in the millions. Xilinx's design flow is especially streamlined when designers use Xilinx's recommended UltraFast™ methodology. In addition, said Mullins, IP qualification costs are low because the Xilinx ecosystem IP is already designed and preverified, while Xilinx tools generate middleware.

As a result, Mullins said, a typical Zynq SoC project runs \$23 million. Thus, to achieve the standard 10x revenue goal for design projects requires lifetime revenue of \$230 million—a 10x goal that is far more achievable and feasible than the \$1.3 billion required to achieve 10x for an ASIC implementation (Table 4).

Using the method described above while analyzing the IBS data, if we as-

sume that an initial complex design implemented in a Zynq SoC was able to capture 100 percent of the same \$1.3 billion targeted market, it would require only a \$23 million investment using 57 engineers for two years to bring the product to completion.

If we assume that the initial Zynq SoC design has the same 20 percent profit margin as the initial ASIC design, the initial Zynq SoC design would have an

	28nm ASIC (IBS Data)			Zynq SoC (Xilinx Estimates)		
	%	Approximate Engineering Months	Total Cost (\$M)	%	Approximate Engineering Months	Total Cost (\$M)
Hardware						
IP qualification	26	704	11.8	20	240	4.0
Architecture	8	209	4.2	45	100	2.1
Verification	53	1431	28.9	35	160	3.0
Physical design	13	350	6.9	0	0	0
Subtotal hardware (design engineering resources)	100	2694	51.8	100	500	9.1
Software		4296	59.8		720	10.0
Prototype cost (\$M)		2.1			1.0	
Validation of prototypes		815	16.6		140	2.8
Total		7805	130.3		1360	22.9

Table 4 – The cost of a Zynq SoC project is considerably lower than that of an equivalent ASIC project.

Zynq SoC Platform at 15% Profit Margin	Lifetime Revenue* (\$M)	R&D Spend (\$M)	Lifetime Net Profit** (\$M)	NPV*** (\$M)	Profitability Index
Initial Complex Zynq SoC design	\$1300	\$23	\$195.00	\$73.67	2.54
Derivative #1 (80% size market)	\$1040	\$9.2	\$156.00	\$69.78	6.02
Derivative #2 (50% size market)	\$650	\$9.2	\$97.50	\$39.55	3.41

* Assumes 7 years

** Assumes profit margin 15%

*** Assumes 15% discount rate

Zynq SoC Platform at 20% Profit Margin	Lifetime Revenue* (\$M)	R&D Spend (\$M)	Lifetime Net Profit** (\$M)	NPV*** (\$M)	Profitability Index
Initial Complex Zynq SoC design	\$1300	\$23	\$260.00	\$107.27	3.70
Derivative #1 (80% size market)	\$1040	\$9.2	\$208.00	\$96.66	8.33
Derivative #2 (50% size market)	\$650	\$9.2	\$130.00	\$56.34	4.86

* Assumes 7 years

** Assumes profit margin 20%

*** Assumes 15% discount rate

Table 5 – The NPV and profitability index show the Zynq SoC to be a far superior platform choice than ASIC-based platforms.

NPV of \$107.27 million, with a PI of 3.7, which is dramatically better than the initial ASIC's NPV of \$12.85 million and its PI of 0.1. The NPV and PI for Zynq SoC derivatives at that same 20 percent profit margin are even more impressive (Table 5).

Xilinx customers have shown that the cost of a derivative in a Zynq SoC platform strategy is typically 60 percent less than their initial design (see sidebar).

Comparing the Zynq SoC platform derivative at the same 20 percent profit margin as the ASIC platform derivative addressing a market 80 percent the size of the initial design, the Zynq SoC platform's NPV is \$96.66 million with a PI of 8.33. This is considerably better than the ASIC derivative, which has an NPV of \$74.78 and a PI of 2.14. Similarly, the NPV for the derivative Zynq SoC design addressing a market half the size of the initial Zynq SoC design's targeted mar-

ket would be \$56.34 million with a PI of 4.86. This is far superior to the ASIC platform derivative's numbers.

Even if we leave the ASIC platform's profit margin at 20 percent and compare the results to a Zynq SoC platform assuming a lower, 15 percent profit margin (accounting for perhaps higher unit costs for the Zynq SoC), the Zynq SoC presents a far superior path to maximizing profitability. The initial Zynq SoC design at a 15 percent profit margin would have an NPV of \$73.67 million, yielding a PI of 2.45. This is a vast improvement over the initial ASIC's NPV of \$12.85 million and its PI of 0.1 even when the ASIC has 20 percent profit margin.

For a Zynq SoC platform design that targets a market of 80 percent (\$1.04 billion), the revenue size of the initial Zynq SoC's targeted market, it would take 23 engineers two years to develop a derivative Zynq SoC-based product. In the end, the product would garner an NPV

of \$69.78 million with a PI of 6.02. This compares with the ASIC derivative's NPV of \$74.78 million, which is slightly better than the Zynq SoC derivative's NPV. However, the PI for the Zynq SoC derivative at a 15 percent profit margin is considerably better than the ASIC derivative's PI of 2.14, even when the ASIC has a higher (20 percent) profit margin.

Further, a derivative Zynq SoC design (again at a 15 percent profit margin) addressing a market half the size of the initial Zynq SoC design's targeted market would garner an NPV of \$39.55 million and a PI of 3.41. That is not only better than the ASIC derivative's PI of 0.98 but also better than the PI of the initial Zynq SoC.

It should be noted that while profit margins will vary depending on the volume needs of a given market, the data shows that the Zynq SoC is a superior platform choice even for high-volume applications. Even when comparing an

CASE STUDY:

National Instruments Achieves New Efficiencies with Zynq SoC

by Mike Santarini

National Instruments was an early adopter of the Zynq SoC and is already showing how leveraging the device as a platform can increase efficiencies and raise profitability.

“What we are doing with the Zynq platform is creating our own platform,” said James Smith, director of embedded systems product marketing at NI (Austin, Texas). “We are a tools provider for scientists and engineers. We are creating a development platform that customers can design on top of.”

Xilinx and National Instruments have long worked closely together on Xilinx product road maps. This was especially the case as Xilinx was developing the Zynq SoC. NI was one of the first customers to receive shipments of the new device in November 2011 and has already put it to good use as a platform.

In the summer of 2013, NI announced not one but three new products based on the Zynq SoC: the high-end CompactRIO-9068 software-designed controller; a low-cost version targeted at students called myRIO; and another product called roboRIO for the First Robotics Competition.

Smith said that NI has been using a platform approach for the last decade, typically pairing a Xilinx FPGA with an off-the-shelf microprocessor. He termed the Zynq SoC the ideal platform for NI's RIO line.

“We get a lot of unique benefits out of using Zynq SoC over previous processing platforms,” said Chris Rake, senior group manager for CompactRIO hardware at NI. “Zynq is a high-value product in that it integrates a processor that gives us about four times the performance of our previous-generation comparable product, along with a very rich Xilinx 7 series logic fabric plus additional DSP resources—and all at a very competitive price point.”

Because the processor and logic are on the same chip, Rake said, “we not only see the processor performance improvement but a dramatic increase in DMA [direct memory access] performance. We have been able to more than double our DMA throughput and dramatically increase the number of DMA channels going between the processor and the programmable logic. None of that was possible with the platform architectures we were previously using. The price point to create an equivalent product would have been prohibitive.”

Rake said that having an integrated processor and FPGA on the same chip also enables smaller form factors. “Instead of having two or three separate packages, we now have one package that represents the heart of the architecture and we can dramatically reduce size,” said Rake. “Zynq allowed us to develop a range of products at the right cost of goods that we needed for the marketplace.”

Rake noted that moving to a new platform always carries higher initial costs, and moving to the Zynq SoC was no exception. “We started the project by porting our software stack to the ARM dual-core A9 processor when Zynq was still in development,” said Rake. “We used Xilinx's early development platform to work toward that, as well as using an ASSP with dual-core A9s that was on the market.”

Then, when the silicon became available, NI began using the Zynq-7020, he said, porting the entire LabVIEW RTOS to NI Linux real-time. “So we had to do all those things upfront, and it was a significant effort. But now we have a core, standard architecture that multiple development teams throughout NI can use for new designs,” said Rake.


NI stores all project schematics and layouts in a central repository. “For teams that are interested in using this processor and programmable logic technology, there are

well-established technical leads that act as points of contact for internal design teams, who assist with design and validation,” Rake said. “The team that pioneered the initial Zynq SoC-based platform is now a team of experts who are a great resource in answering questions related to Zynq. They facilitate the development of the variants. At NI, it is a collaborative effort with the pioneering team.”

Subsequent teams may leverage and reuse the platform schematic or the schematic plus layout and actual hardware components in the new products they are developing. “So after the initial work, now we get to enjoy the benefits of that investment for the coming years as we roll out the products on our road map as well as quickly create any other derivatives that we may add to the road map in the future,” Rake said.

By January 2014, the company had already rolled out two derivative products built on its initial Zynq SoC-based platform (a just-released derivative is highlighted on page 58). “We have those products out already and other derivative products will now be spinning off each of those,” Smith said. “It's really a tree that starts with this reference design as the trunk, sprouting branches, which in turn sprout other branches.”

In addition to achieving greater time-to-market efficiencies, the Zynq SoC platform is also directly impacting the bottom line. In its 2013 Q3 earnings call, NI reported that its cRIO-9068 and sbRIO (single-board) analyzer lines drove record third-quarter revenue, while the myRIO helped lead to a new Q3 revenue record for NI's academic division. Smith estimates that each derivative design costs approximately 60 percent less than the original architecture, and time-to-market is reduced by approximately 30 percent.

The costs of doing the design in an ASIC would have been far higher. 

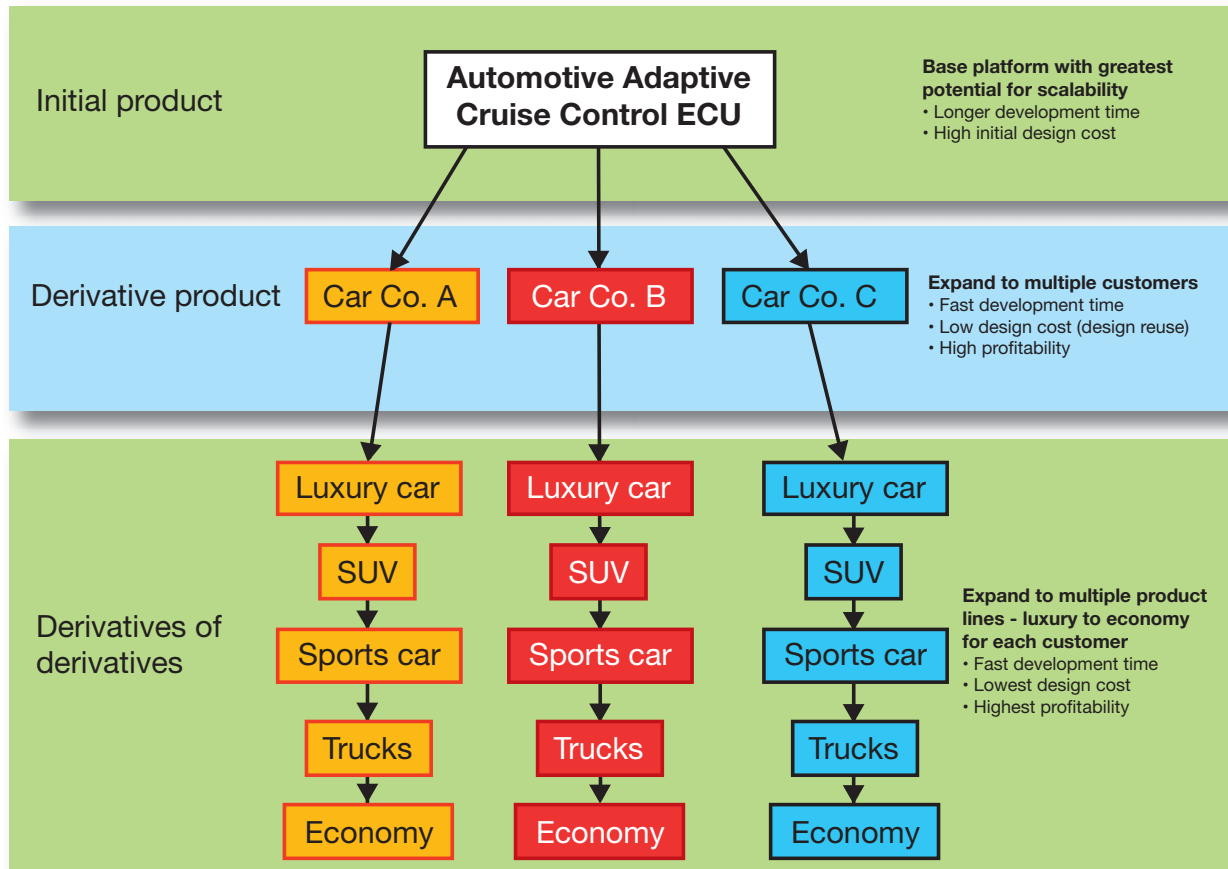


Figure 3 – A Xilinx customer has maximized its initial design investment by using a Zynq SoC platform to serve multiple carmakers and multiple lines and models for each manufacturer, improving profitability.

ASIC platform at a higher profit margin of 20 percent to a Zynq SoC platform at a 15 percent profit margin, the Zynq SoC is a far better platform solution financially as well as technically. At lower volumes, the Zynq SoC platform is of course even more convincingly the best platform choice to maximize profitability.

PROVEN PLATFORM SUCCESS WITH THE ZYNQ SOC

Today, a number of customers in a broad range of application areas are achieving dramatically greater scales of economy by leveraging the Zynq SoC as the heart of their platform strategies. A prime example is a world-renowned maker of high-end electronic control units (ECUs) for the automotive industry. This customer is stan-

dardizing on the Zynq SoC as a platform solution.

Wielding the Zynq SoC and heavily leveraging the reuse of tightly coupled hardware and software IP, the company has created a highly flexible ECU platform that it can quickly customize for the specific needs of multiple automakers and their different lines, models/configurations and accessory bundles (Figure 3). By using the Zynq SoC as a central platform, the company has achieved maximum economy of scale, reducing budgets while increasing the number of products it delivers to a growing number of customers. The upshot is delivering tailored ECUs to customers faster.

For a more detailed examination of another company using the Zynq SoC as a

profitability platform, see sidebar (“Case Study: National Instruments Achieves New Efficiencies with Zynq SoC”).

The Zynq-7000 All Programmable SoC is the best device for implementing a platform strategy for most embedded applications. With its unmatched integration between ARM processing and FPGA logic and I/O programmability, the Zynq SoC allows every level of an enterprise to harmonize their development efforts and bring highly differentiated product lines to market faster than the competition. The Zynq SoC platform is enabling these customers to achieve prolific profitability.

For more information on the Zynq SoC platform, visit <http://www.xilinx.com/products/silicon-devices/soc/zynq-7000/index.htm>.