Xilinx Ships Industry's First 20-nm All Programmable Devices
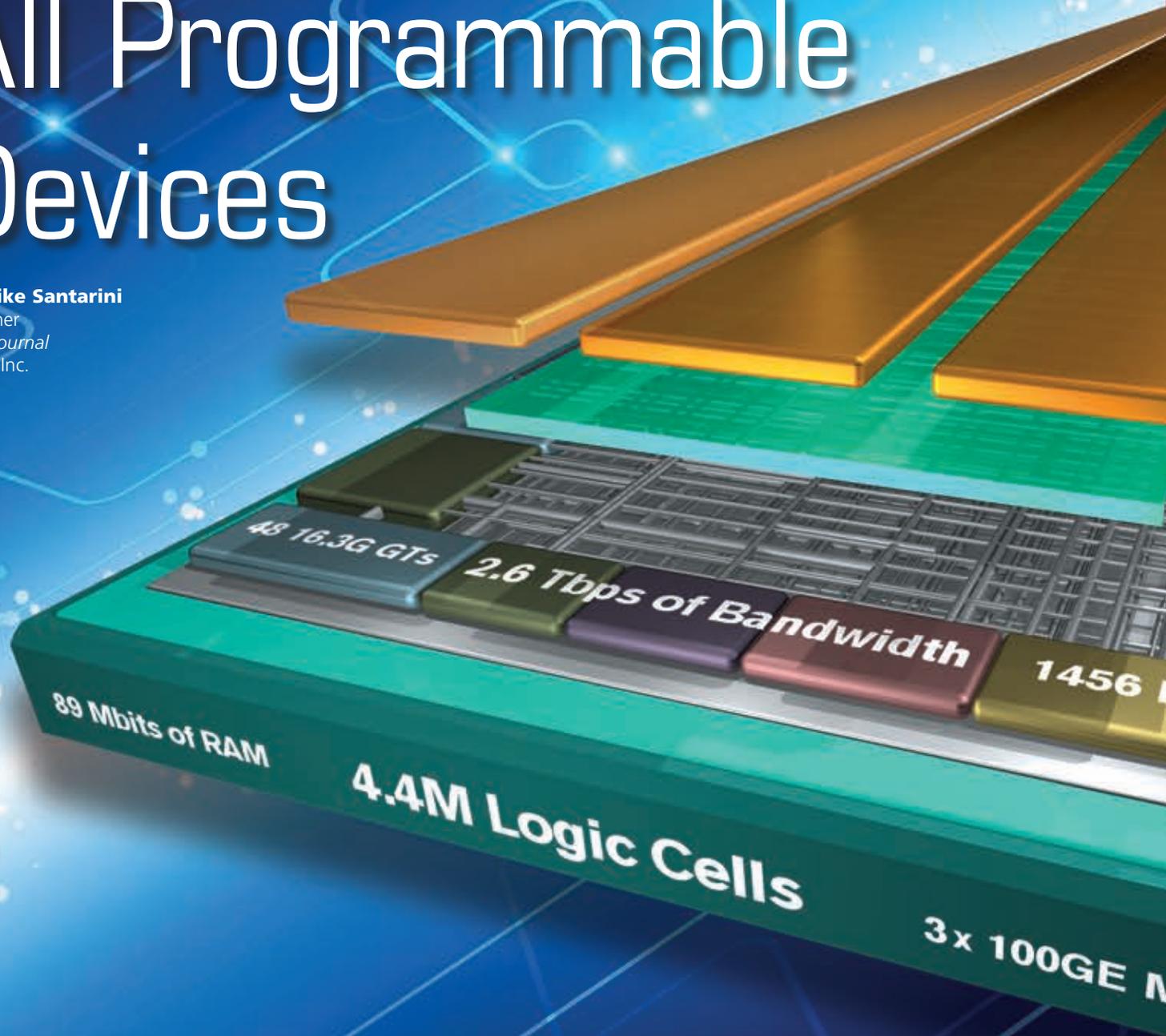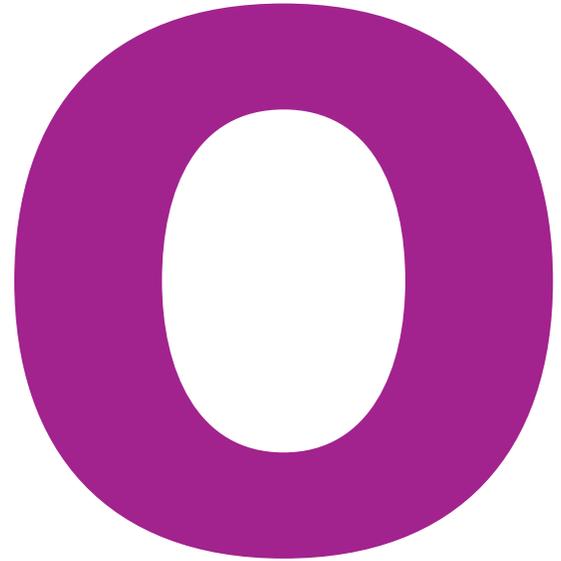
by **Mike Santarini**
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48 16.3G GTs

2.6 Tbps of Bandwidth

1456

89 Mbits of RAM

4.4M Logic Cells

3 x 100GE M

Latest product portfolio sets capacity record with 3D Virtex UltraScale FPGA containing 4.4 million logic cells.

On Nov. 11 of 2013, Xilinx accomplished a key milestone in building on its Generation Ahead advantage by shipping to customers the industry's first 20-nanometer All Programmable FPGA—a Kintex® UltraScale™ XCKU040 device—months ahead of when the competition was purporting to ship its first 20-nm devices. Then, in December, Xilinx built on that accomplishment by unveiling its entire 20-nm Kintex UltraScale and Virtex® UltraScale portfolios, the latter of which includes the Virtex UltraScale VU440. Based on 3D IC technology, this 4.4 million-logic-cell device breaks world records Xilinx already held for the highest-capacity FPGA and largest semiconductor transistor count with its 28-nm Virtex-7 2000T.

"We are open for business at 20 nm and are shipping the first of our many 20-nm UltraScale devices," said Steve Glaser, senior vice president of corporate strategy and marketing at Xilinx. "With the 20-nm UltraScale, we are expanding the market leadership that we firmly established with our tremendously successful 28-nm, 7 series All Programmable devices. Today, we are not only delivering to customers the first 20-nm devices manufactured with TSMC's 20SoC process months ahead of the competition, but are also delivering devices that leverage the industry's most advanced silicon architecture as well as an ASIC- strength design suite and methodology."

All the devices in the 20-nm Kintex UltraScale and Virtex UltraScale portfolios feature ASIC-class performance and functionality, along with lower power and higher capacity than their counterparts in Xilinx's tremendously successful 7 series portfolio (Figure 1). The 7 series devices, built at the 28-nm silicon manufacturing node, currently control more than 70

	KINTEX 7	KINTEX UltraSCALE	VIRTEX 7	VIRTEX UltraSCALE
Logic Cells (LC)	478	1,161	1,995	4,407
Block RAM (BRAM; Mbits)	34	76	68	115
DSP48	1,920	5,520	3,600	2,880
Peak DSP Performance (GMACs)	2,845	8,180	5,335	4,268
Transceiver Count	32	64	96	104
Peak Transceiver Line Rate (Gbps)	12.5	16.3	28.05	32.75
Peak Transceiver Bandwidth (Gbps)	800	2,086	2,784	5,101
PCI Express Blocks	1	6	4	6
100G Ethernet Blocks	-	1	-	7
150G Interlaken Blocks	-	2	-	9
Memory Interface Performance (Mbps)	1,866	2,400	1,866	2,400
I/O Pins	500	832	1,200	1,456

Figure 1 – The 20-nm Kintex and Virtex UltraScale FPGAs deliver industry-leading features complementary to the Kintex and Virtex 7 series devices (max counts listed).

percent of programmable logic device industry market share. What's more, with UltraScale, Xilinx has taken additional steps to refine the device architecture and make ASIC-class improvements to its Vivado® Design Suite. Last October the company introduced a streamlined methodology called the UltraFast Design Methodology (detailed in the cover story of *Xcell Journal* issue 85; *http://issuu.com/xcelljournal/docs/xcell_journal_issue_85/8?e=2232228/5349345*). Xilinx will follow up its 20-nm UltraScale portfolio with 16-nm FinFET UltraScale devices in what it calls its "multinode strategy" (Figure 2).

"We are in a multinode world now where customers will be designing in devices from either our 7 series, our UltraScale 20-nm or our upcoming UltraScale 16-nm FinFET family depending on what is the best fit for their system requirements," said Kirk Saban, product line marketing manager at Xilinx. "For example, if you compare our 20-nm Kin-

tex UltraScale devices with our Kintex-7 devices, we have significantly more logic and DSP capability in Kintex UltraScale than we had in Kintex-7. This is because a vast majority of applications needing high signal-processing bandwidth today tend to demand Kintex-class price points and densities. If the customer's application doesn't require that additional density or DSP capability, Kintex-7 is still a very viable design-in vehicle for them."

Saban said that the multinode approach gives Xilinx's broad user base the most powerful selection of All Programmable devices available in the industry, while the Vivado Design Suite and UltraFast methodology provide unmatched productivity.

"There's a misconception in the industry that Xilinx is going to be leapfrogged by the competition, which is waiting for Intel to complete its 14-nm FinFET silicon design process and then fabricate the competition's next-generation devices," said Saban. "We are

certainly not sitting still. We are already offering our 20-nm UltraScale devices, which allow customers to create innovations today. We will be offering our UltraScale FinFET devices in the same time frame as the competition. We are going to build on our Generation Ahead advantage with these devices and the ASIC-class advantage of our Vivado Design Suite and UltraFast methodology."

These advances are built on a foundation of solid manufacturing, Saban said. "We are confident we have the industry's strongest foundry partner in TSMC, which has a proven track record for delivery and reliability," he said. "Foundry is TSMC's primary business, and they manufacture devices for the vast majority of the who's who in the semiconductor industry. What's more, TSMC's former CTO, now adviser, Chenming Hu actually pioneered the FinFET process, and we are very impressed with their FinFET development for next-gen processes."

KINTEX AND VIRTEX ULTRASCALE TRANSISTOR COUNTS

Each silicon process node presents the industry with a new set of manufacturing and design challenges. The 20-nm node is no exception. This geometry introduced new challenges in terms of routing delays, clock skew and CLB packing. However, with the Kintex UltraScale and Virtex UltraScale devices, Xilinx was able to overcome these challenges and greatly improve overall performance and utilization rates. (See the sidebar, "What's the Right Road to ASIC-Class Status for FPGAs?")

The intricacies of the node also allowed Xilinx to make several block-level improvements to the architecture, all of which Xilinx co-optimized with its Vivado tool suite to deliver max-

imum bandwidth and maximum signal-processing capabilities.

"If we have a closer look at our DSP innovations, we've gone to a wider-input multiplier, which allows us to use fewer blocks per function and deliver higher precision for any type of DSP application," said Saban. "We also included some additional features for our wireless communications customers in terms of FEC, ECC and CRC implementations now being possible within the DSP48 itself."

On the Block RAM front, Xilinx hardened the data cascade outputs and improved not only the power, but also the performance of BRAM with some new, innovative hardened features.

Xilinx is offering two different kinds of transceivers in the 20-nm Kintex and Virtex UltraScale portfolios. Mid- and

high-speed-grade Kintex UltraScale devices will support 16.3-Gbps backplane operation. Even the slowest-speed-grade devices in the Kintex UltraScale family will offer impressive transceiver performance at 12.5 Gbps, which is particularly important for wireless applications. Meanwhile, in its Virtex UltraScale products, Xilinx will offer a transceiver capable of 28-Gbps backplane operation, as well as 33-Gbps chip-to-chip and chip-to-optics interfacing.

"We've added some significant integrated hard IP blocks into UltraScale," said Saban. "We've added a 100-Gbps Ethernet MAC as hard IP to both the Virtex and Kintex UltraScale family devices. We also added to both of these UltraScale portfolios hardened 150-Gbps Interlaken interfaces and hardened PCI Ex-

Past
Single Node, Only FPGAs

FPGA 130nm > **FPGA 90nm** > **FPGA 45/40nm**

Future
Concurrent Nodes with FPGAs, SoCs and 3D ICs

28nm: Long life with optimal price/performance/watt and SoC integrations

Open for business!
20nm: Complements 28nm for new high-performance architectures

16nm: Complements 20nm with FinFET, multiprocessing, memory
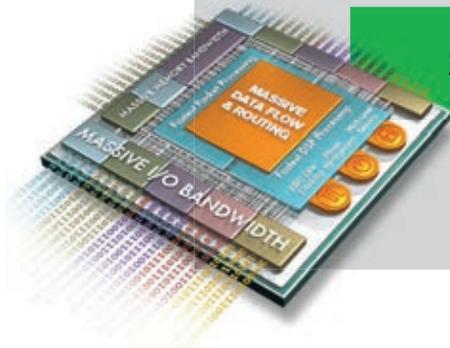
Figure 2 – Xilinx's Generation Ahead strategy favors multinode product development, with the concurrent release of FPGA, SoC and 3D IC product lines on nodes best suited for customer requirements.