XAPP1057 (v1.0) April 3, 2008

# Reference System: PLBv46 PCI Using the RaggedStone1 Evaluation Board

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## Summary

This application note describes how to build a reference system for the Processor Local Bus Peripheral Component Interconnect (PLBv46 PCI) core using the MicroBlaze™ processor-based embedded system in the RaggedStone1 Evaluation Board. The RaggedStone1 Evaluation Board uses the Spartan™-3 FPGA and has a PCI connector.

A set of files containing Xilinx Microprocessor Debugger (XMD) commands is provided for writing to the Configuration Space Header and for verifying that the PLBv46 PCI core is operating correctly. Two software projects illustrate how to configure the PLBv46 PCI cores, set up interrupts, scan configuration registers, and set up and use DMA operations. The procedure for using ChipScope™ Pro Analyzer to analyze PLBv46 PCI functionality is provided.

## Included Systems

This application note includes one reference system:

www.xilinx.com/support/documentation/application_notes/xapp1057.zip

The project name used in xapp1057.zip is rs1_mb_plbv46_pci.

## Required Hardware and Tools

Users must have the following tools, cables, peripherals, and licenses available and installed. EDK provides an evaluation license for PLBv46 PCI.

- Xilinx EDK 9.2.02i
- Xilinx ISE™ 9.2.04i
- Xilinx Download Cable (Board Cable USB or Parallel Cable IV)
- Model Technology ModelSim v6.1e
- ChipScope 9.2.01
- PLBv46 PCI License
- RaggedStone1 Evaluation Board

## Introduction

PCI transactions are done between an initiator and a target. This reference design is for the RaggedStone1 Spartan-3 Evaluation Board. To be useful, it must be inserted into a PCI slot. In the examples provided in this application note, the RaggedStone1 Spartan-3 Evaluation Board is inserted into PCI slot P3 of the Xilinx ML410 Evaluation Platform. This allows both configuration and memory transactions to be done on the PCI bus between an initiator and a target. The examples use the ML410 PLBv46 PCI as the initiator and the RaggedStone1 Spartan-3 Evaluation Board PLBv46 PCI as the target. It is relatively easy to modify the examples so that the initiator and target functions are swapped.

Figure 1 is a functional diagram of the RaggedStone1 Board interfacing to the ML410 Evaluation Platform.

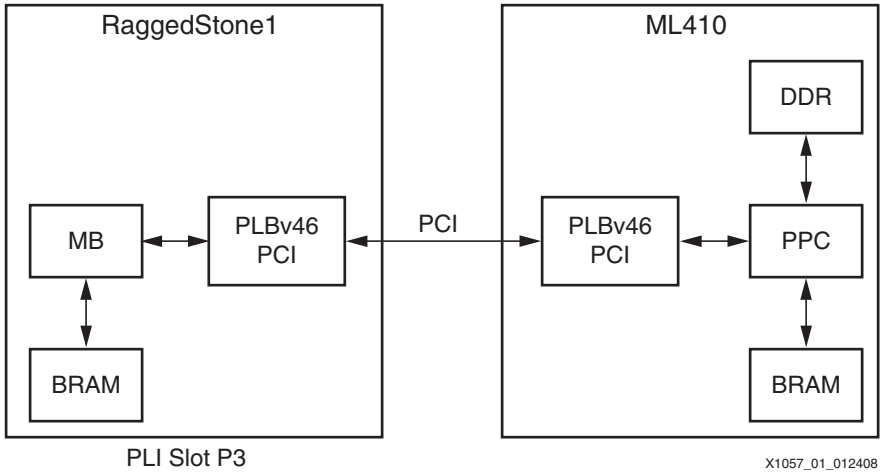


*Figure 1:* **Interfacing RaggedStone1 Spartan-3 PLBv46 PCI with ML410 PLBv46 PCI**

Figure 2 is the RaggedStone1 Evaluation Board.

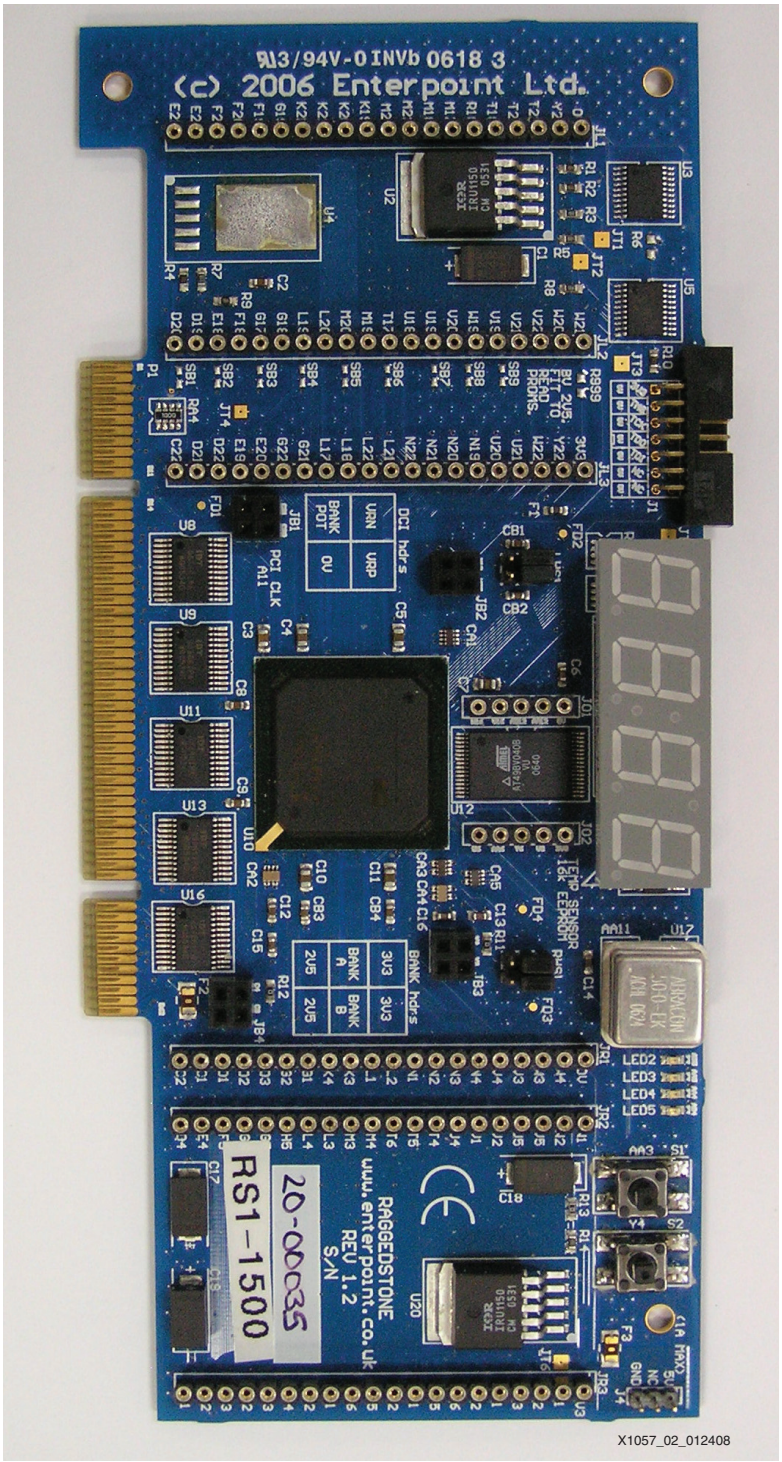


*Figure 2:* **RaggedStone1 Evaluation Board**

Figure 3 is a block diagram of the reference system.

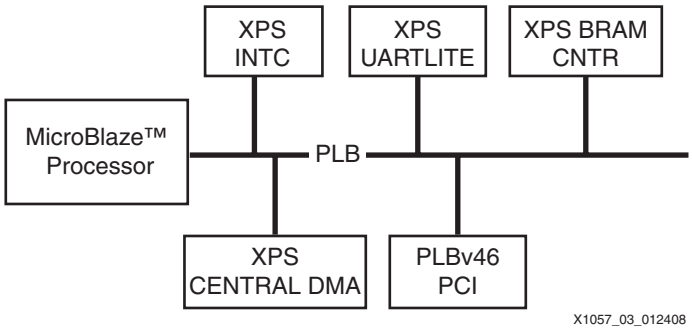


*Figure 3:* **RaggedStone1 Spartan-3 PLBv46 PCI Reference System Block Diagram**

The RaggedStone1 Spartan-3 Evaluation Board has a PCI edge connector on one side of the board. Three variations of the RaggedStone1 Spartan-3 Evaluation Board differ in the use of the XC3S400, XC3S1000, or XC3S1500, each in a 456 pin package.

The functions, devices, and buses in this PLBv46 PCI reference design are addressed using the Configuration Address Port format shown in Figure 4.

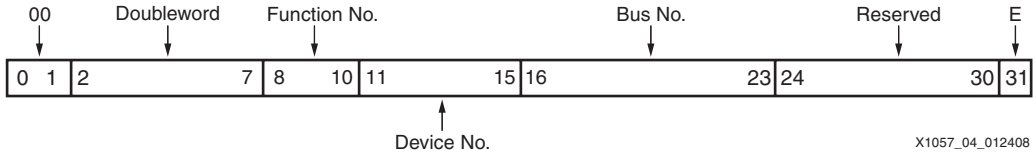


*Figure 4:* **Configuration Address Port Format**

The Configuration Address Port and Configuration Data Port registers in the host bridge PLBv46 PCI Bridge are used to configure multiple PCI bridges when host bridge configuration is enabled. The bit definitions of the Configuration Address Port in the big endian format used by the PLB are given in Table 1.

*Table 1:* **Configuration Address Port Register Definitions**

| Bit | Definition |
|---|---|
| 0-5 | Target word address in configuration space |
| 6-7 | Hardwired to 0 |
| 8-12 | Device |
| 13-15 | Function |
| 16-23 | Bus Number |
| 24 | Enable |
| 25-31 | Hardwired to 0 |

# Reference System Specifics

In addition to the MicroBlaze processor and PLBv46 PCI, this system includes BRAM memory, UART, MDM, XPS Central DMA, and interrupt controller. The PCI Arbiter core is included in the FPGA.

## RaggedStone1 Spartan-3 FPGA PCI Evaluation Board

In the reference design, the PLBv46 PCI in the XC3S1500 on the RaggedStone1 Spartan-3 Evaluation Board interfaces to the PLBv46 PCI in the Virtex-4 ML410 Evaluation Board.

Table 2 provides the address map for the XC3S1500.

*Table 2:* **RaggedStone1 Spartan-3 Address Map**

| Peripheral | Instance | Base Address | High Address |
|---|---|---|---|
| XPS UART Lite | RS232_Uart_1 | 0x84000000 | 0x8400FFFF |
| PLBv46 PCI | plbv46_pci_0 | 0x42600000 | 0x4260FFFF |
| MDM | debug_module | 0x84400000 | 0x8440FFFF |
| XPS INTC | xps_intc_0 | 0x81800000 | 0x8180FFFF |
| XPS CENTRAL DMA | xps_central_dma_0 | 0x81810000 | 0x8181FFFF |
| XPS BRAM | xps_bram_if_cntlr_1 | 0x8AE08000 | 0x8AE0FFFF |

The RaggedStone1 Spartan-3 1500 Evaluation Board includes a 64-bit PCI edge connector, RS232C port, LED displays, Atmel 512K x 8 AT49BV040A Flash Memory, and a JTAG port. The MicroBlaze microprocessor runs at 75 MHz.

The application note XAPP1001 Reference System: PLBv46 PCI in a ML410 Embedded Development Platform provides a link to the hardware design files used for the ML410.

## Configuration of the PLBv46 PCI on the ML410 Board

The PLBv46 PCI bridge uses the 32-bit Xilinx LogiCORE™ PCI32 Interface v3.0 core. For the PLBv46 PCI bridge to perform transactions on the PCI bus, the v3.0 core must be configured using configuration transactions from either the PCI-side or the PLBv46 side. In this system, the ML410 PLBv46 PCI is the host bridge, and it configures itself and then configures the RaggedStone1 Spartan-3 Evaluation Board PLBv46 PCI. The C_INCLUDE_PCI_CONFIG parameter is set to 1.The IDSEL input of the v3.0 is connected to address ports, and the PLBv46 PCI IDSEL port is unused.

To configure the XC4VFX60 with the bitstream, connect the Xilinx download cable to the ML410 JTAG port, and use Impact to download the `ML410 download.bit` file.

Do the following steps to write to the configuration header.

1. Configure the Command and Status Register. The minimum that must be set is the Bus Master Enable bit in the command register. For memory transactions, set the memory space bit. For I/O transactions, set the I/O space bit.
2. Configure the Latency Timer to a non-zero value.
3. Configure at least one BAR. Configure subsequent BARs as needed for other memory/IO address ranges.

The v3.0 core configures itself only after the Bus Master Enable bit is set and the latency timer is set to avoid time-outs. If the v3.0 core latency timer remains at the default 0 value, configuration writes to remote PCI devices do not complete, and configuration reads of remote PCI devices terminate due to the latency timer expiration. Configuration reads of remote PCI devices with the latency timer set to 0 return `0xFFFFFFFF`.

## ML410 XC4VFX60 Address Map

The address map of the ML410 XC4VFX60 is shown in Table 3.

*Table 3:* **ML410 XC4VFX60 System Address Map**

| Peripheral | Instance | Base Address | High Address |
|---|---|---|---|
| MPMC3 | DDR_SDRAM_32Mx64 | 0x00000000 | 0x03FFFFFF |
| XPS UART16550 | RS232_Uart_1 | 0x83E00000 | 0x83E0FFFF |
| XPS INTC | XPS_INTC_0 | 0x81800000 | 0x8180FFFF |
| PLBv46_PCI | PCI32_Bridge | 0x85E00000 | 0x85E0FFFF |
| XPS Central DMA | xps_central_dma_0 | 0x80200000 | 0x8020FFF |
| XPS BRAM | xps_bram_if_cntlr_0 | 0xFFFF0000 | 0xFFFFFFFF |
| XPS GPIO | LEDs_8Bit | 0x81400000 | 0x8140FFFF |
| XPS SysAce | SysACE_CompactFlash | 0x83600000 | 0x8360FFFF |
| XPS IIC | IIC_Bus | 0x81600000 | 0x8160FFFF |

## RaggedStone1 Spartan-3 PLBv46 PCI Generics

The reference design contains the following settings for Spartan 3 PLBv46 PCI generics:

C_FAMILY = spartan3

C_INCLUDE_PCI_CONFIG = 0

C_INCLUDE_BAROFFSET = 0

C_IPIFBAR_NUM = 2

C_PCIBAR_NUM = 2

C_IPIFBAR_0 = 0x20000000

C_IPIFBAR2PCIBAR_0 = 0x80000000

C_IPIFBAR_1 = 0xE8000000

C_IPIFBAR2PCIBAR_1 = 0x90000000

When C_FAMILY is defined as Virtex4 or Spartan3, the PLBv46 PCI uses the v3.0 PCI LogiCORE IP. When C_FAMILY is defined as Virtex5, the PLBv46 PCI uses the v4.0 PCI LogiCORE IP.

Figure 5 shows how to specify the values of the Base Address Registers (BARs) in EDK.

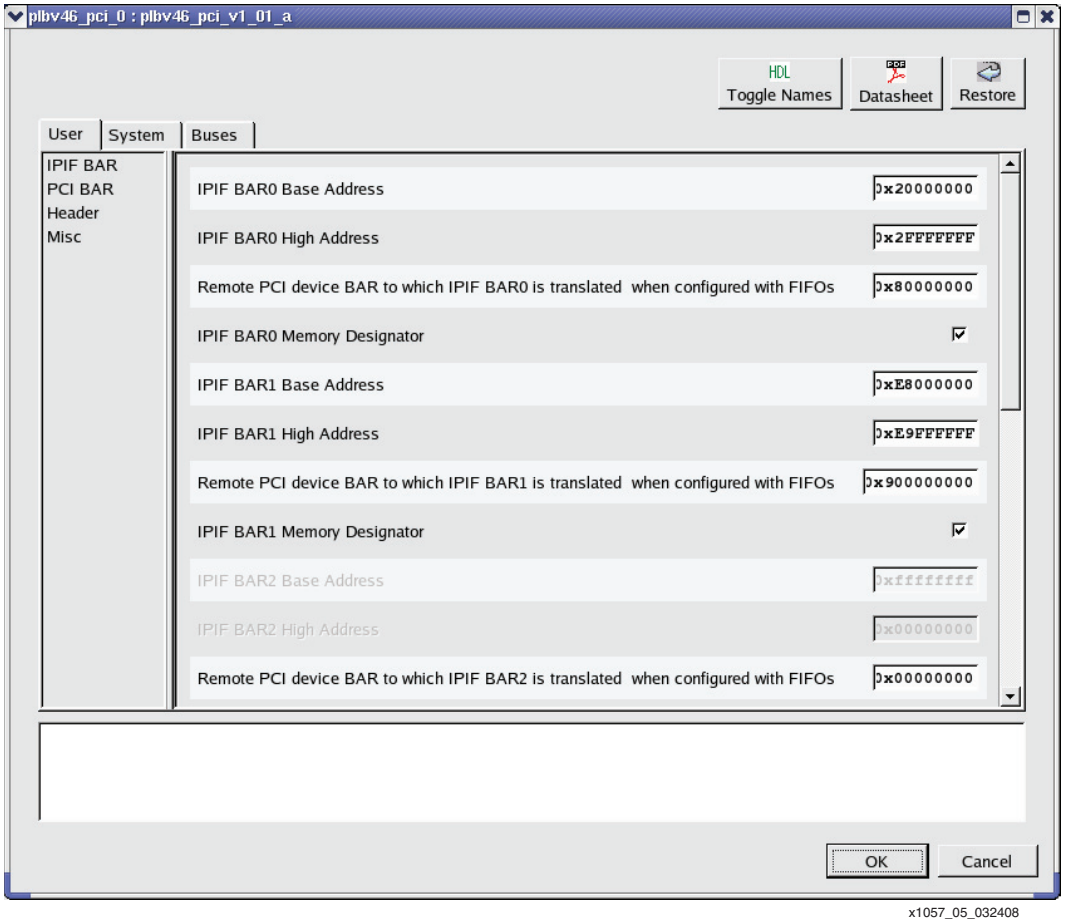


*Figure 5:* **Specifying the Values of Base Address Register Generics in EDK**

Since the ML410 does the configuration in this setup, set C_INCLUDE_PCI_CONFIG to 0. When C_INCLUDE_BAR_OFFSET = 0, the C_IPIFBAR2PCIBAR_* generic(s) are used in address translation instead of IPIFBAR2PCIBAR_* registers. Setting C_IPIFBAR_NUM = 2 specifies that there are two address ranges for PLB to PCI transactions. Setting C_PCIBAR_NUM = 2 specifies that two address ranges are used for PCI to PLBv46 transactions.

Figure 6 provides a functional diagram of the PLBv46 PCI core. The functions in the PLBv46 PCI are the PLBv46 Master, PLBv46 Slave, v3.0 PCI Core, and the IPIF/v3.0 Bridge.

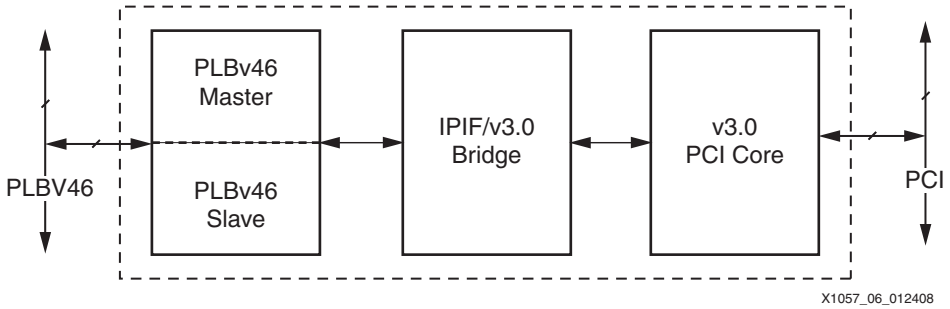


*Figure 6:* **PLBv46 PCI Functional Diagram**

## Configuration of PLBv46 PCI on the RaggedStone1 Evaluation Board

When the RaggedStone1 Spartan-3 FPGA Board is inserted into the ML410 PCI slot P3, the PLBv46 PCI Bridge in the XC4VFX60 FPGA interfaces to an PLBv46 PCI Bridge in the XC3S1500 FPGA on the RaggedStone1 Spartan-3 Board. To configure the XC3S1500, connect the Xilinx download cable to the RaggedStone1 Spartan-3 FPGA Board JTAG port, and use Impact to download the `rs1_mb_plbv46_pci/ready_for_download/download.bit` file.

After downloading the XC3S1500 FPGA bit file, the PCI functionality in the XC3S1500 PLBv46 PCI is configured using Configuration write PCI transactions from the ML410 PLBv46 PCI.

## Executing the Reference System using the Pre-Built Bitstream and the Compiled Software Applications

Use the steps below to execute the system using files inside the `rs1_mb_plbv46_pci/ready_for_download` directory.

1. Change to the `rs1_mb_plbv46_pci/ready_for_download` directory.
2. Use iMPACT to download the bitstream.
   **`impact -batch etc/xapp1057.cmd`**
3. Invoke XMD and connect to the MicroBlaze processor.
   **`xmd -opt etc/xapp1057.opt`**
4. While the PLBv46 PCI in the RaggedStone1 board can act as the host bridge, this reference design uses the PLBv46 PCI in the ML410 as the host bridge. Connect the JTAG cable to the ML410. Download the bitstream. Download the executable.
   **`dow ml410_ppc_plbv46_pci/ready_for_download/hello_pci.elf`**

## Executing the Reference System from EDK

To execute the system using EDK, follow these steps:

1. Select **File Open Project** system.xmp.
2. Select **Hardware** → **Generate Bitstream** to generate a bitstream
3. Download the bitstream to the board using **Device Configuration** → **Download Bitstream**.
4. Invoke XMD with **Debug** → **Launch XMD**.
5. While the PLBv46 PCI in the RaggedStone1 board can act as the host bridge, this reference design uses the PLBv46 PCI in the ML410 as the host bridge. Connect the JTAG cable to the ML410. Download the bitstream. Download the executable using command:
   **`dow ml410_ppc_plbv46_pci/ready_for_download/hello_pci.elf`**

## Verifying the Reference Design with the Xilinx Microprocessor Debugger

After downloading the bitstream file and writing to the configuration header, verify that the RaggedStone1 Spartan-3 reference design is set up correctly.

1. Configure the v3.0 Command Register, Latency Timer, and BAR(s).
2. Read the configuration header.
3. Configure the Command Register, Latency Timer, and BAR(s) of the other devices in the system.
4. Read the configuration headers of the other devices in the system.
5. Perform a memory read of one of the IPIF BARs.
6. Perform a memory write of one of the IPIF BARs.

Verification is done using either Xilinx Microprocessor Debugger (XMD) or the software projects discussed later. TCL scripts using XMD commands are provided in the `rs1_mb_plbv46_pci/xmd_commands` directory. The `410_s3.tcl` script configures and verifies the ML410 and Spartan-3 PLBv46 PCI cores. To run this script, connect the Platform CABLE_USB cable to the ML410 JTAG connector, and enter **`xmd -tcl xmd_commands/410_s3.tcl`** at the command prompt.

The XMD commands in the `410_s3.tcl` file, partially listed in Figure 7, write to the Configuration Address Port and the Configuration Data Port to program the Configuration Space Header. The Command/Status Register, Latency Timer, and Base Address Registers are written and read.

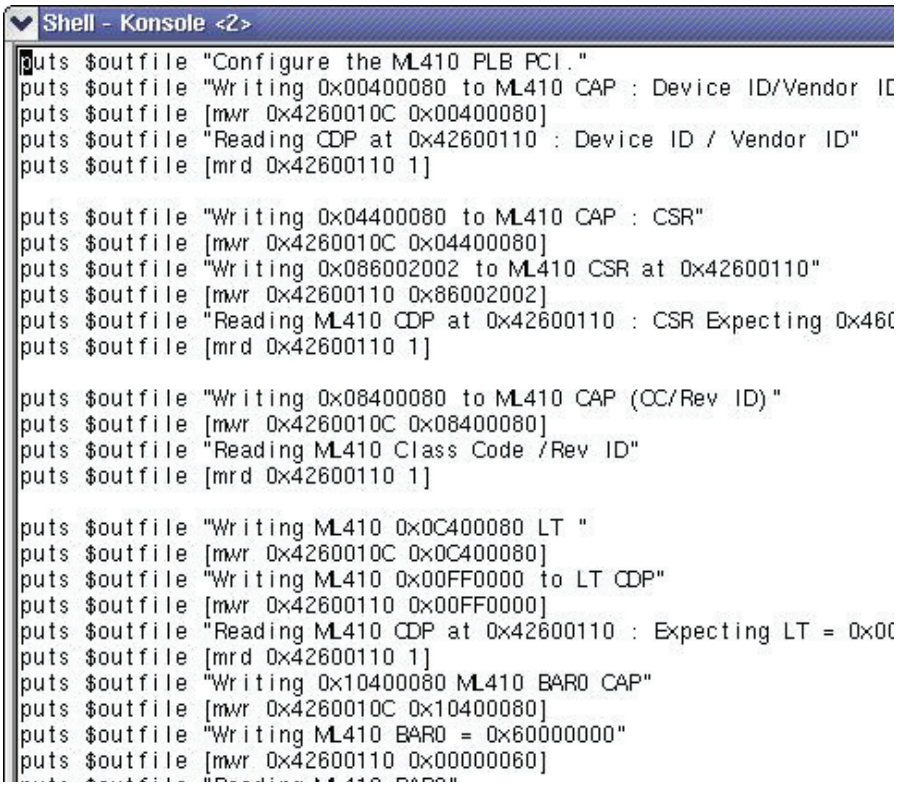


*Figure 7:* **XMD Commands Used in Configuration**

## Software Projects

The reference system contains the following software projects.

**hello_pci:** This project enables master transactions, sets the latency timer, defines the bus number/subordinate bus number, and scans the PCI bus configuration space headers.

**pci_dma:** This project runs DMA operations. The user sets the source address, destination address, and DMA length. This code is used for DMA operations between a variety of source and destination addresses. Figure 8 shows some of the parameters in `pci_dma.c` which can be edited to run DMA transactions between different memory regions.

```
#define MEM_0_BASEADDR 0x20000000
#define MEM_1_BASEADDR 0x20002000

..

DMALength = 1024
```

X1057_08_012408

*Figure 8:* **Defining Source and Destination Addresses, Length in pci_dma.c**

### DMA Transactions

Many of the XMD scripts and C code examples generate Direct Memory Access (DMA) operations. DMA transactions are initiated by writing to the Control, Source Address, Destination Address, and Length registers of the DMA controller. Table 4 provides these register locations of the XPS Central DMA controller.

*Table 4:* **XPS Central DMA Registers**

| | |
|---|---|
| Control Register | C_BASEADDR + 0x04 |
| Source Address Register | C_BASEADDR + 0x08 |
| Destination Address Register | C_BASEADDR + 0x0C |
| Length Register | C_BASEADDR + 0x10 |

An example of XMD code which generates DMA transactions is given in Figure 9.

```
# Write DMA Control Register
mwr 0x80200004 0xC0000004
# Write DMA Source Address Register
mwr 0x80200008 0x20000000
# Write DMA Destination Address Register
mwr 0x8020000C 0x20002000
# Write DMA Length
mwr 0x80200010 64
```

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*Figure 9:* **Generating DMA Transactions**

The `pci_dma.c` code consists of the four functions in the functional diagram in Figure 10.

1. The Barberpole Region function provides a rotating data pattern on the memory located at the source address.
2. The Zero Region function sets the memory located at the destination address to all zeroes.
3. The DMA Region function performs a DMA transaction of data located at the source address to the memory at the destination address.
4. The Verify function verifies that data at the source address and destination address are equal.

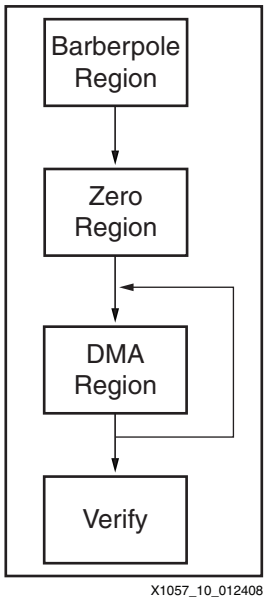


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*Figure 10:* **Functional Diagram of pci_dma.c**

Figure 11 show the Hyperterminal output when running the `pci_dma/executable.elf`.

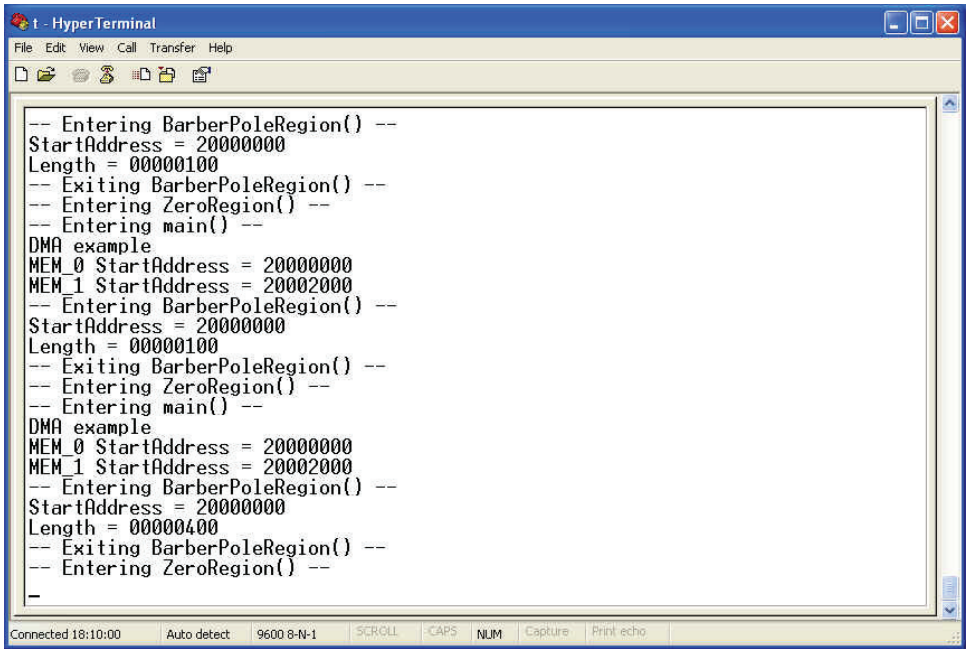


*Figure 11:* **pci_dma.c output**

## Running the Applications

The selection of the hello_pci project is shown in Figure 12. Make the hello_pci project active and the remaining software projects inactive.

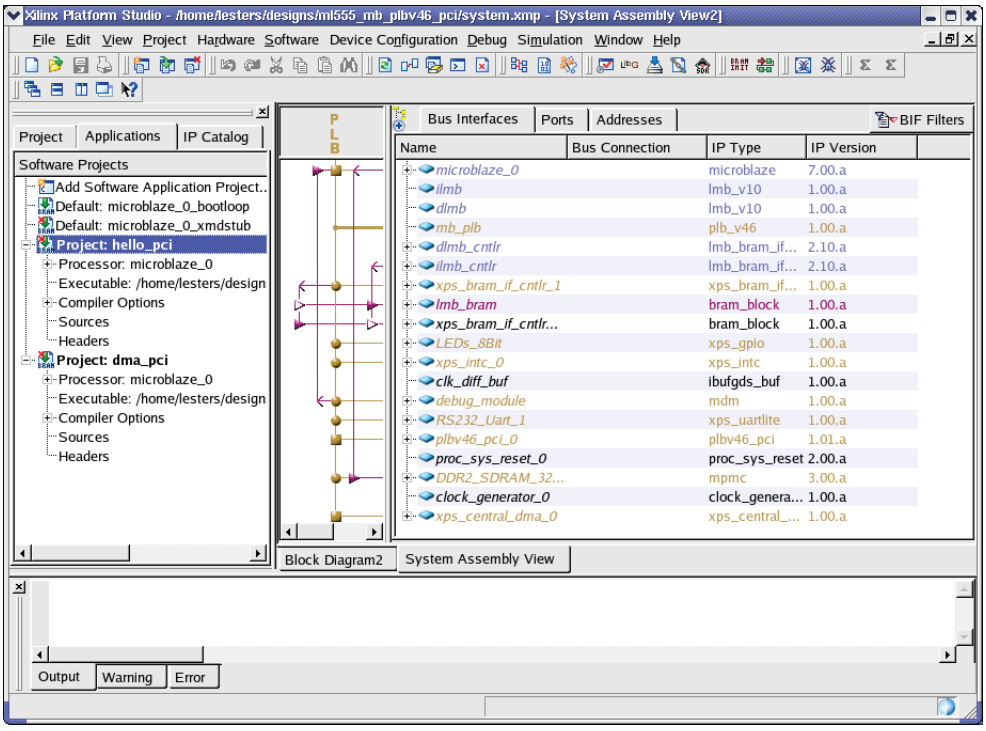


*Figure 12:* **Selecting the hello_pci Software Project**

With hello_pci selected, right click to build the project. Connect a serial cable to the RS232C port on the ML410 board. Start a HyperTerminal session. Set Bits per second to **9600**, Data bits to **8**, Parity to **None**, and Flow Control to **None**, as shown in Figure 13.

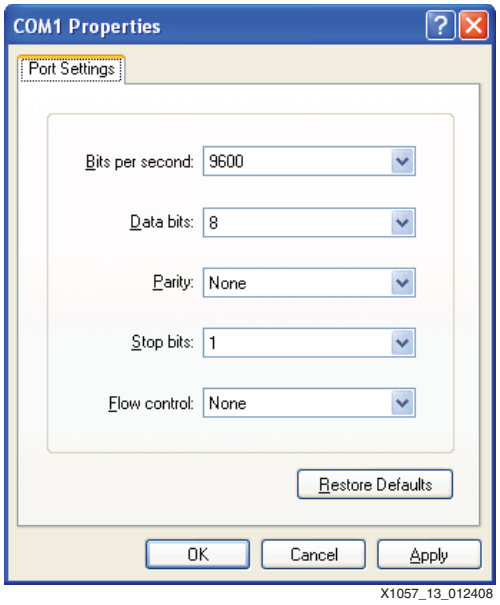


*Figure 13:* **HyperTerminal Parameters**

From XPS, start **XMD** and enter **connect ppc hw** and **rst** at the XMD prompt. Invoke GDB and select **Run** to start the application as shown in Figure 14. The `hello_pci.c` code, originally written for the ML310 Embedded Development Platform, runs without any modifications on this reference system.

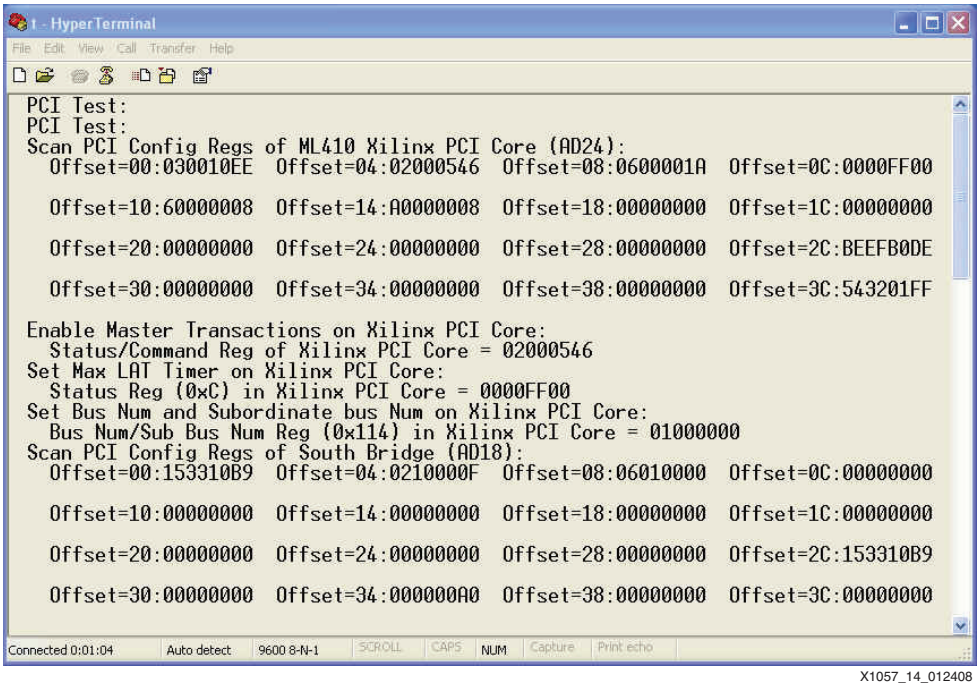


*Figure 14:* **Running hello_pci**

## Using ChipScope with PLBv46 PCI

Because of limited JTAG BSCAN resources, using ChipScope Inserter in a Spartan-3 FPGA usually results in overmapping errors. To avoid these errors, the ICON and the IBA and ILA cores are included in the MHS file, and the design is implemented just as when the ChipScope cores are not included.

Figure 15 shows the use of ChipScope cores in the MHS file.

```
BEGIN chipscope_icon
 PARAMETER INSTANCE = chipscope_icon_0
 PARAMETER HW_VER = 1.01.a
 PARAMETER C_NUM_CONTROL_PORTS = 1
 PARAMETER C_SYSTEM_CONTAINS_MDM = 1
 PORT control0 = chipscope_plbv46_iba_0_icon_ctrl
 ORT control1 = chipscope_plbv46_iba_0_icon_ctrl
END

BEGIN chipscope_ila
 PARAMETER INSTANCE = chipscope_ila_0
 PARAMETER HW_VER = 1.01.a
 PARAMETER C_TRIG0_UNITS = 1
 PARAMETER C_TRIG0_TRIGGER_IN_WIDTH = 1
 PARAMETER C_NUM_DATA_SAMPLES = 512
 PARAMETER C_DATA_SAME_AS_TRIGGER = 0
 PARAMETER C_DATA_IN_WIDTH = 50
 PARAMETER C_ENABLE_TRIGGER_OUT = 1
 PARAMETER C_ENABLE_TRIGGER_OUT = 0
 PORT chipscope_ila_control = chipscope_ila_0_icon_control
 PORT DATA = PCI_monitor & RS232_Interrupt & CDMA_Interrupt
 PORT CLK = sys_clk_s
 PORT TRIG0 = PCI_monitor[0]  & CDMA_Interrupt & mb_plb_
 PLB_PAValid & mb_plb_PLB_MAddrAck
 PORT TRIG0 = PCI_monitor[0]
END


BEGIN chipscope_plbv46_iba
 PARAMETER INSTANCE = chipscope_plbv46_iba_0
 PARAMETER HW_VER = 1.00.a
 PARAMETER C_NUM_DATA_SAMPLES = 512
 PARAMETER C_USE_MU_5_RD_DBUS = 1
 PARAMETER C_USE_MU_4_WR_DBUS = 1
 PARAMETER C_MU_1_TRIG_IN_WIDTH = 1
 BUS_INTERFACE MON_PLB = mb_plb
 PORT chipscope_icon_control = chipscope_plbv46_iba_0_icon_ctrl
 PORT PLB_Clk = sys_clk_s
END
```

X1057_15_012408

*Figure 15:* **Instantiating ChipScope cores in MHS file**

The PCI_Monitor signals are the PCI bus signals: AD, CBE, and the remaining PCI Bus signals. Table 5 defines the functionality of the PCI_Monitor signals. The Filter Pattern *PCI_Monitor* is used to locate the PCI bus signals.

*Table 5:* **PCI Monitor Signals**

| Bit Position | PCI Signal |
|---|---|
| 0 | FRAME_N |
| 1 | DEVSEL_N |
| 2 | TRDY_N |
| 3 | IRDY_N |
| 4 | STOP_N |
| 5 | IDSEL_int |
| 6 | INTA |
| 7 | PERR_N |
| 8 | SERR_N |
| 9 | Req_N_toArb |
| 10 | PAR |
| 11 | REQ_N |
| 12:43 | AD |
| 44:47 | CBE |

To begin debugging, invoke ChipScope Pro Analyzer by selecting

**Start → Programs → ChipScope Pro → ChipScope Pro Analyzer**

Click on the Chain icon located at the top left of Analyzer GUI. Verify that the message in the transcript window indicates that an ICON is found.

The ChipScope Analyzer waveform viewer displays signals named `DATA*`. To replace the `DATA*` signal names with the signal names, select **File → Import** and enter the ila and iba cdc files from the implementation directory in the dialog box.

The Analyzer waveform viewer is more readable when buses rather than discrete signals are displayed. Select the **PLB_ABus<*>** signals, click the right mouse button, and select **Add to Bus → New Bus**. With PLB_ABus<0:31> in the waveform viewer, select and remove the 32 discrete **PLB_ABus<*>** signals.

Repeat this for the PLB data buses. Make PCI Bus signals by creating a new bus for PCI_Monitor(44:47). Rename PCI_Monitor(44:47) PCI_CBE. Make PCI Bus signals for PCI_Monitor(12:43) and rename it PCI AD.

***Note:*** The Reverse Bus Order operation is useful for analyzing bus signals.

1. Set the trigger in the Trigger Setup window. The trigger used depends on the problem being debugged. For example, if debugging a configuration transaction from the ML410 PLB, trigger on an PLB address of C_BASEADDR + 0x10C. If debugging a problem configuring from the PCI side, trigger on the PCI_Monitor(44:47) for a configuration write on PCI_CBE. Change the Windows to N samples to a setting of **500**. Arm the trigger by selecting **Trigger Setup → Arm**, or clicking on the **Arm** icon.
2. Run **XMD** or **GDB** to activate trigger patterns which cause ChipScope to display meaningful output. For example, set the trigger to PA_Valid = **1**, and run `xmd -tcl 410_s3.tcl` at the command prompt.

3. ChipScope results are analyzed in the waveform window as shown in Figure 16. This figure shows the original PCI_monitor<*> signals and the PCI_monitor_ad signal generated. The waveforms may be easier to read if the discrete PCI_monitor<*> signals are removed after they are renamed.

   To share the results with other users, save the results in the waveform window as a Value Change Dump (vcd) file. The vcd files can be translated and viewed in most simulators. The `vcd2wlf` translator in ModelSim reads a vcd file and generates a ModelSim waveform log file (wlf) file for viewing in the ModelSim waveform viewer. The vcd file can be opened in the Cadence Design System, Inc. Simvision design tool by selecting **File** → **Open Database**.

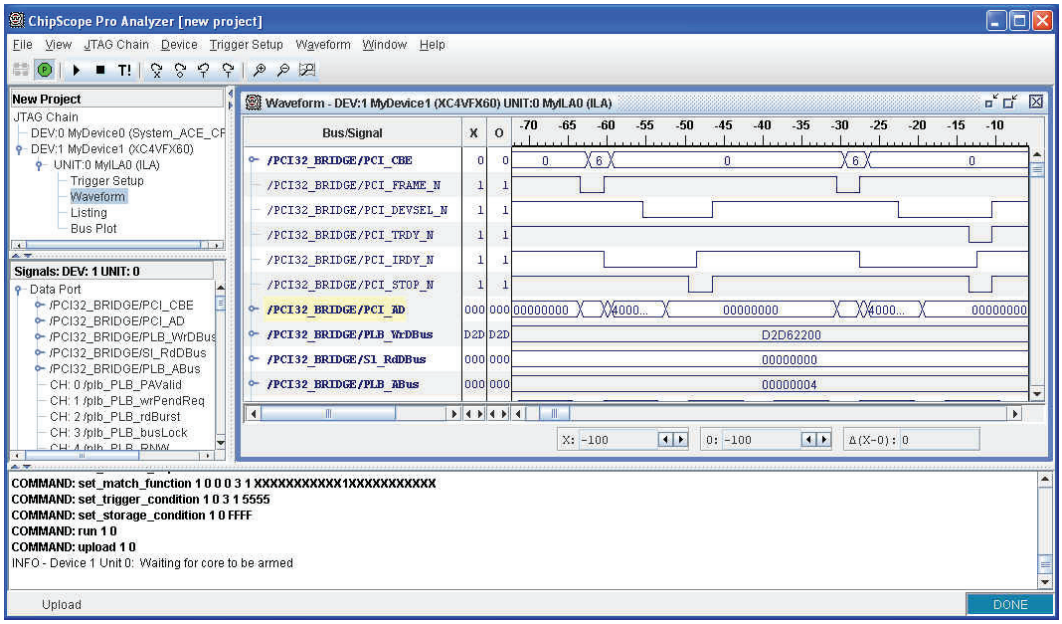


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*Figure 16:* **ChipScope Analyzer Results**

## References


1. DS207 *PCI 64/32 Interface v3.0 Data Sheet*
2. UG159 *LogiCORE IP Initiator/Target v3.1 for PCI*
3. UG262 *LogiCORE IP Initiator/Target v4.5 for PCI*
4. UG085 *ML410 Embedded Development Platform User Guide*
5. UG044 *ChipScope ILA Tools Tutorial*
6. UG241 *OPB PCI v1.02a User Manual*
7. XAPP1001 *PLBv46 PCI Using the ML410 Embedded Development Platform*
8. XAPP998 *PCI Bus Performance Measurements using the Vmetro Bus Analyzer*
9. *RaggedStone1 User Manual* *Issue 1.03 4/1/2006 Enterpoint Ltd*


## Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|---|---|---|
| 4/03/08 | 1.0 | Initial Xilinx release. |

## Notice of Disclaimer