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# Physical Layer HDMI Receiver Using GTP Transceivers

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## Summary

The High-Definition Multimedia Interface™ (HDMI) I/O standard utilizes a 3.3V terminated transition minimized differential signaling (TMDS) standard. Although TMDS signaling can be received natively using the Spartan®-6 FPGA SelectIO™ interface, using the GTP transceivers can increase performance. The focus of this is application note is on techniques to enable systems using the higher bandwidth capability of GTP receivers.

It is possible to use an external passive network to adapt the GTP transceivers to receive a signal that is compliant with HDMI technology. In this application note, two alternative passive networks are presented, analyzed, and compared from both a theoretical and a practical point of view. Both networks were tested on a custom development board to explore their signal integrity limits and to confirm theoretical expectations.

Although the results are general, the chip-to-chip use case is the one primarily considered in this application note. The target data rate used for HDMI is 1.45 Gb/s.


## Introduction

Figure 1 shows the conceptual schematic of an HDMI differential pair as described in the HDMI Specification 1.4a, Section 4.2.1[Ref 1]. In Figure 1, $AV_{CC}$ is expected to be 3.3V.

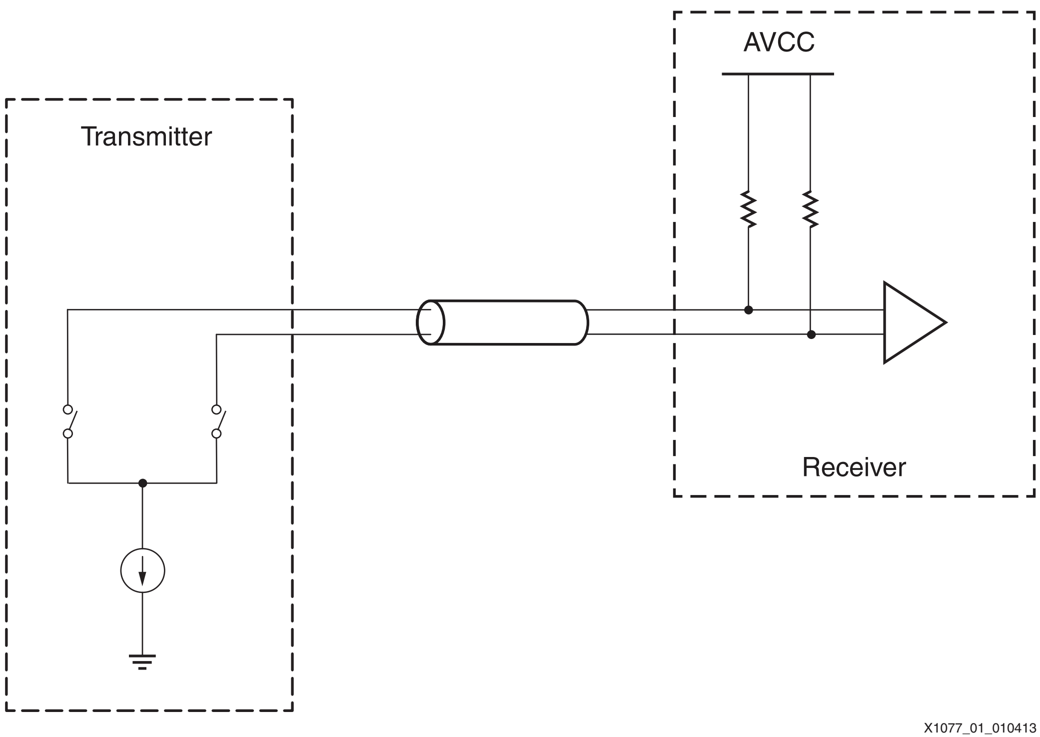


*Figure 1:* **Conceptual Schematic of a TMDS Differential Pair**

Because the $AV_{CC}$ is limited to 1.2V in Spartan-6 devices, the GTP receiver cannot be used directly to receive the HDMI data. A passive external network can be used to overcome this limitation.

Passive Network Examples describes two alternative examples and compares them from both a theoretical and practical point of view. Measurements shows the measurement results that are correlated in Conclusion with the theoretical expectations.

# Passive Network Examples

The following sections provide detailed descriptions of two types of passive networks.

## Passive Network Example 1

Figure 2 illustrates the first passive network example.

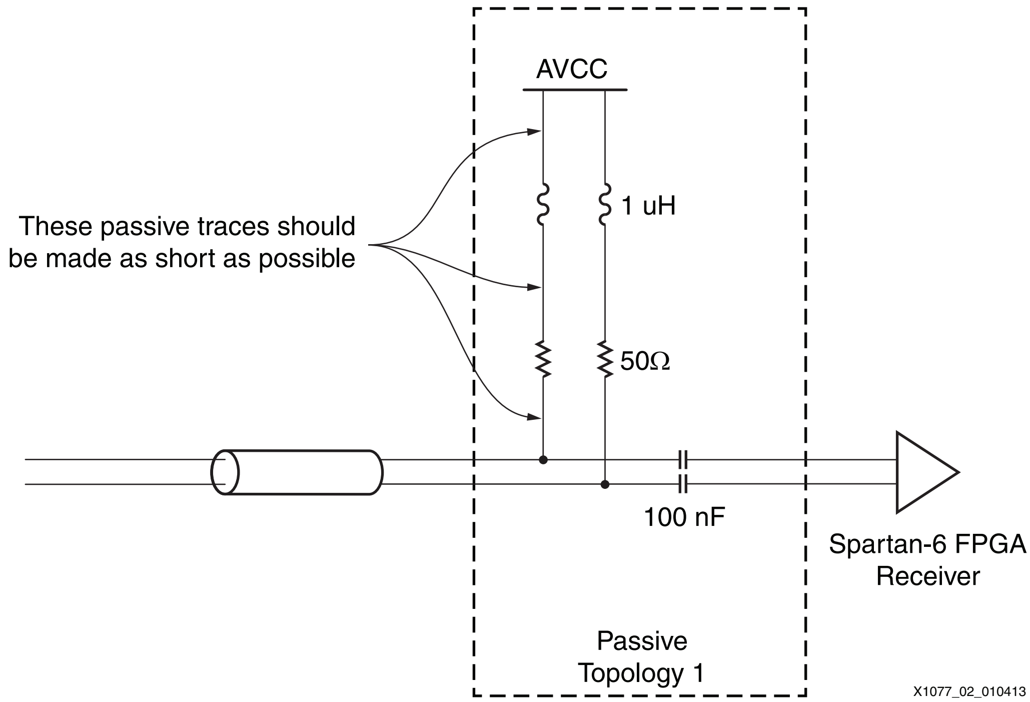


*Figure 2:* **Topology of Passive Network 1**

The internal termination of a Spartan-6 device cannot be disabled, and the maximum voltage it can connect to is 1.2V. For this reason, the termination cannot be used to bias the transmitter at 3.3V.

The inductors offer the biasing path to the transmitter and, because the impedance of the inductors increase with frequency, the inductors disconnect the external termination over frequency. The signal is blocked by the inductors and is terminated by the internal termination in the Spartan-6 FPGAs GTP receiver.

The passive network can be placed at the transmitter end, the receiver end, or in any other position in the transmission line because GTP receivers have signal termination.

The resistor values in this first example must be 50Ω, while the inductor and capacitor values are more flexible.

The 8B/10B coding guarantees DC balancing over 20 bits, thus the condition on the capacitor choice is that the time constant of the RC low-pass filter is greater than 20 times the unit interval of 670 ps.

$$\tau = RC$$
$$\tau = 20 \times 690\text{ps} \geq C = 276\text{pF} \quad \text{Equation 1}$$

Assuming a factor of 50, the minimum value is calculated as being approximately 13 nF. In theory, the maximum capacitor value is not limited. In practice, increasing the capacitor value excessively reduces the signal integrity quality as more parasitic capacitance is added to the line.

In the schematics (see Figure 4), 100 nF was used.

The biasing is provided through the inductor path, which has a cutting frequency much lower than the signal bandwidth. Assuming the signal bandwidth is generally above 75 MHz, the inductor is constrained in this way:

$$f_{CUT} = \frac{R}{2\pi L} = 75\text{MHz} \qquad \textit{Equation 2}$$

Solving for L:

$$L = \frac{R}{2\pi \times 75\text{MHz}} = 0.1\mu\text{H}$$

In theory, there is no limitation on the size of L. However, L is limited by the parasitic capacitance. The size of L in this schematic example is L = 1 μH.

The package size for all passive components must be chosen so that the parasitic capacitance is minimized. The length of the traces are designed to be as short as possible (highlighted in Figure 3).

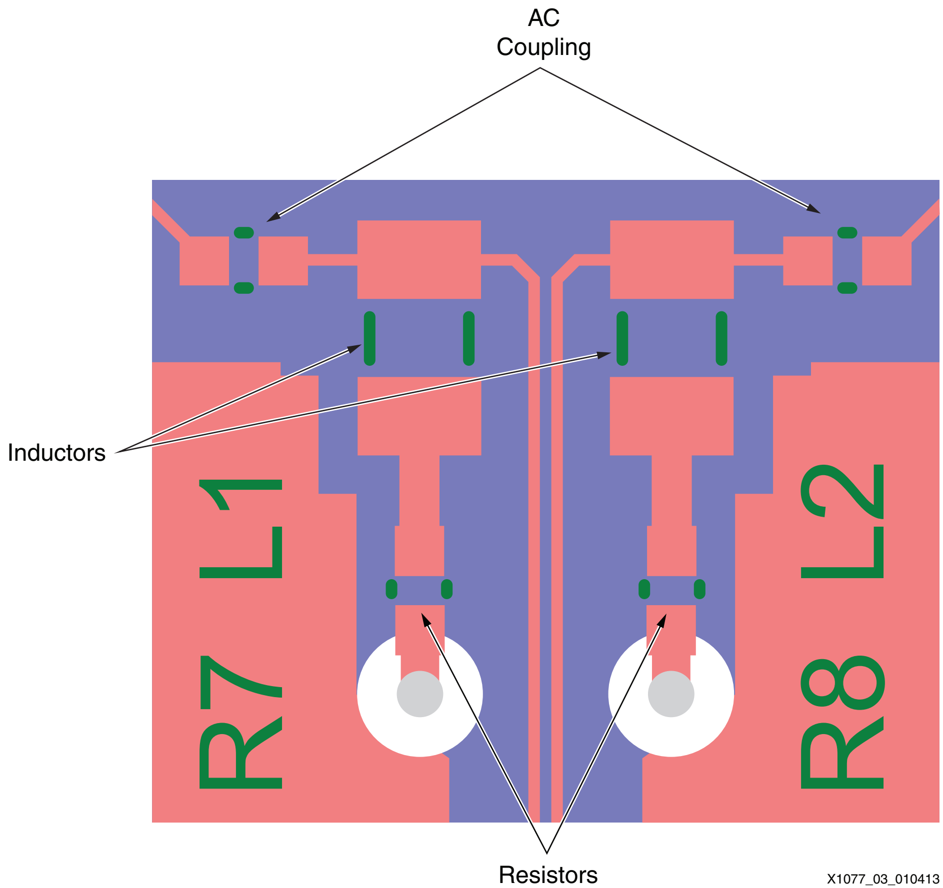


*Figure 3:* **Example Layout to Minimize the Parasitic Capacitance**

An sample schematic for this example is shown in Figure 4.

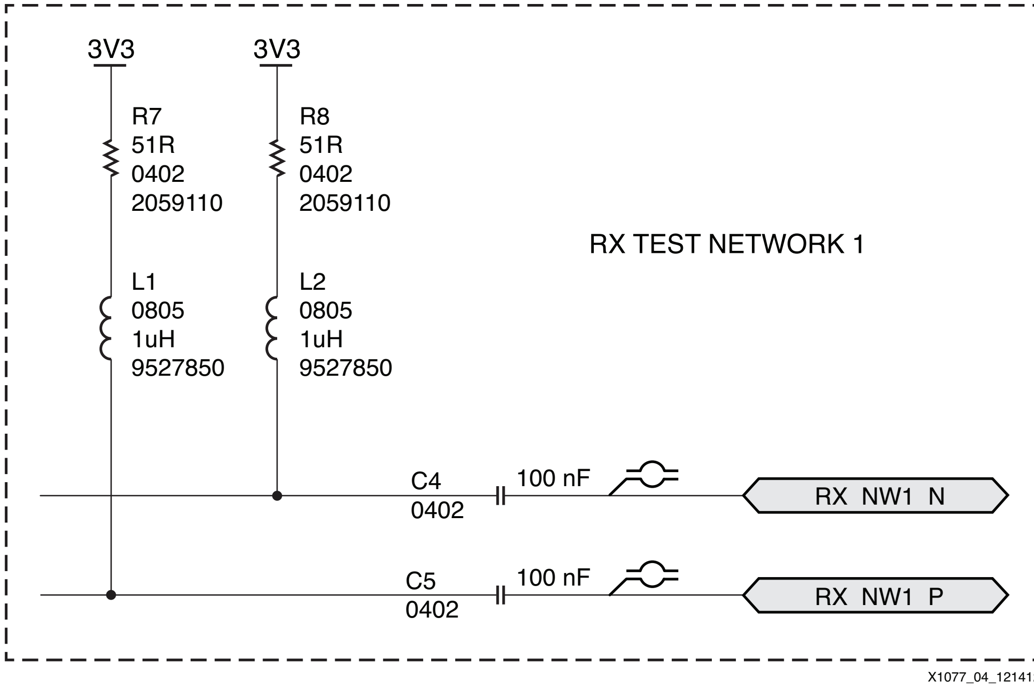


*Figure 4:* **Schematic of Passive Network Example 1**

## Passive Network Example 2

Figure 5 illustrates the second passive network.

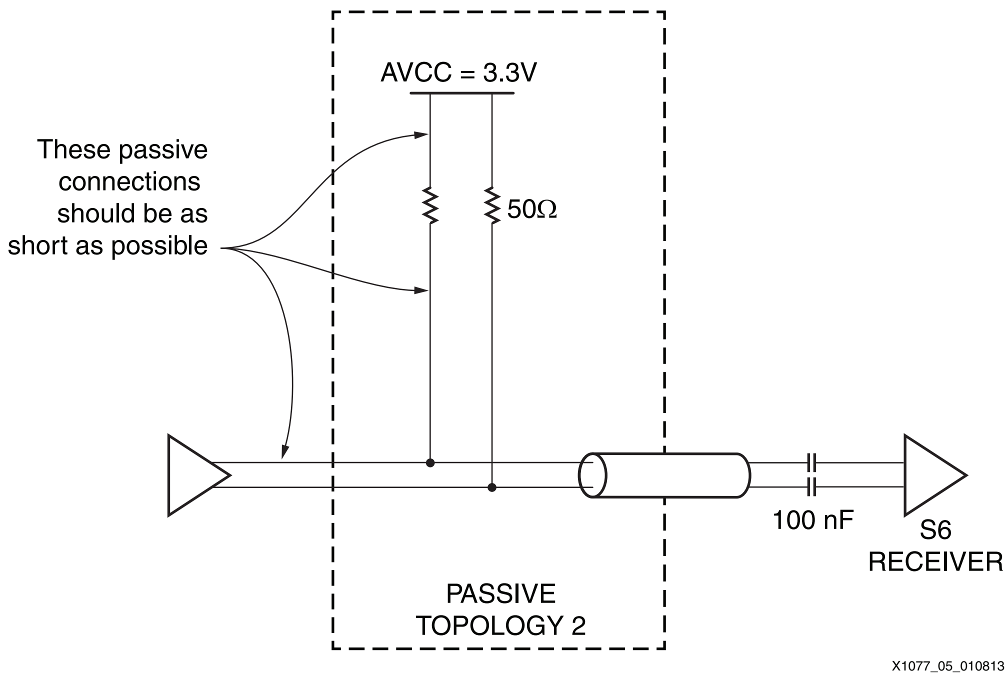


*Figure 5:* **Topology of Passive Network Example 2**

The second passive network example offers the biasing that an HDMI-compliant transmitter expects using 50Ω external resistors. Signal termination is on the receive-side inside the Spartan-6 device.

This network must be placed as close as physically possible to the transmitter to minimize any degradation in signal integrity. Thus, it is used only for HDMI links where the designer controls both the transmitter and the receiver. This situation is often referred to as the *embedded case* or the *chip-to-chip case* and is not compliant with the HDMI specification.

With this second passive network example, only half of the signal amplitude is available at the Spartan-6 device I/O input as compared to the example in passive network 1. Although this is generally a drawback, the Spartan-6 device also works well with 500 mV peak-to-peak differential I/O.

As shown in Figure 6, the network is placed close to the transmitter. The AC coupling is not shown because it is set up close to the connector.

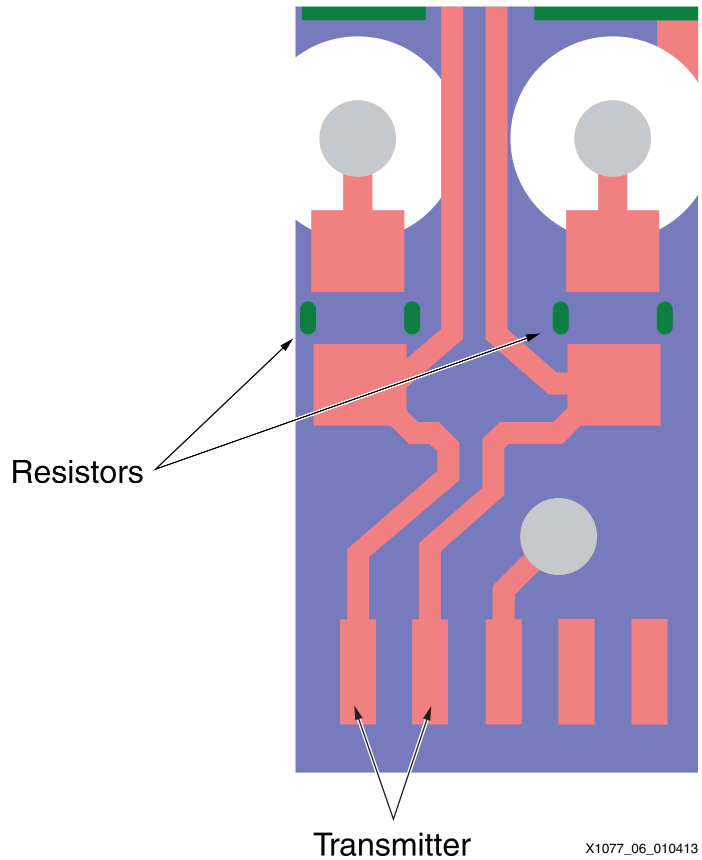


*Figure 6:* **Layout for Passive Network Example 2**

## Comparison of Examples

Table 1 lists the advantages and disadvantages of the two passive network examples.

*Table 1:* **Comparison of Passive Network Examples**

| Example | Advantages | Disadvantages |
|---|---|---|
| Passive Network 1 | A high (1V peak-to-peak) differential amplitude, compliant with the HDMI standard. | Inductors increase board space and add cost. |
| Passive Network 2 | Ideal termination for good signal integrity. | Amplitude is 500 mV peak-to-peak differential. Example is not compliant with HDMI standard. |

The first passive network example has double the amplitude compared to the second example. With a typical 10 mA tail current in the transmitter, the first passive network exhibits a 1V peak-to -peak differential amplitude while the second example is only half the amplitude.

However, the external components at the receive-side degrade the signal integrity more in the first example. Additionally, the first passive network example has an added cost because it uses six external devices instead of four.

On the surface, the second example passive network appears to be a better solution. However, it is not a solution for use with HDMI-compliant transmitters. Because access to the transmitter in a standard HDMI system is not possible when implementing a receiver, termination resistors must be physically located as close as possible to the transmitter to minimize stubs created by the resistors during normal operation of the link at high frequencies. The second example passive network can only be used when the location (and value) of the termination resistor can be selected (such as in an embedded chip-to-chip system where access to both the receive and transmit sides is possible).

It is possible to mitigate the disadvantages listed in Table 1. For example, in the first passive network example, the biasing resistor can be increased as long as the transmitter can operate with a lower than 3.3V termination voltage. Increasing the biasing resistors has the effect of increasing the peak-to-peak differential value of the signal amplitude on the line.

The first passive network example can be simplified by removing the inductor. This is not the second passive network example because the passive capacitors are located close to the receiver. The impedance termination becomes a 50Ω differential resistor instead of a 100Ω resistor that limits the signal integrity (incorrect termination value) and amplitude level. Also in this case, it is possible to increase the resistor value as soon as the transmitter is able to tolerate working with less than 3.3V. This new resistor value increases the overall termination value to between 50Ω and 100Ω. This increased modification is only recommended if the line is very short and therefore not affected by the non-ideal termination value.

# Measurements

This section describes the hardware measurements that were taken on a Spartan-6 FPGA GTP receiver using a commercial HDMI driver from STMicroelectronics [Ref 2].

Figure 7 shows the architecture of the test plan for the HDMI board. This HDMI board was specifically designed and manufactured for making these measurements.

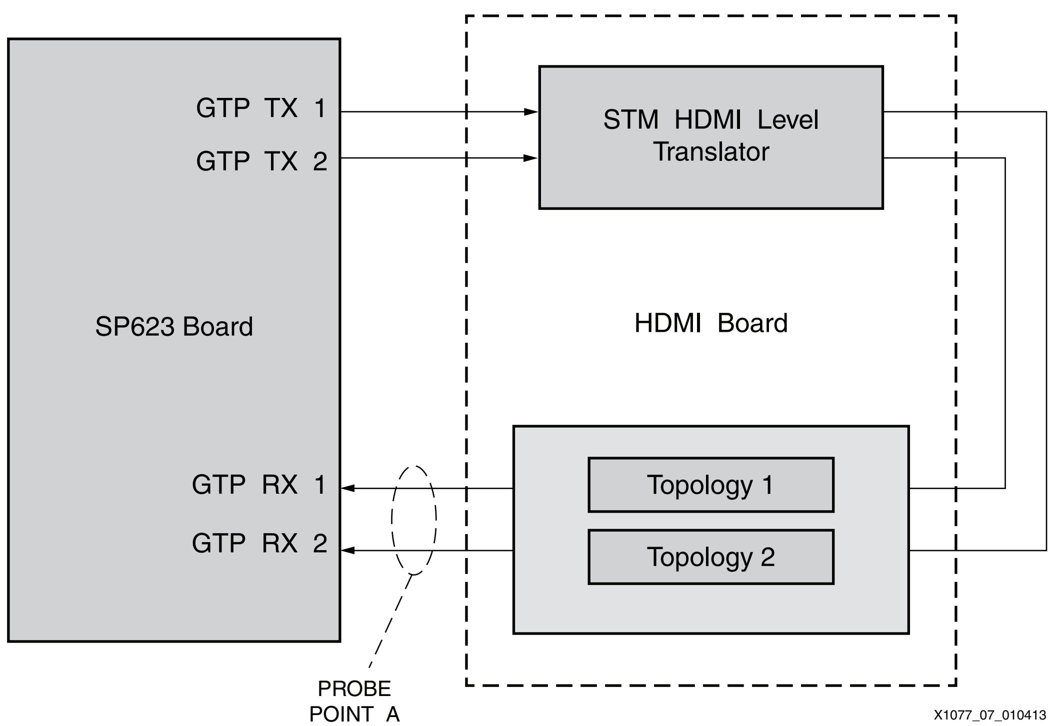


*Figure 7:* **Test Setup for HDMI Board Showing Probe Point A**

For the measurements in this application note, the board hosting the Spartan-6 device is the SP623 (see http://www.xilinx.com/products/boards-and-kits/CK-S6-SP623-G.htm).

The Spartan-6 device, running IBERT, generates pseudorandom binary sequence (PRBS) data for the HDMI board. For more information on PRBS data see the application note *An Attribute-Programmable PRBS Generator and Checker* (XAPP884) [Ref 3].

On the SP623 board, an HDMI-level translator from STMicroelectronics (STHDLS101T) [Ref 2] converts the PRBS to the correct HDMI electrical format (open collector). On the same board, two channels are under test (note the four wires going in and out of the HDMI board). One channel is for the first passive network example and the other is for the second example. Figure 8 includes two photographs of a general HDMI board test setup.

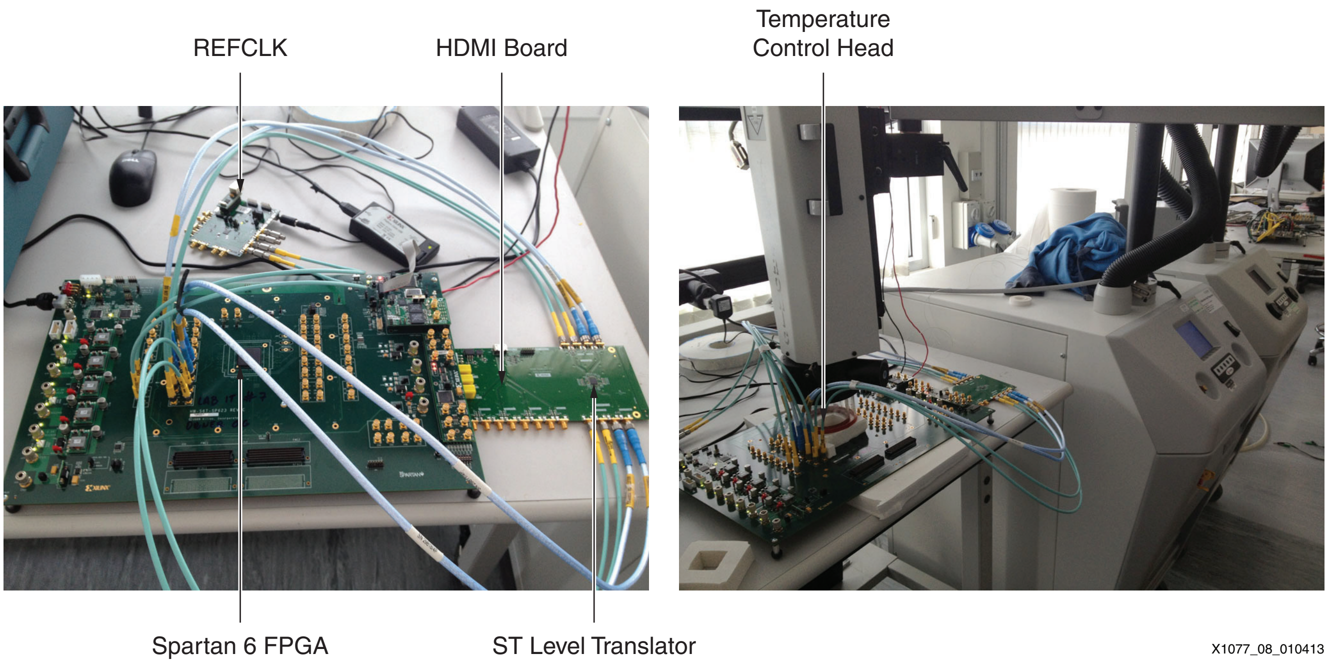


*Figure 8:* **General Test Setup (Temptronic Head Unit Is Shown in the Right Photograph)**

***Note:*** The inductors used in these tests are Murata LQM21NN1R0K10D.

The following conditions are considered for both passive network examples:

- PRBS7 was used for target coding and PRBS31 for stressed coding
- 1.45 Gb/s was used for the target rate and 2.5 Gb/s for the stressed rate
- –40°C, 25°C, and 125°C are the test temperature ranges. Due to setup limitations, these are the intended package temperatures used for these examples.

The first six tests (1–6) consider different combinations of the passive network examples, stressed rate, and temperature. Tests 7, 8, and 9 only use the second passive network example in the non-ideal case where the transmitter biasing resistor is moved about one inch away from its ideal position (close to the transmitter). This is referred to in the rest of this document as the modified example 2. Tests 10 through 19 show the HDMI signal as it goes into the Spartan-6 FPGA receiver. This signal is generated by a standard HDMI driver, processed by the passive network examples 1 and 2, and then sent to a real-time scope with a 40 cm coaxial cable. All measurements are single ended. Further details of the tests include:

- The device under test was labeled as XC6SLX150T 3C-ES FFG676AIV0941 (serial: D4019216A)
- The board under test was labeled as HW-S6T-SP623 rev. C (serial: 62770028)
- IBERT was used with ISE® Design Suite v14.1

Different tests were run combining data rates, patterns, passive network examples, and temperature. The following sections describe each of these tests.

The target data rate for this application is 1.45 Gb/s and the target pattern is HDMI (in the tests, PRBS7 is used to resemble the 8B/10B data pattern). In these tests, many conditions were artificially stressed to determine the robustness of the link. Specifically, the PRBS31 at a rate of 2.5 Gb/s was often used.

In IBERT, the two left-most GTP transceivers used are:

- GTP 101_0: Connected to the first passive network example
- GTP 101_1: Connected to the second passive network example

A REFCLK is provided through reference clock input 101_0 using this setup:

- PRBS data at 1.45 Gb/s: REFCLK of 145 MHz with multiplier factor of 10
- PRBS data at 2.5 Gb/s: REFCLK of 125 MHz with multiplier factor of 20

## Test 1: Temperature = 125°C

Conditions for the test shown in Figure 9:

- Both passive network examples tested
- Operation rate: 1.45 Gb/s
- PRBS31
- Temperature = 125°C

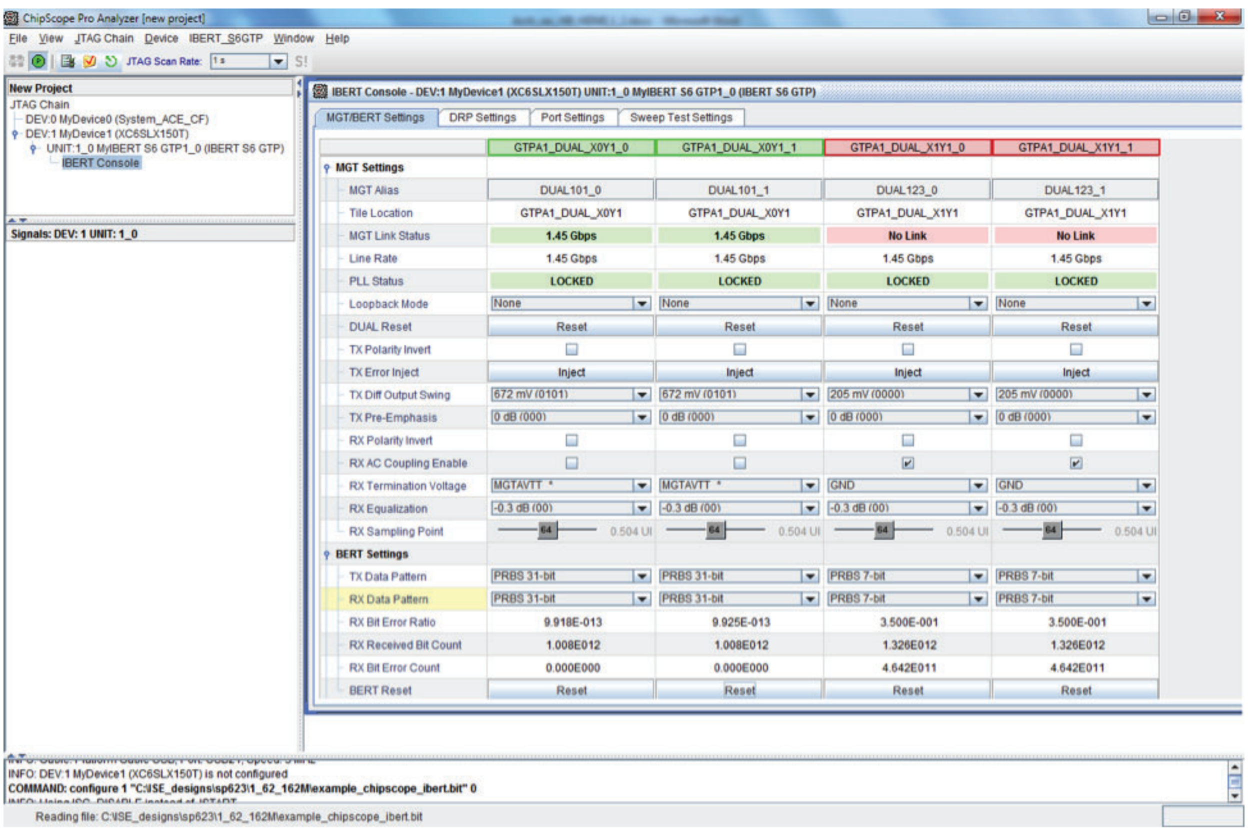


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*Figure 9:* **Test 1: PRBS 31, 1.45 Gb/s, T = 125°C**

## Test 2: Temperature = 25°C

Conditions for the test shown in Figure 10:

- Both passive network examples tested
- Operation rate: 1.45 Gb/s
- PRBS31
- Temperature = 25°C

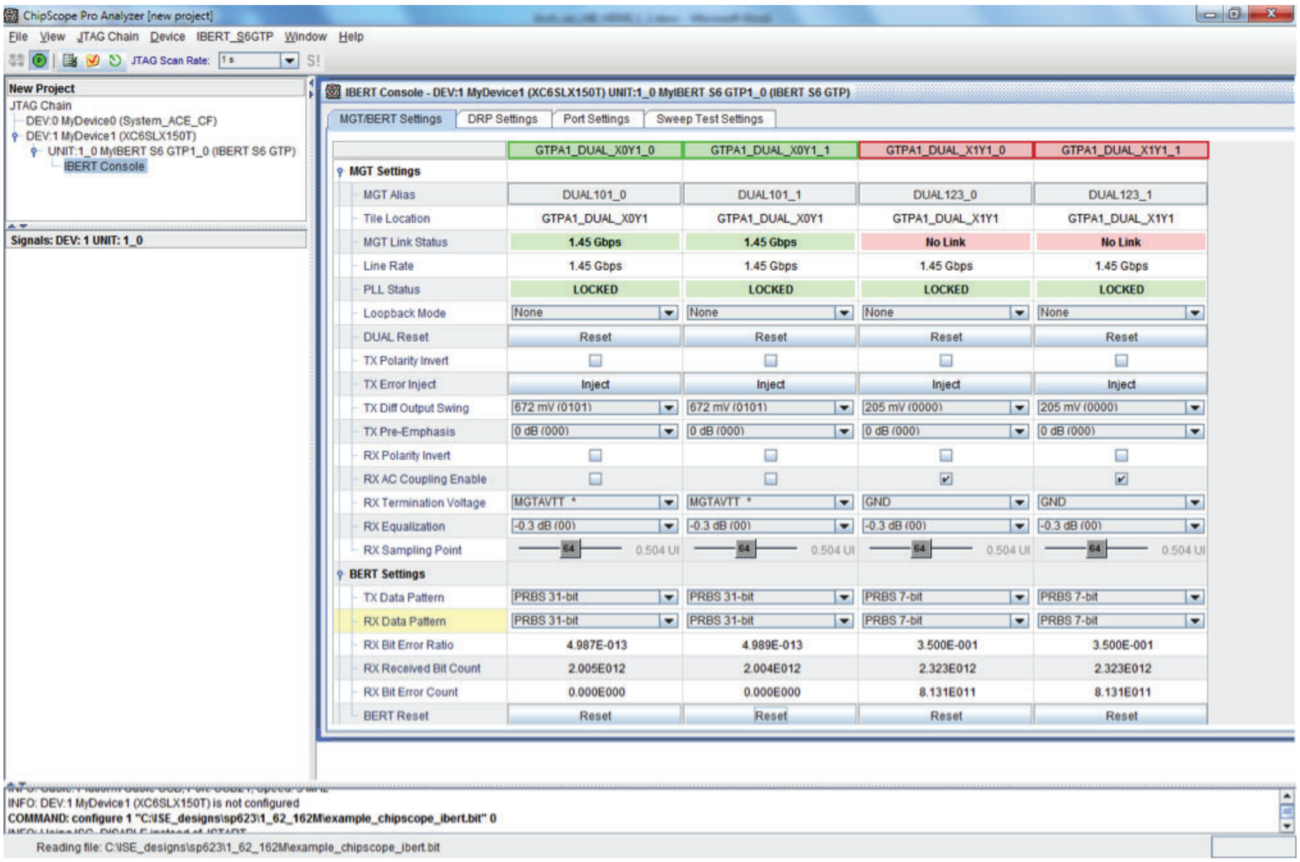


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*Figure 10:* **Test 2: PRBS 31, 1.45 Gb/s, T = 25°C**

## Test 3: Temperature = –40°C

Conditions for the test shown in Figure 11:

- Both passive network examples tested
- Operation rate: 1.45 Gb/s
- PRBS31
- Temperature = –40°C

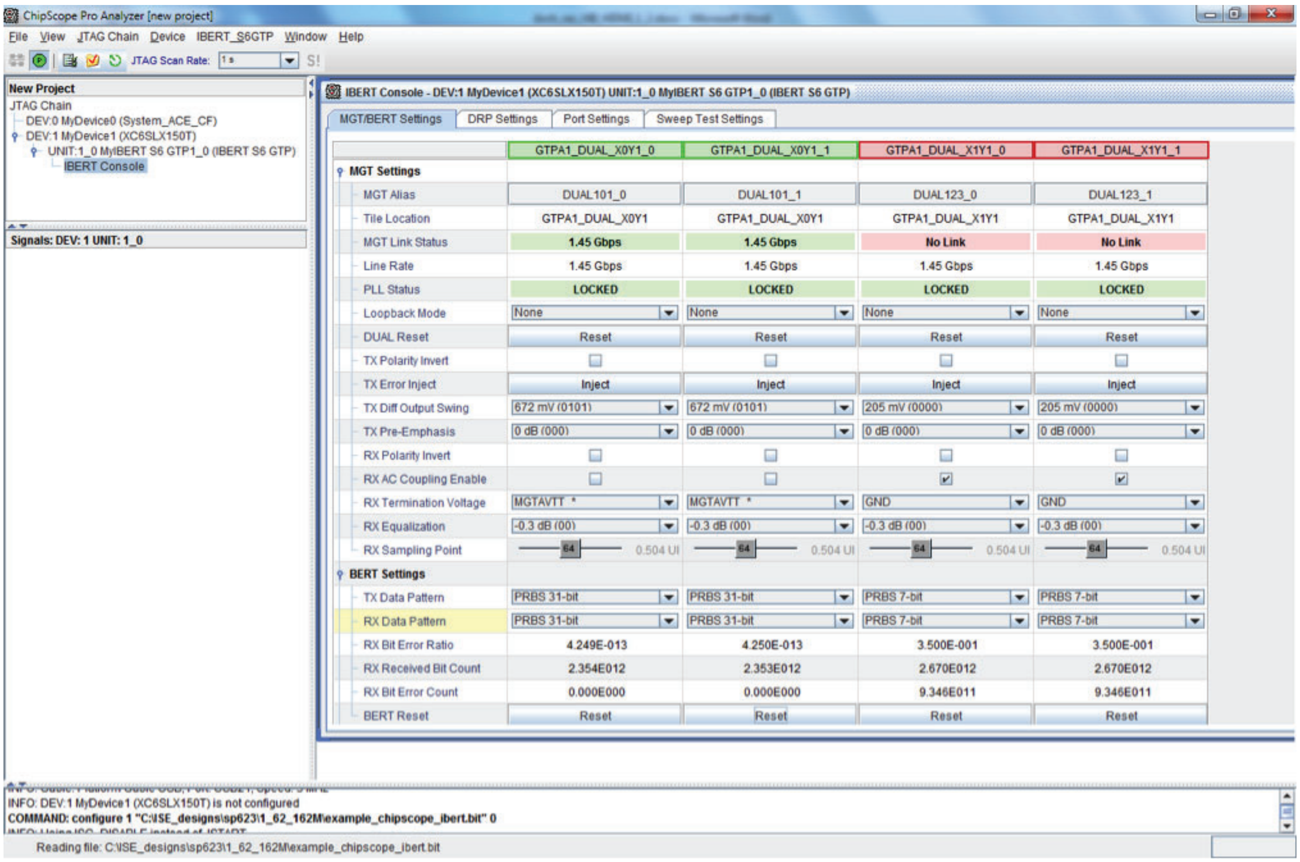


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*Figure 11:* **Test 3: PRBS 31, 1.45 Gb/s, T = –40°C**

## Test 4: Different PRBSs, Temperature = 125°C

Conditions for the test shown in Figure 12:

- Operation rate: 2.5 Gb/s
- Both passive network examples tested:
    - Example 1 using PRBS7
    - Example 2 using PRBS31
- Temperature = 125°C

Passive network example 1 is marginal at 2.5 Gb/s using PRBS31.

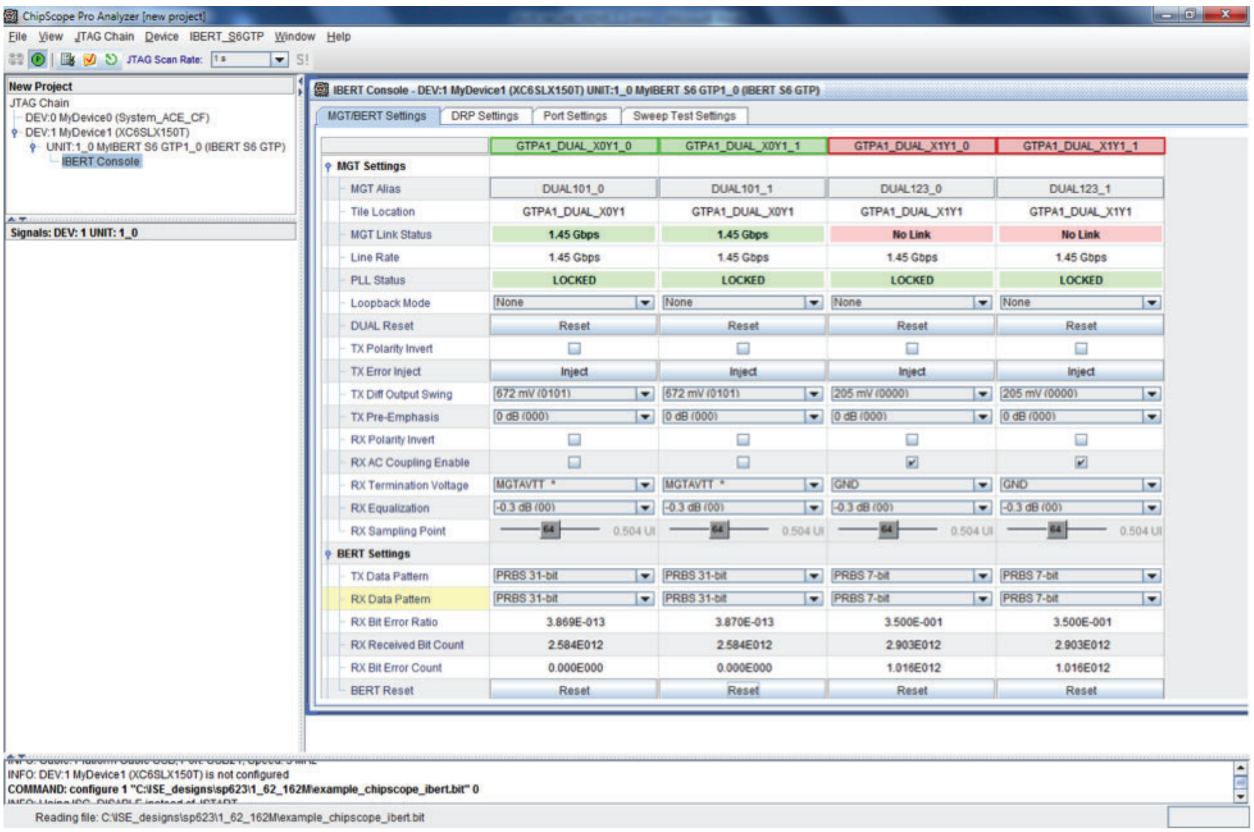


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*Figure 12:* **Test 4: Different PRBSs, 2.5 Gb/s, T = 125°C**

## Test 5: Different PRBSs, Temperature = 25°C

Conditions for the test shown in Figure 13:

- Operation rate: 2.5 Gb/s
- Both passive network examples tested:
    - Example 1 using PRBS7
    - Example 2 using PRBS31
- Temperature = 25°C

Passive network example 1 is marginal at 2.5 Gb/s using PRBS31.

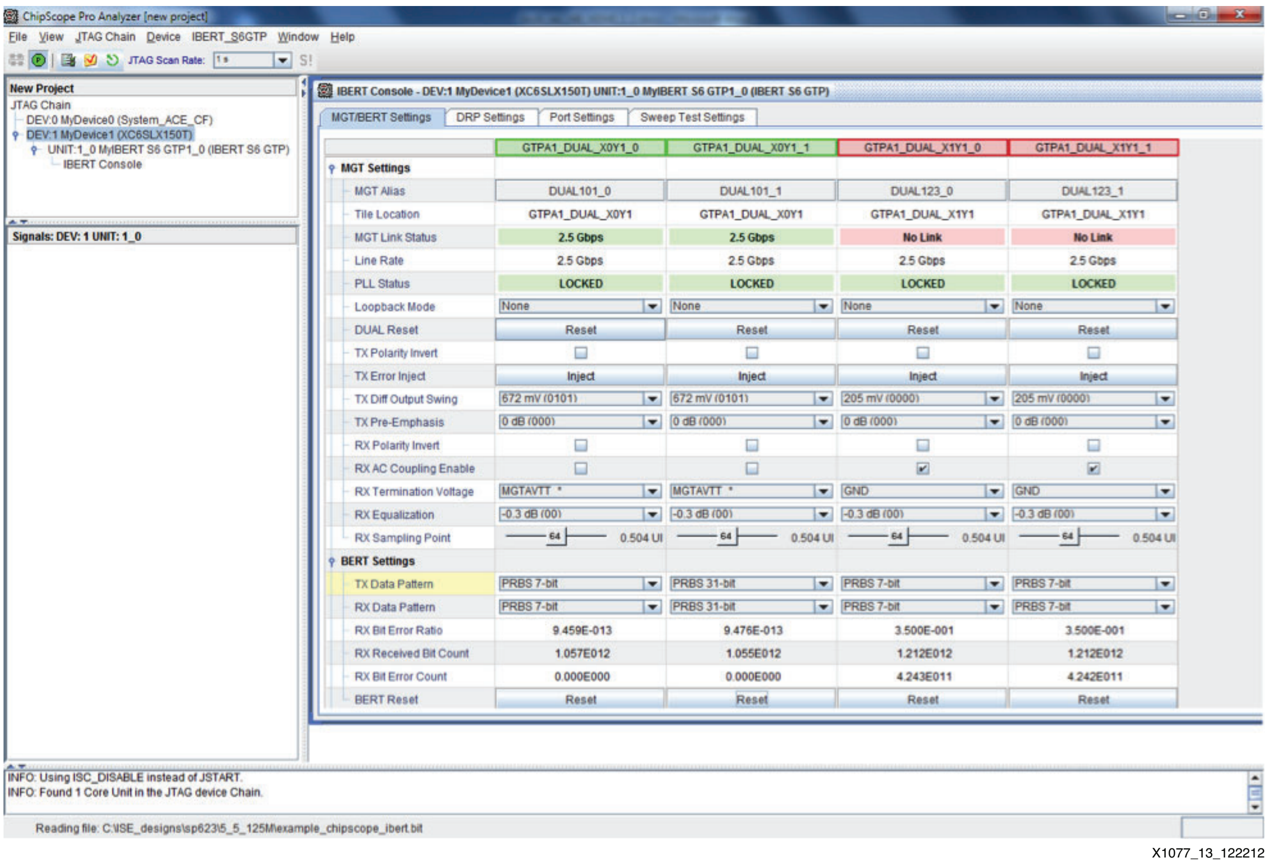


*Figure 13:* **Test 5: Different PRBSs, 2.5 Gb/s, T = 25°C**

## Test 6: Different PRBSs, Temperature = –40°C

Conditions for the test shown in Figure 14:

- Operation rate: 2.5 Gb/s
- Both passive network examples tested:
  - Example 1 using PRBS7
  - Example 2 using PRBS31
- Temperature = –40°C

Passive network example 1 is marginal at 2.5 Gb/s using PRBS31.

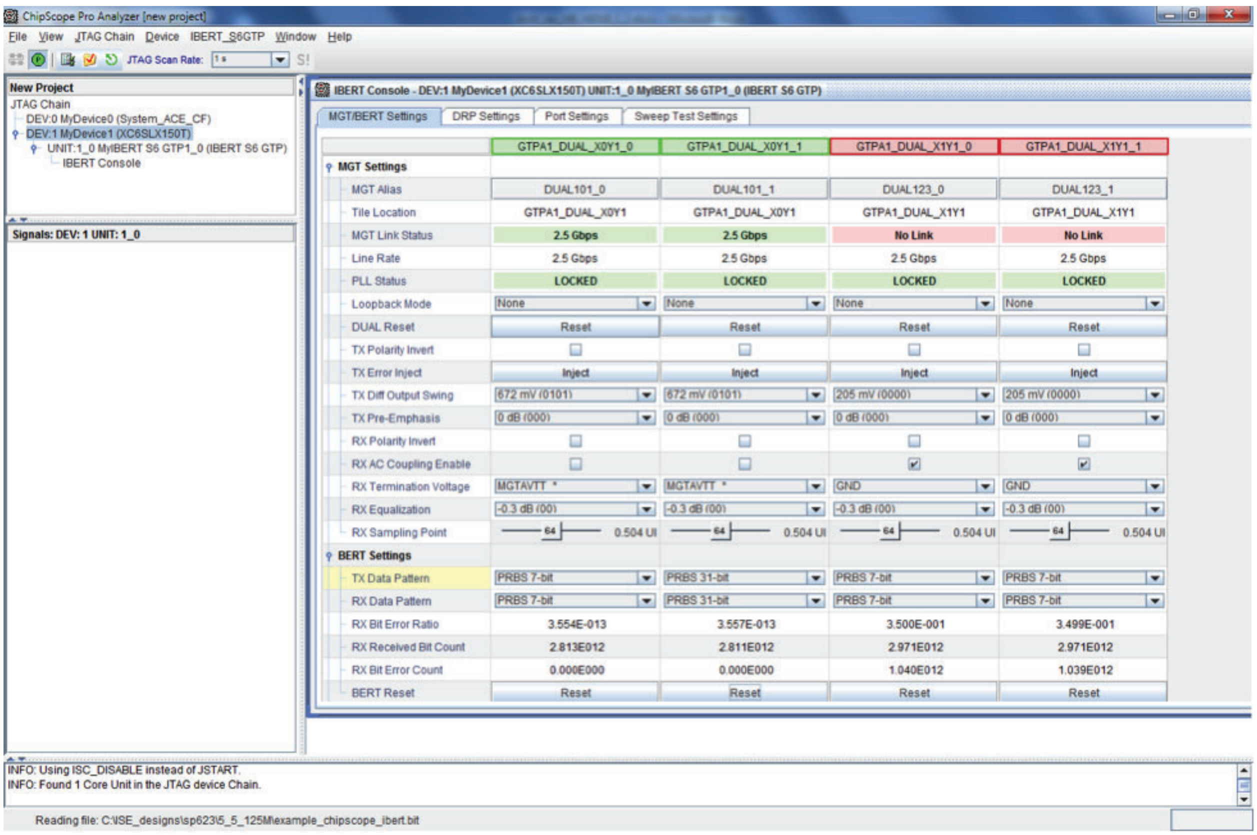


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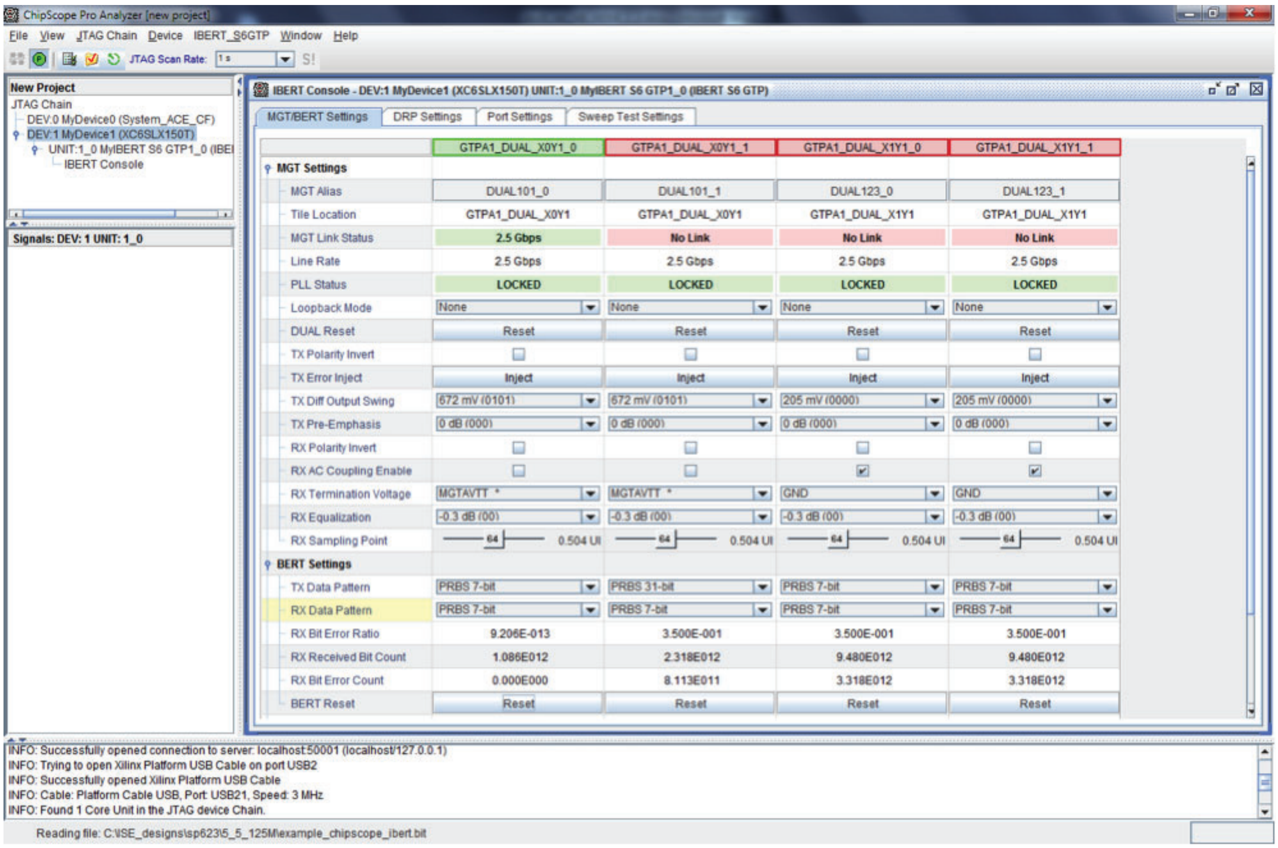
*Figure 14:* **Test 6: Different PRBSs, 2.5 Gb/s, T = –40°C**

## Test 7: Modified Example 2, Temperature = 125°C

Example 2 was modified by placing a 50Ω biasing resistor one inch away from the transmitter. Only the left-most GTP transceiver was used in this test.

Conditions for the test shown in Figure 15:

- Operation rate: 2.5 Gb/s
- PRBS31
- Temperature = 125°C



X1077_15_122212

*Figure 15:* **Test 7: PRBS31, 2.5 Gb/s, T = 125°C**

## Test 8: Modified Example 2, Temperature = 25°C

Example 2 was modified by placing a 50Ω biasing resistor one inch away from the transmitter. Only the left-most GTP transceiver was used in this test.

Conditions for the test shown in Figure 16:

- Operation rate: 2.5 Gb/s
- PRBS31
- Temperature = 25°C

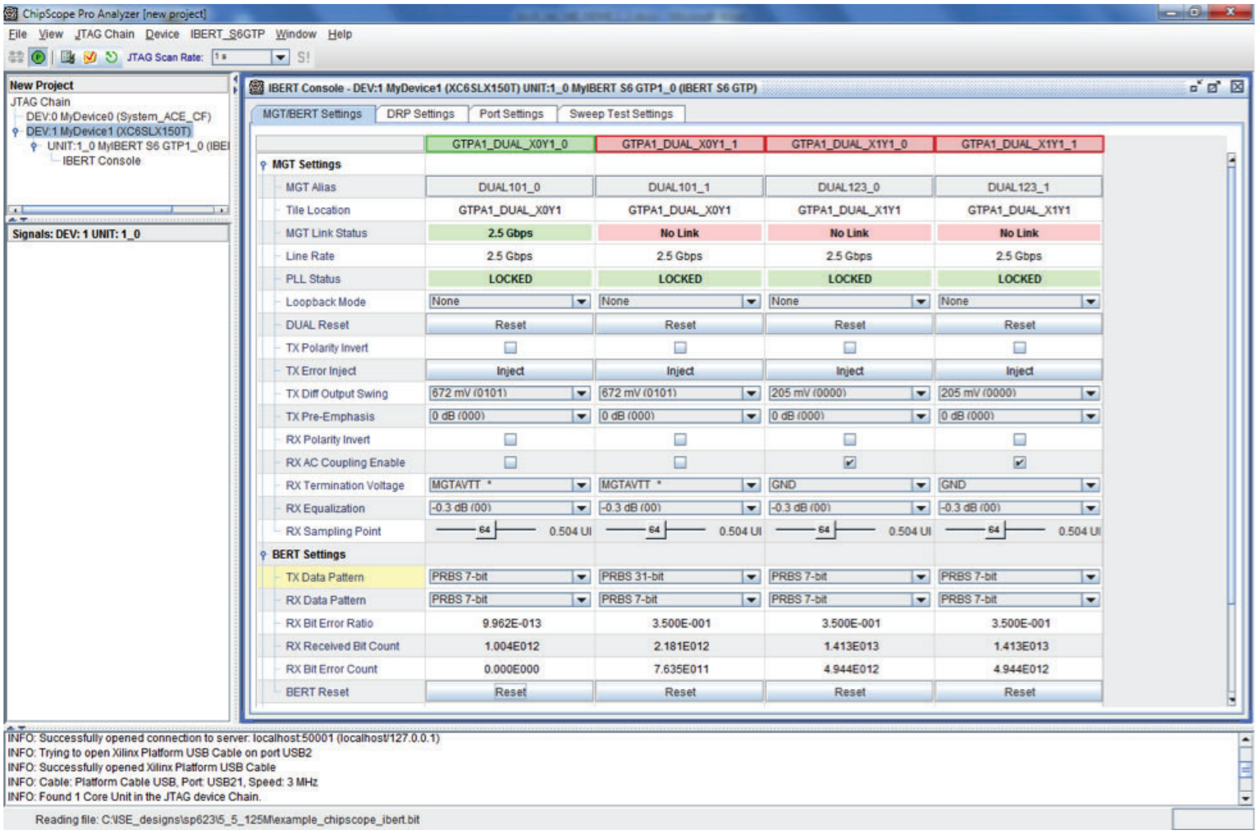


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*Figure 16:* **Test 8: PRBS31, 2.5 Gb/s, T = 25°C**

## Test 9: Modified Example 2, Temperature = –40°C

Example 2 was modified by placing a 50Ω biasing resistor one inch away from the transmitter. Only the left-most GTP transceiver was used in this test.

Conditions for the test shown in Figure 17:

- Operation rate: 2.5 Gb/s
- PRBS31
- Temperature = –40°C

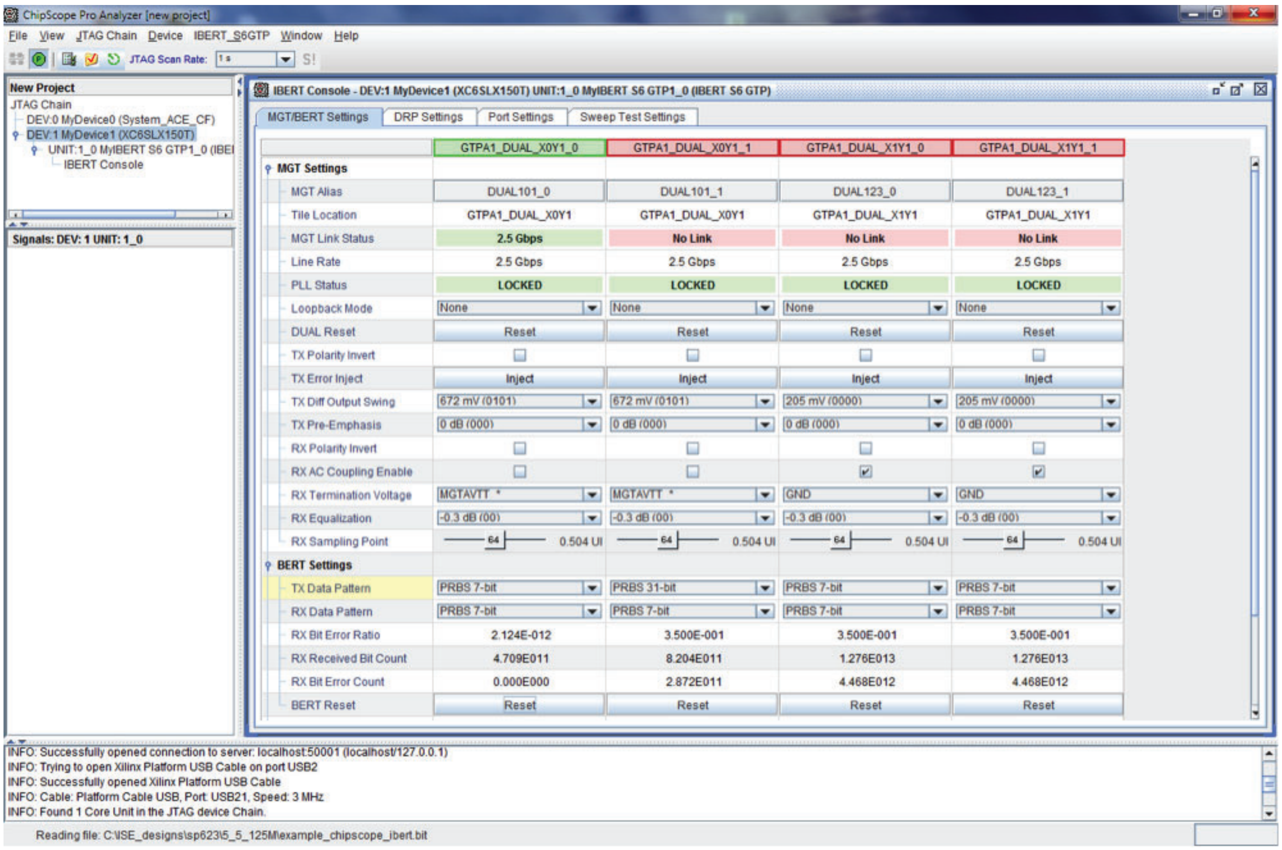


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*Figure 17:* **Test 9: PRBS31, 2.5 Gb/s, T = –40°C**

## Test 10: Jitter Analysis using Example 1, PRBS7, Rate = 1.45 Gb/s

The purpose of this test is to show the effect of the first passive network example in terms of jitter. The location of the probe point positions is shown in Figure 7.

Conditions for the test shown in Figure 18:

- Probe point: A
- Operation rate: 1.45 Gb/s
- PRBS7

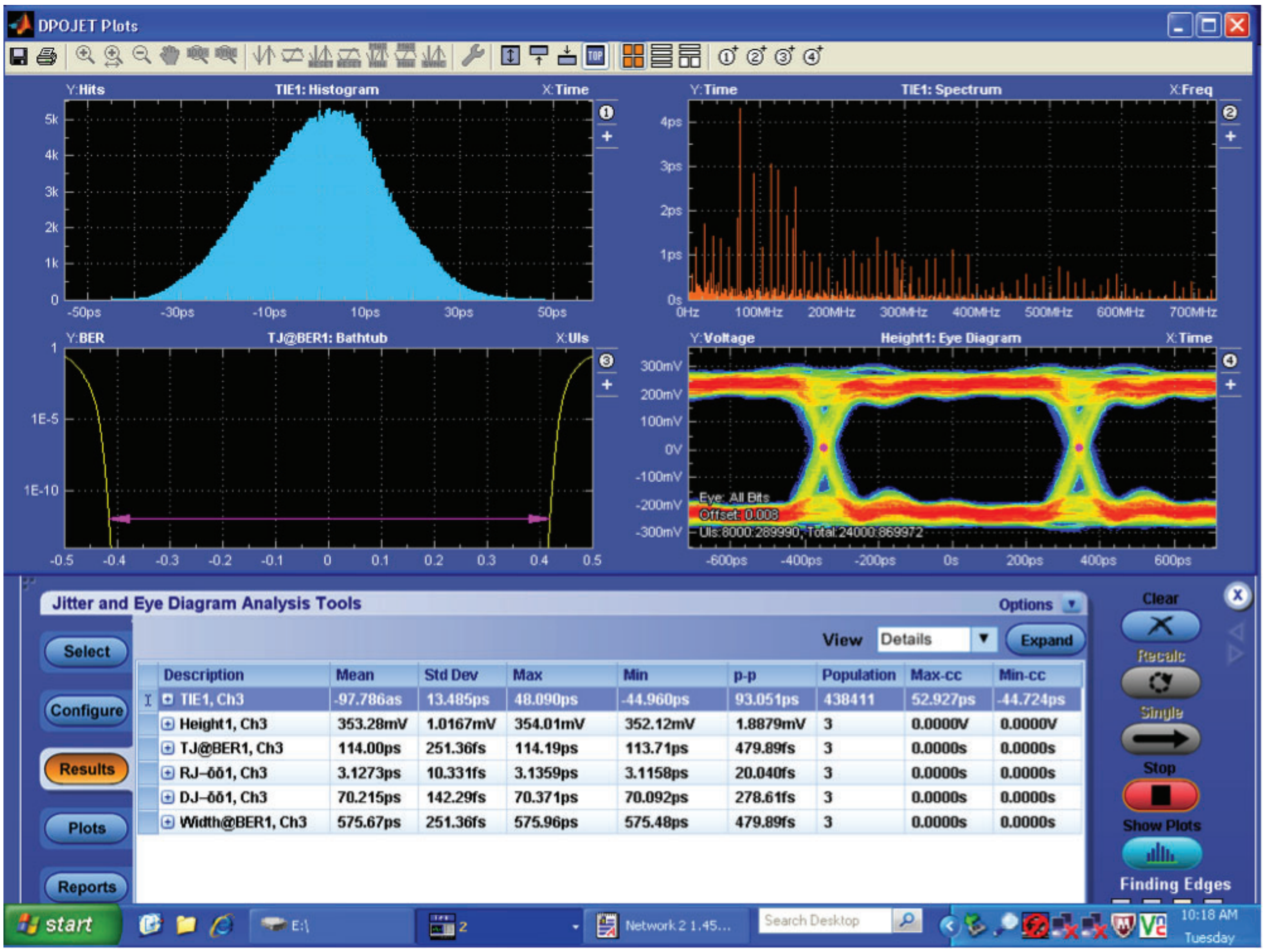


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*Figure 18:* **Test 10: Example 1, PRBS7, 1.45 Gb/s**

## Test 11: Jitter Analysis using Example 2, PRBS7, Rate = 1.45 Gb/s

The purpose of this test is to show the effect of the second passive network example in terms of jitter. The location of the probe point positions is shown in Figure 7.

Conditions for the test shown in Figure 19:

- Probe point: A
- Operation rate: 1.45 Gb/s
- PRBS7

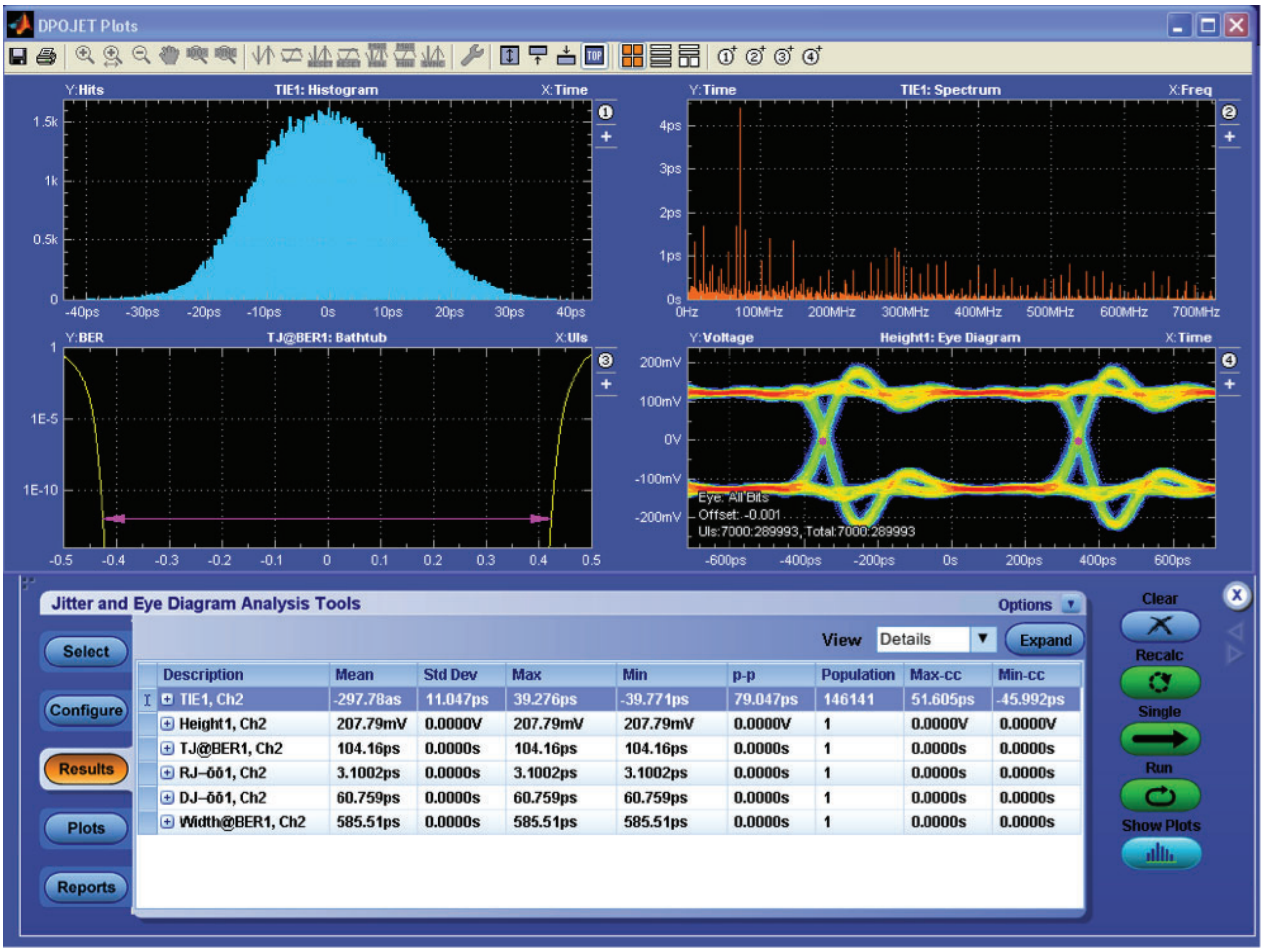


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*Figure 19:* **Test 11: Example 2, PRBS7, 1.45 Gb/s**

## Test 12: Jitter Analysis using Example 1, PRBS31, Rate = 1.45 Gb/s

The purpose of this test is to show the effect of the first passive network example in terms of jitter. The location of the probe point positions is shown in Figure 7.

Conditions for the test shown in Figure 20:

- Probe point: A
- Operation rate: 1.45 Gb/s
- PRBS31

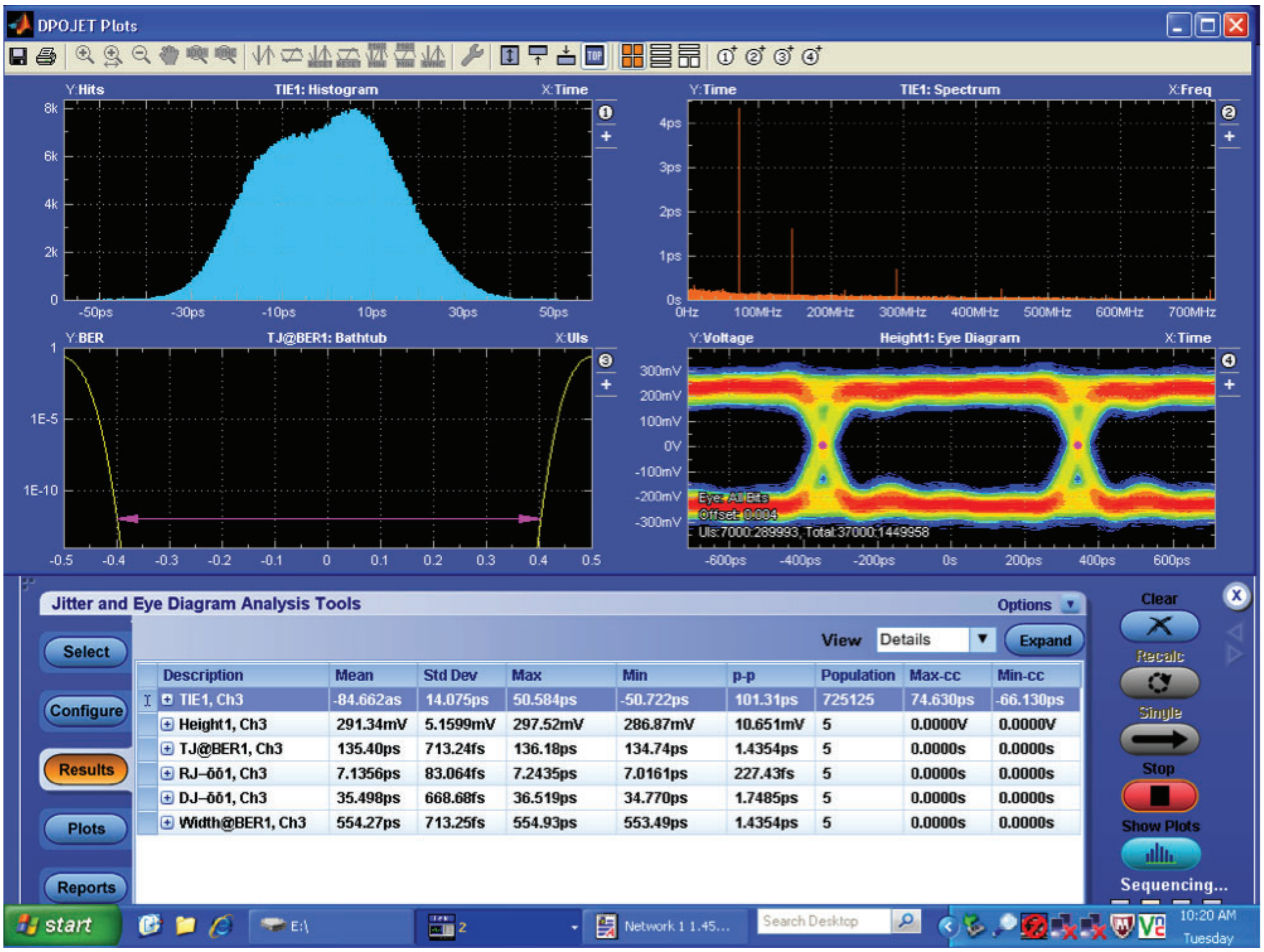


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*Figure 20:* **Test 12: Example 1, PRBS31, 1.45 Gb/s**

## Test 13: Jitter Analysis using Example 2, PRBS31, Rate = 1.45 Gb/s

The purpose of this test is to show the effect of the second passive network example in terms of jitter. The location of the probe point positions is shown in Figure 7.

Conditions for the test shown in Figure 21:

- Probe point: A
- Operation rate: 1.45 Gb/s
- PRBS31

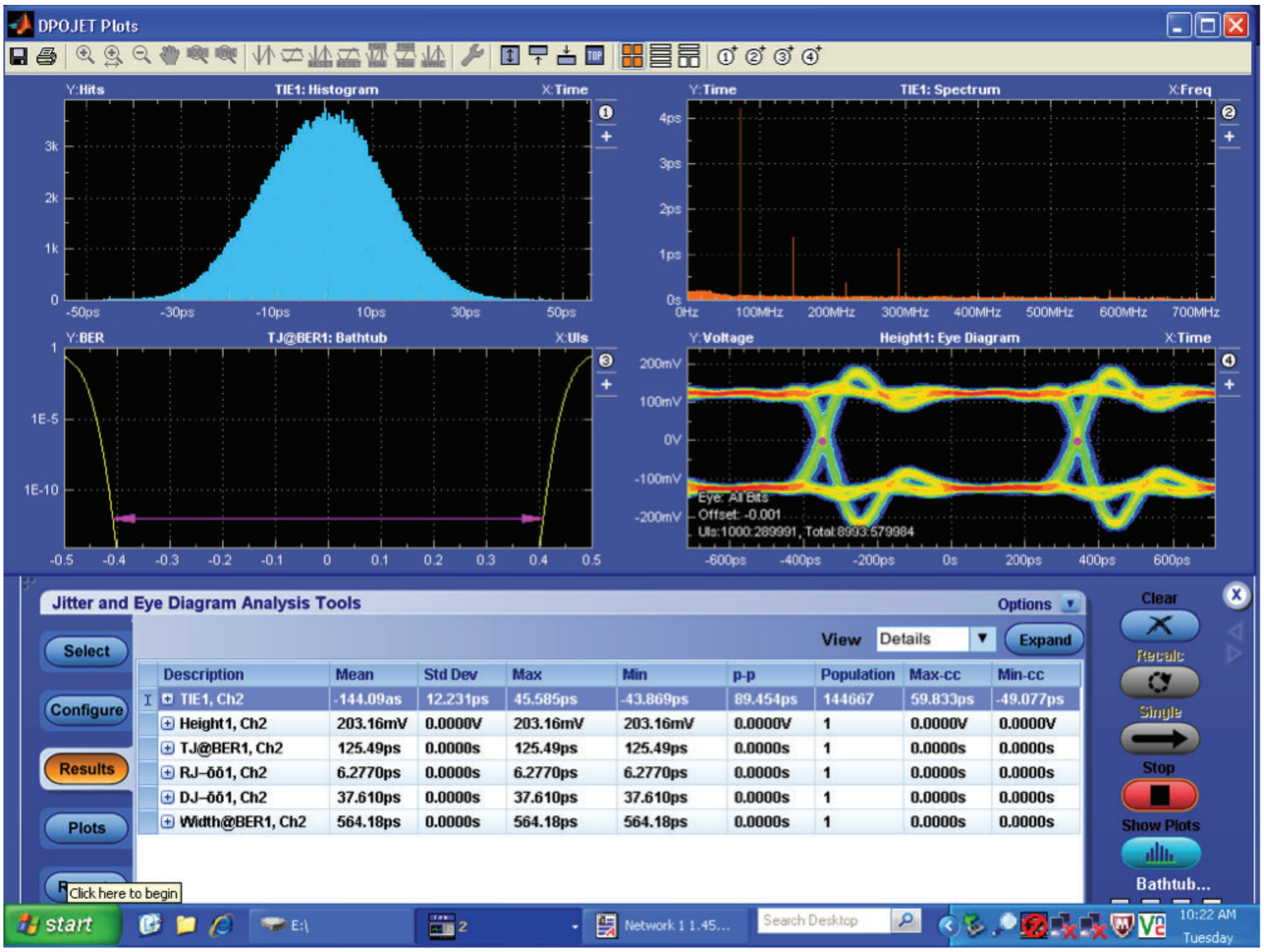


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*Figure 21:* **Test 13: Example 2, PRBS31, 1.45 Gb/s**

## Test 14: Jitter Analysis using Example 1, PRBS7, Rate = 2.5 Gb/s

The purpose of this test is to show the effect of the first passive network example in terms of jitter. The location of the probe point positions is shown in Figure 7.

Conditions for the test shown in Figure 22:

- Probe point: A
- Operation rate: 2.5 Gb/s
- PRBS7

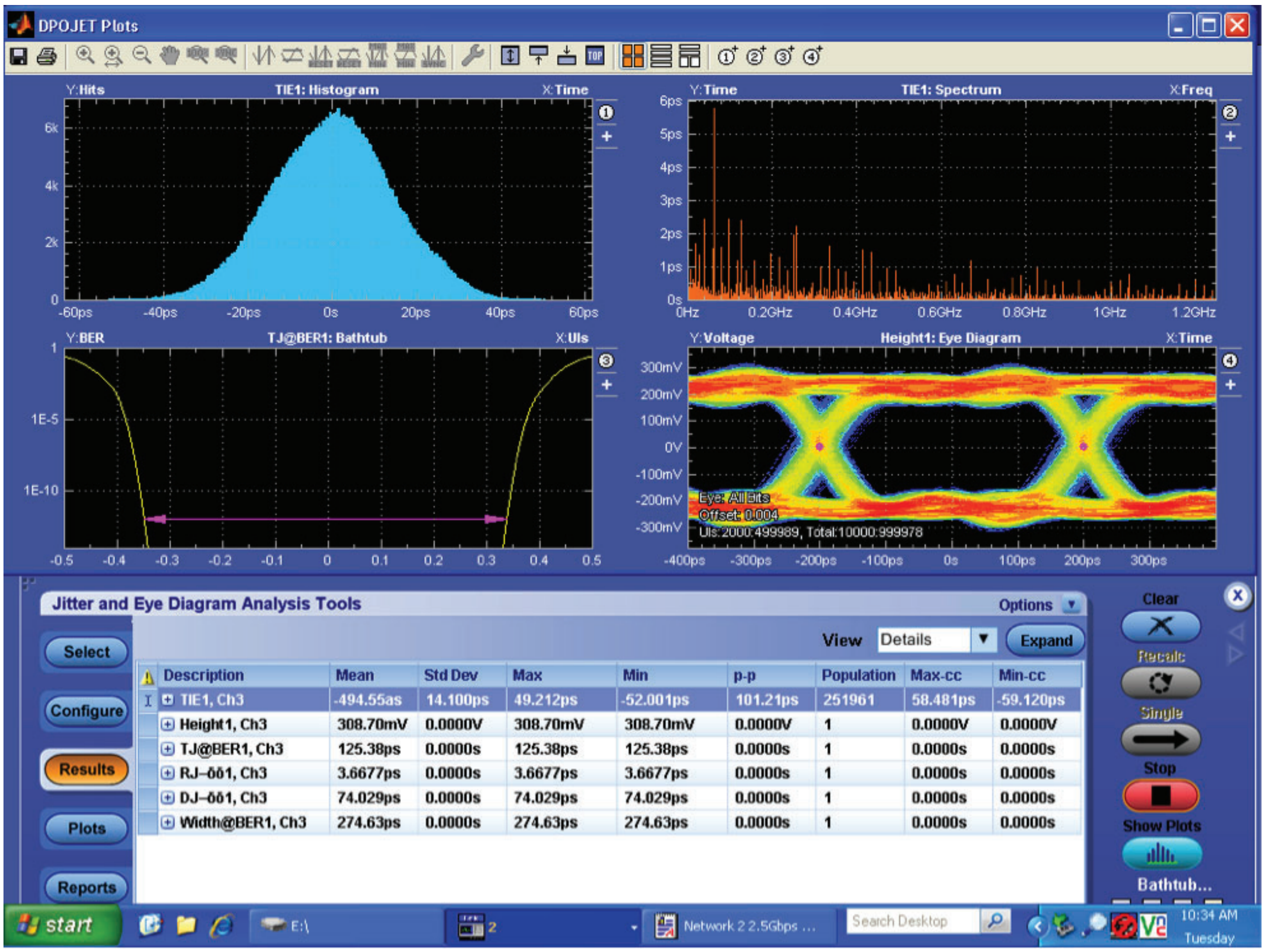


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*Figure 22:* **Test 14: Example 1, PRBS7, 2.5 Gb/s**

## Test 15: Jitter Analysis using Example 2, PRBS7, Rate = 2.5 Gb/s

The purpose of this test is to show the effect of the second passive network example in terms of jitter. The location of the probe point positions is shown in Figure 7.

Conditions for the test shown in Figure 23:

- Probe point: A
- Operation rate: 2.5 Gb/s
- PRBS7

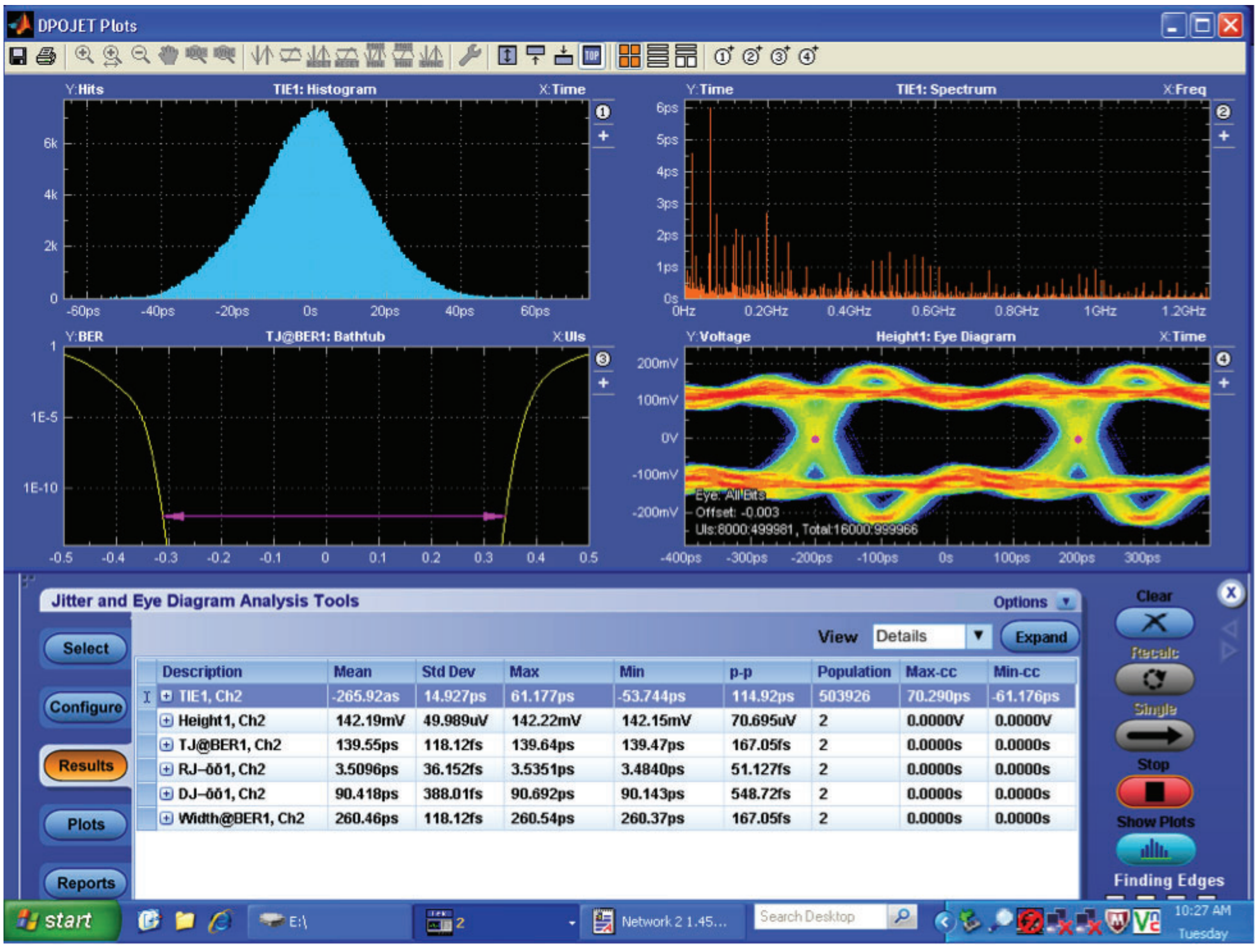


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*Figure 23:* **Test 15: Example 2, PRBS7, 2.5 Gb/s**

## Test 16: Jitter Analysis using Example 1, PRBS31, Rate = 2.5 Gb/s

The purpose of this test is to show the effect of the example 1 passive network in terms of jitter. The location of the probe point positions is shown in Figure 7.

Conditions for the test shown in Figure 24:

- Probe point: A
- Operation rate: 2.5 Gb/s
- PRBS31

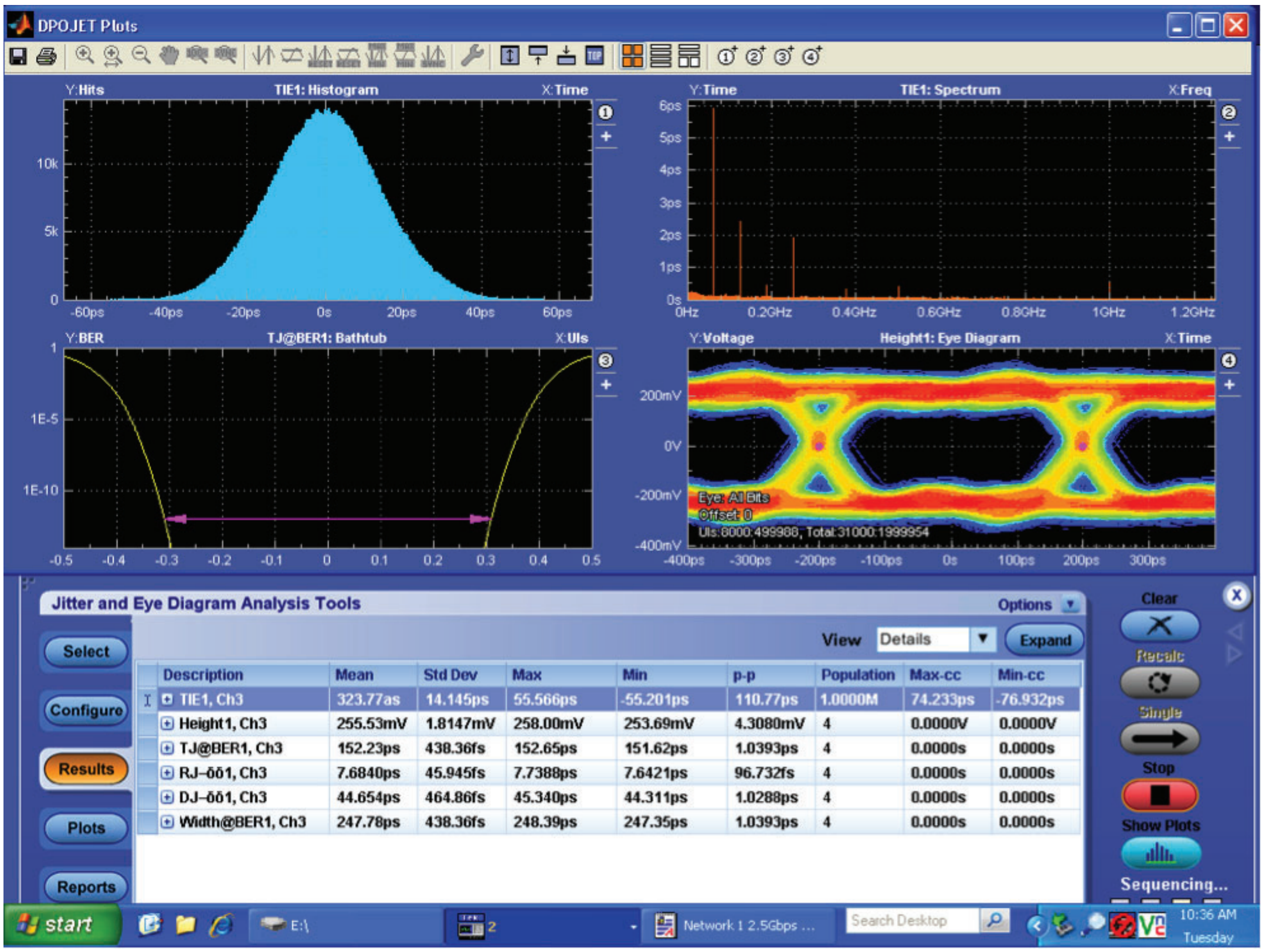


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*Figure 24:* **Test 16: Example 1, PRBS31, 2.5 Gb/s**

## Test 17: Jitter Analysis using Example 2, PRBS31, Rate = 2.5 Gb/s

The purpose of this test is to show the effect of the example 2 passive network in terms of jitter. The location of the probe point positions is shown in Figure 7.

Conditions for the test shown in Figure 25:

- Probe point: A
- Operation rate: 2.5 Gb/s
- PRBS31

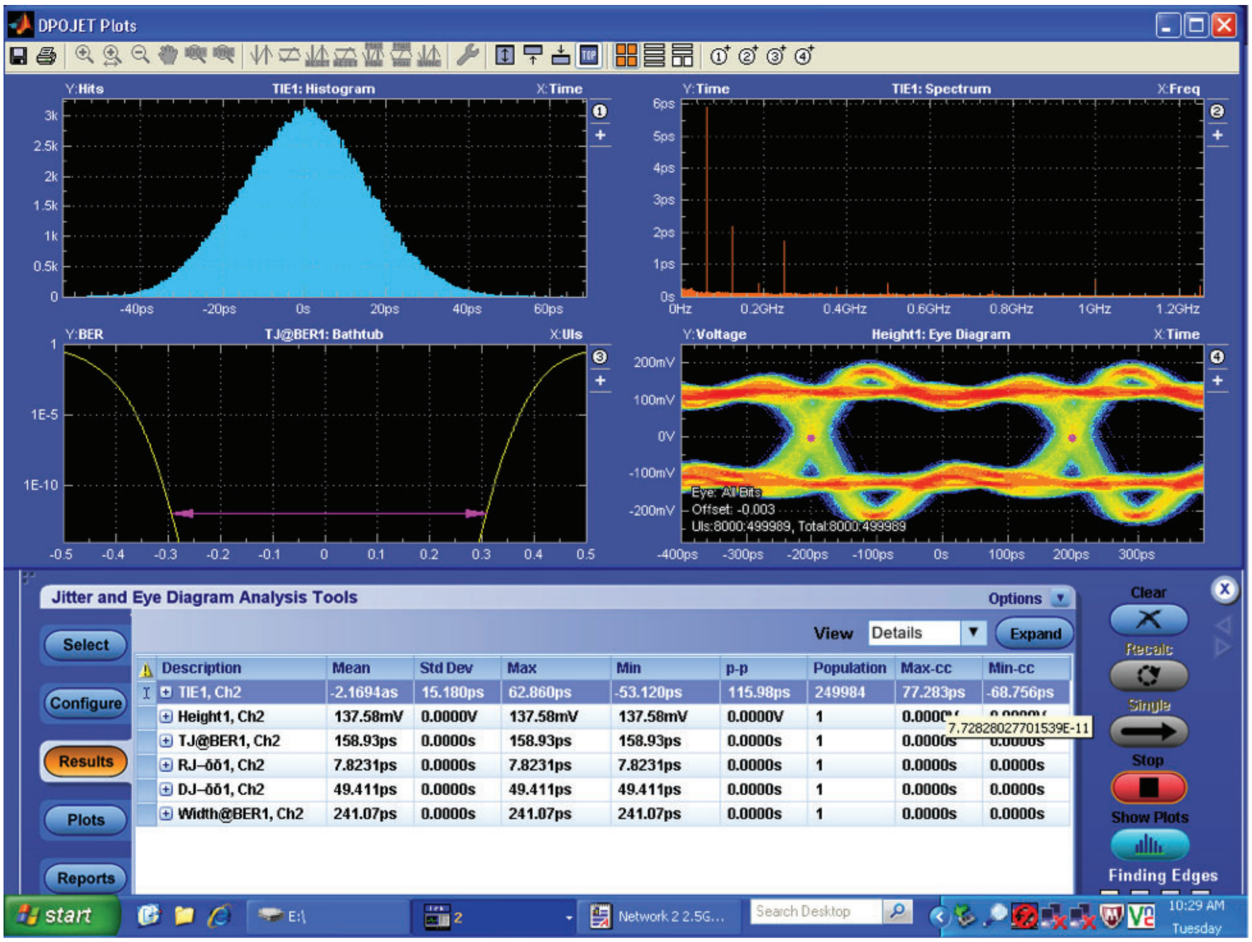


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*Figure 25:* **Test 17: Example 2, PRBS31, 2.5 Gb/s**

## Test 18: Jitter Analysis using Modified Example 2, PRBS7, Rate = 2.5 Gb/s

The purpose of this test is to show the effect of the modified example 2 passive network in terms of jitter. The location of the probe point positions is shown in Figure 7.

Conditions for the test shown in Figure 26:

- Probe point: A
- Operation rate: 2.5 Gb/s
- PRBS7

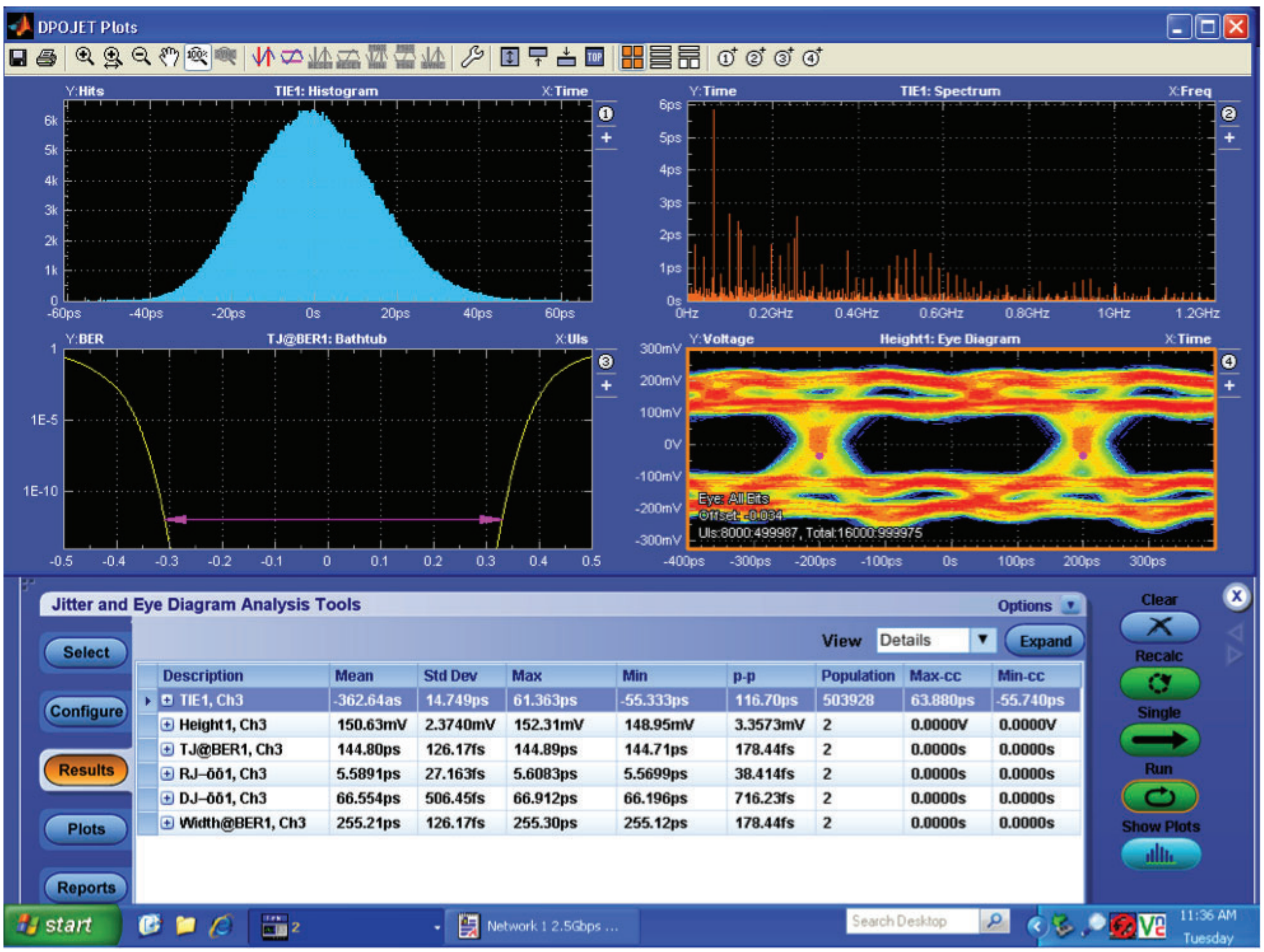


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*Figure 26:* **Test 18: Modified Example 2, PRBS7, 2.5 Gb/s**

Figure 27 shows visible reflections during Test 18.


*Figure 27:* **Test 18 with Reflections Visible**

### Test 19: Jitter Analysis using Modified Example 2, PRBS31, Rate = 2.5 Gb/s

The purpose of this test is to show the effect of the modified example 2 passive network in terms of jitter. This stressed case produces one to two errors every 10 minutes, and the results are considered marginal. The location of the probe point positions is shown in Figure 7.

Conditions for the test shown in Figure 28:

- Probe point: A
- Operation rate: 2.5 Gb/s
- PRBS31

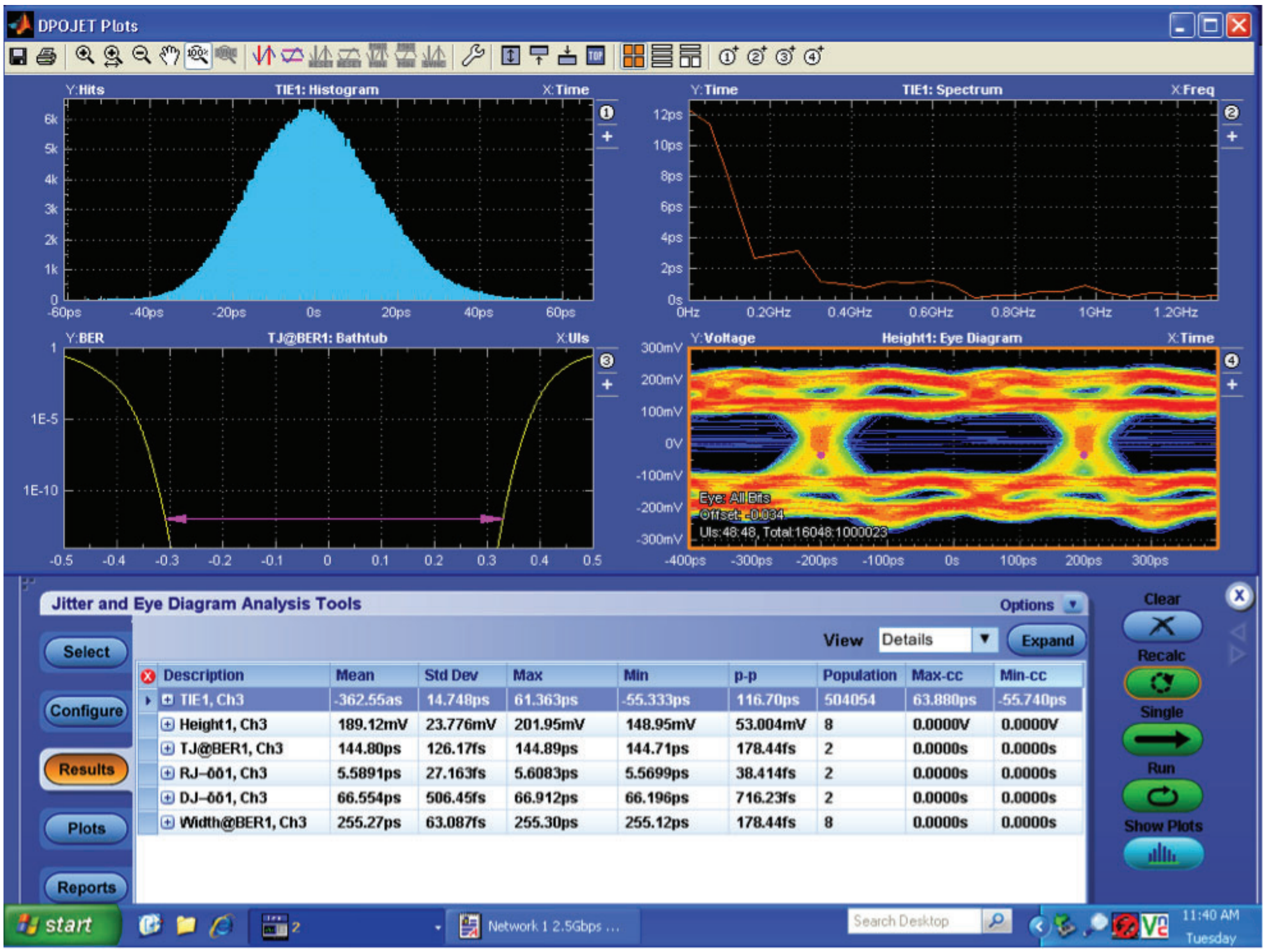


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*Figure 28:* **Test 19: Modified Example 2, PRBS31, 2.5 Gb/s**

## Conclusion

All three passive network examples (example 1, example 2, and modified example 2) have solid performance at the target rate and pattern. Highly stressful conditions were applied to compare behaviors and to observe operating limits. In practice, the link was run at 2.5 Gb/s (72% line rate increase) and PRBS31 (442% increase in the run-length) over the 125°C to –40°C temperature range.

The PRBS standard data patterns are used to stress, at different levels, the capability of a clock data recovery (CDR) to stay locked in the presence of consecutive identical bits (run-length) which are the consecutive missing transitions. A PRBS7 has a run-length of up to 7 and a

PRBS31 of up to 31. Therefore, it is more difficult to receive a PRBS31 data pattern correctly. PRBS7 is the most realistic pattern that resembles HDMI.

In general, example 2 provided better results than example 1. This agrees with the theory that both terminations are ideal from the construction point of view. However, example 1 has more passive components that cause a slight increase in signal integrity degradation. Example 2 cannot be used in the general case but can only be used in the embedded case, as described in Passive Network Example 2, page 4.

When working at PRBS31 and a rate of 2.5 Gb/s, a very small subset of test cases involving example 1 start to show a very low bit error rate (BER). Example 2 is stable when all stressful conditions are applied at the same time.

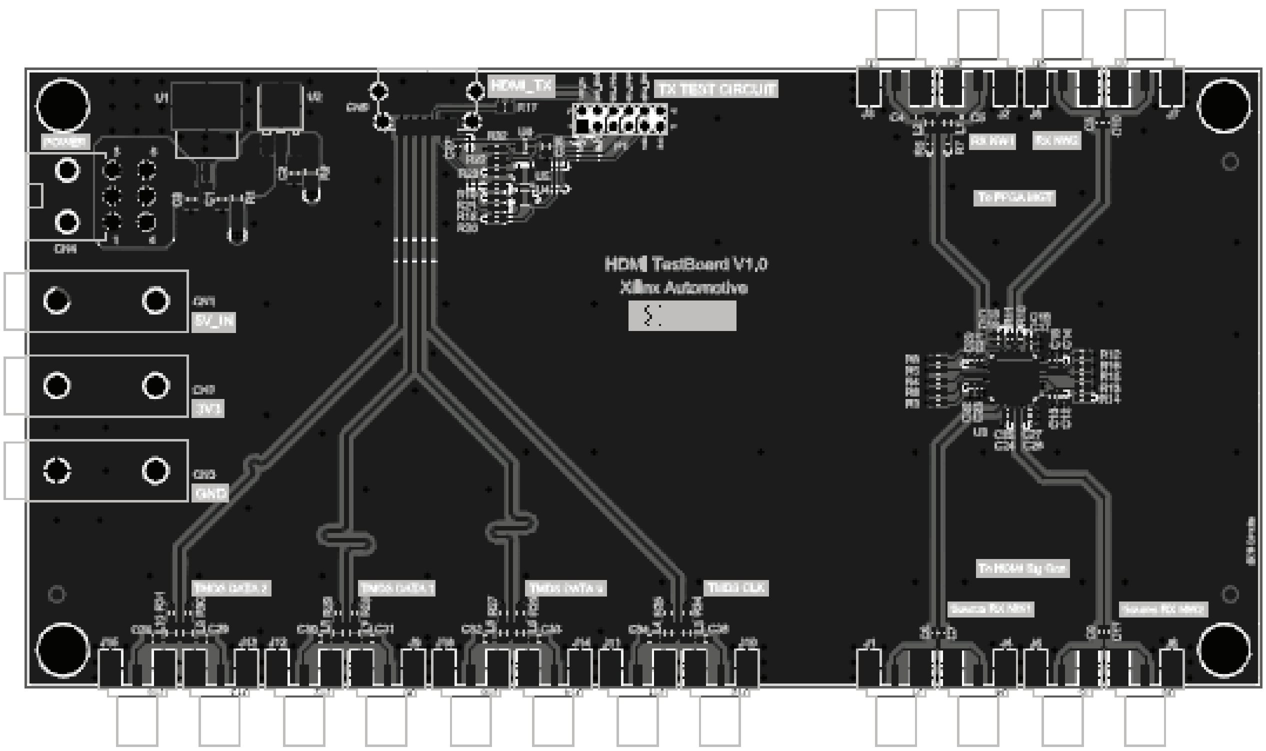
However, example 2 must be placed close to the transmitter. When moved about one inch away, performance starts degrading. With PRBS31 and a rate of 2.5 Gb/s, the modified example 2 displays very few errors over a 10 minute period. When used at the target line rate and coding, the modified example 2 exhibits solid performance over the tested temperature range.

In general, at the target conditions of 1.45 Gb/s and PRBS7, all three networks exhibited solid performance over the tested temperature ranges.

The passive networks analyzed in this application note and the associated measurements results are intended as data points to manage the risks of using Spartan-6 FPGAs to receive an HDMI data stream. These results are delivered as-is and cannot be considered as a qualification report or guarantee of compliance.

## Appendix

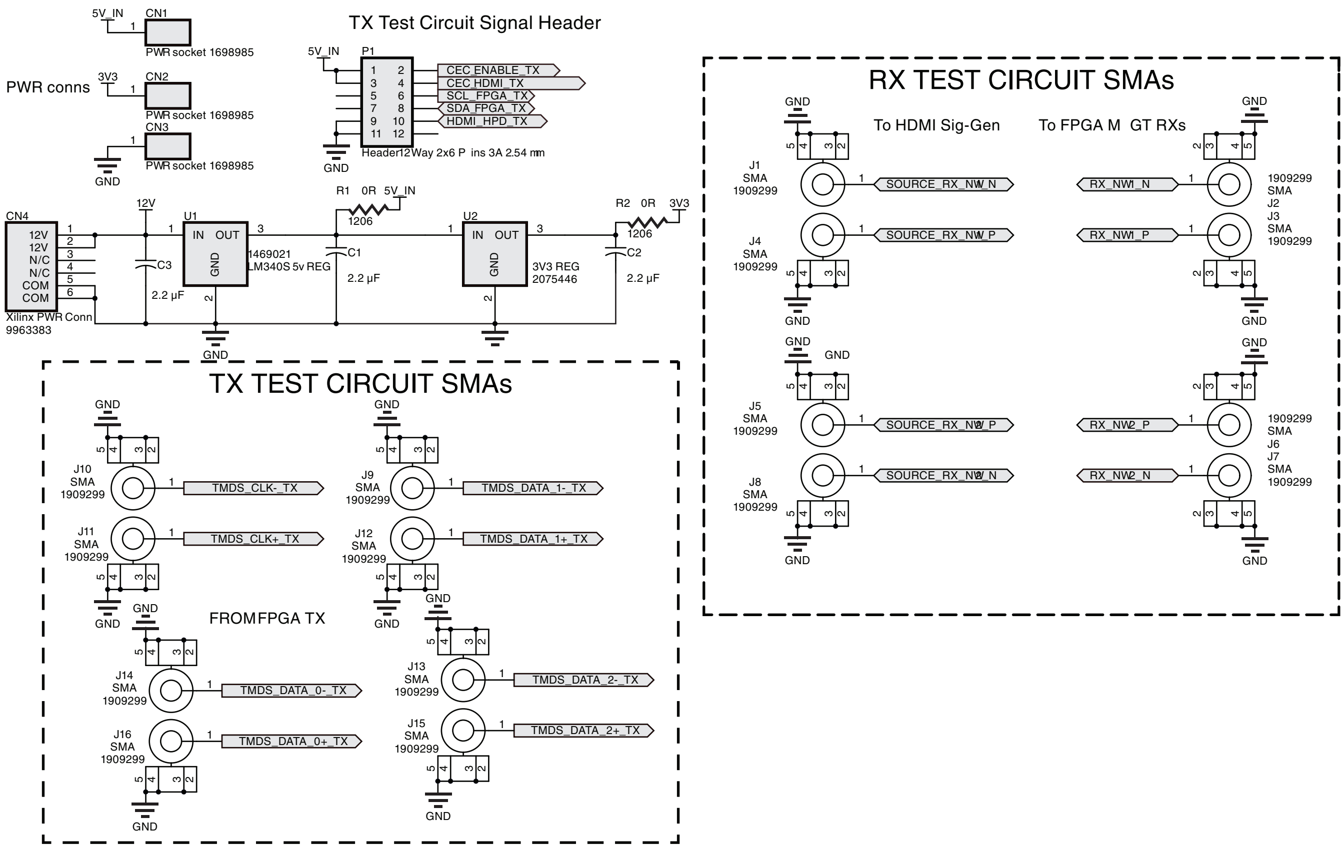
The figures of this appendix include the HDMI card layout (Figure 29) and schematic (Figure 30).




X1077_29_121412

*Figure 29:* **Layout of HDMI Card**

Connectors




X1077_30_010413

*Figure 30:* **Schematic of HDMI Card**

## References


1. HDMI Specification 1.4a, Section 4.2.1
   http://www.hdmi.org/manufacturer/hdmi_1_4
2. STHDLS101T: *AC coupled HDMI level shifter with configurable HPD output* – ST Microelectronics
   http://www.st.com/st-web-ui/static/active/en/resource/technical/document/datasheet/CD00202849.pdf
3. XAPP884, *An Attribute-Programmable PRBS Generator and Checker*


## Revision History

The following table shows the revision history for this document.

| Date | Version | Description of Revisions |
|---|---|---|
| 02/12/13 | 1.0 | Initial Xilinx release. |
| 01/17/14 | 1.0.1 | Corrected typographical errors in Measurements. Updated STHDLS101T reference in References. |

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