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Virtex-6 Embedded Tri-Mode Ethernet MAC Hardware Demonstration Platform

Summary

This application note describes a system using the Virtex®-6 FPGA Embedded Tri-Mode Ethernet MAC (Ethernet MAC) Wrapper core on a Xilinx® Virtex-6 FPGA ML605 development board. The embedded system is controlled by a PC-based Graphical User Interface (GUI) which provides access to the Ethernet MAC's features and several data flow options.

Introduction

The hardware demonstration platform demonstrates the functionality of the following Xilinx LogiCORE™ IP and embedded Ethernet products:

- Virtex-6 Embedded Tri-Mode Ethernet MAC
- Virtex-6 Embedded Tri-Mode Ethernet MAC Wrapper v1.3 core
- Ethernet Statistics v3.3 core

The design demonstrates how to integrate these cores into a system, generate the required clock resources, handle the Ethernet data flow using packet FIFOs and flow control, and connect to a physical interface. An embedded microprocessor is used to manage the embedded system and the Ethernet MAC. Data flow occurs in the fabric logic and is not handled by the microprocessor in real time.

Xilinx provides a GUI which controls the platform through a USB cable allowing the user to change the configurations of the Ethernet MAC, select various data sources, monitor frame information, and observe the Ethernet MAC statistics.

Requirements

Development Board

The Xilinx ML605 development board is the target board in this example; however, the design can be adapted to any board with suitable hardware. The minimum hardware is a Virtex-6 device and a suitable Ethernet interface (GMII/MII, RGMII, and SGMII are all provided in this demonstration platform).

A second Ethernet port is available on the ML605 board, which connects to an SFP optical transceiver capable of 1000BASE-X Gigabit Ethernet functionality. This interface can be used by the demonstration platform in place of the on-board copper PHY. As shipped by Xilinx, the SFP module is not included with the board.

PC

The demonstration platform requires a PC to run the standard Windows XP application. A spare USB port is required to connect the GUI to the development board.

Demonstration Platform System Design

Overview

The hardware demonstration platform consists of the following components:

- An ML605 development board with the demonstration bitstream loaded in the FPGA
- A PC to control the hardware design using a USB A-to-Mini-B cable
- A connection partner (or the design can optionally operate in loopback mode)

Ethernet MAC Hardware Design

Figure 1 illustrates the FPGA design on the ML605, which includes a Virtex-6 Embedded Tri-Mode Ethernet MAC Wrapper core from the CORE Generator™ tool. This wrapper includes a soft FIFO example, clocking logic, and the logic required to interface to the PHY. GMII/MII, RGMII, SGMII and 1000BASE-X PCS/PMA interfaces are used in this example. Also included in the design (and shaded in Figure 1) is the Ethernet Statistics core from the CORE Generator tool.

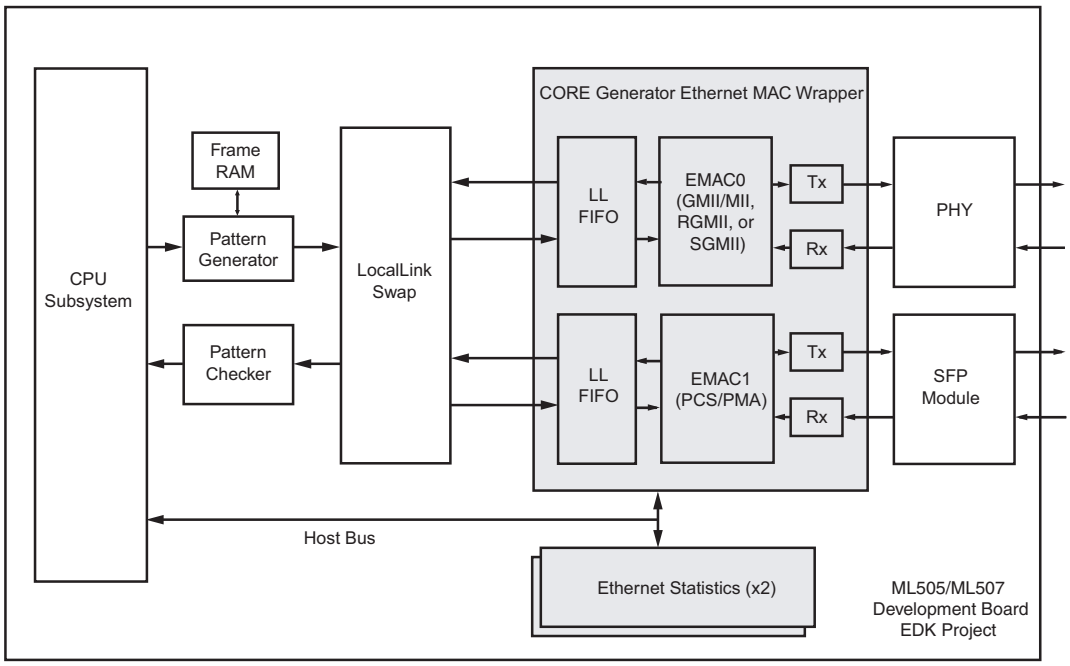

Figure 1: **Ethernet MAC FPGA Block Diagram**

Virtex-6 Embedded Tri-Mode Ethernet MAC Wrapper

The Ethernet MAC wrapper core generated by the CORE Generator software is used with the Virtex-6 Embedded Tri-Mode Ethernet MAC and includes the following components:

- Instantiation of the Embedded Tri-Mode Ethernet MAC primitive.
- Soft FIFO with LocalLink interface (optional). Users can choose to use a direct interface to the Ethernet MAC in their own designs. The FIFO is based on the LocalLink FIFO design. See XAPP691, *Parameterizable LocalLink FIFO Application Note*.
- Clocking logic. See UG368, *Virtex-6 FPGA Embedded Tri-Mode Ethernet MAC User Guide*, for clock options.
- Logic required to interface to the PHY. In this example, GMII/MII, RGMII, SGMII and 1000BASE-X PCS/PMA interfaces are all available.

This demonstration platform instantiates two Ethernet MACs. One Ethernet MAC has a GMII/MII, RGMII, or SGMI interface, and the other uses the optional 1000BASE-X PCS/PMA logic for direct connection to a GTX serial transceiver, which then connects to an SFP optical transceiver device for 1000BASE-X operation. Pinout constraints on the board dictate the serial transceiver and connection options for the 1000BASE-X PCS/PMA interface. See the *Virtex-6 FPGA Embedded Tri-Mode Ethernet MAC User Guide* for detailed information about these constraints and 1000BASE-X PCS/PMA logic.

The Ethernet MAC wrapper cores were generated using the options in the XCO files included in the CORE Generator directory of the .zip file provided with this application note.

Statistics Counters

An instance of the CORE Generator Ethernet Statistics core is used to provide statistical counters for each Ethernet MAC instance. The Ethernet Statistics core is generated using the options in the XCO file included in the CORE Generator directory of the .zip file provided with this application note.

Physical Interfaces

As described in "Virtex-6 Embedded Tri-Mode Ethernet MAC Wrapper" previously, the CORE Generator Ethernet MAC wrapper provides the logic for the physical interfaces. The GMII/MII, RGMII, or SGMII interface is connected to an external 10/100/1000BASE-T PHY (Marvell Alaska 88E1111) included on the ML605. The PHY provides loopback capability to enable the demonstration platform to function without being connected to a link partner.

The 1000BASE-X PCS/PMA interface is connected internally to a GTX serial transceiver, which is connected to the SFP socket on the ML605. An SFP optical module is not provided with the board. The GMII/MII, RGMII, or SGMII interface can be used for all demonstration functions if a transceiver and link partner are not available.

Clock Management

The embedded system provides all necessary clocks for the design. Except for SGMII configurations, an on-board 200 MHz reference clock drives a Mixed-Mode Clock Manager (MMCM), which in turn provides the majority of the clocks for the embedded system. This includes the Ethernet MAC logic at 125 MHz, 25 MHz, or 2.5 MHz, as defined by the Embedded MAC operating speed. The clocking management logic also provides phase-shifting abilities to align the PHY's clock and data on the receive interface. When the physical interface is put into loopback, the clock management logic sets the receiver clock input to the transmitter clock.

LocalLink Swap

The LocalLink Swap module provided allows the LocalLink interface from the pattern generator to be connected to either Ethernet MAC. This module also provides the loopback function that connects the RX FIFO to the TX FIFO so the user can inject frames at the physical interfaces and see them echoed back. Optionally, the loopback function can swap the source and destination addresses of the Ethernet frame to provide a basic *ping*-type function.

Microprocessor System

Figure 2 illustrates the microprocessor system, which is based on a soft MicroBlaze™ v7.20b processor and PLB v4.6-based subsystem containing 16k RAM, UART (uartlite), interrupt controller, LMB (for block RAM connection), GPIO, and custom peripherals for connecting the Ethernet MACs through the LocalLink interface.

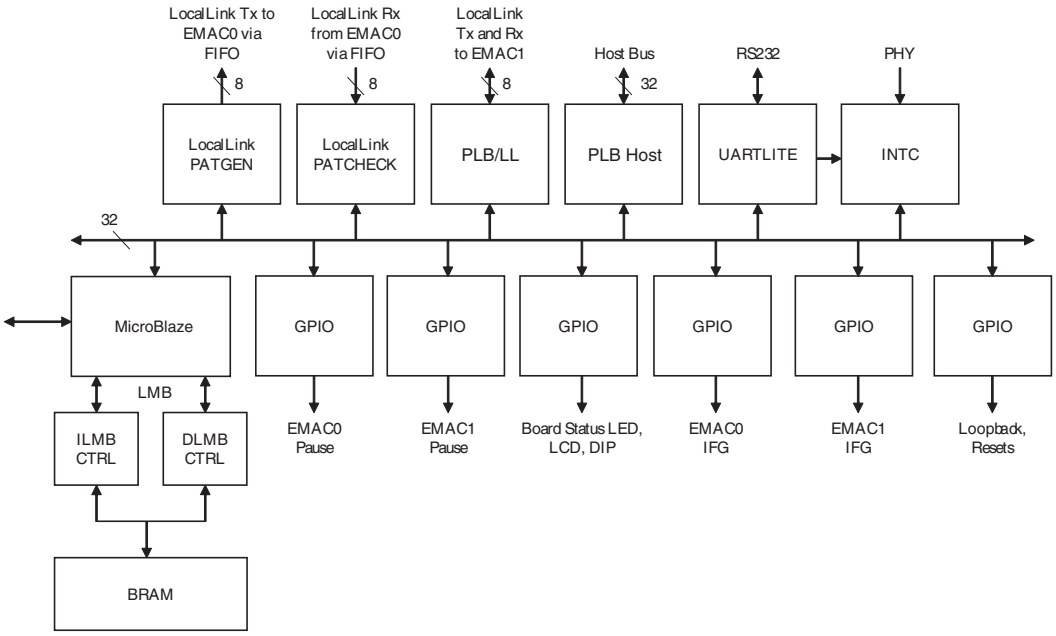

Figure 2: **Microprocessor System Block Diagram**

Custom Peripherals

- **Pattern Generator** (plb_ll_patgen). The Pattern Generator peripheral holds all the logic required to access the client-side transmit data stream of the Ethernet MAC, allowing data to be written to the TX FIFO. The patterns are stored in dedicated block RAM which can be loaded by the processor and read by logic. Then, the data is passed to the FIFO through the LocalLink interface.
- **Pattern Checker** (plb_ll_pat_chk). The Pattern Checker peripheral logic, when configured in the user mode, uses the LocalLink interface to access the client side received data from the Ethernet MAC. The pattern checker must be configured in user mode (the default mode) if one wishes to read the data received. The pattern checker can be configured in auto mode to run line speed tests. In auto mode, the pattern checker verifies that the received data are pre-determined sequences.
- **PLB/LL** (plb_ll). The pattern generator is connected to the one Ethernet MAC as selected by the GUI. The unused Ethernet MAC is connected to the PLB v4.6 through a simple byte-wide interface. It is not used by the GUI or demonstration platform.
- **Host** (plb_host). The Host peripheral allows the management interface of the Ethernet MAC to be accessed. Through this interface, the MAC configuration can be read and modified, the statistics counters can be read, and the MDIO transactions can be made to control the physical layer.

Microprocessor Software

The microprocessor runs software that monitors the serial interface and responds to commands issued by the GUI. On startup, the microprocessor detects what design is operating on the FPGA, configures the logic on the FPGA appropriately, and then waits for and processes commands from the PC.

Setting up the Demonstration Platform

ML605 Configuration

Power Supply

The power supply provided with the ML605 is used to power the demonstration board.

Switch and Jumper Settings

Various DIP switches and jumpers must be configured to enable proper Ethernet operation on the ML605. Table 1 defines switch settings to enable both JTAG and System ACE™ technology bitstream downloading.

Table 1: **DIP Switch Settings**

Switch	Setting
S1	• 1 = OFF • 2 = OFF • 3 = OFF • 4 = ON
S2	• 1 = OFF • 2 = ON • 3 = ON • 4 = OFF • 5 = ON • 6 = OFF

The jumpers in Table 2 must be installed. Note that J67 and J68 are set according to the desired physical interface connection to the BASE-T Ethernet PHY and must match the bitstream downloaded to the FPGA (individual GMII/MII, RGMII, and SGMII bitstreams are provided). Jumpers not listed here can be left in their default state or unpopulated. See UG534, *ML605 Hardware User Guide*, for detailed information about the function of each jumper and switch.

Table 2: **Jumper Settings**

Jumper	Setting
J17	Jumper between pins 1 and 2
J18	Jumper between pins 1 and 2
J54	Jumper between pins 1 and 2
J65	Jumper between pins 1 and 2
J66	For GMII/MII connectivity to Ethernet PHY: Jumper between pins 1 and 2 For RGMII connectivity to Ethernet PHY: Jumper between pins 1 and 2 For SGMII connectivity to Ethernet PHY: Jumper between pins 2 and 3
J67	For GMII/MII connectivity to Ethernet PHY: Jumper between pins 1 and 2 For RGMII connectivity to Ethernet PHY: Open For SGMII connectivity to Ethernet PHY: Jumper between pins 2 and 3
J68	For GMII/MII connectivity to Ethernet PHY: Open For RGMII connectivity to Ethernet PHY: Jumper between pins 1 and 2 For SGMII connectivity to Ethernet PHY: Open

UART

Connect a USB A-to-Mini-B cable to the port labeled "UART" on the ML605 and a spare USB port on the PC. When the board is powered on, Windows XP will install a USB-to-UART bridge driver. However, Xilinx recommends installing the driver provided with the ML605. Please see the Hardware Setup Guide included with the ML605 for details.

LCD

The LCD provides basic information about the status of the MicroBlaze processor software.

On-board Tri-Speed PHY

The ML605 includes a Marvell tri-speed BASE-T PHY. This is connected to an Ethernet MAC in the demonstration platform. A gigabit compatible RJ45 patch lead should be connected to the PHY. A crossover cable is required for direct connection to another Gigabit Ethernet device; otherwise, use a normal cable for connection to a Gigabit Switch.

FPGA Configuration

There are two ways to configure the FPGA:

- Using iMPACT to download the appropriate bitfile via JTAG. For GMII/MII connectivity to the BASE-T PHY, use `download.bit`; for RGMII connectivity, use `download_rgmii.bit`; for SGMII connectivity, use `download_sgmii.bit`. Note that the bitfile used must be accompanied by the matching jumper settings as specified in Table 2. All bitfiles include 1000BASE-X PCS/PMA connectivity to the optional SFP device.
- Using a properly-formatted CompactFlash card containing a System ACE file generated from one of the bitfiles provided with this application note. The System ACE controller on the ML605 will read from the CompactFlash card and configure the FPGA upon power up. For more information on the System ACE tool, refer to System ACE solution resources at www.xilinx.com/support/documentation/system_ace_solutions.htm.

Graphical User Interface

The GUI lets the user control the Ethernet MAC wrapper core in the demonstration platform and the other components within the design, and is comprised of the following:

- Serial Port Selection and Interface Selection dialog boxes, displayed on startup
- Main screen, which contains several tabs for setting design options
- MAC Statistics Screen

Installing and Running the GUI

1. Extract the project files from the application note .zip file into a new directory on the PC (for example, `c:\xapp1144`).

   Note: Do not download the demonstration platform to a directory path containing spaces; this causes errors when running the GUI.
2. Download the appropriate hardware design onto the FPGA.
3. Navigate to `c:\xapp1144\code\pc\rtf\` (if you saved the zip file contents to `c:\xapp1144`).
4. Double-click `xapp1144.exe` to start the GUI.

Serial (COM) Port Selection

Figure 3 displays the Serial Port selection dialog box, used to select the COM port to communicate with the board.

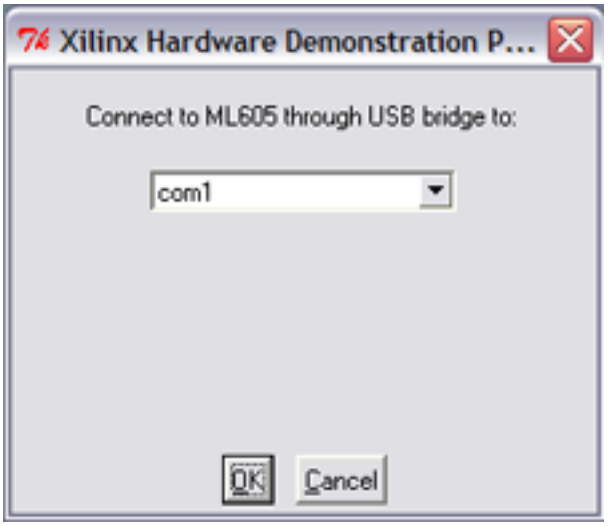

Figure 3: **Serial (COM) Port Selection Screen**

To select a port:

1. Select the appropriate COM port from the drop-down menu. The USB-to-UART bridge controller's assigned COM port can be determined from the Windows XP Device Manager, under **Ports (COM & LPT)**.
2. Click OK and wait for the link to be established with the board. After connection, the Interface Selection dialog box will appear.

   If a link is established with the board, the board and Ethernet MAC type will be displayed at the bottom of the screen.
3. If a connection to the board cannot be established, an error message will appear at the bottom of the main screen. Verify that the board is turned on, the FPGA is configured with the correct bitfile, the USB cable is connected, the correct COM port was chosen, and then restart the GUI.

Ethernet Interface Selection

Figure 4 displays the Interface Selection dialog box, which appears after selecting the correct COM port.

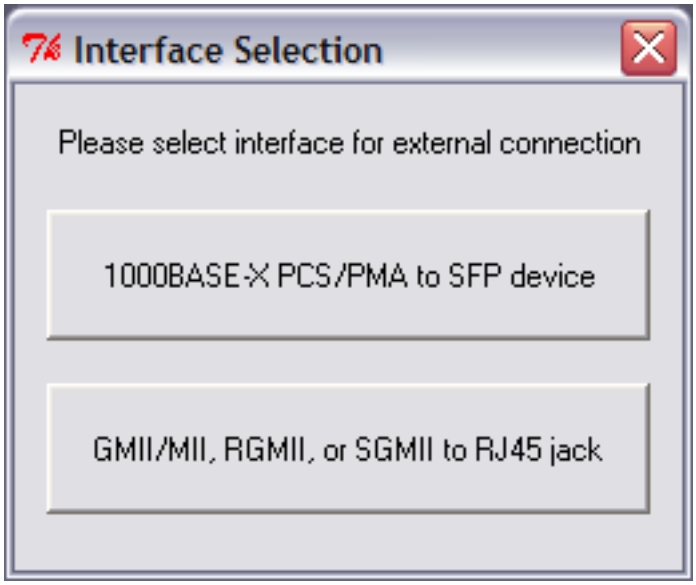

Figure 4: **Interface Selection**

To select an interface:

Click the physical interface that you intend to use. For copper connectivity using the RJ45 jack, either GMII/MII, RGMII, or SGMII can be used, and is determined through the choice of bitstream and jumper settings as previously described. For 1000BASE-X PCS/PMA connectivity to the SFP device, a Gigabit Ethernet-compatible SFP device must be installed. If the demonstration platform will be used in loopback, either interface can be selected.

Main Screen

Figure 5 displays the main GUI screen.

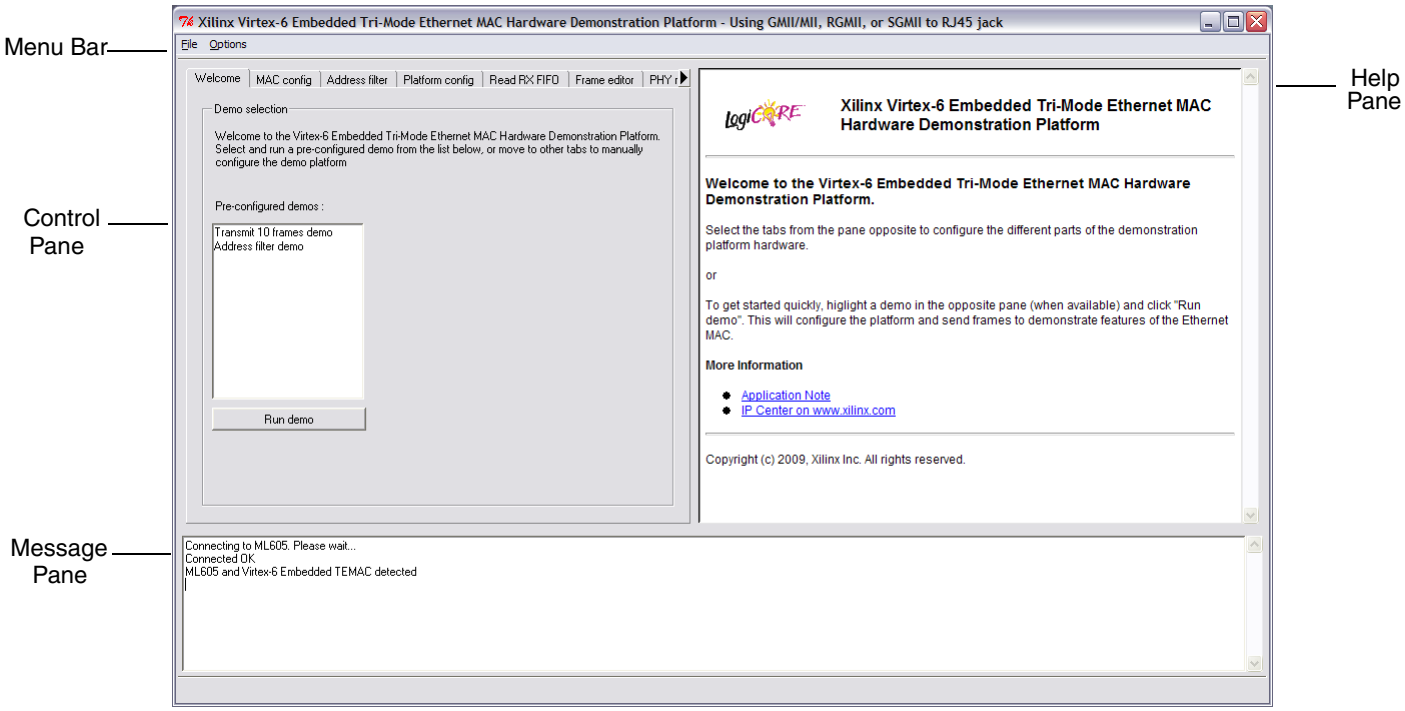

Figure 5: **Main Screen**

The Main Screen consists of four areas:

Menu Bar

A standard Windows toolbar across the top of the screen.

Control Pane

The control pane at the left side of the window displays several tabs for selecting design options:

- Welcome
- MAC Config
- Address Filter
- Platform Config
- Read RX FIFO
- Frame Editor
- PHY Registers

Help Pane

Displays context-sensitive help at the right side of the window.

Message Pane

Displays debug and status messages at the bottom of the window.

Function Tabs

The following tabs in the Control Pane are used to select design options.

Welcome Tab

The Welcome Tab (Figure 6) is used to run pre-configured demos. The available pre-configured demos are “Transmit 10 frames demo,” which transmits 10 frames in PHY loopback mode and reads them from the FIFO, and “Address filter demo,” which demonstrates the effects of the address filter. These demos are currently available only for GMII/MII, RGMII, or SGMII configurations.

To run a demo:

Click a selection in the Pre-configured demos area of the dialog box, then click **Run demo**. After the demo runs, a message appears in the Message pane.

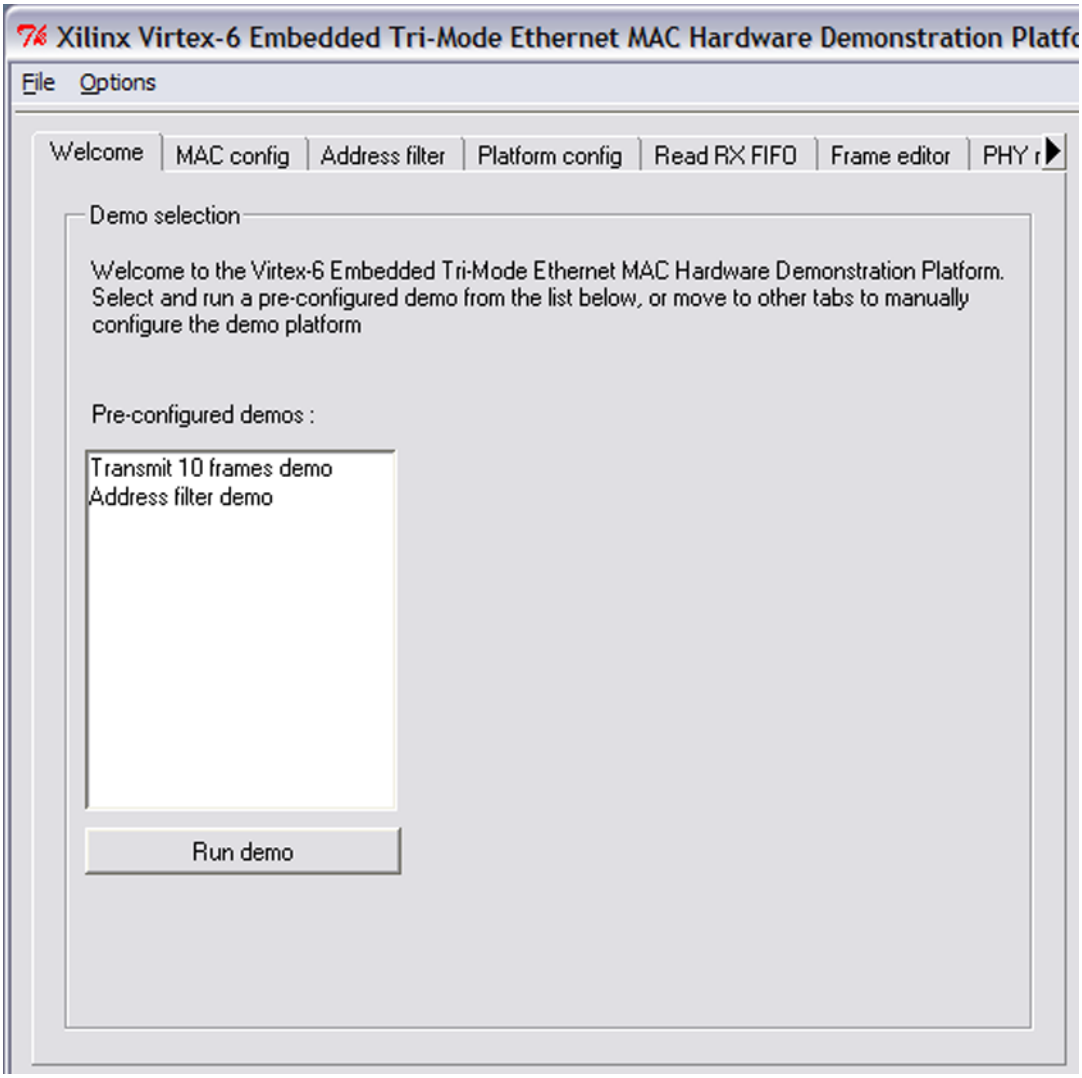

Figure 6: **Control Pane**

MAC Config Tab

The MAC config tab (Figure 7) modifies the configurable features of the selected Ethernet MAC. When the FPGA is configured, this screen displays the default configuration for the Ethernet MAC.

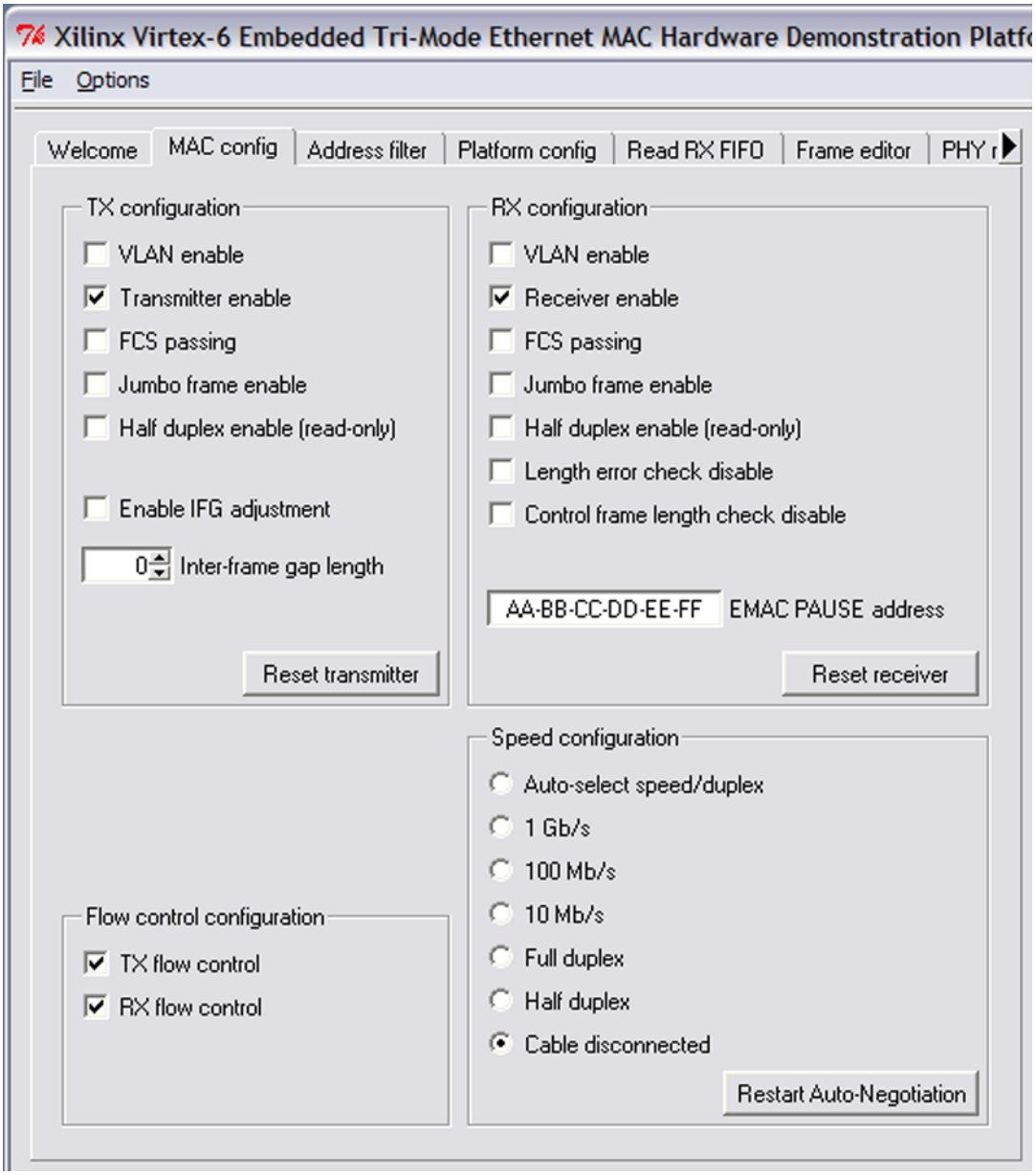

Figure 7: **MAC Config Tab**

Transmitter Configuration

TX (Transmitter) configuration options:

- **VLAN enable**. When selected, enables transmission of VLAN frames.
- **Transmitter enable**. Enables the transmitter to send frames.
- **FCS passing**. Client provides the FCS for each frame rather than the Ethernet MAC.
- **Jumbo frame enable**. Enables transmission of jumbo frames.
- **Half duplex enable (read-only)**. Indicates whether half-duplex mode is in use for the transmitter.

- **Enable IFG adjustment**. Select this option to subsequently enter an inter-frame gap length.
- **Inter-frame gap length**. When Enable IFG adjustment is selected, the value in this field is the inter-frame gap length used between frames while transmitting.

Receiver Configuration

RX (Receiver) configuration options:

- **VLAN enable**. When selected, enables reception of VLAN frames.
- **Receive enable**. Enables the receiver to receive frames.
- **FCS passing**. Receiver passes the received FCS to the client.
- **Jumbo frame enable**. Enables reception and passing of jumbo frames.
- **Half duplex enable (read-only)**. Indicates whether half-duplex mode is in use for the receiver.
- **Length error check disable**. Received frames are not checked for length errors.
- **Control frame length check disable**. Enables reception of control frames larger than 64 bytes.
- **EMAC PAUSE address.** The PAUSE address used in the generated PAUSE frames.

Flow Control Configuration

Transmit and Receive flow control can be enabled or disabled by the user, allowing observation of the flow control functionality.

Speed Configuration

The speed configuration for the Ethernet MAC demonstration platform does not provide direct access to the speed registers in the Ethernet MAC, but rather sets the advertised speed and duplex for auto-negotiation purposes. Once auto-negotiation has completed, the Ethernet MAC speed registers are updated accordingly. The speed configuration selected depends on whether loopback is selected.

- **Auto select speed/duplex**. Allows auto-negotiation to determine the speed and duplex mode.
- **1 Gb/s**. Sets the advertised link speed to 1 Gb/s.
- **100 Mb/s.** Sets the advertised link speed to 100 Mb/s.
- **10 Mb/s**. Sets the advertised link speed to 10 Mb/s.
- **Full duplex**. Sets the advertised mode to full-duplex mode of operation.
- **Half duplex**. Sets the advertised mode to half-duplex mode of operation.
- **Cable disconnected**. Indicates that no cable is connected.
- **Restart Auto-Negotiation**. Causes the Ethernet MAC to initiate auto-negotiation. Auto-negotiation is automatically initiated by Ethernet MAC on power on, reset, or loss of link.

Loopback Mode Setting

When the interface is set to loopback mode (see "Platform Configuration Tab," page 14) configure the speed in the following way:

1. Select Auto select speed/duplex to use the Ethernet MAC at the fastest speed or select a specific speed and duplex combination.
2. Click Restart Auto-Negotiation. The GUI speed/duplex options are deasserted until the Ethernet MAC has been configured for the new speed.

Note: As the physical side is being looped back, only full-duplex operation can be used. Half-duplex mode fails.

External Device Mode

When an external device is being used and the physical interface is selected to use the external device, configure the speed in the following way:

1. Select either Auto select speed/duplex to use the Ethernet MAC at the fastest speed, or select a specific speed and duplex combination.
2. Click Restart Auto-Negotiation. The GUI speed/duplex options are deasserted until the Ethernet MAC has been configured for the new speed.

If Auto select speed/duplex is selected, clicking Restart Auto-Negotiation forces the PHY to advertise all speed/duplex combinations or to advertise only the requested speed/duplex combination. The PHY is then set to restart Auto-Negotiation with the external device.

After completion of Auto-Negotiation, the demonstration platform reads the PHY registers to determine the link speed/duplex and then appropriately configures the Ethernet MAC. The GUI speed/duplex options are then reasserted to show the operating speed/duplex. If an error occurs during Auto-Negotiation, it is displayed in the message pane.

Note: If the link to the external device goes down at any time, the GUI speed/duplex options disappear from the speed configuration and return when the link is re-established.

Address Filter Tab

The Address filter tab (Figure 8) controls address filtering on the receiver of the Embedded Tri-Mode Ethernet MAC. Address filtering can be enabled or disabled and addresses can be written into the table in hexadecimal using the Address filter tab.

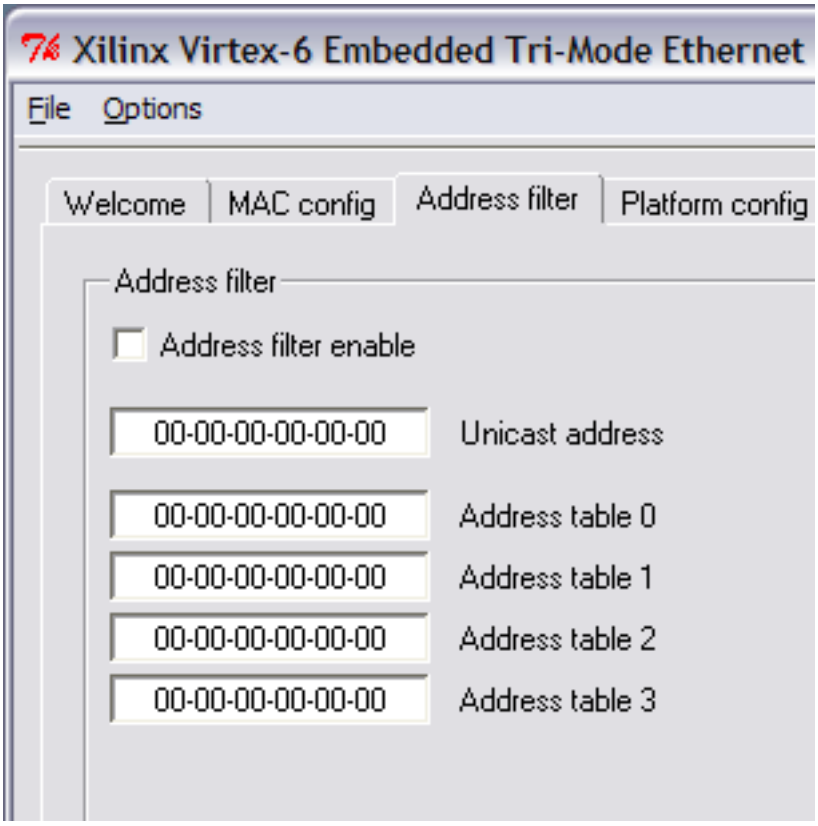

Figure 8: **Address Filter Tab**

If an external device is connected to the demonstration platform and is intended to receive frames from the device, the address filter must be configured with the MAC address the external device is using as a Destination Address. Otherwise, disable address filtering.

If loopback is selected on the Platform configuration tab, the address filter should be configured with the address set in the frame editor, the destination address used by the pattern generator (11-22-33-44-55-66), or disabled.

Platform Configuration Tab

The Platform config tab (Figure 9) controls the data sources in the demonstration platform.

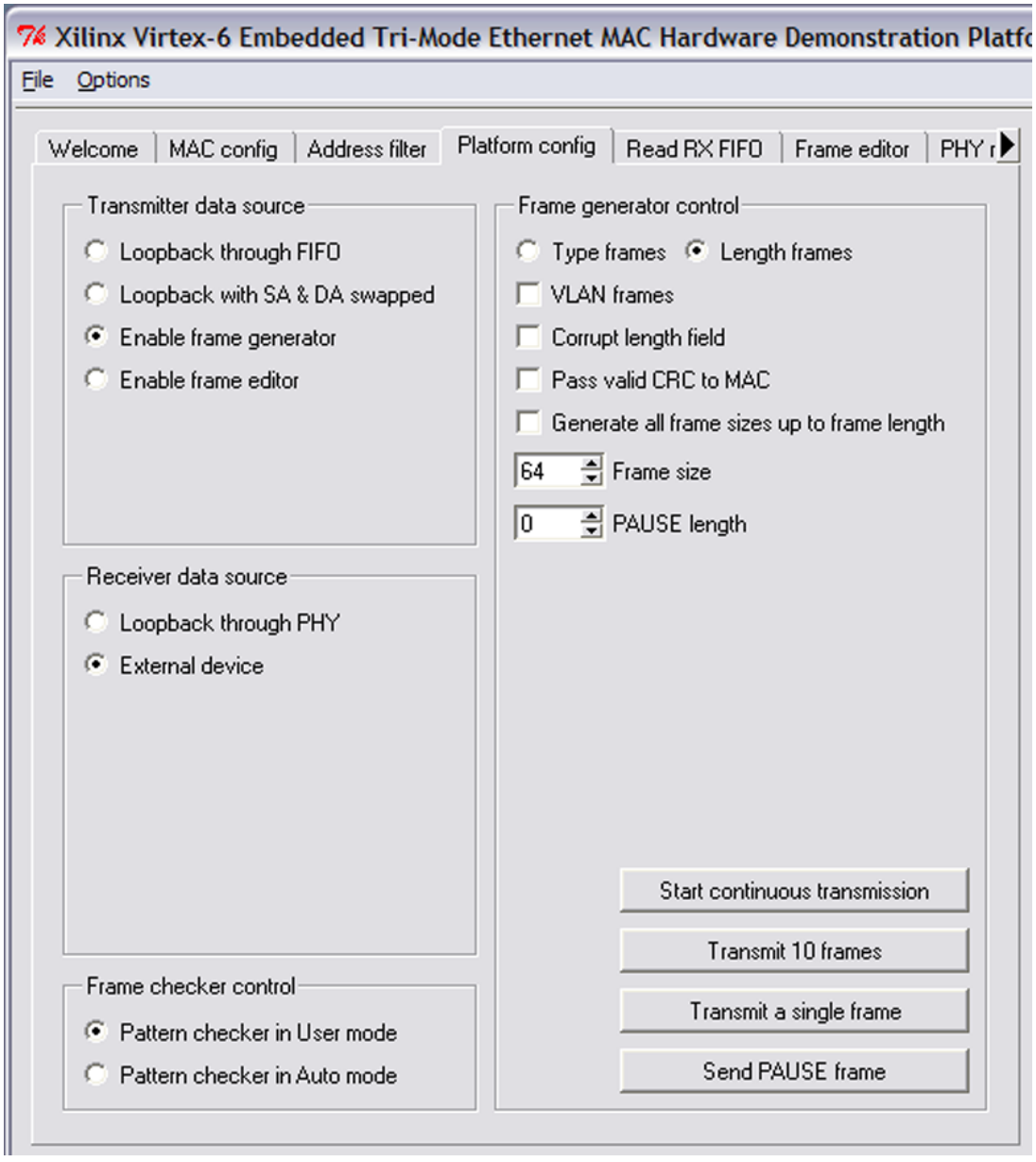

Figure 9: **Platform Config Tab**

Transmitter Data Source

The client side transmitter interface of the Ethernet MAC can be connected to one of three data sources:

- **Loopback through FIFO** and **Loopback with SA & DA swapped** (source address and destination address). Connects the data path from the Ethernet MAC client-side receiver to the transmit path. Data passes from the Ethernet MAC receiver to the receive FIFO, then directly to the transmit FIFO and finally to the Ethernet MAC transmitter.

  If Loopback with SA & DA swapped is selected, the first 6 bytes of each frame are swapped with the following 6 bytes, switching the source and destination address. This *ping*-style loopback allows an external device to send frames to the demonstration platform and receive correctly addressed frames back.
- **Enable frame generator**. Connects the transmit FIFO to the hardware pattern generator. Options for controlling the pattern generator are also set in this tab and are described in "Frame Generator Control."
- **Enable frame editor**. Connects the transmit FIFO to the block RAM-based frame editor, allowing the user to enter and transmit any frame using the GUI. The Frame editor is controlled in the Frame editor tab; see "Frame Editor Tab," page 19.

Receiver Data Source

- **Loopback through PHY**. Connects the transmitter to the receiver through the external BASE-T PHY or internal 1000BASE-X PCS/PMA logic.
- **External Device.** Configures the receiver for connection to an external device.

Frame Generator Control

The Frame Generator generates various frame types and lengths.

- **Type frames**. The pattern generator inserts hexadecimal 0800 in the length/type field of each frame.
- **Length frames**. The pattern generator inserts the length of the data contained in each frame into the length/type field of each frame.
- **VLAN frames**. The pattern generator inserts a VLAN tag into each frame. The total length of each frame is unchanged but the length field is adjusted to indicate less data in each frame.
- **Corrupt length field**. The length field is set incorrectly, resulting in an errored frame.
- **Pass valid CRC to MAC**. Complete frame along with the received CRC (FCS field) is passed to the client.
- **Generate all frame sizes up to frame length**. The pattern generator starts transmitting 19-byte frames (padded by the Ethernet MAC) and continually increments the length of subsequent frames by 1 byte. When the length is equal to the length selected for frame length, the length is set back to 19 and the process repeats. Use this option for transmitting frames continuously.
- **Frame size**. Sets the total size for frames sent to the transmitter. If the value is less than 60, the Ethernet MAC pads the frame unless configured for FCS passing.
- **PAUSE length**. Sets the 16-bit pause length input to the Ethernet MAC, which is used if Send PAUSE frame is selected.

The four buttons below the Frame Generator section send frames to the Ethernet MAC transmitter and trigger transmission by the pattern generator.

- **Start continuous transmission**. Sends frames to the Ethernet MAC until the same button, (now **Stop transmission**) is clicked.
- **Transmit 10 frames**. Enables one-shot mode, in which ten frames are sent.
- **Transmit a single frame**. Enables one-shot mode in which a single frame is sent.
- **Send PAUSE frame**. Sends a single PAUSE frame by asserting the pause request input to the Ethernet MAC.

To enable these options, the Transmitter data source must be set to Enable frame generator.

Read RX FIFO Tab

The Read RX FIFO tab (Figure 10) reads frames from the receive-side FIFO received by the Ethernet MAC core. The FIFO cannot be read if the platform is configured for loopback through the FIFO.

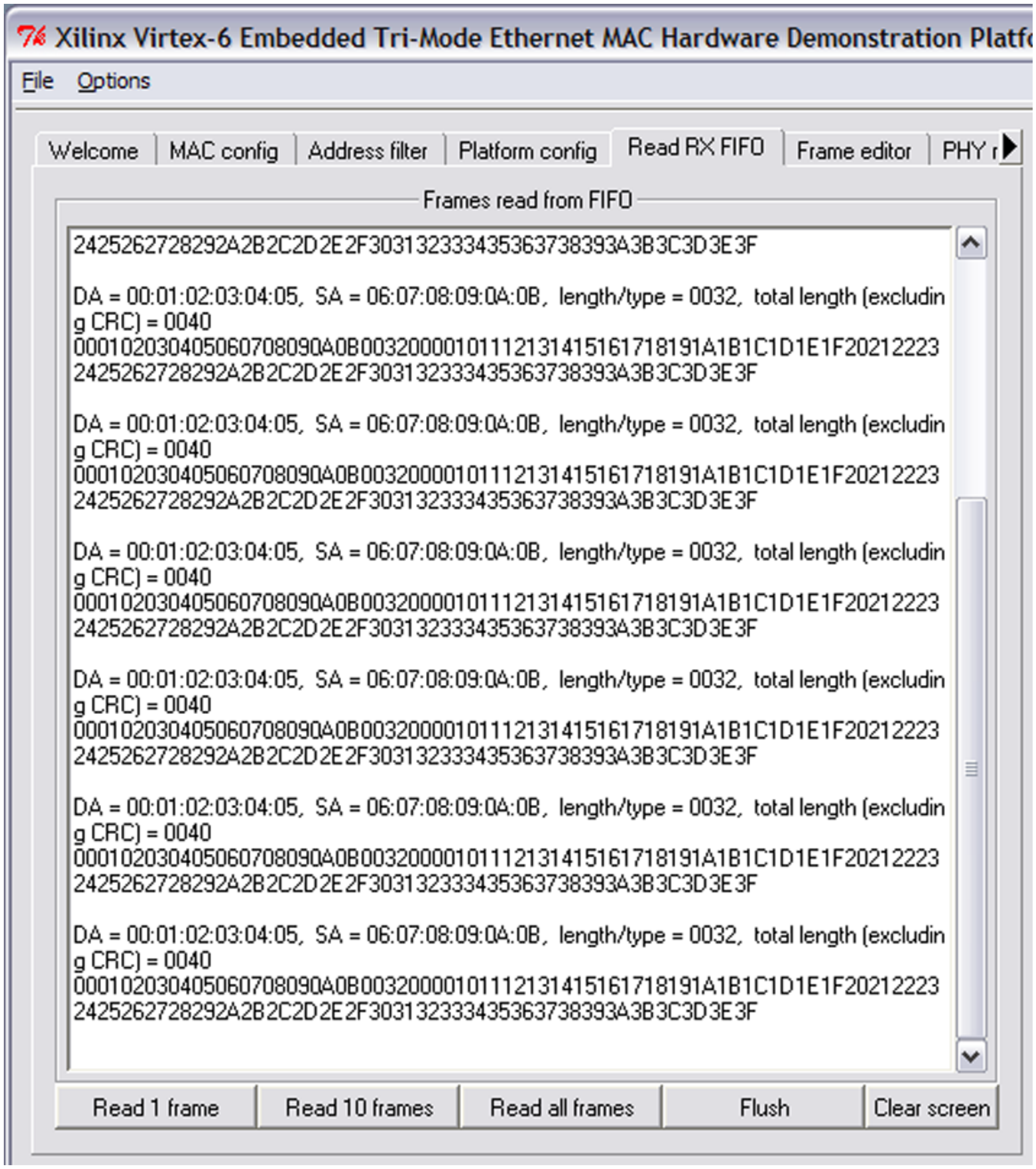

Figure 10: **Read Receive FIFO Tab**

Read frame options include:

- Read 1 frame
- Read 10 frames
- Read all frames
- Flush
- Clear screen

The FIFO stores all frames received from the Ethernet MAC until it is full. When full, the FIFO discards further incoming frames. The FIFO is 4 kilobytes deep.

Care should be taken when mixing frame sizes. If the FIFO is nearing full and a frame larger than the remaining space is received, it is discarded. If the next frame is smaller than the remaining space, it is stored in the FIFO. This situation should not be confused with frame loss.

To read frames from the receive FIFO, flush the FIFO before initiating transmission to ensure that the FIFO has space to store the new frames. After transmission is started, the FIFO can be read. During continuous reception of frames, a snapshot of the data can be captured by flushing the FIFO, which will cause it to discard any stored frames, and store the next 4 kilobytes of frame data received. The user can read a single frame or all available frames.

During continuous reception, the FIFO is unlikely to empty because data can enter the FIFO at a much faster rate than can be transmitted across the serial link to the GUI. To prevent an endless upload of frames to the GUI, a maximum of 64 frames can be read at once. To read more frames, continue clicking **Read all frames**.

Frame Editor Tab

The Frame editor tab (Figure 11) loads frames into the RAM in the pattern generator, which can then be sent to the Ethernet MAC core for transmission. Enable frame editor must be selected on the Platform config tab to enable this functionality.

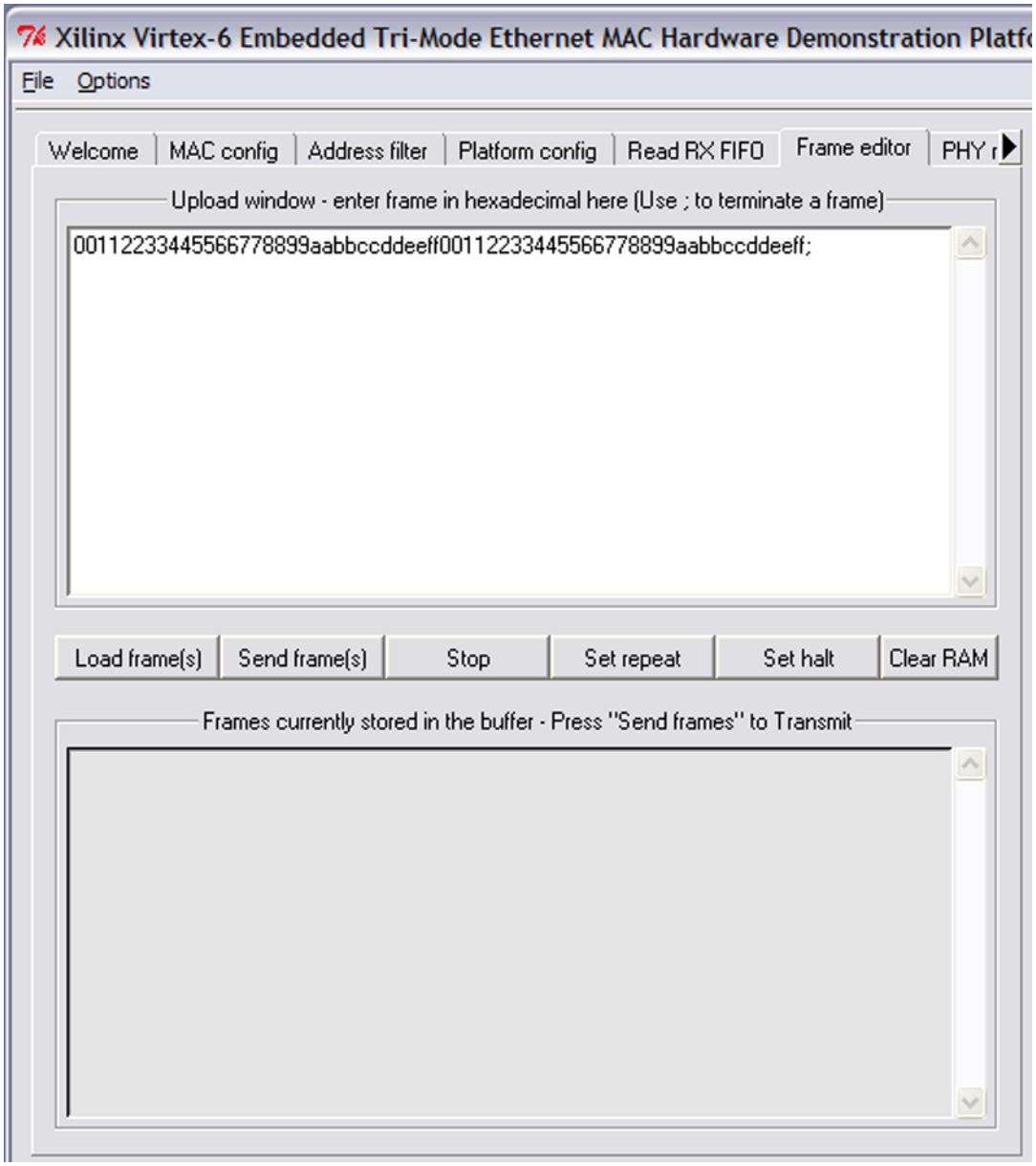

Figure 11: **Frame Edit Tab: Data Entry**

Frame data should be entered in hexadecimal in the Upload window, as displayed above. Multiple frames can be entered and uploaded at the same time.

Syntax for entering frames:

- White space and CR/LF characters are ignored
- Data must only contain the characters 01234567890ABCDEFabcdef
- Each frame must be terminated with a semicolon
- Each frame must have an even number of characters (nibbles)

Valid frame example:

```
1122334455667788990OAAbbCCddEE;
1 2 3 4 5 6 7 8;11223344; 2 35556;
```

Invalid frames example:

```
123456789;
11223344rt56;
```

(uneven number of nibbles will give a warning)
(invalid hex characters)

Example inaccuracies:

```
11223344556677889900
12345678123456789012;
```

The input is treated as a single frame. The carriage return is not treated as a frame terminate character.

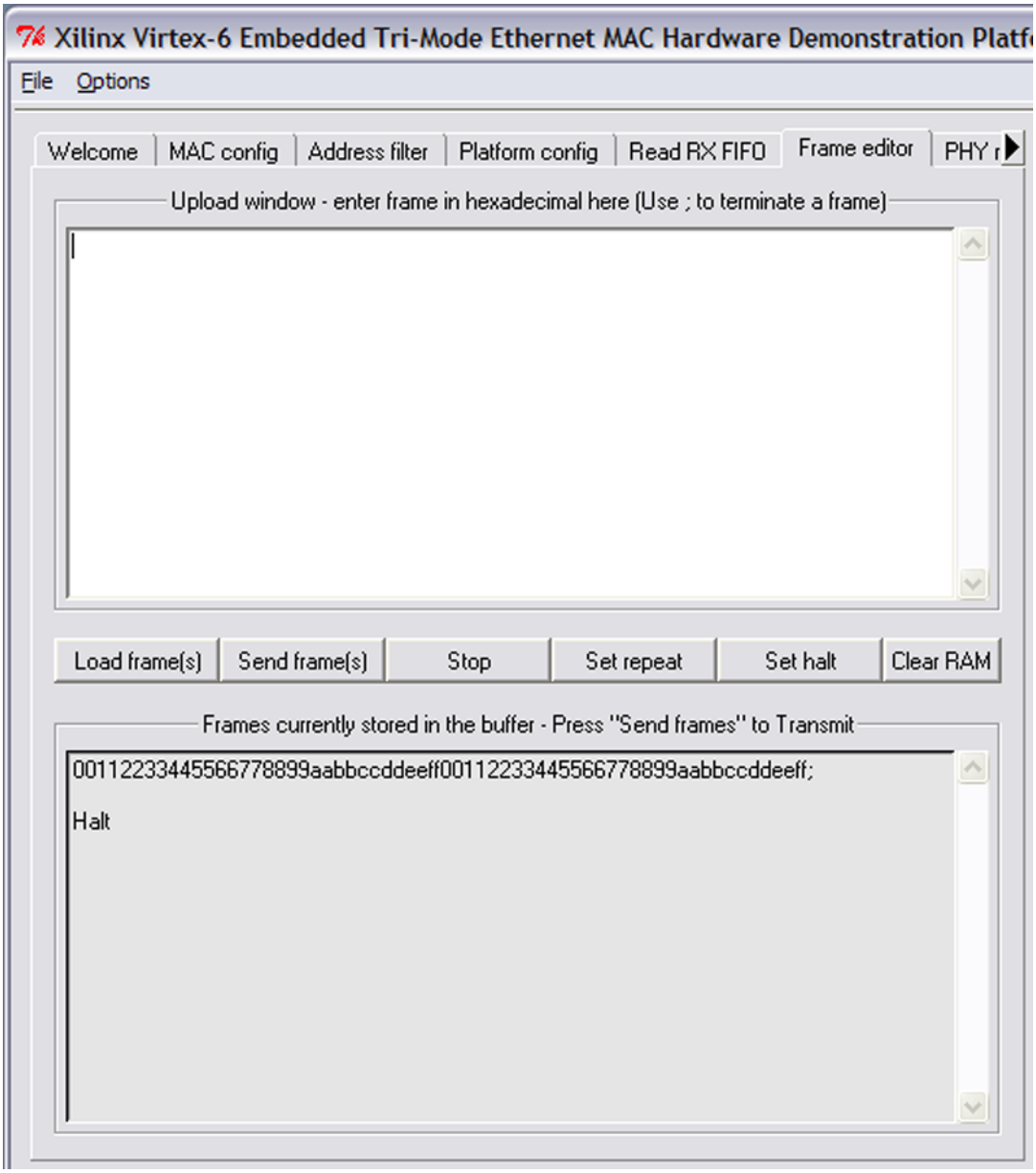

Figure 12: **Frame Edit Tab: Buffer Display**

- **Load frames(s)**. Loads frames into the block RAM. When an error is detected on an entered frame, it is highlighted to the user and the frame remains in the upload window. For example, if the user enters three frames and the first two are valid but the third is invalid, the first two are uploaded and the third remains in the edit window. However, if an error occurs in the first frame, all three frames remain in the upload window.
- **Send frames**. Starts sending frames to the Ethernet MAC.
- **Stop**. Stops transmission of frames to the Ethernet MAC.
- **Set repeat**. Requests continuous transmission of frames by continuously looping through all the frames in the RAM.
- **Set halt**. Requests that frames in the RAM are sent only once.
- **Clear RAM**. Clears the RAM.

PHY Registers Tab

The PHY Registers tab (Figure 13) displays the information gathered by the Ethernet MAC core about the 1000BASE-X PCS/PMA registers used for 1000BASE-X connectivity to the SFP device using the MDIO. This tab is not used for the Marvell BASE-T PHY's registers.

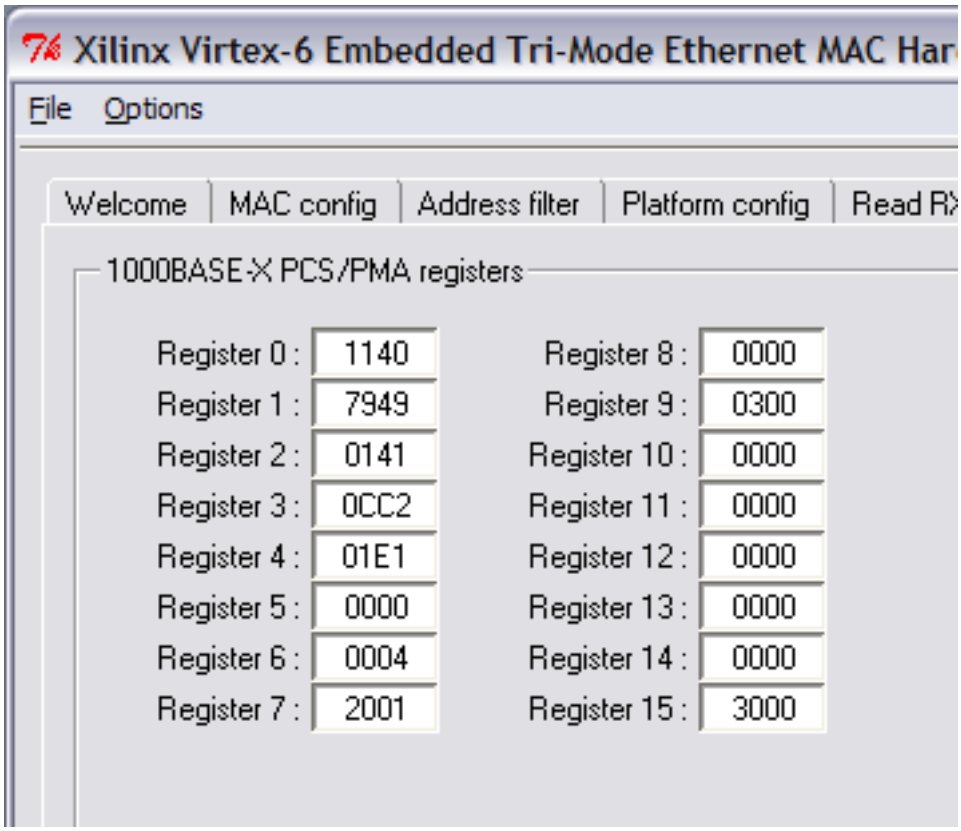

Figure 13: **PHY Registers Tab**

MAC Statistics

Statistics counter values (Figure 14) are displayed by choosing **Options** > **Show TEMAC Stats**, and can be reset to 0 by choosing **Options** > **Clear stats** counters.

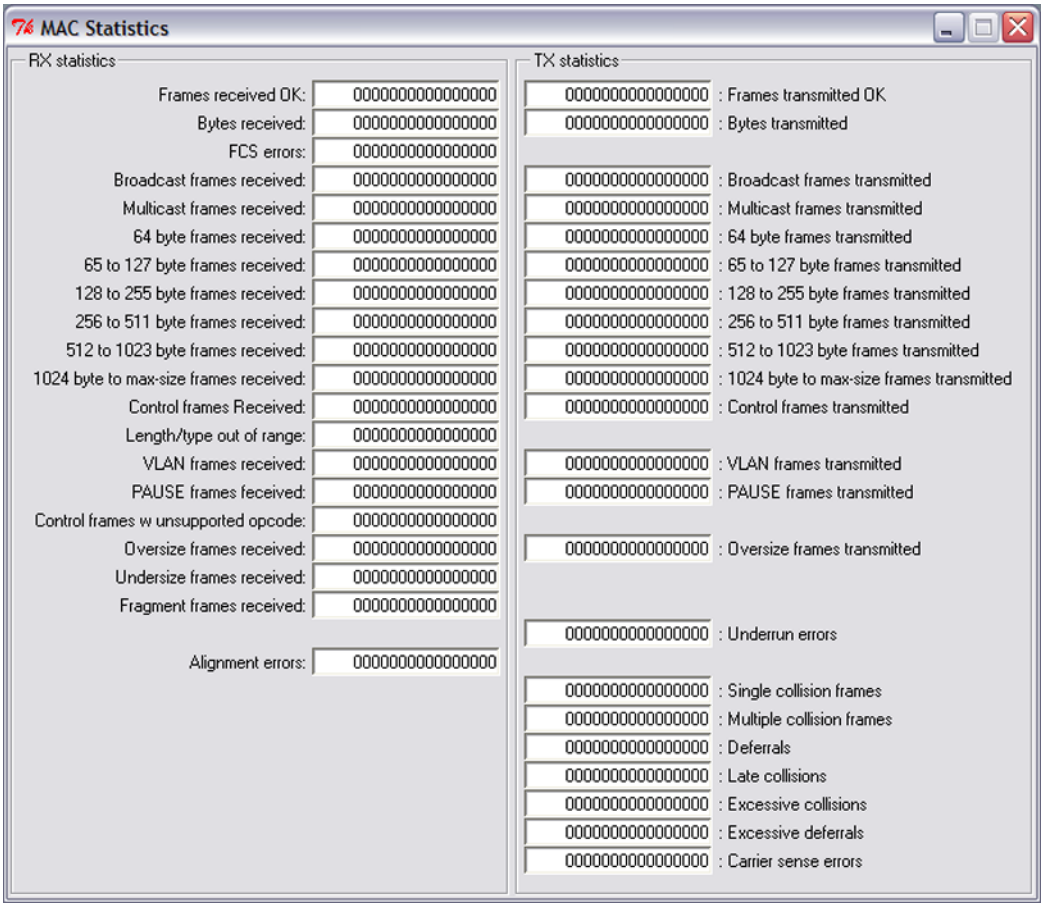

Figure 14: **Statistics Window**

Building the Hardware

Ready-to-use bitfiles are provided. Only use the information in this section if changes to the design are necessary.

The design consists of two XPS projects containing the components used in the design. The designs are identical except for their physical interface to the BASE-T PHY; `system.xmp` uses the GMII/MII physical interface, `system_rgmii.xmp` uses the RGMII physical interface, and `system_sgmii.xmp` uses the SGMII physical interface. HDL source code and support files are provided for each component (pcore) unique to the design. Standard XPS peripherals are provided by XPS when it is installed; these are not included with the design source.

Source Code Directory Structure

The main components of the hardware design include:

- An XPS top-level project containing the MicroBlaze processor peripherals and software
- Multiple RTL- and NGC-based pcores containing the Ethernet MAC Wrapper core and board-specific logic

The following illustrates the organization of the source code directories.

- **<top level>**
  Top-level folder created when .zip file is unzipped. Contains XPS project files and bitfiles.
  - code
    Source code and header files are here for the embedded processor. The GUI application is in pc/rtf sub-directory.
  - docs
    Contains the file for this application note, `xapp1144.pdf`.
  - etc
    Commands used by XPS to create the bitfile and download it to the ML605.
  - data
    Top-level constraints file used by the tools when run from within XPS.
  - pcores
    Peripherals used in the design.
  - driver
    Driver source files used by XPS when building the MicroBlaze processor application.
  - coregen
    Ethernet MAC Wrapper core and supporting files used by XPS.

Building All Demonstration Platforms

CORE Generator IP

The Ethernet MAC wrapper and Ethernet Statistics cores are created using the CORE Generator tool in the coregen directory. The CORE Generator software output for both cores is included with the application note source .zip file. A CORE Generator project file and parameter files are also included in the coregen directory. If either of the cores is regenerated, the same names must be used and the cores generated in the coregen directory, because the XPS build process copies the source and NGC files from the coregen directory each time the design is built from scratch. Note that a free license for the Ethernet Statistics core will need to be generated.

XPS Project

To build the bitfile containing both hardware and MicroBlaze processor software, using EDK version 11.3, do the following:

1. Using XPS, open `system.xmp` (GMII/MII connectivity to BASE-T PHY), `system_rgmii.xmp` (RGMII connectivity to BASE-T PHY), or `system_sgmii.xmp` (SGMII connectivity to BASE-T PHY).
2. Choose Project > Clean all Generated Files to remove any old files.
3. From the Device Configuration menu, select Update Bitstream to build both the hardware and software.

For detailed information about the build process, see the EDK documentation, located at www.xilinx.com/ise/embedded/edk_docs.htm.

Configuration

XPS can be used to download the bitfile directly using a suitable JTAG cable. From the Device Configuration menu, choose Download Bitstream. Other Xilinx tools may alternatively be used, such as iMPACT or ChipScope™ Pro.

References

1. UG170, *LogiCORE IP Ethernet Statistics User Guide*.
2. UG368, *Virtex-6 FPGA Embedded Tri-Mode Ethernet MAC User Guide*.
3. UG534, *ML605 Hardware User Guide*.
4. UG545, *Virtex-6 FPGA Embedded Tri-Mode Ethernet MAC Wrapper Getting Started Guide*.

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
10/15/2009	1.0	Initial Xilinx release.
11/23/2009	1.1	Added support for SGMII connectivity.

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