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Spartan FPGAs – The Gate Array Solution

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Summary

This application note discusses the enormous strides made by Spartan™ series FPGAs in terms of density and performance and how it should be viewed as the Gate Array replacement. The Spartan family from Xilinx offers many of the features that are desired by Gate Array designers with one major advantage — programmability, which can prove to be the key factor in the success of the product.

Introduction

Gate Array designers have a set of performance requirements that traditionally used to be beyond the capabilities of FPGAs. But with the advent of the Internet age and an evolving market that constantly changes to accommodate new standards, it is important that the designers react quickly to capitalize on a new product. Gate Array design methodology does not lend itself well to rapid prototyping and getting to production fast. On the other hand, in the past FPGAs did not have the performance and density to provide a solution to these designers. With the advance in process technology and a simpler design flow, FPGAs have reached performance levels that rival Gate Arrays in price and time-to-market. When **programmability,** the basic feature of an FPGA, is factored in with its advantages, FPGAs are more cost effective than Gate Arrays.

Programmability – A New Requirement for Gate Arrays

Spartan FPGAs have now started to match Gate Arrays in density, performance and price. With a tool flow that is somewhat similar, Gate Array designers are now able to use the basic features of FPGAs to react to a small market window. **Programmability** in Spartan FPGAs now enables Gate Array designers to get their products completed faster hence dramatically reducing the overall time-to-market. Other advantages of a programmable solution include less development cost – no NRE and no costly respins and the ability to support field upgrades and remote download that will extend the longevity of the product in the market (time-in-market). Because programmability opens up new possibilities, gate array designers are becoming more and more interested in this technology and are willing to consider FPGAs as a viable replacement. Figure 1 depicts the time-to-market savings by using FPGAs.

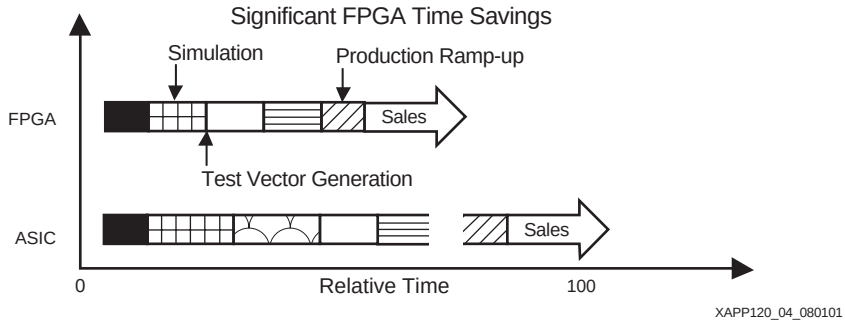

Figure 1: **Savings in Time-to-Market — FPGAs vs. Gate Arrays**

Spartan Series Closes the Price/ Performance Gap Between FPGAs and Gate Arrays

The Spartan family (Spartan-XL and Spartan-II) is the lowest cost FPGA series solution in the industry. The logic gate count ranges from 15K-200K with I/O ranges between 86 to 284, with a wide variety of popular packages. The family incorporates ASIC-like features with embedded memory (distributed and dual port, synchronous block RAM) with support of system frequencies up to 200 MHz. The Spartan-II series is made from an advanced process technology (0.22µ down to 0.18µ), with a system gate count that reaches up to 200K and 284 I/Os. With competitive volume pricing, the family attains a price performance level that is comparable to Gate Arrays. Figure 2 compares the process technologies of Gate Arrays with that of FPGAs. FPGAs will continue to use leading edge process technologies with higher gate count that support multiple V_{CC} and I/O standards.

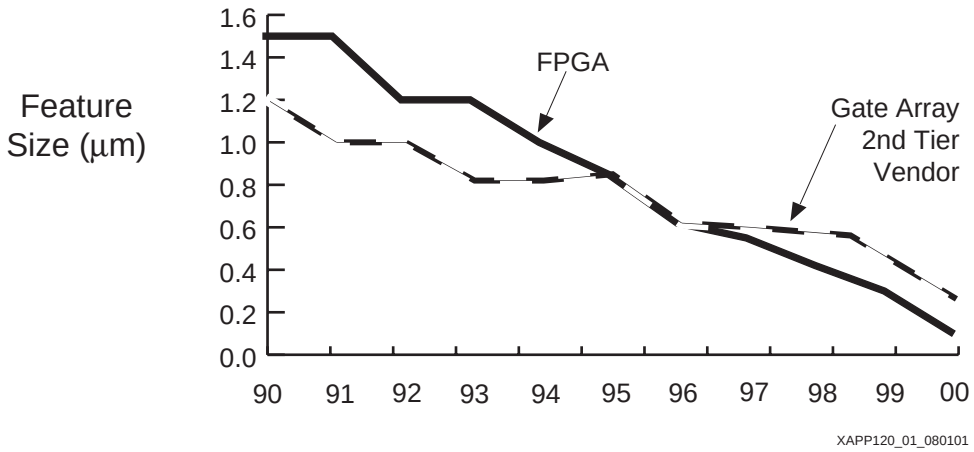

Figure 2: **FPGA vs Gate Array Technology**

Gate Array – A Diminishing Market

Mask gate arrays incur a large penalty when migrating to deep submicron processes. Because transistors have shrunk much faster than metal lines, smaller transistors drive larger and longer metal lines. The result is that interconnect delay now dominates gate delay. (See Figure 3) Minimizing interconnect delay requires adding metal mask layers to create more routing resources.

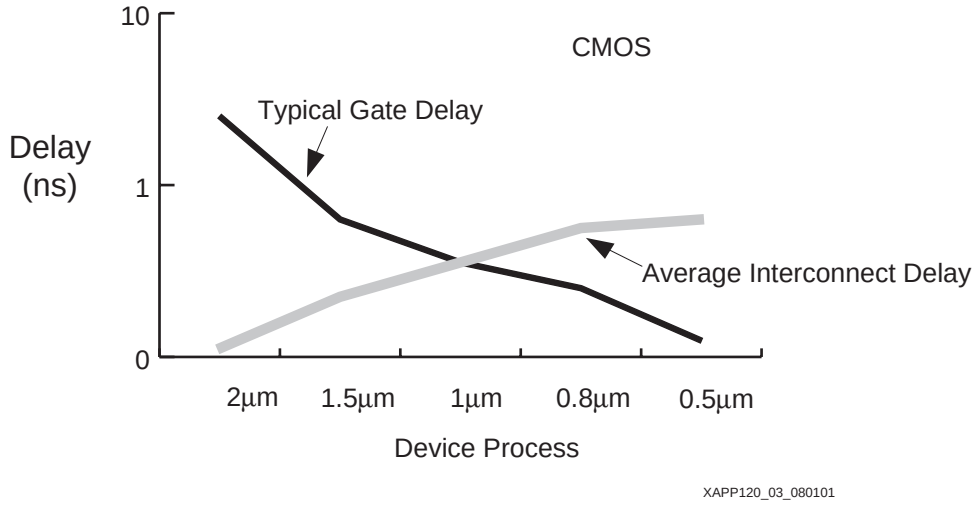

Figure 3: **Importance of Interconnect vs Gate Delay**

As an example, each additional mask layer for the 0.35µ process costs the Gate Array supplier up to $15K, in addition to extending the prototype time in the fab. Since most Gate Array technology today is fabricated with 4-5 metal layers, a $60-75K cost for mask sets easily results in over $100K of non-recurring engineering (NRE) charges to the customer! In contrast, the FPGAs designed with the 0.22µ process do not incur the same penalties of higher cost and longer turnaround time since each mask set is created just once to serve hundreds of different customers over the lifetime of the product. A deep submicron Gate Array loses much of its value when NREs are more than $100K and the prototype phase is extended by a few extra weeks. As process technology decreases consequently raising wafer and mask costs, the Gate Array industry is undergoing a fundamental transition.

Major suppliers, like Motorola, IBM and LSI Logic, have decided not to engage in further gate array business due to capital investments that yield low returns and instead to re-focus on high-end standard cell products that have higher returns due to larger NRE and volumes. According to Dataquest, the Gate Array market will continue to decline over the next four years, with FPGAs and Standard Cells gaining the market share from Gate Arrays (shown in Table 1).

Table 1: **Growth in Estimated Worldwide ASIC Consumption by Product (Percentage Growth)**

	1998	1999	2000	2001	2002	2003	2004	CAGR (%) 1999 to 2004
Total ASIC	**–5.8**	**14.4**	**36.3**	**26.7**	**19.0**	**6.7**	**16.0**	**20.5**
Gate Array	–25.8	–22.0	1.4	–9.6	–13.7	–15.9	–15.5	–10.9
PLD	–1.1	23.1	54.5	37.3	18.2	8.4	15.9	27.6
Cell Based IC	4.6	27.3	39.1	10.8	23.3	8.3	17.9	23.4

Notes:
1. Columns may not add to totals shown because of rounding

Source: Gartner Dataquest (October 2000)

Another reason for the shrinking Gate Array market is the lack of system integration and IP support that has now become available with FPGAs and Standard Cells. The Gate Array market is currently populated with second tier suppliers whose major focus is not Gate Arrays (which implies that Gate Arrays take on the role of "fab fillers" during market downturns) and who cannot make the investment or commitment to Gate Array customers to provide the most cost effective solutions that yield better performance and features.

Spartan Series Advantages Over Gate Arrays

Because today's product life cycles are so brief (12-18 months), it is vital to attain the best development-to-production cycle time. Programmable logic provides both rapid prototyping and a quick ramp to full production. With in-system (re)programmability, FPGAs demonstrate the fastest development time of any ASIC technology. Early availability of prototype hardware means less time spent in extensive simulation. Rapid prototyping also facilitates concurrent engineering and real-time debugging of applications such as video, graphics, and sound cards. Prototyping with FPGAs enables bugs to be eliminated before they reach costly silicon. And since Xilinx FPGAs are 100% factory tested, the usual scan insertion, test vector generation and Automatic Test Pattern Generation (ATPG) services are optional for lower density FPGAs. (Xilinx recommends test vectors, however, for the higher density FPGAs.)

Table 2: **Xilinx Spartan-II FPGAs**

Device	Logic Cells	System Gates (Logic and RAM)	CLB Array (C x R)	Total CLBs	Maximum Available User I/O	Total Distributed RAM Bits	Total Block RAM Bits
XC2S15	432	15,000	8 x 12	96	86	6,144	16K
XC2S30	972	30,000	12 x 18	216	132	13,824	24K
XC2S50	1,728	50,000	16 x 24	384	176	24,576	32K
XC2S100	2,700	100,000	20 x 30	600	196	38,400	40K
XC2S150	3,888	150,000	24 x 36	864	260	55,296	48K
XC2S200	5,292	200,000	28 x 42	1,176	284	75,264	56K

Embedded Memory, IP Support, Multiple I/O Standard Support

The Spartan Series has always had distributed RAM which efficiently implements small FIFOs, scratch pads, and storage locations of constants for high performance math intensive applications. Spartan-II devices add Block RAM with True Dual-Port capability which is excellent for implementing large FIFOs, packet buffering, cache tag memory, video line buffering or most memory needs. By using the SelectI/O™ interface, Spartan FPGAs offer an excellent interface to high-speed external memories thus eliminating the need for special interfaces. Gate Array applications in the past that have been forced to seek additional external memory support or migrate to Standard Cell technology because of limitations in the technology that does not support memory blocks, now have a more ideal solution with Spartan FPGAs.

The Spartan family also supports an extensive list of IP cores (available from Xilinx and its IP partners) that make integration and system-on-a-chip a reality for Gate Array customers. Cores that are in everyday use and cores specific to certain market segments such as communications are part of this offering. This helps the designer in the design and prototype phase by removing any uncertainty that may exist at the design phase.

Spartan FPGAs also support a wide variety of I/O standards that could be useful in interfacing with different logic standards and to work efficiently under a range of circumstances, thus ensuring the integrity of the signal and being able to meet required system speeds.

Gate Array vs FPGAs - A Methodology Update

Gate Array designers, over a long period of time, have become used to a certain flow that has become ingrained in their daily design process and to learn or migrate to a different flow becomes almost an emotional issue. In the past, the FPGA design flow, though simpler, did not require as many steps in the design process. Consequently, it was viewed as being inadequate in yielding ASIC like results in spite of the advanced process technology that was being used to manufacture the FPGAs. In the last several years, Xilinx had undertaken a monumental effort in making the tools more ASIC-like so that the software can yield performance results and meet Gate Array performance.

With the advent of hardware languages such as VHDL and Verilog, Xilinx has released sets of tools that can be used to make generic code FPGA friendly, so that it can be optimized for the Xilinx architecture. Also available are verification (functional and timing) tools that can be used to ensure operation of the product to a design specification. Other tools such as to accommodate incremental design changes and to probe specific points in the FPGA to ensure timing specifications and obtain timing closures using physical synthesis are also available. This plethora of tools ensures timing and performance closure. The availability of these tools make it easier for the designer to move from one tool environment to another especially when the tools are easy to use and have the same look and feel as the ASIC tools.

Shortening Your Time-to-Market

Time-to-Market (TTM) and Time-in-Market (TIM) are two very important concepts in today's ever changing design landscape. Ideas are generated in a "New York minute" and to engage the interest (and hence the market) of the consumer is the challenge that can make a product a success. With the consumer being constantly presented with new and better products, and new standards and specifications being generated to support new 'ideas', the product supplier needs to be always on their toes to adapt to the ever changing needs of the consumer. Designing your application with a programmable product is the only way to get ahead and to be able to react quickly before the consumer's attention shifts. And having a programmable product not only helps in getting to market faster (TTM), it also helps in being in business longer (TIM) by adding new features or adapting to a different standard. This can only be possible due to the programmable nature of the ASIC solution – FPGAs, used in the application.

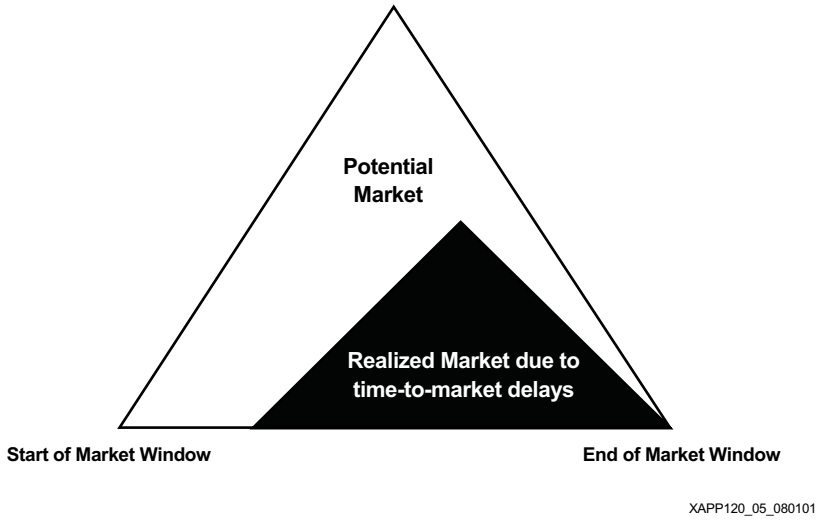

Figure 4: **Time-to-Market Diagram**

Supply Chain Management

Another often overlooked advantage of FPGAs is the fact that they are standard products found in distribution inventory. Gate Arrays are not standard products but semi-custom and in nature and hence associated with all the issues of such products like long lead times, liability due to market fluctuations and expensive overruns. Another factor could be the Gate Array distribution stocking arrangements that can end up being expensive. In addition Gate Array factory deliveries can sometimes be affected by fab yields, assembly mishaps, and tester down time, which all affect the supply of the product. On the other hand FPGAs eliminate the risk of missed deliveries and safeguard inventory and work-in-process if design changes occur or the market demand is weak.

FPGA to Gate Array Conversions – An Expensive Undertaking

It is becoming increasingly difficult today to justify the cost of FPGA to Gate Array conversions because of the lower unit cost of FPGAs and quickly changing markets. Conversion to a Gate Array means losing FPGA advantages and incurring design risks. Added costs such as NREs, conversion fees, silicon iterations, test vector creation for adequate fault coverage, board re-layout, new device characterization, and design re-spins negate a slight unit cost difference between the two technologies. FPGA to Gate Array conversion time to production typically exceeds four months.

A typical conversion time frame is as follows: design conversion — three weeks, prototype - three weeks, full production - ten weeks. A total of 16 weeks is needed before production is ramped and the transition from FPGA to Gate Array may begin. With either a short product life or a required mid-life product enhancement, many conversions may not be cost justified. In addition, FPGA users have no minimum order quantity. Cash and credit availability is preserved

when there are no large gate array order commitments and the IC stock levels are minimal. Small and emerging companies will appreciate conserving their credit availability and valuable working capital for product development, test and marketing.

There are compelling advantages in using programmable logic in development and production. Spartan FPGAs support standard Verilog and VHDL design flows that help in the transition of Gate Array designs to programmable logic. Advanced process technology has leveled the playing field, and programmability has changed the field in favor of FPGAs. Now Gate Array designers are starting to accept the fact that in today's Internet age, their solution has to include FPGAs.

Refer to the Xilinx website (**www.xilinx.com**) for the latest product information.

Additional Information

Spartan Series datasheet on the Xilinx website:

(**http://www.xilinx.com/partinfo/databook.htm**)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/01/98	1.1	Updated.
08/01/01	2.0	Expanded and updated for Spartan-II Family.