Summary

UltraScale™ and UltraScale+™ FPGAs feature a built-in primitive named MASTER_JTAG that provides the same functionality as the external JTAG port. The internal FPGA logic can use MASTER_JTAG to load the AES decryption key into the battery-backed RAM (BBRAM). It can also use the MASTER_JTAG primitive to program various one-time programmable (OTP) eFUSEs from within the device, instead of using the external JTAG port. This application note abstracts the low-level commands needed to communicate with the MASTER_JTAG primitive by providing the necessary Xilinx® supplied HDL and C library functions for a MicroBlaze™-based Soft Processor Core [Ref 1] design. These designs can be modified and enhanced for various use cases.

You can download the reference design files for this application note from the Xilinx website. For detailed information about the design files, see Reference Design.

Introduction

Xilinx devices have featured both BBRAM and eFUSE non-volatile (NVM) memory since Virtex®-6 FPGAs. The primary use of a BBRAM in UltraScale and UltraScale+ devices is to store the 256-bit AES bitstream decryption key. This AES key can also be stored in the eFUSEs with the important difference that it can neither be modified nor erased. A 32-bit FUSE_USER register that can be programmed for custom use cases is also available.

UltraScale and UltraScale+ FPGAs have introduced an additional programmable 128-bit register, FUSE_USER_128, for use as a maintenance log, a tamper activity log, or for a custom use case. A 384-bit eFUSE register that can be programmed with the hash of a RSA-2048 public key as a part of the device's authentication scheme is also available. The eFUSE-based control bits including read/write disables, decryption disable, external JTAG disable, and RSA enable can also be programmed. Refer to the UltraScale Architecture Configuration User Guide (UG570) [Ref 2] and Vivado Design Suite User Guide: Programming and Debugging (UG908) [Ref 3] for more information.

Traditionally, BBRAM and eFUSEs are programmed through the external JTAG port using the Xilinx ISE iMPACT or Vivado® Hardware Manager. Starting with UltraScale and UltraScale+ FPGAs, BBRAM and eFUSEs can also be programmed using the internal MASTER_JTAG port.

The ability to program using an internal path has a number of advantages, especially in security applications. For instance, it is possible to perform a field update of the BBRAM key remotely and securely by instantiating a secure key exchange function in the FPGA logic. The new key can travel safely over an unsecured network because it is encrypted (black), decrypted in the FPGA logic.
logic (red), and then stored in the BBRAM from within the device. Other security use cases are internal programming of eFUSEs such as tamper log information, AES decryptor disable, and JTAG disable as responses to a tamper event. Refer to the Developing Tamper-Resistant Designs with UltraScale and UltraScale+ FPGAs Application Note (XAPP1098) [Ref 7].

A MicroBlaze Soft Processor Core [Ref 1] is instantiated in the FPGA logic to interface with the internal MASTER_JTAG port. The Xilinx-supplied XILSKEY library provides an application programming interface (API) to simplify and abstract the necessary low-level JTAG commands. The hardware and software development required to use the XILSKEY library is outlined in Hardware and Software Development Overview. Refer to the LibXil SKey for Zynq-7000 UltraScale and Zynq UltraScale+ MPSoC AP SoC Devices User Guide [Ref 8] for more information about the XILSKEY library.

Following the design flow described in this application note, one Vivado hardware project, and three different SDK applications are created. These SDK applications perform the following tasks:

• Internally program the BBRAM AES key.
• Create a Hello World design with an encrypted bitstream to verify the BBRAM key.
• Internally program eFUSE bits. The internal eFUSE programming is verified by the SDK application as well as by the Vivado Hardware Manager.

This application note assumes that you are familiar with the Vivado tools flow methodology (including IP Integrator—IPi), and are experienced with building simple SDK projects. See Vivado Design Suite User Guide: Programming and Debugging (UG908) [Ref 3], Vivado Design Suite User Guide: Design Flows Overview (UG892) [Ref 4], Vivado Design Suite User Guide: Using the Vivado IDE (UG893) [Ref 5], and Vivado Design Suite User Guide: Designing IP Subsystems Using IP Integrator (UG994) [Ref 6] for more information.

Hardware and Software Requirements

The hardware and software requirements for the internal programming of BBRAM and eFUSEs memory are as follows.

For UltraScale FPGAs:

• KCU105 Kintex® UltraScale FPGA evaluation kit [Ref 9] based on the XCKU040-2FFVA1156E FPGA
• AC to DC power adapter (12 VDC)
• USB type-A to micro-B USB cable for JTAG
• USB type-A to micro-B USB cable for UART
• Xilinx Vivado design suite version 2016.3 or later [Ref 10]
• Xilinx Software Development Kit (XSDK) version 2016.3 or later [Ref 11]
• Serial communications terminal application such as Tera Term [Ref 12]
Hardware and Software Development Overview

For UltraScale+ FPGAs:

- KCU116 Kintex UltraScale+ FPGA evaluation kit [Ref 13] based on the XCKU5P-2FFVB676E FPGA
- AC to DC power adapter (12 VDC)
- USB type-A to micro-B USB cable for JTAG
- USB type-A to micro-B USB cable for UART
- Xilinx Vivado design suite version 2017.3 or later [Ref 10]
- Xilinx Software Development Kit (XSDK) version 2017.3 or later [Ref 11]
- Serial communications terminal application such as Tera Term [Ref 12]

IMPORTANT: The BBRAM key cannot be used if the EFUSE_KEY_ONLY control eFUSE is already programmed on the KCU105 or KCU116 evaluation board’s FPGA. Refer to the UltraScale Architecture Configuration User Guide (UG570) [Ref 2] for more information.

Special Considerations When Using MASTER_JTAG to Internally Program eFUSEs

Certain special considerations must be taken to ensure reliability when MASTER_JTAG is used to internally program eFUSEs.

1. The configuration memory must not be accessed during internal programming. This includes activities such as a single-event upset (SEU) scan, readback capture, and partial reconfiguration (PR). For example, the Xilinx Soft Error Mitigation (SEM) IP core [Ref 14] should not be operational during eFUSE programming.

2. The board/system design must take into consideration the additional current required for programming eFUSEs. The programming current is available in the appropriate UltraScale device data sheets [Ref 15].

Hardware and Software Development Overview

This application note outlines the steps to create a MicroBlaze processor-based Vivado tools design that indirectly interfaces the MASTER_JTAG primitive using the general purpose I/O (GPIO). A Vivado hardware project is created and exported to the SDK. The SDK tool is launched with the MicroBlaze processor-based Vivado tools design as its hardware platform. Three different software applications based on the available software libraries and example code are then created. After these SDK applications are compiled and built into executable and linkable format (ELF) files, they are brought back into the Vivado tools. Three separate FPGA bitstreams are then generated to perform and verify the functions described in this application note.
In addition to the MicroBlaze processor, two VHDL files are included in this project (see Reference Design for more information):

- `int_prog_ctl_us.vhd`
- `jtag_monitor.vhd`

**INT_PROG_CTL_US Module**

Most of the time, the JTAG signaling can come directly from the MicroBlaze processor’s GPIO interface. However, to provide precise control over the duration of the actual eFUSE programming pulse, the INT_PROG_CTL_US module is required. This module instantiates the MASTER_JTAG primitive.

The INT_PROG_CTL_US module passes the MicroBlaze processor’s GPIO signals directly to and from the MASTER_JTAG primitive, except when it enters the actual eFUSE programming phase. Upon entering this phase, the XILSKEY software polls for the INT_PROG_CTL_US module using a READY signal. After the software detects that the module is READY, it asserts the START_PROG input to command the module to take control of the JTAG signaling (TCK and TMS) to get a precise 5 µs programming pulse. When the eFUSE programming is complete, the INT_PROG_CTL_US module asserts the END_PROG signal and allows the software to regain control of the JTAG signals. This interface is illustrated in Figure 1.

If you want to internally program just the BBRAM and not the eFUSE, then you can ignore this module. Xilinx recommends including this module because it consumes few resources and allows future internal eFUSE programming. However, if you decide to ignore it, then you must instantiate the MASTER_JTAG primitive and connect it directly to the MicroBlaze processor’s GPIO.

If your design is also instantiating the Xilinx Security Monitor IP Core (see the Security Monitor IP Core Product Brief [Ref 16]), the INT_PROG_CTL_US module must be modified, because the Security Monitor instantiates the MASTER_JTAG primitive. The MASTER_JTAG primitive must be removed from the INT_PROG_CTL_US module and the corresponding JTAG signals brought up to the module’s port list to connect to the Security Monitor’s MASTER_JTAG interface.
**JTAG_MONITOR Module**

The optional JTAG_MONITOR module provides an EFUSE_PROG_PULSE output that can be routed up to an external header pin on the KCU105 board or KCU116 board to measure the eFUSE programming pulse width (this signal mirrors the amount of time the JTAG controller is in the programming phase).

The JTAG_MONITOR can also be used to debug/monitor the JTAG signals and display the current JTAG state. When using the Vivado Integrated Logic Analyzer (ILA) IP core to monitor the JTAG states, the INT_PROG_CTL_US module must have its TEST_MODE generic set to true (MASTER_JTAG is not instantiated) to allow the ILA to communicate using external JTAG. Otherwise, the ILA does not work, because external JTAG is disconnected when MASTER_JTAG is instantiated within a design.

The JTAG_MONITOR module is useful for development and debugging. It is optional and can be removed in a field deployed system.

**Building the Vivado Hardware Project**

One common Vivado project is the hardware required for this application note. It is based upon a MicroBlaze soft processor using GPIO to indirectly interface with the MASTER_JTAG primitive through the INT_PROG_CTL_US Module. The following steps are used to create the Vivado hardware project.

*Note:* Depending on the Vivado tools version used, some of the figures can vary slightly from the actual tool.

1. Open the Vivado tools (version 2016.3 or later for UltraScale FPGAs and version 2017.3 or later for UltraScale+ FPGAs) in graphical user interface (GUI) mode.
2. From the welcome screen under Quick Start select **Open Example Project** (Figure 2).
3. Click **Next**, select **Base MicroBlaze**, and click **Next** (Figure 3).

![Project Template Base MicroBlaze](image)

**Figure 3:** Project Template Base MicroBlaze

4. Enter the project name: **internal_prog_proj**.

5. Enter the appropriate project location and (optionally) keep the create project subdirectory checkbox selected.

   **Note:** The maximum allowed path length on Windows is 260 bytes.
6. Click **Next**, select **Kintex-UltraScale KCU105 Evaluation Platform** or **Kintex UltraScale+ KCU116 Evaluation Platform**, and click **Next** (Figure 4).

**Figure 4: Project Evaluation Platform**
7. Click **Finish**. The Vivado tools create the base MicroBlaze processor project (Figure 5 and Figure 6).

---

**Figure 5: Project Summary**

*New Project Summary*

- A new project named 'internalProg_prog' will be created from the 'Base MicroBlaze' template.
- The default part and product family for the new project:
  - Default Board: Kintex UltraScale KCU105 Evaluation Platform
  - Default Part: xcuv1000-kcu1156-2-e
  - Product: Kintex UltraScale
  - Family: Kintex UltraScale
  - Package: tlv1156
  - Speed Grade: -2
- A new block design will be created based on the 'Base MicroBlaze' IP Integrator template.

To create the project, click Finish

---

**Figure 6: Example MicroBlaze Design in IP Integrator**

Simple MicroBlaze Design

For instructions look at the MicroBlaze_example_design_readme.pdf file in...

To Export this Design to SDK:
1. Click on the Generate Bitstream in Flow Navigator
2. Select File => Export => Export Hardware

---

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www.xilinx.com
8. Double-click the Clocking Wizard IP block, select the Output Clocks tab, verify clk_out1 is selected, and the requested and actual frequency is 100 MHz. Click OK. This is the main clock for the MicroBlaze core.

9. Under the Output Clock column, check the box next to clk_out2 and type in 8.000. Verify that the actual column reports back 8.000 MHz. This is the clock used by the INT_PROG_CTL_US Module to provide precise time during the actual programming of the eFUSEs. Click OK (Figure 7).

---

**IMPORTANT:** For eFUSE programming, the 8.000 MHz clock feeds into the INT_PROG_CTL_US block. This is critical for generating the required programming pulses. The JTAG TAP machine must transition using an accurate clock during this phase to provide a 5 µs pulse for each eFUSE programmed. If the programming pulses are not accurate, eFUSE programming and reliability can be adversely affected.
10. Right-click on the clk_out2 port of the Clocking Wizard IP block, select Create Port, set Port Name to CLK_8MHZ, and click OK (Figure 8).

![Create Port](image)

**Figure 8: Create Port**

11. From within the IPI block diagram window search and add the following IP blocks by selecting the Add IP icon on the left (or top) side of the IPI window.

   a. **System Management Wizard** (used to monitor on-chip temperature and voltage prior to reading and writing eFUSEs).

   b. **AXI Timer** (used as a watchdog in the eFUSE programming code section).

12. Towards the top of the IPI window, next to where it says Designer Assistance available, click **Run Connection Automation**.
13. Select the **All Automation** checkbox to select all the checkboxes and click **OK** to automatically connect up the recently added IP blocks *(Figure 9).*

![Run Connection Automation](image)

*Figure 9: Run Connection Automation*

14. Right-click on the **External Interface: led_8bits** connected to the AXI GPIO IP block and click **Delete.**

15. Double-click the **AXI GPIO** IP block to re-customize the IP.
16. Using the drop-down boxes, ensure that both the IP Interfaces GPIO and GPIO2 are set to **Custom Board Interface** (Figure 10).

**Figure 10:** Re-customize IP Interfaces
17. Select the **IP Configuration** tab, check the **All Outputs** checkbox for GPIO, set **GPIO Width** to 4, check the **Enable Dual Channel** checkbox, check the **All Inputs** checkbox for GPIO 2, set **GPIO Width** to 3, and click **OK** (Figure 11).

**Figure 11:** Re-customize IP GPIO Width
18. Right-click on the GPIO port of the AXI GPIO IP block, select **Create Interface Port**, set the **Interface Name** to **GPO**, and click **OK** (Figure 12).

![Create Interface Port (GPIO)](image)

**Figure 12:** Create Interface Port (GPIO)

19. Right-click on the GPIO2 port of the AXI GPIO IP block, select **Create Interface Port**, set the **Interface Name** to **GPI**, and click **OK** (Figure 13).

![Create Interface Port (GPIO2)](image)

**Figure 13:** Create Interface Port (GPIO2)

20. Right-click on the Vp_Vn port of the **System Management Wizard** IP block and select **Make External**.
21. Select the **Address Editor** tab at the top of the IPI window, set the **Range** for `microblaze_0_local_memory/dlmd_bram_if_cntlr` to 256K using the drop-down box, and set the **Range** for `microblaze_0_local_memory/ilmd_bram_if_cntlr` to 256K using the drop-down box (Figure 14).

![Figure 14: Address Editor](X18328-011117)

22. Select the **Diagram** tab at the top of the IPI window to return to the block diagram.

23. Click the **Validate Design** icon on the left (or top) side of the IPI window and correct any issues if the validation does not pass.

24. The large text labels on the block diagram can be moved and/or renamed.

25. Click the **Regenerate Layout** icon on the left (or top) side of the IPI window to clean up the block diagram display. It should look similar to Figure 15. After the edits are complete, save the block diagram.

![Figure 15: MicroBlaze-based Internal BBRAM/eFUSE Programming Project Layout](X18327-011117)

26. From the top-level Vivado tools menu, select **Tools > Project Settings** or **Settings > Target Language VHDL > OK**.
27. In the center window, select the **Sources** tab, select the **Hierarchy** tab, right-click on `base_mb_i`, select **Create HDL Wrapper**, choose **Copy generated wrapper to allow user edits**, and click **OK** (Figure 16 and Figure 17).

**Figure 16:** Sources

**Figure 17:** Create HDL Wrapper
28. In the center window, under Design Sources, double-click **base_mb_wrapper** to bring up the HDL file in the text editor and make the following changes:

   a. Remove the GPIO ports from the top-level port list and assign as internal signals.

   b. Instantiate and connect the **INT_PROG_CTL_US** component (this block instantiates the **MASTER_JTAG** primitive). See the **INT_PROG_CTL_US Module** for more information.

   c. Instantiate and connect the **JTAG_MONITOR** component (optional). See the **JTAG_MONITOR Module** for more information.

29. The following VHDL code sample demonstrates these changes (the VHDL wrapper file can also be downloaded from Xilinx.com). See Reference Design for more information.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
library UNISIM;
use UNISIM.VCOMPONENTS.ALL;

entity base_mb_wrapper is
  port (  
    Vp_Vn_v_n            : in  std_logic;
    Vp_Vn_v_p            : in  std_logic;
    default_sysclk_300_clk_n : in  std_logic;
    default_sysclk_300_clk_p : in  std_logic;
    reset                : in  std_logic;
    rs232_uart_rxd       : in  std_logic;
    rs232_uart_txd       : out std_logic;
    EFUSE_PROG_PULSE     : out std_logic  
  );
end base_mb_wrapper;

architecture STRUCTURE of base_mb_wrapper is
  signal clk_8mhz  : std_logic;
  signal gpi_tri_i : std_logic_vector(2 downto 0);
  signal gpo_tri_o : std_logic_vector(3 downto 0);
  signal jtag_mon  : std_logic_vector(3 downto 0);

  component base_mb is
    port (  
      default_sysclk_300_clk_n : in  std_logic;
      default_sysclk_300_clk_p : in  std_logic;
      rs232_uart_rxd       : in  std_logic;
      rs232_uart_txd       : out std_logic;
      Vp_Vn_v_n            : in  std_logic;
      Vp_Vn_v_p            : in  std_logic;
      reset                : in  std_logic;
      CLK_8MHZ             : out std_logic;
      GPI_tri_i            : in  std_logic_vector(2 downto 0);
      GPO_tri_o            : out std_logic_vector(3 downto 0)
    );
  end component base_mb;

  component INT_PROG_CTL_US is
    generic (  
      TEST_MODE : boolean := FALSE
    );
    port (  
      RESET : in  std_logic  
    );
  end component INT_PROG_CTL_US;
```

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
library UNISIM;
use UNISIM.VCOMPONENTS.ALL;

entity base_mb_wrapper is
  port (  
    Vp_Vn_v_n            : in  std_logic;
    Vp_Vn_v_p            : in  std_logic;
    default_sysclk_300_clk_n : in  std_logic;
    default_sysclk_300_clk_p : in  std_logic;
    reset                : in  std_logic;
    rs232_uart_rxd       : in  std_logic;
    rs232_uart_txd       : out std_logic;
    EFUSE_PROG_PULSE     : out std_logic  
  );
end base_mb_wrapper;

architecture STRUCTURE of base_mb_wrapper is
  signal clk_8mhz  : std_logic;
  signal gpi_tri_i : std_logic_vector(2 downto 0);
  signal gpo_tri_o : std_logic_vector(3 downto 0);
  signal jtag_mon  : std_logic_vector(3 downto 0);

  component base_mb is
    port (  
      default_sysclk_300_clk_n : in  std_logic;
      default_sysclk_300_clk_p : in  std_logic;
      rs232_uart_rxd       : in  std_logic;
      rs232_uart_txd       : out std_logic;
      Vp_Vn_v_n            : in  std_logic;
      Vp_Vn_v_p            : in  std_logic;
      reset                : in  std_logic;
      CLK_8MHZ             : out std_logic;
      GPI_tri_i            : in  std_logic_vector(2 downto 0);
      GPO_tri_o            : out std_logic_vector(3 downto 0)
    );
  end component base_mb;

  component INT_PROG_CTL_US is
    generic (  
      TEST_MODE : boolean := FALSE
    );
    port (  
      RESET : in  std_logic  
    );
  end component INT_PROG_CTL_US;
CLK_8MHZ : in std_logic; -- accuracy of the 5μs efuse prog pulse depends on this 8MHz clock
GPIO_IN : in std_logic_vector(3 downto 0); -- from software using gpio output
GPIO_OUT : out std_logic_vector(2 downto 0); -- to software using gpio input
JTAG_OUT : out std_logic_vector(3 downto 0) -- for monitoring jtag signals
);
end component INT_PROG_CTL_US;

component JTAG_MONITOR is
  port (  
    JTAG_MON         : in  std_logic_vector(3 downto 0); -- tdi=0, tms=1, tck=2, tdo=3  
    EFUSE_PROG_PULSE : out std_logic  
  );
end component JTAG_MONITOR;

begin

  base_mb_i: base_mb
  port map (    
    CLK_8MHZ                 => clk_8mhz,  
    GPI_tri_i                => GPI_tri_i,  
    GPO_tri_o                => GPO_tri_o,  
    Vp_Vn_v_n                => Vp_Vn_v_n,  
    Vp_Vn_v_p                => Vp_Vn_v_p,  
    default_sysclk_300_clk_n => default_sysclk_300_clk_n,  
    default_sysclk_300_clk_p => default_sysclk_300_clk_p,  
    reset                    => reset,  
    rs232_uart_rxd           => rs232_uart_rxd,  
    rs232_uart_txd           => rs232_uart_txd  
  );

  INT_PROG_CTL_US_i : INT_PROG_CTL_US
  generic map (    
    TEST_MODE => FALSE  
  )
  port map (    
    RESET    => reset,  
    CLK_8MHZ => clk_8mhz,  
    GPIO_IN  => GPO_tri_o,  
    GPIO_OUT => GPI_tri_i,  
    JTAG_OUT => jtag_mon  
  );

  JTAG_MONITOR_i : JTAG_MONITOR
  port map (    
    JTAG_MON       => jtag_mon,  
    EFUSE_PROG_PULSE => EFUSE_PROG_PULSE  
  );

end STRUCTURE; -- base_mb_wrapper
30. Download the project VHDL files `int_prog_ctl_us.vhd` and `jtag_monitor.vhd` to your local computer. See Reference Design for more information.

31. In the center Sources window, right-click on Design Sources, select Add Sources, click Next, select Add or create design sources, and click Add Files. Navigate to and add `int_prog_ctl_us.vhd` and `jtag_monitor.vhd` (files downloaded in step 30), check Copy Sources into project, and click Finish (Figure 18).

![Add or Create Design Sources](image)

**Figure 18:** Add or Create Design Sources

32. Download the project constraint file `xapp1283.xdc` (for UltraScale FPGAs) or `xapp1283_usp.xdc` (for UltraScale+ FPGAs) to your local computer (see Reference Design for more information). The constraint file sets up the external reset pin input and the EFUSE_PROG_PULSE monitor output pin.
33. In the center Sources window, right-click on Design Sources, select Add Sources, select Add or create constraints, click Next, and click Add Files. Navigate to and add the xapp1283.xdc or xapp1283_usp.xdc (file downloaded in the step 32), check Copy constraints files into project, and click Finish (Figure 19).

![Add or Create Constraints](image)

**Figure 19:** Add or Create Constraints

34. From the left Flow Navigator window, select Run Implementation under the Implementation section, click Yes to automatically launch synthesis prior to implementation.

**Note:** Any critical synthesis or implementation warnings associated with the board’s dip switch can be safely ignored because it is not being used in this application note.

**Note:** Interface port names can be slightly different than those in the provided reference design. Ensure the port names match prior to synthesis.

35. After the implementation is successfully completed, click Cancel.
36. From the top-level Vivado tools menu, select **File**, select **Export**, choose **Export Hardware**, and leave **Include bitstream** unchecked. Click **OK** to export **Local to Project** (Figure 20).

![Export Hardware](image)

*Figure 20: Export Hardware*

37. From the top-level Vivado tools menu, select **File > Launch SDK**. Click **OK** to launch **Local to Project** (Figure 21).

![Launch SDK](image)

*Figure 21: Launch SDK*
Building the SDK Applications

The method to create three different SDK applications is explained in this section. In step 37 of the Vivado hardware section the SDK tool is launched with the MicroBlaze processor design as its hardware platform. The following steps are required for the creation of the SDK software applications.

1. From the top-level SDK menu, select **File > New > Board Support Package**.

2. Set the project name to **internal_prog_bsp**, check the **Use default location** checkbox, select **standalone Board Support Package OS**, and click **Finish** (Figure 22).

![Figure 22: Board Support Package Project](image-url)
3. From the Board Support Package Settings popup window, select **xilskey** (6.0 or later for UltraScale FPGAs and 6.3 or later for UltraScale+ FPGAs) **Xilinx Secure Key Library** and click **OK** (Figure 23).

![Figure 23: Board Support Package Settings](image)

4. Select the **system.mss** tab in the center window and then select **Import Examples** under the **Libraries** section at the bottom.
5. Check the **xilskey_bbram_ultrascale_example** checkbox, check the **xilskey_efuse_example** checkbox, and click **OK** (Figure 24).

![Import Examples](image)

*Figure 24: Examples for xilskey*

6. On the left side of the SDK project explorer window, expand the **internal_prog_bsp_xilskey_bbram_ultrascale_example_1** project, expand **src**, and double-click **xilskey_bbram_ultrascale_input.h** to open up the header file in the SDK text editor.

7. Scroll down the header file to find the `#define` statement for **XSK_BBRAM_AES_KEY** and note and record the key value in quotations. Save any changes. The default value can be used in this example or you can enter your own value using exactly 64 hexadecimal characters. For this project, the obfuscated key (XSK_BBRAM_OBFUSCATED_KEY) is not used and can be ignored (Figure 25).

```c
#define XSK_BBRAM_OBFUSCATED_KEY "b1c276899d71fb4cdd4a0a7965ea46c2e11f9574d9c7ea23b76b67de713ccdd1"
#define XSK_BBRAM_AES_KEY "0000000000000000000000000000000000000000000000000000000000000000"```

*Figure 25: XSK_BBRAM_AES_KEY Value*

8. On the left side of the SDK project explorer window, expand the **internal_prog_bsp_xilskey_efuse_example_1** project, expand **src**, and double-click **xilskey_input.h** to open up the header file in the SDK text editor.
9. Scroll down the header file to find the #define statement for `XSK_EFUSEPS_DRIVER` and comment it out (this is only used for Zynq® SoC designs). Save the changes (Figure 26).

```c
#define XSK_EFUSEPL_DRIVER ...
//#define XSK_EFUSEPS_DRIVER
```

**Figure 26: XSK_EFUSEPS_DRIVER**

10. Scroll through the `xilskey_input.h` file to see the different options (commands and values) for programming eFUSEs. For programming details refer to *LibXil SKey for Zynq-7000 UltraScale and Zynq UltraScale+ MPSoC AP SoC Devices User Guide* [Ref 8]. In this example a value is programmed into the 32-bit FUSE_USER register.

**IMPORTANT:** eFUSEs are OTP and the programming is irreversible. Be extremely careful in choosing the eFUSEs that are programmed because they can affect the configuration and operation of the device.

**IMPORTANT:** Do not enable `XSK_EFUSEPL_ENABLE_RSA_AUTH` (PL RSA authentication eFUSE bit) for the XCKU040-2FFVA1156E FPGA device located on the KCU105 evaluation platform. UltraScale devices have a minimum configuration width when RSA is enabled and the KCU105 evaluation board does not conform to this requirement. Enabling the PL RSA authentication eFUSE bit makes the device on this board permanently unconfigurable.

11. Find the #define statement for `XSK_EFUSEPL_PROGRAM_USER_KEY` and set its value to `TRUE` to program the 32-bit FUSE_USER register. Save the changes (Figure 27).

```c
#define XSK_EFUSEPL_PROGRAM_USER_KEY TRUE /**< TRUE burns
 * the USER key */
```

**Figure 27: XSK_EFUSEPL_PROGRAM_USER_KEY Value**

12. Find the #define statement for `XSK_EFUSEPL_READ_USER_KEY` and set its value to `TRUE` in order to read the 32-bit FUSE_USER register. Save the changes (Figure 28).

```c
#define XSK_EFUSEPL_READ_USER_KEY TRUE /**< TRUE read
 * USER key */
```

**Figure 28: XSK_EFUSEPL_READ_USER_KEY Value**
13. Find the #define statement for 32-bit FUSE_USER register value **XSK_EFUSEPL_USER_KEY** (this is not the AES decryption key) and set its value using exactly eight hexadecimal characters. All hexadecimal combinations are permitted with the exception of 0x00000000. Note and record this value. Save the changes (see the example value in Figure 29).

```
#define XSK_EFUSEPL_USER_KEY "012345ED"
```

Figure 29: XSK_EFUSEPL_USER_KEY Value

14. From the top-level SDK menu, select **File**, select **New**, select **Application Project**, and set the project name to **hello_encrypted**. Under Board Support Package, check **Use existing**, click **Next**, select **Hello World** template, and click **Finish** (Figure 30 and Figure 31).

Figure 30: Create an Application Project
15. From the top-level SDK menu, select **Project > Clean > Clean all projects**, and click **OK**.

16. From the top-level SDK menu, select **Project** and click **Build All**. This generates the necessary binary ELF files for each of the three application projects.
Bitstream Generation

In this section, the three ELF files created in the SDK are imported back into the Vivado tools to merge the associated MicroBlaze processor instructions and data into each of the bitstreams. The bitstreams for programming the BBRAM AES key and the 32-bit user eFUSE register are unencrypted and the Hello application is encrypted (using the same key value from the C header file). The following steps outline the generation of these bitstreams.

1. Return to the Vivado tools GUI with the recently built internal_prog_proj project loaded.
2. In the center window, select the Sources tab and then select the Hierarchy tab.
3. Right-click on Design Sources > Add Sources > Add or create design sources > Next > Add Files.
4. Browse to <project_path>/internal_prog_proj/internal_prog_proj.sdk. From this location point to each of the following ELF files and add them to the project:
   a. hello_encrypted/<Debug or Release>/hello_encrypted.elf
   b. internal_prog_xilskey_bbram_ultrascale_example_1/<Debug or Release>/internal_prog_bsp_xilskey_bbram_ultrascale_example_1.elf
   c. internal_prog_xilskey_efuse_example_1/<Debug or Release>/internal_prog_bsp_xilskey_efuse_example_1.elf
5. Do not check Copy sources into project.
6. Click Finish (Figure 32).
Figure 32: Add Sources
7. The three ELF files should now be visible under Design Sources and ELF (Figure 33).

8. Under Design Sources right-click on `internal_prog_bsp_xilskey_bbram_ultrascale_example_1.elf` > Associate ELF Files. Under Associated ELF File for Design Sources browse, select `internal_prog_bsp_xilskey_bbram_ultrascale_example_1.elf`, click OK, and click OK (Figure 34).
9. From the flow navigator window on the left of the Vivado tools screen, under Program and Debug select **Generate Bitstream**.

10. When the bitstream generation is completed, click **Cancel**.

11. Using a file browser, navigate to

   `project_path>/ internal_prog_proj/internal_prog_proj.runs/impl_1` (this path is used again when the bitstreams are programmed into the device).

12. Rename `base_mb_wrapper.bit` to `prog_bbram.bit`. Copy `prog_bbram.bit` to a temporary folder for later use.

13. Under Design Sources right-click on `internal_prog_bsp_xilskey_efuse_example_1.elf`, select **Associate ELF Files**. Under Associated ELF File for Design Sources, browse , select `internal_prog_bsp_xilskey_efuse_example_1.elf`, click **OK**, and click **OK** (Figure 35).

   ![Associate ELF Files](image)

   **Figure 35**: Associate ELF Files (eFUSE)

14. From the flow navigator window on the left of the Vivado tools screen, under Program and Debug, select **Generate Bitstream**.

15. When the bitstream generation is completed, click **Cancel**.

16. Using a file browser, navigate to

   `<project_path>/ internal_prog_proj/internal_prog_proj.runs/impl_1`

17. Rename `base_mb_wrapper.bit` to `prog_efuse.bit`. Copy `prog_efuse.bit` to the same temporary folder as `prog_bbram.bit`.
18. Under Design Sources, right-click on `hello_encrypted.elf` > Associate ELF Files. Under Associated ELF File for Design Sources, browse to, select `hello_encrypted.elf`, click OK, and click OK (Figure 36).

![Associate ELF Files](image)

**Figure 36:** Associate ELF Files (hello)

19. From the flow navigator window on the left of the Vivado tools screen, under Implementation, select Open Implemented Design.

20. Ignore any warning messages that appear and click OK.

21. From the flow navigator window on the left of the Vivado tools screen, under Program and Debug, select Bitstream Settings or right-click on Generate Bitstream and select Bitstream Settings.

22. Select Configure additional bitstream settings, on the left select Encryption, set Enable Bitstream Encryption: Yes, and Select location of encryption key: BBRAM.

23. Copy and paste the 256-bit AES key (the XSK_BBRAM_AES_KEY value from `xilskey_bbram_ultrascale_input.h`) from Building the SDK Applications section into the Starting AES encryption key (key0) text box.
24. Set **Number of encryption blocks per key: 256**, click **OK**, and click **OK** (Figure 37). For more information on encryption block selection, refer to the *UltraScale Architecture Configuration User Guide* (UG570) [Ref 2]. For more information on key rolling, refer to the *Developing Tamper-Resistant Designs with UltraScale and UltraScale+ FPGAs Application Note* (XAPP1098) [Ref 7].

![Edit Device Properties](image)

*Figure 37: Edit Device Properties*
25. From the flow navigator window on the left of the Vivado tools screen, under Program and Debug, select **Generate Bitstream** Generate Bitstream, select **Save**, check **Select an existing file**, set the filename as **xapp1283.xdc** (for UltraScale FPGAs) or **xapp1283_usp.xdc** (for UltraScale+ FPGAs), click **OK**, and click **Overwrite** (Figure 38 and Figure 39). This adds the encryption options and key value to the constraints file.

![Save Project](image_url)

*Figure 38: Save Project*

```plaintext
1 set_property PACKAGE_PIN AN16 [get_ports EFUSE_PROG_PULSE]
2 set_property IOSTANDARD LVCMOS33 [get_ports EFUSE_PROG_PULSE]
3
4 set_property PACKAGE_PIN ANB [get_ports reset]
5 set_property IOSTANDARD LVCMOS33 [get_ports reset]
6
8 set_property BITSTREAM.ENCRYPTION.ENCRYPT YES [current_design]
9 set_property BITSTREAM.ENCRYPTION.KEY 00000000000000000524156a5950bcdeadbeebaae341e505aaabbeaa [current_design]
10 set_property BITSTREAM.ENCRYPTION.KEYLIFE 256 [current_design]
```

*Figure 39: set_property*

26. When the bitstream generation is completed, click **Cancel**.

27. Using a file browser, navigate to
   `<project_path>/internal_prog_proj/internal_prog_proj.runs/impl_1`.

28. Rename `base_mb_wrapper.bit` to `hello_encrypted.bit`. Copy `hello_encrypted.bit` to the same temporary folder as `prog_bbram.bit` and `prog_efuse.bit`
Verification

After the three bitstreams `prog_bbram.bit`, `prog_efuse.bit`, and `hello_encrypted.bit` are successfully generated, you can load each onto the Kintex UltraScale or UltraScale+ device located on the KCU105 or KCU116 evaluation kit respectively, and verify their functionality. The following steps outline the verification of each of these bitstreams.

1. Power up and connect the KCU105 (or KCU116) evaluation board to a computer using the USB JTAG and USB UART cables. For more information when using the UltraScale device, refer to the KCU105 Quick Start Guide (XTP391) [Ref 17] and KCU105 Board User Guide (UG917) [Ref 18]. For more information when using the UltraScale+ device, refer to the KCU116 Evaluation Kit Quick Start Guide (XTP471) [Ref 19] and KCU116 Evaluation Board User Guide (UG1239) [Ref 20].

2. On the KCU105 evaluation board set dip switch **SW15** to the following settings for the JTAG configuration mode:
   - Positions 1 through 5 = OFF
   - Position 6 = ON

On the KCU116 evaluation board set dip switch **SW21** to the following settings for the JTAG configuration mode:
   - Position 6 = ON

3. Determine the COM port that connects to the MicroBlaze processor’s UART using Windows device manager. The USB UART connection establishes two COM ports (standard and enhanced) on the computer (the Silicon Labs serial driver must be installed on the system). The computer COM port associated with the Silicon Labs Standard COM port connects to the MicroBlaze processor’s UART.

4. Start up the serial communications terminal program. The serial port settings should be as follows:
   - COM Port = Silicon Labs Standard COM Port
   - Baud rate: 115200
   - Data: 8
   - Parity: none
   - Stop: none
   - Flow control: none

5. Press and release the PROGRAM_B switch **SW4** on the KCU105 board (or switch **SW5** on the KCU116 board).

**IMPORTANT:** The PROGRAM_B switch must be pressed between each bitstream load because the design contains the MASTER_JTAG primitive. Failure to do so blocks the external JTAG path and the computer’s USB JTAG communications fail.
6. In the Vivado tools from the flow navigator window on the left of the screen, under Program and Debug, select **Hardware Manager**, select **Open Target**, and click **Auto Connect**.

7. In the center hardware window, right-click on the **xcku040_0** device (or **xcku5p_0** device), select **Clear BBR Key**, and click **OK** (Figure 40).

---

**Figure 40:** Hardware Manager BBR Key
8. In the center hardware window, right-click on the **xcku040_0** device (or **xcku5p_0** device), select **Program Device** (Figure 41).

![Hardware Manager Program Device](image1)

**Figure 41:** Hardware Manager Program Device

9. Set **Bitstream file**: `<path_to_bitstreams>/hello_encrypted.bit` and click **Program** (Figure 42).

![Program Device](image2)

**Figure 42:** Program Device (hello_encrypted.bit)

10. The hardware manager attempts to program the device. However, because there is no BBRAM key, the configuration fails. When the bitstream finishes loading, verify that the DONE LED (DS34 for the KCU105 evaluation board and DS32 for the KCU116 evaluation board) is OFF.

11. Power cycle the board with the main power switch **SW1**. Then press and release the **PROGRAM_B** switch **SW4** on the KCU105 board (**SW5** on the KCU116 board).
12. In the center hardware window, right-click on the `xcku040_0` device (or `xcku5p_0` device), select **Program Device**, set **Bitstream file**: `<path_to_bitstreams>/prog_bbram.bit`, and click **Program** (Figure 43).

![Program Device](image)

**Figure 43:** Program Device (prog_bbram.bit)

13. When the bitstream finishes loading, the DONE LED (DS34 for the KCU105 board and DS32 for the KCU116 board) turns ON. Because the MASTER _JTAG is instantiated in the design, it blocks the FPGA’s external JTAG port and causes communication errors in the Vivado Tcl console. These errors are expected and can be safely ignored.

14. The serial terminal window should display a message for a successfully programmed and verified BBRAM (Figure 44).

![Serial Terminal](image)

**Figure 44:** Programmed and Verified BBRAM Key

15. Press and release the **PROGRAM_B** switch **SW4** on the KCU105 board (**SW5** on the KCU116 board).

16. In the center hardware window, right-click on the `xcku040_0` device (or `xcku5p_0` device), select **Program Device**, set **Bitstream file**: `<path_to_bitstreams>/hello_encrypted.bit`, and click **Program**.

17. When the bitstream finishes loading, the DONE LED (DS34 for the KCU105 board and DS32 for the KCU116 board) turns ON because the BBRAM key is loaded internally by the last bitstream (ignore the errors in the Vivado Tcl console).
18. The serial terminal window should display a Hello World message that is appended to the last message. This indicates that the `prog_bbram.bit` bitstream (loaded earlier), wrote the BBRAM key successfully (Figure 45).

![Serial Terminal Window](image)

*Figure 45: Hello World*

19. Press and release the **PROGRAM_B** switch **SW4** on the KCU105 board (**SW5** on the KCU116 board).

20. Clear the serial terminal program screen.

21. If you instantiated the optional **JTAG_MONITOR Module**, connect an oscilloscope probe to J53-2 (PACKAGE_PIN AM16) for the KCU105 board and J87-1 (PACKAGE_PIN D13) for the KCU116 board. This is the EFUSE_PROG_PULSE signal that mirrors the actual eFUSE programming phase. You should see a 5 µs pulse for each eFUSE bit that is programmed from a 0 to a 1.

22. In the center hardware window, right-click on the **xcku040_0** device (or **xcku5p_0** device), select **Program Device**, set **Bitstream file**: `<path_to_bitstreams>/prog_efuse.bit`, and click **Program**.

   **Note:** The `prog_efuse.bit` file is not encrypted. It can be encrypted (if required) using the BBRAM key because the key is already loaded in the device.

23. When the bitstream finishes loading, the DONE LED (DS34 for the KCU105 board and DS32 for the KCU116 board) turns ON (ignore the errors in the Vivado Tcl console).
24. The serial terminal window should display a message for a successfully programmed eFUSE. The 32-bit FUSE_USER register should contain the value that you entered earlier in the header file for XSK_EFUSEPL_USER_KEY (Figure 46).

![Serial terminal window showing eFUSE status bits](image)

*Figure 46: Programmed eFUSE*

25. The eFUSE can be further verified using the Vivado Hardware Manager.

26. Press and release the **PROGRAM_B** switch **SW4** on the KCU105 board (**SW5** on the KCU116 board).

27. In the center hardware window, right-click on the **xcku040_0** device (or **xcku5p_0** device) > **Refresh Device**.

28. In the center hardware window, right-click on the **xcku040_0** device (or **xcku5p_0** device) > **Hardware Device Properties**.
29. In the hardware device properties window (directly below the hardware window), click the **Properties** tab and expand the properties tree at **REGISTER** and then **EFUSE**. The FUSE_USER field should contain the recently programmed eFUSE value (Figure 47).

![Figure 47: FUSE_USER](x18364-011117)

**Conclusion**

This application note describes a procedure to internally program the BBRAM and eFUSE memory of an UltraScale and UltraScale+ FPGA. Internal programmability is valuable, especially in the context of security-critical applications. The method presented takes advantage of the MASTER_JTAG primitive, an existing MicroBlaze-based hardware example design, Xilinx-supplied HDL modules, a software library (XILSKEY), and software examples that are used to create functional applications. The procedure explained in this application note can modify and enhance examples to fit various use models including a tamper event driven model to impose penalties and a field update of a BBRAM AES key over a secure link.
Reference Design

You can download the reference design files for this application note from the Xilinx website.

Table 1 shows the reference design matrix.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
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<tbody>
<tr>
<td><strong>General</strong></td>
<td></td>
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<tr>
<td>Developer name</td>
<td>Ed Peterson</td>
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<tr>
<td>Target devices</td>
<td>UltraScale and UltraScale+ FPGAs</td>
</tr>
<tr>
<td>Source code provided</td>
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<tr>
<td>Source code format</td>
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<td>Design uses code and IP from existing Xilinx application note and reference designs or third party</td>
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<tr>
<td><strong>Simulation</strong></td>
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<tr>
<td>Functional simulation performed</td>
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</tr>
<tr>
<td>Timing simulation performed</td>
<td>No</td>
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<tr>
<td>Test bench used for functional and timing simulations</td>
<td>No (Verification using ILA debugger)</td>
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<td>Test bench format</td>
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<tr>
<td>Simulator software/version used</td>
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<tr>
<td>SPICE/IBIS simulations</td>
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</tr>
<tr>
<td><strong>Implementation</strong></td>
<td></td>
</tr>
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</table>
| Synthesis software tools/versions used | Vivado design suite 2016.3 for UltraScale FPGAs  
Vivado design suite 2017.3 for UltraScale+ FPGAs |
| Implementation software tools/versions used | Vivado design suite 2016.3 for UltraScale FPGAs  
Vivado design suite 2017.3 for UltraScale+ FPGAs |
| Static timing analysis performed | Yes |
| **Hardware Verification** | | |
| Hardware verified | Yes |
| Hardware platform used for verification | KCU105 Evaluation Board for UltraScale FPGAs  
KCU116 Evaluation Board for UltraScale+ FPGAs |
References

1. MicroBlaze Soft Processor Core
2. UltraScale Architecture Configuration User Guide (UG570)
7. Developing Tamper-Resistant Designs with UltraScale and UltraScale+ FPGAs Application Note (XAPP1098)
8. LibXil SKey for Zynq-7000 UltraScale and Zynq UltraScale+ MPSoC AP SoC Devices User Guide (UG643)
9. Xilinx Kintex Ultrascale FPGA KCU105 Evaluation Kit
10. Vivado Design Suite
11. Xilinx Software Development Kit
12. Tera Term http://ttssh2.osdn.jp/index.html.en
13. Xilinx Kintex UltraScale+ FPGA KCU116 Evaluation Kit
14. Soft Error Mitigation Core
15. UltraScale device data sheets:
   - UltraScale Architecture and Products Overview (DS890)
   - Kintex UltraScale Architecture Data Sheet: DC and AC Switching Characteristics (DS892)
   - Virtex UltraScale Architecture Data Sheet: DC and AC Switching Characteristics (DS893)
16. Security Monitor IP Core Product Brief
17. KCU105 Quick Start Guide (XTP391)
18. KCU105 Board User Guide (UG917)
19. KCU116 Evaluation Kit Quick Start Guide (XTP471)
20. KCU116 Evaluation Board User Guide (UG1239)
Revision History

The following table shows the revision history for this document.

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Revision</th>
</tr>
</thead>
<tbody>
<tr>
<td>03/08/2017</td>
<td>1.0</td>
<td>Initial Xilinx release.</td>
</tr>
<tr>
<td>02/15/2018</td>
<td>1.1</td>
<td>Added support for UltraScale+ FPGAs.</td>
</tr>
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</table>

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