## Revision History

The following table shows the revision history for this document.

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Revision</th>
</tr>
</thead>
<tbody>
<tr>
<td>04/29/2019</td>
<td>1.4</td>
<td>Added support for floating-lid designs throughout document.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Added figures, schematics, and relevant information for new devices.</td>
</tr>
<tr>
<td>07/02/2018</td>
<td>1.3.1</td>
<td>Updated web description. No technical content changes.</td>
</tr>
<tr>
<td>06/08/2018</td>
<td>1.3</td>
<td>Added figures, schematics, and relevant information for new devices.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Added Appendix A, Recommended Thermal Solution Installation of Xilinx FCBGA Lidless Packages.</td>
</tr>
<tr>
<td>02/28/2018</td>
<td>1.2</td>
<td>Revised text and updated figures throughout document.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Minor editorial updates and clarifications.</td>
</tr>
<tr>
<td>08/22/2017</td>
<td>1.1</td>
<td>Updated figures.</td>
</tr>
<tr>
<td>01/09/2017</td>
<td>1.0</td>
<td>Initial Xilinx release.</td>
</tr>
</tbody>
</table>
# Table of Contents

Revision History ................................................................. 2

**Chapter 1: Mechanical and Thermal Design Guidelines**

Summary .................................................................................. 4
Introduction .............................................................................. 5
Lidless Flip-Chip Packages ...................................................... 6
Package Mechanical Specifications ......................................... 6
Mechanical Support for Testing ............................................... 7
Thermal Management Strategy ................................................ 16
Thermal Simulation and the Use of Thermal Models ................. 28
Example Heat Sink Thermal Performance ............................. 47
Removing Heat Sink Phase Change Material ......................... 49
Measurement Debug ............................................................... 50
Reference Design Files ............................................................ 50
Conclusion ............................................................................... 51

**Appendix A: Recommended Thermal Solution Installation of Xilinx FCBGA Lidless Packages**

Overview .................................................................................. 52
Challenges ............................................................................... 52
Installation Control ................................................................. 53

**Appendix B: Additional Resources and Legal Notices**

Xilinx Resources ...................................................................... 77
Solution Centers ...................................................................... 77
Documentation Navigator and Design Hubs ............................ 77
References ............................................................................... 78
Please Read: Important Legal Notices ................................. 79
Chapter 1

Mechanical and Thermal Design Guidelines

Summary

This application note describes specifications, guidelines, and best practices for using the Virtex UltraScale+ and Zync UltraScale+ products with the lidless flip-chip device/package combinations listed in Table 1-1.

Table 1-1: Lidless Device/Packag...
Chapter 1: Mechanical and Thermal Design Guidelines

Introduction

Changes to the size, performance, and complexity of programmable logic designs and increases in power density warrant new approaches to system thermal management. Xilinx’s investment in new packaging technology addresses the need to reduce device thermal resistance, allows for increased power dissipation while in the same thermal environment, without increasing junction temperature. The Virtex UltraScale+ and Zync UltraScale+ device/package combinations in Table 1-1 have an innovative lidless packaging design that targets the largest Xilinx 16 nm FinFET technology devices, allowing for up to a 10°C cooler operation with the same power dissipation.

For these packages, component thermal management must be carefully designed to obtain optimum device performance and long-term component reliability. Due to the wide range of mechanical designs available for different applications, it is necessary to design system-level thermal simulations that analyze the thermal interaction of the devices using a specific chassis.

To facilitate system-level thermal design and analysis, this application note describes the thermal models of the device/package combinations listed in Table 1-1. These thermal models can be incorporated into system-level thermal models and analyzed using computational fluid dynamics (CFD) simulation software (e.g., Ansys IcePak and Mentor FloTHERM). This application note discusses how the thermal models are created using simulation software packages and how to use these models.

Precise mechanical design is vital to the optimum performance of programmable logic designs. Often, these devices must be subjected to severe mechanical shock and vibration tests. With good mechanical design, these devices can meet the performance stress requirements. In addition, to maintain good contact between heat sinks and the device, innovative designs are implemented for maximum thermal performance.

This application note presents the unique thermal and mechanical designs and requirements for these Virtex UltraScale+ and Zync UltraScale+ device/package combinations. The reference designs are available in Reference Design Files.

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Heat Sink Design</th>
<th>Thermal Models</th>
<th>Floating Lid Design</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCVU29P</td>
<td>FIGD2104</td>
<td>Figure 1-14</td>
<td>Figure 1-22</td>
<td>Table 1-6</td>
</tr>
<tr>
<td>XCVU29P</td>
<td>FSGA2577</td>
<td>Figure 1-14</td>
<td>Figure 1-22</td>
<td>Table 1-6</td>
</tr>
</tbody>
</table>
Chapter 1: Mechanical and Thermal Design Guidelines

Lidless Flip-Chip Packages

The Xilinx lidless flip-chip ball grid array (BGA) packages use the same package substrate design as traditional lidded flip-chip packages, including the same electrical board and thermal conductivity as traditional flip-chip packaging. However, removing the lid (heat spreader) and adding thermal interface material allows direct contact between the external heat sink and the die. Lidless packages reduce the thermal resistance, improve the thermal behavior, and facilitate using custom passive or active heat-sink designs that incorporate two-phase (heat pipe, vapor chamber, or even liquid) cooling methods directly adjacent to the source of the dissipated heat on the die. All these advantages produce more efficient means of removing the heat from the device. Consequently, the device can operate in higher ambient temperature environments, area-constrained surroundings, and/or higher power operations.

![Lidless Flip-Chip Package Diagram](X18048-011718)

Figure 1-1: Lidless Flip-Chip Package Diagram

Package Mechanical Specifications

Package Mechanical Description and Drawings

Xilinx FPGAs packaged in the flip-chip BGA package are soldered directly to a PCB surface. Detailed mechanical drawings, including package dimensions and BGA ball pitch, are available for the lidless packages in the UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification User Guide (UG575) [Ref 1] and Zynq UltraScale+ Device Packaging and Pinouts Product Specification User Guide (UG1075) [Ref 2], as appropriate. Refer to these user guides for the precise mechanical specification of each package.

A unique feature of the lidless Xilinx packages is the addition of a stiffener ring around the periphery of the package substrate. The stiffener ring provides additional package rigidity to improve the overall package coplanarity (flatness). It also serves as a guide for the heat sink solution applied to the device.
Mechanical Support for Testing

To support the introduction of lidless packages, Xilinx FPGAs can include an accompanying floating lid. To reduce package warpage, Xilinx lidless FPGAs can be designed with a stiffener ring that is higher than the die. When not using a heat sink or test socket with a raised island to contact the die, a floating lid may be used. The floating lid applies pressure to the die, ensuring good contact between the package and test socket or thermal solution.

Floating lids are intended for temporary use in bring-up. If a more permanent testing solution is required, please contact Xilinx support. These designs are provided as-is and are not qualified. Be aware that using a floating lid can reduce thermal performance compared to direct installation of a heat sink on the silicon.

Xilinx provides reference designs for floating lids on some of its lidless packages. These designs are intended to be used with thermal interface material between the die and floating. This material layer should be approximately 100µm thick. Illustrations of the floating lids without this material layer are shown in the following figures. Drawings (.dwg and .pdf) are available in the Reference Design Files.

Floating lids can be ordered from JenTech Precision Industrial Co., LTD (http://www.jentech.com.tw/).
Chapter 1: Mechanical and Thermal Design Guidelines

Floating Lid Designs

The floating lid for XCVU11P-FSGD2104 is available from JenTech (http://www.jentech.com.tw/) (part number not available). Drawings of the design are available in the Reference Design link.

Figure 1-2: Floating Lid for XCVU11P-FSGD2104
The floating lid for XCVU9P-FSGD2104 is available from JenTech (http://www.jentech.com.tw/), part number 60004745.

Drawings of the design are available in the Reference Design link.

**Figure 1-3:** Floating Lid for XCVU9P-FSGD2104
The floating lids for XCVU13P-FIGD2104, XCVU13P-FSGA2577, XCVU27P-FIGD2104, XCVU27P-FSGA2577, XCVU29P-FIGD2104, and XCVU29P-FSGA2577 are available from JenTech (http://www.jentech.com.tw/), part number 60004989.

Drawings of the design are available in the Reference Design link.

Figure 1-4: Floating Lid for XCVU13P-FIGD2104, XCVU13P-FSGA2577, XCVU27P-FIGD2104, XCVU27P-FSGA2577, XCVU29P-FIGD2104, and XCVU29P-FSGA2577
The floating lid for XCZU25DR-FSVE1156, XCZU27DR-FSVE1156, and XCZU28DR-FSVE1156 is available from JenTech (http://www.jentech.com.tw/), part number 60005403.

Drawings of the design are available in the Reference Design link.

**Figure 1-5:** Floating Lid for XCZU25DR-FSVE1156, XCZU27DR-FSVE1156, and XCZU28DR-FSVE1156
Chapter 1: Mechanical and Thermal Design Guidelines

The floating lid for XCZU25DR-FSVG1517, XCZU27DR-FSVG1517, and XCZU28DR-FSVG1517 is available from JenTech (http://www.jentech.com.tw/), part number 60005404.

Drawings of the design are available in the Reference Design link.

Figure 1-6: Floating Lid for XCZU25DR-FSVG1517, XCZU27DR-FSVG1517, and XCZU28DR-FSVG1517

Drawings of the design are available in the Reference Design link.

*Figure 1-7: Floating Lid for XCZU29DR-FSVF1760*
The floating lid for XCVU31P-FSVH1924 is available from JenTech (http://www.jentech.com.tw/), part number 60005649. Drawings of the design are available in the Reference Design link.

Figure 1-8: Floating Lid for XCVU31P-FSVH1924
The floating lids for XCVU33P-FSVH2104 and XCVU35P-FSVH2104 are available from JenTech (http://www.jentech.com.tw/), part number 60005552. Drawings of the design are available in the Reference Design link.

Figure 1-9: Floating Lid for XCVU33P-FSVH2104 and XCVU35P-FSVH2104
The floating lids for XCVU35P-FSVH2892 and XCVU37P-FSVH2892 are available from JenTech (http://www.jentech.com.tw/), part number 60005552. Drawings of the design are available in the Reference Design link.

**Thermal Management Strategy**

Exceptional thermal management starts with good package design. However, it only comes into fruition when accompanied by a well-designed heat-sink solution.

**Keep-Out Zones**

In BGA packages, capacitors can be placed in the area surrounding the die. These die-side capacitors are only slightly shorter than the die height. Since the capacitors could be electrically conductive, contact with electrically conductive materials must be avoided.

A thermal and mechanical solution design must not interfere with the package stiffener where it is higher than the die. Therefore, the thermal solution must have an island. The following example uses the XCVU13P-D2104.
Dimensional properties of the XCVU13P-FIGD2104 contact island:

Width = 34 mm
Length = 42 mm
Height = 1.5 mm
Flatness: < 75 µm
Surface roughness = 3~5 µm

- For more information, see the heat-sink for XCVU13P-FIGD2104 (Figure 1-14). The island requires a thermal interface material coverage of 35.5 x 44 mm. The reference design used Laird (PCM780SP) or Honeywell (PTM6500D).
- The total thermal contact of the thermal interface material is determined based on the above parameters from the thermal interface supplier’s data sheet.
- The applied pressure on the package must follow the guidelines in Heat Sink Pressure. Lower pressure risks poor thermal contact and higher pressure risks damaging the device; therefore, strict control of pressure is required. See the Applied Pressure from Heat Sink to the Package via Thermal Interface Materials recommendation in the UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification User Guide (UG575) [Ref 1] and Zynq UltraScale+ MPSoC Packaging and Pinouts Product Specification User Guide (UG1075) [Ref 2].
- Consider all uncertainties in thermal modeling, including manufacturing variations from the thermal solutions (for example, fan airflow tolerance, heat pipe or vapor chamber performance tolerance, variation of the attachment of fins to the heat sink base, and surface flatness).

The heat sink design examples include CAD files and documentation for designing heat sinks specifically for these device/package combinations. The example heat sink designs serve as a reference for the devices/packages listed in Table 1-1.

Heat Sink Solutions at the System Level

Taking into consideration the system's physical, mechanical, and environmental constraints, the overall thermal budget must be maintained so that it does not exceed the device's maximum operating temperature. The heat sink is an integral, if not the most important, part of the thermal management solution to maintain a safe operating temperature. As a result, the following are important:

- Detailed instructions on recommended Thermal Solution Installation of Xilinx's FCBGA Lidless Packages are provided in Appendix A.
- $\Theta_{JC}$ parameters from UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification User Guide (UG575) [Ref 1] and Zynq UltraScale+ MPSoC Packaging and Pinouts Product Specification User Guide (UG1075) [Ref 2] must not be directly used to
determine the thermal performance of the device application. These parameters are calculated according to JEDEC JESD51 standards, where system parameters differ greatly from most applications. Instead, run system thermal simulations in worst-case environmental conditions using the DELPHI thermal models, which more accurately represent the device thermal performance under all boundary conditions.

- Consider the mechanical specifications of the package, as well as selecting the best thermal interface between the die and the thermal management solution to ensure the lowest thermal contact resistance.

- Figure 1-11 shows the PCM780SP coverage after 1000 Thermal BLR Cycles for 0°C to 100°C. The package passed 5000 Thermal cycles without any failure.

![Example of Heat Sink for VU13P-FIGD2104 with PCM780SP](image)
Chapter 1: Mechanical and Thermal Design Guidelines

Heat Sink Designs

The reference design file includes heat sink design examples with CAD files, to assist in designing heat sinks for these packages. Figure 1-12 through Figure 1-18 are examples of heat sink designs.

Figure 1-12: Heat Sink (Heat-pipe with Etching Design) for XCVU11P-FSGD2104

The heat-pipe with etching design for XCVU11P-FSGD2104 is available from supplier NTK (HK) LIMITED using part number 19020000009 (www.ntkltd.com). A 3D model of this design is available in STEP format in the Reference Design link.
The heat-pipe with etching design for XCVU9P-FSGD2104 is available from supplier NTK (HK) LIMITED using part number 19020000010 (www.ntkltd.com). A 3D model of this design is available in STEP format in the Reference Design link.
The heat-pipe with etching design for the XCVU13P-FIGD2104, XCVU13P-FSGA2577, XCVU27P-FIGD2104, XCVU27P-FSGA2577, XCVU29P-FIGD2104, and XCVU29P-FSGA2577 is available from supplier NTK (HK) LIMITED using part number 19020000011 (www.ntkltd.com). A 3D model of this design is available in STEP format in the Reference Design link.
Chapter 1: Mechanical and Thermal Design Guidelines

The heat-pipe heat sink design for the XCVU31P-FSVH1924 and XCVU33P-FSVH2104 is available from the supplier NTK (HK) LIMITED using part number 1902000006 (www.ntkltd.com). A 3D model of this design is available in STEP format in the Reference Design link.
Chapter 1: Mechanical and Thermal Design Guidelines

The heat-pipe heat sink design for the XCVU35P-FSVH2104 and XCVU35P-FSVH2892 is available from the supplier NTK (HK) LIMITED using part number 19020000007 (www.ntkltd.com). A 3D model of this design is available in STEP format in the Reference Design link.

Figure 1-16: Heat Sink (Heat-pipe Design) for XCVU35P-FSVH2104 and XCVU35P-FSVH2892

The heat-pipe heat sink design for the XCVU35P-FSVH2104 and XCVU35P-FSVH2892 is available from the supplier NTK (HK) LIMITED using part number 19020000007 (www.ntkltd.com). A 3D model of this design is available in STEP format in the Reference Design link.
The heat-pipe heat sink design for the XCVU37P-FSVH2892 is available from the supplier NTK (HK) LIMITED using part number 19020000008 (www.ntkltd.com). A 3D model of this design is available in STEP format in the Reference Design link.
Chapter 1: Mechanical and Thermal Design Guidelines

The heat-pipe heat sink design for the XCZU25DR-FSVE1156, XCZU25DR-FSVG1517, XCZU27DR-FSVE1156, XCZU27DR-FSVG1517, XCZU28DR-FSVE1156, XCZU28DR-FSVG1517, and XCZU29DR-FSVF1760 is available from the supplier NTK (HK) LIMITED using part number 15029000217 (www.ntkltd.com). A 3D model of this design is available in STEP format in the Reference Design link.

Figure 1-18: Heat Sink (Heat-pipe Design) for XCZU25DR-FSVE1156, XCZU25DR-FSVG1517, XCZU27DR-FSVE1156, XCZU27DR-FSVG1517, XCZU28DR-FSVE1156, XCZU28DR-FSVG1517, and XCZU29DR-FSVF1760
Chapter 1: Mechanical and Thermal Design Guidelines

Heat Sink Pressure

The typical engineering practice is to use 20 to 50 psi pressure, based on die size, pin count, and other factors. This optimizes thermal performance contact between the silicon and the thermal solution via the thermal interface material (TIM).

**Note:** In the past, Xilinx has recommended 20 to 40 psi in some places and 5 to 10 g force per pin in other places. These recommendations were based on individual product cases, which were verified to work. Typical industry recommendations are 20-60 psi or 5-15 g force per pin (varies by die and package size).

The amount of force the screws apply on the heat sink should be approximately equal to the amount of force the heat sink applies on the die, transferred through the TIM. When designing the heat sink, the amount of force the screws will apply on the heat sink can be approximated by:

\[ F = n \times k \times \delta \]  
*Equation 1-1*

Where \( n \) is the number of springs, \( k \) is the spring constant and \( \delta \) is the compression length of the spring. In the reference designs provided here, \( n \) is 4. The spring constant can be obtained from the vendor or measured. The compression length is:

\[ \delta = l_c - l_0 \]  
*Equation 1-2*

Where \( l_c \) is the compressed spring length and \( l_0 \) is the uncompressed or initial spring length. These spring lengths can be determined by performing a stack-up analysis of the components as shown in Figure 1-19. For example, \( l_c \) is [1] in Figure 1-19. An example of stack-up analysis, in which the screw stop is on the top of the motherboard, is:

\[ l_c = h_s - h_c - h_{TIM} - h_{HS} \]  
*Equation 1-3*

Where \( h_s \) is the dimension of the spring between the stopper and screw-head (e.g. [1] + [2] in Figure 1-19, \( h_c \) is the dimension of the assembled package (BGA to die surface), \( h_{TIM} \) is the thickness of the TIM1.5, and \( h_{HS} \) is the dimension of the heat sink from the heat sink island to the plane the spring sits on.
Based on the force the heat sink applies on the die, the pressure can be calculated as:

\[ P = \frac{F}{A_{\text{die}}} \]

Equation 1-4

Where \( A_{\text{die}} \) is the die area, which can be obtained from Zynq UltraScale+ MPSoC Packaging and Pinouts Product Specification User Guide (UG1075) [Ref 1] or Zynq UltraScale+ MPSoC Packaging and Pinouts Product Specification User Guide (UG1075) [Ref 2].

Xilinx recommends using heat sink dynamic mounting, which refers to using screw-springs to attach the heat sink. As the board warps during thermal excursion or other deflection occurs due to mechanical force, the springs will adjust to apply greater force at smaller deflections, dynamically adjusting to any changes. Through screw-spring design, as detailed above, the compressed length of the spring should be fixed, creating a product with consistent heat sink force. For a given product, the die size is fixed, leading to a constant heat sink pressure on the die. Xilinx also recommends using a back bracket or back plate to provide mechanical support.
During installation, the amount of screw torque necessary to obtain that pressure is best determined through measurement, as detailed in Appendix A. Xilinx has found that a torque of 2.5 in-lbf on each screw usually produces a pressure within the desired range. Any screw torque should be verified for pressure on the die.

During pressure measurement (or normal operation), thermocouples should not be present between the package and the heat sink, as their presence will degrade the thermal contact and result in incorrect thermal measurements. The best practice is to select the appropriate pressure for the optimum thermal contact performance between the package and the thermal system solution, and the mechanical integrity of the package, with the thermal solution to pass all mechanical stress and vibration qualification tests.

---

**Thermal Simulation and the Use of Thermal Models**

Xilinx offers and supports a suite of integrated device power analysis tools to help quickly and accurately estimate the power requirements of your design. Download and fill out the latest version of the Xilinx Power Estimator (XPE) at [https://www.xilinx.com/power](https://www.xilinx.com/power). The variability of design power requirements makes it difficult to apply predetermined thermal solutions. The estimated power of the device using XPE, coupled with system operating conditions and constraints dictate the appropriate solution.

Xilinx recommends using the simplified thermal model, DELPHI thermal model, or detailed thermal model during thermal modeling of the system. Xilinx does not recommend using a 2-resistor model for thermal simulation and design due to lack of precision and accuracy. A detailed model representation of the package might consume more simulation memory and runtime during use. The user of the thermal model needs to consider thermal sensor accuracy, thermal interface material parameters, and manufacturing variations on the thermal solution. Examples of manufacturing variations include airflow tolerance from a fan, performance tolerance of the heat pipe and vapor chamber, and the manufacturing variation of attaching fins to the heat-sink base and the flatness of the surface.

**Simplified Model**

A simplified model seeks to capture the thermal behavior of the package more accurately to predict the junction temperature with reduced package modeling complexity. Unlike a full 3D model, simplified models are computationally efficient and work well in an integrated system simulation environment. Simplified models are appropriate in the early stages of a design to have an estimated value of the thermal solution. However, a Detailed Model should be completed before finalizing a design.

A simplified model is available on the Xilinx support download center under UltraScale+ FPGAs - Package Thermal Models. Simplified models are available in both Ansys IcePak and Mentor FloTHERM formats.
The constructed model must accurately present the package, especially if your simulation tool is not FloTHERM or Icepack. The definition of the TIM2 or contact surface for the top of the simplified model must be correctly defined for the package to produce the correct results. This simplified model has a defined top-contact surface of the die, which may not be the full package size.

**Two-Resistor Model**

A two-resistor thermal model is not recommended because with different thermal solutions, the heat spreading inside the package varies. The same variation of $\Theta_{JB}$ also occurs when the package is mounted in a PCB with different layers and the PCB can dissipate its heat to the surrounding ambient environment. The thermal resistance from junction to case ($\Theta_{JC}$) and the thermal resistance of junction to board ($\Theta_{JB}$) as functions of the surrounding conditions are available.

Do not place a thermocouple between the die and any surface in contact with it because it could create a poor thermal contact and lead to the package overheating. Junction temperature values should be taken using the System Monitor.

Table 1-2 shows the variation of $\Theta_{JC}$ functions of the surrounding conditions and Table 1-3 shows the thermal resistance from junction to board, $\Theta_{JB}$, for the selected device/package combinations. The reported $\Theta_{JC}$ and $\Theta_{JB}$ enable comparison of different packages under the same condition.

<table>
<thead>
<tr>
<th>Device</th>
<th>$h$ (W/m$^2$K)</th>
<th>100</th>
<th>1000</th>
<th>5000</th>
<th>10000</th>
<th>JEDEC</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCVU11P-FSGD2104</td>
<td>$\Theta_{JC}$</td>
<td>0.004</td>
<td>0.004</td>
<td>0.004</td>
<td>0.004</td>
<td>0.004</td>
</tr>
<tr>
<td>XCVU9P-FSGD2104</td>
<td>$\Theta_{JC}$</td>
<td>0.003</td>
<td>0.003</td>
<td>0.003</td>
<td>0.003</td>
<td>0.003</td>
</tr>
<tr>
<td>XCVU13P-FIJD2104, XCVU13P-FSGA2577</td>
<td>$\Theta_{JC}$</td>
<td>0.003</td>
<td>0.003</td>
<td>0.003</td>
<td>0.003</td>
<td>0.003</td>
</tr>
<tr>
<td>XCVU31P-FSVH1924</td>
<td>$\Theta_{JC}$</td>
<td>0.367</td>
<td>0.324</td>
<td>0.247</td>
<td>0.213</td>
<td>0.055</td>
</tr>
<tr>
<td>XCVU33P-FSVD2104</td>
<td>$\Theta_{JC}$</td>
<td>0.306</td>
<td>0.270</td>
<td>0.208</td>
<td>0.180</td>
<td>0.034</td>
</tr>
<tr>
<td>XCVU35P-FSVH2104</td>
<td>$\Theta_{JC}$</td>
<td>0.145</td>
<td>0.127</td>
<td>0.100</td>
<td>0.088</td>
<td>0.017</td>
</tr>
<tr>
<td>XCVU35P-FSVH2892</td>
<td>$\Theta_{JC}$</td>
<td>0.142</td>
<td>0.126</td>
<td>0.099</td>
<td>0.087</td>
<td>0.017</td>
</tr>
<tr>
<td>XCVU37P-FSVH2892</td>
<td>$\Theta_{JC}$</td>
<td>0.086</td>
<td>0.078</td>
<td>0.065</td>
<td>0.059</td>
<td>0.013</td>
</tr>
<tr>
<td>XCUZU25DR-FSVE1156, XCUZU27DR-FSVE1156, XCUZU28DR-FSVE1156</td>
<td>$\Theta_{JC}$</td>
<td>0.0189</td>
<td>0.0188</td>
<td>0.0186</td>
<td>0.0183</td>
<td>0.0164</td>
</tr>
<tr>
<td>XCUZU25DR-FSVG1517, XCUZU27DR-FSVG1517, XCUZU28DR-FSVG1517</td>
<td>$\Theta_{JC}$</td>
<td>0.0190</td>
<td>0.0188</td>
<td>0.0185</td>
<td>0.0170</td>
<td>0.0164</td>
</tr>
</tbody>
</table>
### Table 1-2: Variation of $\Theta_{JC}$ with Different External Thermal Solution by Customer

<table>
<thead>
<tr>
<th>Device</th>
<th>$h$ (W/m² K)</th>
<th>100</th>
<th>1000</th>
<th>5000</th>
<th>10000</th>
<th>JEDEC</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCZU29DR-FSVF1760</td>
<td>$\Theta_{JC}$</td>
<td>0.0190</td>
<td>0.0188</td>
<td>0.0185</td>
<td>0.0183</td>
<td>0.0164</td>
</tr>
<tr>
<td>XCVU27P-FIGD2104</td>
<td>$\Theta_{JC}$</td>
<td>0.003</td>
<td>0.003</td>
<td>0.003</td>
<td>0.003</td>
<td>0.003</td>
</tr>
</tbody>
</table>

### Table 1-3: Variation of $\Theta_{JB}$ with the Different External Thermal Solutions

<table>
<thead>
<tr>
<th>Devices</th>
<th>$h$ (W/m² K)</th>
<th>$K_{x,y}=25, K_{z}=0.4$</th>
<th>$K_{x,y}=50, K_{z}=0.75$</th>
<th>$K_{x,y}=90, K_{z}=1.5$</th>
<th>$K_{x,y}=110, K_{z}=5$</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCVU11P-FSGD2104</td>
<td>100</td>
<td>0.324 (modified JEDEC)</td>
<td>0.292</td>
<td>0.253</td>
<td>0.219</td>
</tr>
<tr>
<td>XCVU9P-FSGD2104</td>
<td>100</td>
<td>0.340 (modified JEDEC)</td>
<td>0.300</td>
<td>0.257</td>
<td>0.220</td>
</tr>
<tr>
<td>XCVU13P-FIGD2104XCVU13P-FSGA2577</td>
<td>100</td>
<td>0.272 (modified JEDEC)</td>
<td>0.244</td>
<td>0.212</td>
<td>0.185</td>
</tr>
<tr>
<td>XCVU31P-FSVH1924</td>
<td>100</td>
<td>0.70 (modified JEDEC)</td>
<td>0.63</td>
<td>0.54</td>
<td>0.47</td>
</tr>
<tr>
<td>XCVU33P-FSVH2104</td>
<td>100</td>
<td>0.74 (modified JEDEC)</td>
<td>0.66</td>
<td>0.56</td>
<td>0.47</td>
</tr>
<tr>
<td>XCVU35P-FSVH2104</td>
<td>100</td>
<td>0.45 (modified JEDEC)</td>
<td>0.40</td>
<td>0.33</td>
<td>0.28</td>
</tr>
<tr>
<td>XCVU35P-FSVH2892</td>
<td>100</td>
<td>0.55 (modified JEDEC)</td>
<td>0.48</td>
<td>0.40</td>
<td>0.33</td>
</tr>
<tr>
<td>XCVU37P-FSVH2892</td>
<td>100</td>
<td>0.39 (modified JEDEC)</td>
<td>0.34</td>
<td>0.28</td>
<td>0.24</td>
</tr>
<tr>
<td>XCZU25DR-FSVE1156</td>
<td>100</td>
<td>1.13</td>
<td>0.99</td>
<td>0.86</td>
<td>0.76</td>
</tr>
<tr>
<td>XCZU27DR-FSVE1156</td>
<td>100</td>
<td>1.18</td>
<td>1.02</td>
<td>0.86</td>
<td>0.74</td>
</tr>
<tr>
<td>XCZU29DR-FSVF1760</td>
<td>100</td>
<td>1.25</td>
<td>1.05</td>
<td>0.88</td>
<td>0.75</td>
</tr>
<tr>
<td>XCVU27P-FIGD2104XCVU27P-FSGA2577XCVU29P-FIGD2104XCVU29P-FSGA2577</td>
<td>100</td>
<td>0.272 (modified JEDEC)</td>
<td>0.244</td>
<td>0.212</td>
<td>0.185</td>
</tr>
</tbody>
</table>
Chapter 1: Mechanical and Thermal Design Guidelines

The effective thermal conductivity of the PCB, $k_e$, as referenced in Lemczyk et al. (1992)

$$k_e = \frac{2(k_x k_z)}{k_x + k_z}$$  

Equation 2

The relation of $\Theta_{JB}$ as a function of $k_e$ can be correlated as shown in Figure 1-20 through Figure 1-30:

For XCVU11P-FSGD2104: $\Theta_{JB} = 0.3063k_e^{-0.157}$

(R$_{JB}$ based on modified JEDEC is 0.324)

$R_{JB} = 0.3063k_e^{-0.157}$

*Figure 1-20: XCVU11P-FSGD2104: The Relationship between $\Theta_{JB}$ and $k_e$*
For XCVU9P-FSGD2104: $\Theta_{JB} = 0.318 k_e^{-0.173}$

Figure 1-21: XCVU9P-FSGD2104: The Relationship between $\Theta_{JB}$ and $k_e$

(R$_{JB}$ based on modified JEDEC is 0.340)
For XCVU13P-FIGD2104, XCVU13P-FSGA2577, XCVU27P-FIGD2104, XCVU27P-FSGA2577, XCVU29P-FIGD2104, and XCVU29P-FSGA2577: \( \Theta_{JB} = 0.2564k_e^{-0.154} \)

\[
R_{JB} = 0.2564k_e^{-0.154}
\]

(R\textsubscript{JB} based on modified JEDEC is 0.272)

**Figure 1-22**: XCVU13P-FIGD2104, XCVU13P-FSGA2577, XCVU27P-FIGD2104, XCVU27P-FSGA2577, XCVU29P-FIGD2104, and XCVU29P-FSGA2577: The Relationship between \( \Theta_{JB} \) and \( k_e \)
For XCVU31P-FSVH1924: $\Theta_{JB} = 0.66k_{e}^{-0.16}$

**Figure 1-23:** XCVU31P-FSVH1924: The Relationship between $\Theta_{JB}$ and $k_{e}$

For XCVU33P-FSVH2104 $\Theta_{JB} = 0.6961k_{e}^{-0.182}$

**Figure 1-24:** XCVU33P-FSVH2104: The Relationship between $\Theta_{JB}$ and $k_{e}$
Chapter 1: Mechanical and Thermal Design Guidelines

For XCVU35P-FSVH2104 $\Theta_{JB} = 0.4206k_{e}^{-0.191}$

*Figure 1-25: XCVU35P-FSVH2104: The Relationship between $\Theta_{JB}$ and $k_{e}$*

For XCVU35P-FSVH2892 $\Theta_{JB} = 0.5115k_{e}^{-0.205}$

*Figure 1-26: XCVU35P-FSVH2892: The Relationship between $\Theta_{JB}$ and $k_{e}$*
For XCVU37P-FSVH2892 $\Theta_{JB} = 0.3606k_e^{-0.194}$
For XCZU25DR-FSVE1156, XCZU27DR-FSVE1156, and XCZU28DR-FSVE1156: $\Theta_{JB} = 1.0518k_e^{-0.156}$

**Figure 1-28:** XCZU25DR-FSVE1156, XCZU27DR-FSVE1156, and XCZU28DR-FSVE1156: The Relationship between $\Theta_{JB}$ and $k_e$
Chapter 1: Mechanical and Thermal Design Guidelines

For XCZU25DR-FSVG1517, XCZU27DR-FSVG1517, and XCZU28DR-FSVG1517: \( \Theta_{JB} = 1.0895k_{e}^{-0.185} \)

Figure 1-29: XCZU25DR-FSVG1517, XCZU27DR-FSVG1517, and XCZU28DR-FSVG1517: The Relationship between \( \Theta_{JB} \) and \( k_{e} \)

\( \Theta_{JB} \) based on modified JEDEC is 1.13°C/W
For XCZU29DR-FSVF1760: $\Theta_{JB} = 1.1382k_e^{-0.2}$

**Detailed Model**

A detailed thermal model is a direct representation of the device and package. This model provides geometric details describing the packaging, specifically in regards to the lid, TIM, die, under fill, substrate, and solder balls or leads. Each specific component in the detailed model has associated material properties. When using the detailed model, account for the following:

1. Use the correct top surface contact for the package when modeling TIM on top of the detailed model, as the top surface contact may not be the actual full package size.
2. The Cu block included is a reference design of a Cu heat spreader contacting the heat sink with TIM2. The TIM of 70um thickness with a conductivity of 20 W/mK is represented in the model to provide effective correlation to the measurement results. This effective TIM1.5 reflects the contact surface etching of the Cu block in combination with the TIM material PCM780SP.
3. The temperature junction monitor point is at the die center. The junction monitor point needs to be positioned or added to the relevant location for your design.
4. The uniform power defined in the die is a default power and not necessarily realistic. You need to input the specific power requirement, especially if the power density varies throughout the die.

**Figure 1-30: XCZU29DR-FSVF1760: The Relationship between $\Theta_{JB}$ and $k_e$**
Due to the computationally intensive nature of this model, do not use it early in thermal management development when several iterations might be needed to find the solution. Instead, use the more agile simplified representation of the package, saving the detailed model for the end of the development cycle to more precisely verify the system’s thermal margin.

For accurate results, a constructed model must accurately represent the package, especially if your simulation tool is not FloTHERM or IcePak. Since the reported simplified model is more accurate when compared to a detailed or two-resistor model, your simulations must account for any accuracy differences.

**DELPHI Model**

The DELPHI model seeks to capture the thermal behavior of the packages more accurately at predetermined critical points (junction, case, top, leads, and so on) with the reduced set of nodes. Unlike a full 3D model, these are computationally efficient and work well in an integrated system simulation environment. The DELPHI model is more appropriate for estimating the value of the thermal solution in the early stages of a design.

The DELPHI model is available on the Xilinx support download center (under Model Type, see Package Thermal Models).

*Table 1-4 through Table 1-9 show the thermal resistances for Xilinx’s lidless flip-chip packages.*

**Table 1-4: XCVU11P-FSGD2104 DELPHI Thermal Resistance Value (°C/watt)**

<table>
<thead>
<tr>
<th></th>
<th>Top Inner</th>
<th>Bottom Inner</th>
<th>Top Outer</th>
<th>Bottom Outer</th>
<th>Side</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction</td>
<td>0.004</td>
<td>0.39</td>
<td>∞</td>
<td>5.38</td>
<td>225.00</td>
</tr>
<tr>
<td>Top Inner</td>
<td></td>
<td>∞</td>
<td>∞</td>
<td>135.18</td>
<td>∞</td>
</tr>
<tr>
<td>Bottom Inner</td>
<td></td>
<td></td>
<td>∞</td>
<td>17.79</td>
<td>∞</td>
</tr>
<tr>
<td>Top Outer</td>
<td></td>
<td></td>
<td>∞</td>
<td></td>
<td>∞</td>
</tr>
<tr>
<td>Bottom Outer</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.44</td>
</tr>
</tbody>
</table>

**Table 1-5: XCVU9P-FSGD2104 DELPHI Thermal Resistance Value (°C/watt)**

<table>
<thead>
<tr>
<th></th>
<th>Top Inner</th>
<th>Bottom Inner</th>
<th>Top Outer</th>
<th>Bottom Outer</th>
<th>Side</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction</td>
<td>0.003</td>
<td>0.40</td>
<td>∞</td>
<td>4.78</td>
<td>75.00</td>
</tr>
<tr>
<td>Top Inner</td>
<td></td>
<td>∞</td>
<td>∞</td>
<td>661.15</td>
<td>∞</td>
</tr>
<tr>
<td>Bottom Inner</td>
<td></td>
<td></td>
<td>∞</td>
<td>35.21</td>
<td>∞</td>
</tr>
<tr>
<td>Top Outer</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>∞</td>
</tr>
<tr>
<td>Bottom Outer</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.43</td>
</tr>
</tbody>
</table>
The DELPHI model is available precompiled in both Ansys IcePak and Mentor FloTHERM. If using a different thermal modeling tool, the DELPHI model can be constructed using the above thermal resistances. These thermal resistances must be in a block with the structure shown in Figure 1-31 and the dimensions specified in Table 1-10.
## Chapter 1: Mechanical and Thermal Design Guidelines

**Figure 1-31:** The Top Inner Area Location in the Top Outer Area

**Table 1-10:** Top Inner and Top Outer Dimensions (mm)

<table>
<thead>
<tr>
<th>Device</th>
<th>Top Inner</th>
<th>Top Outer</th>
<th>Side</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>X</td>
<td>Y</td>
<td>X</td>
</tr>
<tr>
<td>XCVU11P-FSGD2104</td>
<td>28.72</td>
<td>27.78</td>
<td>47.5</td>
</tr>
<tr>
<td>XCVU9P-FSGD2104</td>
<td>25.55</td>
<td>34.44</td>
<td>47.5</td>
</tr>
<tr>
<td>XCVU13P-FSGD2104</td>
<td>28.72</td>
<td>37.08</td>
<td>52.5</td>
</tr>
<tr>
<td>XCVU13P-FSGA2577</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XCVU28DR-FSVE1156</td>
<td>21.13</td>
<td>18.144</td>
<td>35</td>
</tr>
<tr>
<td>XCVU25DR-FSVE1156</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XCVU27DR-FSVE1156</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XCVU28DR-FSVG1517</td>
<td>21.13</td>
<td>18.144</td>
<td>40</td>
</tr>
<tr>
<td>XCVU25DR-FSVG1517</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XCVU27DR-FSVG1517</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XCVU29DR-FSVF1760</td>
<td>21.13</td>
<td>18.144</td>
<td>42.5</td>
</tr>
<tr>
<td>XCVU27P-FJGD2104,</td>
<td>28.72</td>
<td>37.08</td>
<td>52.5</td>
</tr>
<tr>
<td>XCVU27P-FSGA2577</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XCVU29P-FJGD2104</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XCVU29P-FSGA2577</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
The bottom inner area is shown in Figure 1-32 and the dimensions are specified in Table 1-11.

![Figure 1-32: The Bottom Inner Area Location in the Bottom Outer Area](image)

**Table 1-11: Bottom Inner and Bottom Outer Dimensions (mm)**

<table>
<thead>
<tr>
<th>Device</th>
<th>Bottom Inner</th>
<th>Bottom Outer</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>X</td>
<td>Y</td>
</tr>
<tr>
<td>XCVU11P-FSGD2104</td>
<td>28.72</td>
<td>27.78</td>
</tr>
<tr>
<td>XCVU9P-FSGD2104</td>
<td>25.56</td>
<td>34.46</td>
</tr>
<tr>
<td>XCVU13P-FIGD2104</td>
<td>30.07</td>
<td>38.82</td>
</tr>
<tr>
<td>XCVU13P-FSGA2577</td>
<td></td>
<td></td>
</tr>
<tr>
<td>XCZU25DR-FSVE1156</td>
<td>21.22</td>
<td>18.22</td>
</tr>
<tr>
<td>XCZU27DR-FSVE1156</td>
<td></td>
<td></td>
</tr>
<tr>
<td>XCZU28DR-FSVE1156</td>
<td></td>
<td></td>
</tr>
<tr>
<td>XCZU25DR-FSVG1517</td>
<td>21.27</td>
<td>18.27</td>
</tr>
<tr>
<td>XCZU27DR-FSVG1517</td>
<td></td>
<td></td>
</tr>
<tr>
<td>XCZU28DR-FSVG1517</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Chapter 1: Mechanical and Thermal Design Guidelines

For accurate results, ensure that the constructed model accurately represents the package, especially if the simulation tool is not FloTHERM or IcePak. The reported DELPHI model has better accuracy compared to the detail model versus solely the two-resistor model.

Model Comparisons

This section shows model comparisons between simplified models, DELPHI models, and detailed models, as available. Temperature comparisons are made using degrees Celsius. These comparisons are based on Icepak simulations.

Table 1-12: Comparison between the Detailed Model and Different DELPHI Model for XCVU11P-FSGD2104

<table>
<thead>
<tr>
<th>Boundary</th>
<th>h (W/m² K)</th>
<th>Detailed Model</th>
<th>DELPHI Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top Boundary</td>
<td>100</td>
<td>X</td>
<td>0.999X</td>
</tr>
<tr>
<td></td>
<td>10000</td>
<td>X</td>
<td>1.000X</td>
</tr>
<tr>
<td>Bottom Boundary</td>
<td>100 (kₑ = 0.78)</td>
<td>X</td>
<td>0.991X</td>
</tr>
<tr>
<td></td>
<td>100 (kₑ = 9.6)</td>
<td>X</td>
<td>1.009X</td>
</tr>
</tbody>
</table>

Table 1-13: Comparison between the Detailed Model and Different DELPHI Model for XCVU9P-FSGD2104

<table>
<thead>
<tr>
<th>Boundary</th>
<th>h (W/m² K)</th>
<th>Detailed Model</th>
<th>DELPHI Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top Boundary</td>
<td>100</td>
<td>X</td>
<td>1.000X</td>
</tr>
<tr>
<td></td>
<td>10000</td>
<td>X</td>
<td>1.000X</td>
</tr>
<tr>
<td>Bottom Boundary</td>
<td>100 (kₑ = 0.78)</td>
<td>X</td>
<td>0.995X</td>
</tr>
<tr>
<td></td>
<td>100 (kₑ = 9.6)</td>
<td>X</td>
<td>1.009X</td>
</tr>
</tbody>
</table>

Table 1-14: Comparison between the Detailed Model and Different DELPHI Model for XCVU13P-FIGD2104, XCVU13P-FSGA2577, XCVU27P-FIGD2104, XCVU27P-FSGA2577, XCVU29P-FIGD2104, and XCVU29P-FSGA2577

<table>
<thead>
<tr>
<th>Boundary</th>
<th>h (W/m² K)</th>
<th>Detailed Model</th>
<th>DELPHI Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top Boundary</td>
<td>100</td>
<td>X</td>
<td>1.000X</td>
</tr>
<tr>
<td></td>
<td>10000</td>
<td>X</td>
<td>0.929X</td>
</tr>
</tbody>
</table>
Table 1-14: Comparison between the Detailed Model and Different DELPHI Model for XCVU13P-FIGD2104, XCVU13P-FSGA2577, XCVU27P-FIGD2104, XCVU27P-FSGA2577, XCVU29P-FIGD2104, and XCVU29P-FSGA2577

<table>
<thead>
<tr>
<th>Boundary</th>
<th>h (W/m² K)</th>
<th>Detailed Model</th>
<th>DELPHI Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bottom Boundary</td>
<td>100 (kₑ = 0.78)</td>
<td>X</td>
<td>1.040X</td>
</tr>
<tr>
<td></td>
<td>100 (kₑ = 9.6)</td>
<td>X</td>
<td>1.054X</td>
</tr>
</tbody>
</table>

Table 1-15: Comparison between the Simplified Model and Detailed Model for XCVU31P-FSVH1924

<table>
<thead>
<tr>
<th>Boundary</th>
<th>h (W/m² K)</th>
<th>Detailed Model T_ J</th>
<th>Simplified Model T_ J</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top Boundary</td>
<td>100</td>
<td>X</td>
<td>1.0178X</td>
</tr>
<tr>
<td></td>
<td>10000</td>
<td>X</td>
<td>0.9860X</td>
</tr>
<tr>
<td>Bottom Boundary</td>
<td>100 (kₑ = 0.78)</td>
<td>X</td>
<td>1.0144X</td>
</tr>
<tr>
<td></td>
<td>100 (kₑ = 9.6)</td>
<td>X</td>
<td>1.0310X</td>
</tr>
</tbody>
</table>

Table 1-16: Comparison between the Simplified Model and Detailed Model for XCVU33P-FSVH2104

<table>
<thead>
<tr>
<th>Boundary</th>
<th>h (W/m² K)</th>
<th>Detailed Model T_ J</th>
<th>Simplified Model T_ J</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top Boundary</td>
<td>100</td>
<td>X</td>
<td>1.0126X</td>
</tr>
<tr>
<td></td>
<td>10000</td>
<td>X</td>
<td>0.9600X</td>
</tr>
<tr>
<td>Bottom Boundary</td>
<td>100 (kₑ = 0.78)</td>
<td>X</td>
<td>1.0106X</td>
</tr>
<tr>
<td></td>
<td>100 (kₑ = 9.6)</td>
<td>X</td>
<td>1.0297X</td>
</tr>
</tbody>
</table>

Table 1-17: Comparison between the Simplified Model and Detailed Model for XCVU35P-FSVH2104

<table>
<thead>
<tr>
<th>Boundary</th>
<th>h (W/m² K)</th>
<th>Detailed Model T_ J</th>
<th>Simplified Model T_ J</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top Boundary</td>
<td>100</td>
<td>X</td>
<td>1.0114X</td>
</tr>
<tr>
<td></td>
<td>10000</td>
<td>X</td>
<td>0.9890X</td>
</tr>
<tr>
<td>Bottom Boundary</td>
<td>100 (kₑ = 0.78)</td>
<td>X</td>
<td>1.0083X</td>
</tr>
<tr>
<td></td>
<td>100 (kₑ = 9.6)</td>
<td>X</td>
<td>1.0245X</td>
</tr>
</tbody>
</table>

Table 1-18: Comparison between the Simplified Model and Detailed Model for XCVU35P-FSVH2892

<table>
<thead>
<tr>
<th>Boundary</th>
<th>h (W/m² K)</th>
<th>Detailed Model T_ J</th>
<th>Simplified Model T_ J</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top Boundary</td>
<td>100</td>
<td>X</td>
<td>1.0103X</td>
</tr>
<tr>
<td></td>
<td>10000</td>
<td>X</td>
<td>0.9860X</td>
</tr>
<tr>
<td>Bottom Boundary</td>
<td>100 (kₑ = 0.78)</td>
<td>X</td>
<td>1.0126X</td>
</tr>
<tr>
<td></td>
<td>100 (kₑ = 9.6)</td>
<td>X</td>
<td>1.0314X</td>
</tr>
</tbody>
</table>
Table 1-19: Comparison between the Simplified Model and Detailed Model for XCVU37P-FSVH2892

<table>
<thead>
<tr>
<th>Boundary</th>
<th>h (W/m² K)</th>
<th>Detailed Model T_J</th>
<th>Simplified Model T_J</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top Boundary</td>
<td>100</td>
<td>X</td>
<td>1.0100X</td>
</tr>
<tr>
<td></td>
<td>10000</td>
<td>X</td>
<td>0.9820X</td>
</tr>
<tr>
<td>Bottom Boundary</td>
<td>100 (k_e = 0.78)</td>
<td>X</td>
<td>1.0086X</td>
</tr>
<tr>
<td></td>
<td>100 (k_e = 9.6)</td>
<td>X</td>
<td>1.0242X</td>
</tr>
</tbody>
</table>

Table 1-20: Comparison between the Detailed Model and DELPHI Model for XCZU25DR-FSVE1156, XCZU27DR-FSVE1156, and XCZU28DR-FSVE1156

<table>
<thead>
<tr>
<th>Boundary</th>
<th>h (W/m² K)</th>
<th>Detailed Model T_J</th>
<th>Detailed Model T_J</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top Boundary</td>
<td>100</td>
<td>X</td>
<td>1.0002X</td>
</tr>
<tr>
<td></td>
<td>10000</td>
<td>X</td>
<td>0.9948X</td>
</tr>
<tr>
<td>Bottom Boundary</td>
<td>100 (k_e = 0.78)</td>
<td>X</td>
<td>0.9938X</td>
</tr>
<tr>
<td></td>
<td>100 (k_e = 9.6)</td>
<td>X</td>
<td>0.9944X</td>
</tr>
</tbody>
</table>

Table 1-21: Comparison between the Detailed Model and DELPHI Model for XCZU25DR-FSVG1517, XCZU27DR-FSVG1517, and XCZU28DR-FSVG1517

<table>
<thead>
<tr>
<th>Boundary</th>
<th>h (W/m² K)</th>
<th>Detailed Model T_J</th>
<th>Detailed Model T_J</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top Boundary</td>
<td>100</td>
<td>X</td>
<td>0.9998X</td>
</tr>
<tr>
<td></td>
<td>10000</td>
<td>X</td>
<td>0.9974X</td>
</tr>
<tr>
<td>Bottom Boundary</td>
<td>100 (k_e = 0.78)</td>
<td>X</td>
<td>0.9867X</td>
</tr>
<tr>
<td></td>
<td>100 (k_e = 9.6)</td>
<td>X</td>
<td>0.9846X</td>
</tr>
</tbody>
</table>

Table 1-22: Comparison between the Detailed Model and DELPHI Model for XCZU29DR-FSVF1760

<table>
<thead>
<tr>
<th>Boundary</th>
<th>h (W/m² K)</th>
<th>Detailed Model T_J</th>
<th>Detailed Model T_J</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top Boundary</td>
<td>100</td>
<td>X</td>
<td>1.0003X</td>
</tr>
<tr>
<td></td>
<td>10000</td>
<td>X</td>
<td>0.9948X</td>
</tr>
<tr>
<td>Bottom Boundary</td>
<td>100 (k_e = 0.78)</td>
<td>X</td>
<td>0.9762X</td>
</tr>
<tr>
<td></td>
<td>100 (k_e = 9.6)</td>
<td>X</td>
<td>0.9881X</td>
</tr>
</tbody>
</table>
Example Heat Sink Thermal Performance

Figure 1-33 through Figure 1-35 present graphical data extracted from experiments done using the detailed thermal model with the VU13P-FIGD2104.

The graph data in Figure 1-34 and Figure 1-35 was extracted from thermal simulations using the VU13P-FIGD2104 package models with the heat sink solution shown above for a 150 Watt FPGA design. Using the first graph on the left in Figure 1-34, with an air flow rate of 30 CFM, you can calculate an effective thermal resistance of ~0.23°C/Watt. Using the second graph (Figure 1-34, on the right), the thermal solution operating at that airflow measures (at SYSMON) approximately 35°C above ambient, implying that the maximum ambient under these conditions can be as high as 65°C. Using an equivalent lidded package like the B2104 would yield a maximum ambient temperature of 58°C (7°C lower), as shown in the experiment data in Figure 1-35.
**Chapter 1: Mechanical and Thermal Design Guidelines**

**Figure 1-34:** 150W Design

**Figure 1-35:** Experimental Comparison between Lid and Lidless Devices
The following pad recommendations are listed in the *Recommended PCB Design Rules for BGA Packages* chapter of *UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification User Guide* (UG575) [Ref 1] and *Zynq UltraScale+ MPSoC Packaging and Pinouts Product Specification User Guide* (UG1075) [Ref 2], as appropriate.

- PCB Pad Recommendations
- Pad Type Recommendations
- Solder Pad Recommendation

### Removing Heat Sink Phase Change Material

If heat sinks are removed or reworked, the phase change material residue must be removed from the die surface. Laird Technologies, Inc. has provided the following guidance for complete removal of the phase change material from the component.

**Instructions:**

1. **Separate the Components**
2. **Clean Remaining Residue with Solvent**
3. **Working with Laird Material**

#### Separate the Components

At room temperature, use a back and forth twisting motion to break the bond between the phase change TIM and mated components (i.e., heat sink and CPU). See Figure 1-36.

![Figure 1-36: Breaking the Bond between TIM and Mated Components](image)
For smaller components (typically 15mm x 15mm or less), the bond usually breaks free easily at room temperature. For larger components, situations where minimal movement is available, or if using fragile components, heat the component (preferable) or heat sink to between 40°C and 60°C before removal.

While the guideline is between 40°C and 60°C, you might find that heating to 35°C is adequate. Others might prefer to heat to 70°C so that the phase change TIM is very soft and the components are easy to separate.

**Clean Remaining Residue with Solvent**

Using a clean cloth/wipe, wet it with one of the solvents below and wipe away any remaining residue.

- Toluene (best)
- Acetone (very good)
- Isoparaffinic hydrocarbon (trade names Isopar and Soltrol) (very good)
- Isopropyl alcohol (OK)

**Working with Laird Material**

Safe handling, disposal, and first-aid measures for working with phase-change material are included in the Laird Technologies material safety data sheet (MSDS). Read the MSDS before using or handling. See the Laird Technologies, Inc. website, [www.lairdtech.com](http://www.lairdtech.com).

---

**Measurement Debug**

When performing in-system thermal testing, to ensure accurate data and not incur damage to the device, do not place a thermocouple in between the die and the heat sink. On the extreme side, it might cause additional mechanical and/or thermal stress to the die, leading to damage. Even if damage does not occur, it often leads to thicker and or uneven TIM thickness, leading to different thermal performance from a system without the thermocouple. To obtain the device temperature, use System Monitor (SYSMON) because it is a non-invasive means to get accurate die measurements while debugging the system.

---

**Reference Design Files**

Download the [reference design files](http://www.xilinx.com) for this application note from the Xilinx website.
Conclusion

This application note addresses the specific mechanical and thermal design requirements of the device and package combinations listed in Table 1-1. Further information on removing a heat sink, including removal of phase change material, is available in the UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification User Guide (UG575) [Ref 1] and Zynq UltraScale+ MPSoC Packaging and Pinouts Product Specification User Guide (UG1075) [Ref 2], as appropriate.
Appendix A

Recommended Thermal Solution Installation of Xilinx FCBGA Lidless Packages

Overview

This appendix presents the recommended installation procedure for the Xilinx FCBGA lidless packages. These devices are capable of generating high power and thus large amounts of heat, so a thermal solution (cooler) is required to dissipate the energy to keep the device working within the specific operating temperature limits. Attaching the cooler to the device with fasteners can be a challenge while not damaging the silicon.

Challenges

To achieve the best thermal conductivity, the interface between the silicon and cooler must have very good contact. Due to inevitable mechanical limitations, the two surfaces are not perfectly flat or smooth and a Thermal Interface Material (TIM) is typically applied to fill any imperfections.

The TIM grain size must be smaller than the gaps so it is only filling the voids and not creating a thick bond line between the two devices. A certain pressure is required to hold the two devices together, maintaining minimum bond line and not damaging the silicon. This pressure is usually provided by the device manufacturer.

The device should be attached to the thermal solution by mechanical fasteners. The installation process has to be well designed so that the pressure is evenly distributed over the silicon surface and the two surfaces are parallel with a specific pressure. The TIM is evenly spread filling the voids and maintaining the minimum bond line.
Appendix A: Recommended Thermal Solution Installation of Xilinx FCBGA Lidless

Installation Control

The assembly floor should have similar tools as listed here to ensure that the thermal solution is appropriately assembled on the top of the FCBGA.

Equipment and Calibration

The equipment used for the mechanical installation process are:

- Adjustable torque screwdriver (Figure A-1) and calibrator (Figure A-2)
- Tekscan FlexiForce A201 pressure gauge with multiple handle ELF system (Figure A-3)
- Tactilus free form square pressure sensors (Figure A-4)

Figure A-1: Digital Torque Screwdriver (Top) and Hios CL 2000 (Bottom)
Appendix A: Recommended Thermal Solution Installation of Xilinx FCBGA Lidless

Figure A-2: Screw Torque Calibrator – Hios HP-10

Figure A-3: Pressure Gauge – Tekscan FlexiForce A201 Multiple Handle ELF System
Appendix A: Recommended Thermal Solution Installation of Xilinx FCBGA Lidless

Figure A-4: Pressure Sensor – Tactilus Free Form Square Sensors

Figure A-5: Tekscan Pressure Sensor – Zoomed In
Set Up and Calibration

The torque of the screwdriver is calibrated by the calibrator and set to the torque (calculated based on the required pressure, die surface area) using the digital torque meter. For guidelines on pressure recommendations, see Heat Sink Pressure.

Note: Calibration of the digital torque calibrator/meter is done annually.

Process Qualification

Pressure and Force Verification

The screw-spring has to be designed with the required force that can achieve the target pressure at the interface between the die surface and the cooler. For example:

- Chosen target pressure = 32 psi (between 20 and 50 psi)
- Die size = 0.5 inch by 0.5 inch
- Target force = 32 psi × 0.5 inch × 0.5 inch = 8 lbf

Installation Verification

Use the exact FCBGA, PCB, and thermal solution with the screws verified in the previous section. Install and verify if the target is achieved.

Figure A-6 shows the FCBGA board layouts.
The target force can be reproduced and the force exerted on the die surface is close to the target of 32 psi.

**Installation Process**

There are different approaches to assemble the heat thermal solution on the FCBGA. This depends on the type of mechanical attachment. The following examples illustrate how the screws affect the thermal solution from either the back side of the board or the front side of the board.
Appendix A: Recommended Thermal Solution Installation of Xilinx FCBGA Lidless

Heat Sink Assembly for Dynamic Back Side Mounting

This example is given based on the PCIe card, which has the following items:

- Board back plate (Figure A-8)
- PCIe component (Figure A-9)
- Active heat sink (Figure A-10)

Figure A-8: Board Back Plate
Appendix A: Recommended Thermal Solution Installation of Xilinx FCBGA Lidless

Figure A-9: PCIe Card

Figure A-10: Active Heat Sink Assembly

Figure A-11 shows a flowchart of the heat sink assembly.
Appendix A: Recommended Thermal Solution Installation of Xilinx FCBGA Lidless

Figure A-11: Flowchart of the Heat Sink Assembly
Appendix A: Recommended Thermal Solution Installation of Xilinx FCBGA Lidless

The following details the assembly procedure for the heat sink. Before you begin, Figure A-12 shows a jig template which is critical for smooth and faster alignment during assembly.

*Figure A-12: Jig Template*
Appendix A: Recommended Thermal Solution Installation of Xilinx FCBGA Lidless

1. Place the active heat sink into position of the jig with contact surface facing up.

![Active Heat Sink in Jig](image1)

*Figure A-13: Active Heat Sink in Jig*

2. Position the PCIe card and back plate on the top of the heat sink. This placement is aligned using the jig.

![PCIe Card with Back Plate in Jig](image2)

*Figure A-14: PCIe Card with Back Plate in Jig*
3. Lightly fasten the four screws numbered. Use the preset torque screwdriver to tighten screws in the number sequence to finish assembly.

*Figure A-15: Screw Sequence for Final Assembly*
4. The assembly is complete.

*Figure A-16: Assembly Completed*

**Heat Sink Assembly for Dynamic Top Side Mounting of Lidless Unit**

The following components are used for this heat sink assembly:

- Heat sink and back clip (*Figure A-17*)
- PCB board (*Figure A-18*)
Appendix A: Recommended Thermal Solution Installation of Xilinx FCBGA Lidless

Figure A-17: Heat Sink and Back Clip

Figure A-18: PCB Board
Figure A-19 shows a flowchart of the heat sink assembly for a lidless unit.

Figure A-19: Flowchart of the Heat Sink Assembly
The following details the assembly procedure for the heat sink. Before you begin, Figure A-20 shows a jig template which can be used during assembly.

Figure A-20: Jig Template

1. Place the heat sink back clip into the defined position of the jig template.

Figure A-21: Heat Sink in Jig
2. Position the test board with the lidless unit on top of the heat sink back clip into the defined position of the jig template.

![Figure A-22: Test Board and Lidless Unit in Jig](image)

3. Place the heat sink on top of the lidless unit on the board. Align to the screw holes (highlighted in red) of the back clip.

![Figure A-23: Screw Locations for Heat Sink and Lidless Unit in Jig](image)
Appendix A: Recommended Thermal Solution Installation of Xilinx FCBGA Lidless

4. Lightly fasten the screws to hold the clip. Use the preset screwdriver to tighten the four screws of the heat sink in the following sequence to finish assembly.

![Figure A-24: Heat Sink and Lidless Unit in Jig](image)

![Figure A-25: Screw Sequence for Final Assembly](image)
Appendix A: Recommended Thermal Solution Installation of Xilinx FCBGA Lidless

**Heat Sink Assembly for Dynamic Bottom Side Mounting of Wireless Heat Sink**

The following components are used for this heat sink assembly:

- Lidless unit on board (Figure A-26)
- Cu block with pedestal (Figure A-27)
- Heat sink for wireless application (Figure A-28)

*Figure A-26: Lidless Unit on Board*

*Figure A-27: Cu Block with Pedestal – Bottom Side and Top Side*
Figure A-29 shows a flowchart of the heat sink assembly for a wireless application.

1. **Heat sink assembly for wireless.**
2. Acquire components: Cu block, PCB board, and heat sink.
3. Place Cu block into the jig template.
4. Position PCB board into the jig and align with Cu block screw holes.
5. Fasten and tighten screws with appropriate torque to attach Cu block.
6. Place assembled board with Cu block into jig on top of heat sink and align.
7. Fasten and tighten screws with the appropriate torque to attach heat sink.
8. **Assembly completed.**

Figure A-29: Flowchart of the Heat Sink Assembly
The following details the assembly procedure for the heat sink. Before you begin, Figure A-30 and Figure A-31 show the jig templates that can be used during assembly.

![Figure A-30: Jig Template for Cu Block with Pedestal](image)

![Figure A-31: Jig Template for Wireless Heat Sink and Board](image)
1. Apply thermal interface material to the Cu block pedestal.

   ![Thermal Interface Material to Cu Block Pedestal](image1)

   *Figure A-32: Thermal Interface Material to Cu Block Pedestal*

2. Place Cu block into the defined location of the jig template.

   ![Cu Block in Jig](image2)

   *Figure A-33: Cu Block in Jig*

3. Flip over and position board on top of the Cu block in the jig and align to screw holes (highlighted in red) of Cu block.

   ![Screw Locations for Cu Block on Board](image3)

   *Figure A-34: Screw Locations for Cu Block on Board*
4. Rotate the screws for a couple turns to hold the board in place. Use the preset screwdriver to tighten the four screws of the heat sink in the sequence as shown.

Figure A-35: Screw Sequence for Board

5. Finish assembled board with the Cu block.

Figure A-36: Assembled Board with Cu Block
6. Place heat sink into the defined location of the jig.

![Heat Sink in Jig](image)

*Figure A-37: Heat Sink in Jig*

7. Assemble board with the Cu block on top of the heat sink. Align to screw holes (highlighted in red) of the heat sink.

![Screw Locations for Cu Block on Heat Sink](image)

*Figure A-38: Screw Locations for Cu Block on Heat Sink*
8. Fasten screws in the appropriate sequence to finish assembly

Figure A-39: Screw Sequence for Final Assembly
Appendix B

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select Help > Documentation and Tutorials.
- On Windows, select Start > All Programs > Xilinx Design Tools > DocNav.
- At the Linux command prompt, enter docnav.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the Design Hubs View tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.
Appendix B: Additional Resources and Legal Notices

References

For additional information on heat management and contact information:

3. Virtex UltraScale+ FPGA Package Thermal Models (Xilinx support)

Refer to the following websites for CFD tools supported by Xilinx with thermal models:

1. Mentor (FloTHERM)
2. ANSYS (IcePak)

Refer to the following papers on thermal modeling:

Please Read: Important Legal Notices

The information disclosed to you hereunder (the “Materials”) is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available “AS IS” and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx’s limited warranty, please refer to Xilinx’s Terms of Sale which can be viewed at https://www.xilinx.com/legal.htm#tos; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx’s Terms of Sale which can be viewed at https://www.xilinx.com/legal.htm#tos.

AUTOMOTIVE APPLICATIONS DISCLAIMER

AUTOMOTIVE PRODUCTS (IDENTIFIED AS “XA” IN THE PART NUMBER) ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS OR FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE (“SAFETY APPLICATION”) UNLESS THERE IS A SAFETY CONCEPT OR REDUNDANCY FEATURE CONSISTENT WITH THE ISO 26262 AUTOMOTIVE SAFETY STANDARD (“SAFETY DESIGN”). CUSTOMER SHALL, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE PRODUCTS, THOROUGHLY TEST SUCH SYSTEMS FOR SAFETY PURPOSES. USE OF PRODUCTS IN A SAFETY APPLICATION WITHOUT A SAFETY DESIGN IS FULLY AT THE RISK OF CUSTOMER, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.

© Copyright 2017–2019 Xilinx, Inc. Xilinx, the Xilinx logo, Artix, ISE, Kintex, Spartan, Virtex, Vivado, Zynq, and other designated brands included herein are trademarks of Xilinx in the United States and other countries. All other trademarks are the property of their respective owners.