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# Horizontal Synchronization Locking System for Video Applications

Author: David Taylor, Vincent Vendramini, and Robert Green

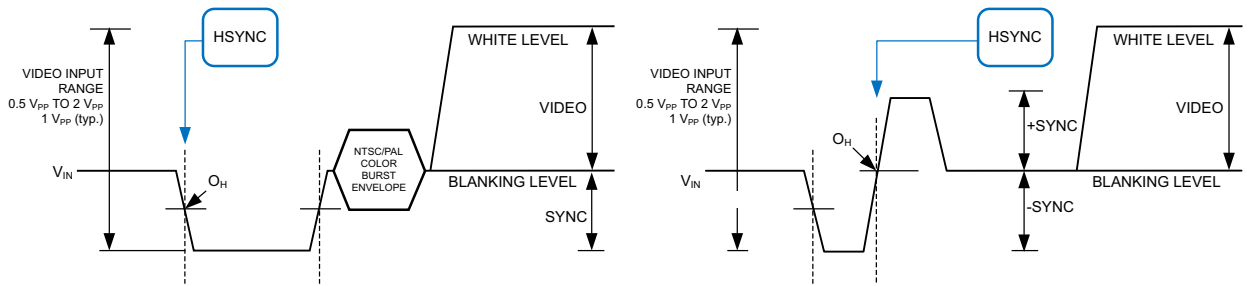
## Summary

This application note describes a technique using Xilinx® devices and phase interpolator controlled crystal oscillator (PICXO) that removes the external PLL circuitry to allow SDI video outputs to be synchronized to an input HSYNC clock. This simplifies external PCB design and lowers costs by reducing external FPGA components, and enables a scalable approach to support multiple channel designs, particularly useful in switchers and routers that must support hundreds of channels. The reference design files and method described here provide a clocking system that can be integrated into the user's application or Xilinx SDI IP cores as a further design exercise, rather than a complete implemented SDI subsystem.

Download the [reference design files](#) for this application note from the Xilinx website. For detailed information about the design files, see [Reference Design](#).

## Introduction to HSYNC in Modern Video Applications

Video is transitioning to digital formats supporting up to 8K ultra high-definition (7680 x 4320 pixels), offering faster frame rates with 120 frames per second for sharper images and higher dynamic range (HDR) for more natural visual presentation. However, the creation, production, and delivery of content uses a large aggregate of legacy technologies from the analog video world that must still be supported, such as interlaced video and non-integer frame rates, despite the increasing demand for progressive-only LCD and OLED displays. An area where the transition to fully digital capability is yet to happen is in timing and synchronization of video and audio signals. Despite the emergence of new synchronization techniques based on the IEEE 1588 precision time protocol (PTP), there still remains a requirement for modern equipment to support genlock, where various sources such as cameras are synchronized in a production switcher or mixer to enable seamless transitions between multiple sources. Furthermore, there is a need to extract synchronization signals for the video and audio signals so downstream processing can act appropriately to resynchronize streams after processing. Horizontal synchronization (HSYNC) is one of these synchronization signals. The HSYNC signal is used to cue monitors that a new line of pixels should be created on the screen, and in an HD frame there are 1080 HSYNC signals, one for each line of active video in the frame. There are similar synchronization signals for start of frame and field. The HSYNC signal is provided at the front of the active video data, shown in [Figure 1](#).

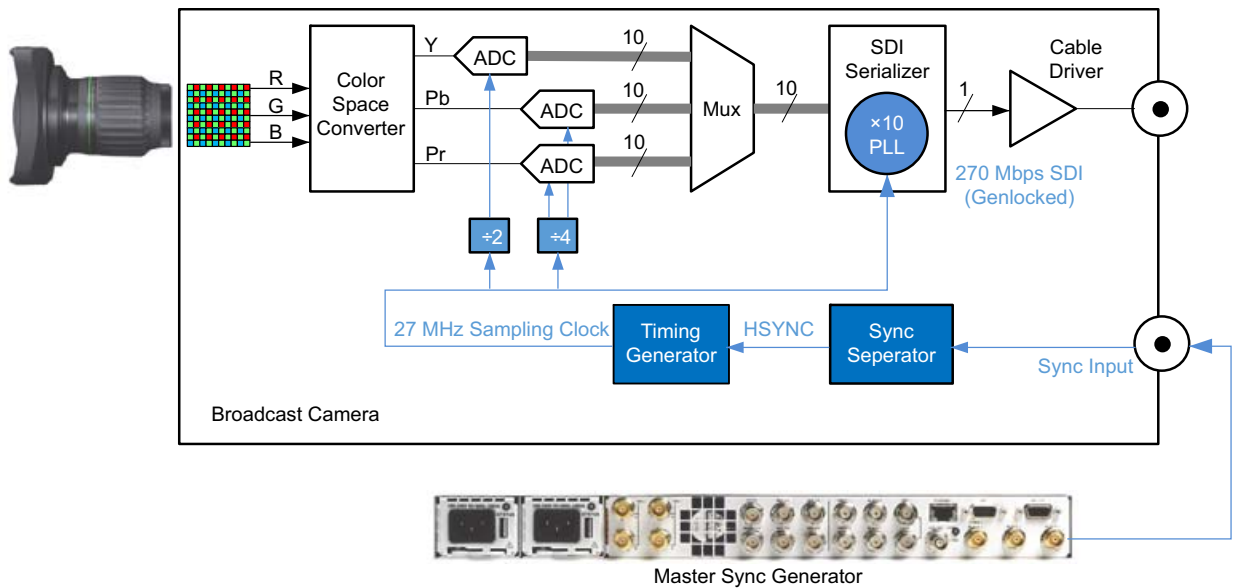


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Figure 1: HSYNC at the Start of Each Line of Active Video

1. (Left: bi-level standard definition and enhanced definition; Right: tri-level high definition)

HSYNC is also used as a more general synchronization pulse for genlocking, where it generates the sampling clock for a serial digital interface (SDI) stream so that the SDI output is synchronized to the master sync generator in the studio (which other equipment in the studio can also be synchronized to) as shown in Figure 2.



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Figure 2: HSYNC in Synchronization of Camera SDI Output to the Studio Master Synchronization

Typically, a video sync separator such as the TI LMH1981 handles the generation of HSYNC, vertical synchronization (VSYNC), composite and other timing signals from incoming bi-level or tri-level sync from analog SD and HD video but requires a PLL-based jitter cleaning circuit on the output so that the jitter is not passed through to the SDI reference clocks on the output of the application, thereby degrading performance. The PICXO-based reference design effectively removes the need for this external PLL circuitry to clean up HSYNC jitter. Or it can be used to recover an HSYNC signal directly from an input source and use it to apply a clean reference clock to genlock SDI video outputs.

## Clocking Architecture Analysis

The requirement to lock an arbitrary SDI output of any rate to an external HSYNC pulse requires the following features to be available for the fabric digital PLLs (DPLLs):

- A fractional pre-scaler circuit to enable both 148.5 MHz and 148.5/1.001 MHz to be locked to any HSYNC reference clock
- A DPLL to be able to clean jitter from a SYNC separator device output chip with typically many nanoseconds (ns) of jitter



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**TIP:** *The PICXO circuit uses the clock rising edge as its reference. Many SYNC separator devices reference the falling edge so the SYNC input logic must be inverted before being applied to the circuit.*

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- Ability to have a high multiplication ratio because HSYNC rates are in the kHz range – 560i PAL being 15.625 kHz giving a multiplication to 12G-SDI of 760,320
- Provision for fast locking – dynamic bandwidth setting facility to improve lock times in low bandwidth systems
- Compliant with Society of Motion Picture & Television Engineers (SMPTE) jitter specifications – using DPLLs that are capable of the phase resolution accuracy required to meet both alignment and timing jitter requirements

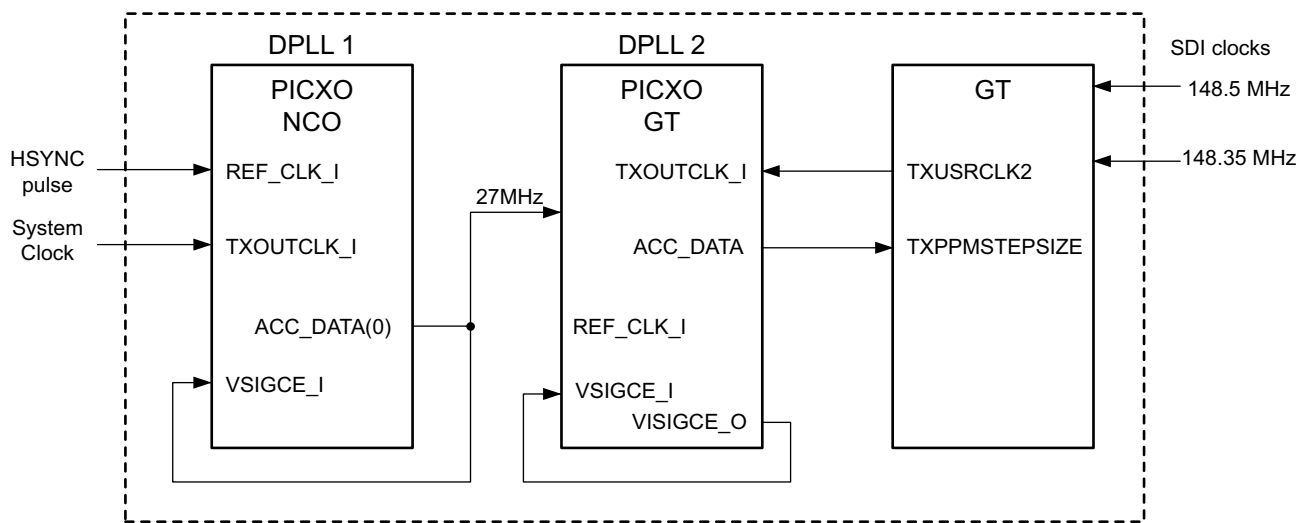
To meet these diverse requirements, a two-step DPLL implementation is used in this application note.

The first stage is a DPLL based on a numerically controlled oscillator (NCO) that up converts the input HSYNC clock to an on-chip 27 MHz clock. The DPLL multiplication ratio is determined by the video standard being used as the reference. All HSYNC rates can be multiplied to 27 MHz with an integer multiplier.

The second stage is a standard PICXO-based DPLL with the addition of a fractional pre-scaler to allow both 148.5 MHz and 148.5/1.001 MHz rates to lock to the internal 27 MHz derived clock. See the *All Digital VCXO Replacement for Gigabit Transceiver Applications (UltraScale FPGAs) Application Note [Ref 4]* and the *All Digital VCXO Replacement for Gigabit Transceiver Applications (7 Series/Zynq-7000) Application Note [Ref 5]* for more information.

To facilitate implementation, both DPLLs use the same PICXO-base source code; in the NCO (NO\_GT) implementation the circuit is configured to run standalone without connecting to a transceiver.

Figure 3 shows the basic two-step architecture of the system.



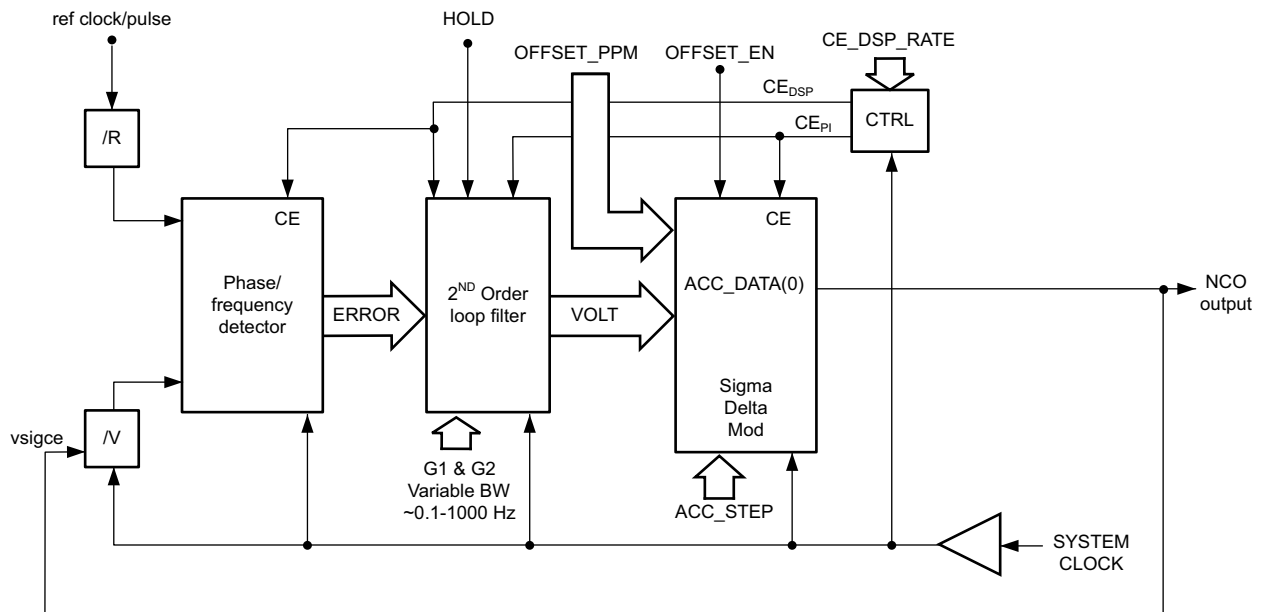
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Figure 3: Basic HSYNC Locking Architecture

As shown in Figure 3, DPLL 1 provides the first stage step up and jitter cleaning; DPLL 2 provides the second stage multiplication with further jitter cleaning to the SDI line rates and has the fractional capability to pre-scale the SDI line rate by 5.5 or 5.45, depending on the required output standard.

## NCO Implementation

The NCO implementation (NO\_GT) is shown in Figure 4, where the PICXO design instantiated is not related to a GT block. Instead, it forms a standalone DPLL capable of generating a clock enabled at a rate determined by the  $R$  and  $V$  dividers in the wrapper. The design goal is to provide the same flexibility and performance as the existing PICXO while having the scalability to operate over a wide frequency range without needing to use a GT block directly.



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Figure 4: NCO Mode PICXO Architecture

The NCO function is performed by using the Sigma Delta output to drive the  $V$  divider clock enable. The Sigma Delta output is a pulse stream whose duty cycle is directly controlled by the VOLT output on the DPLL. That is, when the VOLT output is 0:

- The Sigma Delta output is 0
- The  $V$  dividers are never enabled
- 0 Hz is applied to the phase frequency detector (PFD)

When the VOLT output is at maximum, the  $V$  divider is continuously enabled meaning the frequency applied to the PFD is the system clock frequency divided by  $V$ .

When the system is in lock, the DPLL maintains the NCO output rate equal to the PFD compare frequency multiplied by  $V$ . For this to occur, the theoretical minimum system clock frequency must be at a rate 2x the required output locked NCO clock because the maximum usable range of the NCO output is at 50% duty ratio.



**TIP:** It is recommended that the system clock be a minimum of 4x the required NCO output rate to ensure reliable locking.

To aid the NCO system design and optimization, two options are provided. First, a simulation test bench is supplied with the NO\_GT PICXO design to exhibit locking and transient performance of the DPLL. Secondly, the frequency response estimator spreadsheet has a worksheet that can estimate the frequency response of the circuit with the user parameters.

Figure 5 shows a simulation of the NO\_GT circuit locking.

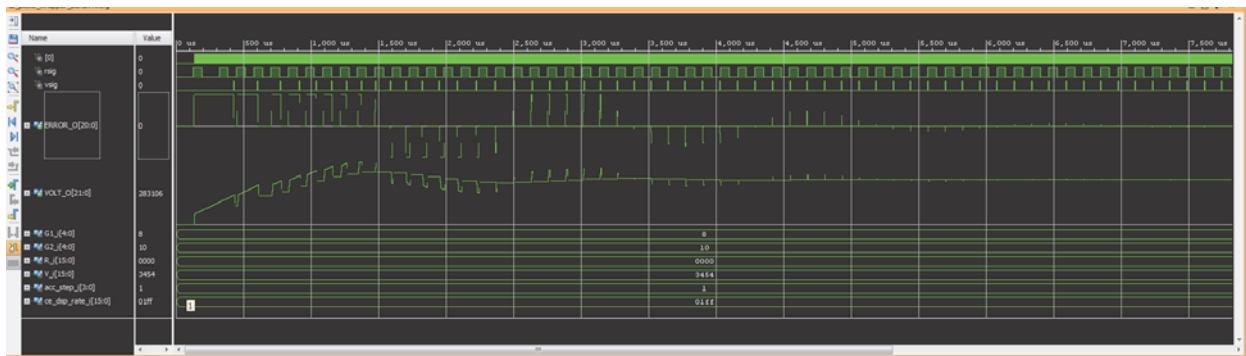


Figure 5: Simulation Waveforms of NCO Mode Circuit Locking

The `rsig` and `vsig` signals are at the phase detector input and exhibit the locking process where the DPLL frequency and phase aligns the NCO rate to the input HSYNC rate. In this example, the HSYNC input is 15.625 kHz.

Figure 6 show the detail of the phase alignment and the output clock enable using an average rate of 27 MHz.

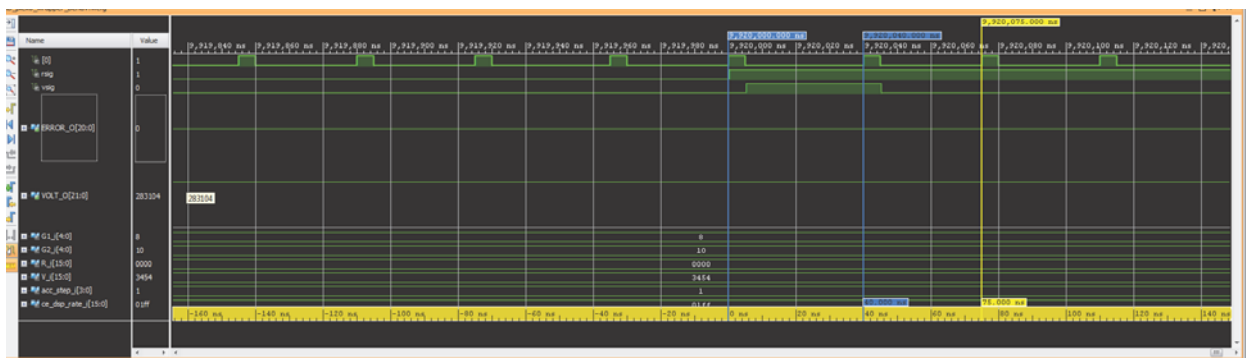


Figure 6: Simulation Waveforms of NCO Mode Phase Alignment

As the NO\_GT system is operated from a 200 MHz clock, the output 27 MHz clock averages at the exact lock rate with 5 ns jitter. The choice of system clock rate is important to ensure that the jitter generated by the NCO DPLL can be filtered by the downstream PICXO, therefore the frequency used for the system clock should be fast and unrelated to the generated 27 MHz. The theoretical minimum speed for the system clock is 2x the desired output rate. To allow headroom when the system is locking, it is recommended this minimum ratio be a factor of 4x.

## Fractional Division in the PICXO Architecture

The PICXO IP core requires minimal modifications to support video frequency synthesis fractional division. The changes from the PICXO architecture are highlighted in Figure 7 in red, and the new ports are described in Table 1.

First, the `V` divider must be modulated by adding a clock enable (`VSIGCE_I`) to this divider.

Secondly, the `TXOUTCLK_I` signal must be fractionally divided by adding a pre-scaler implemented by a dual-modulus counter.

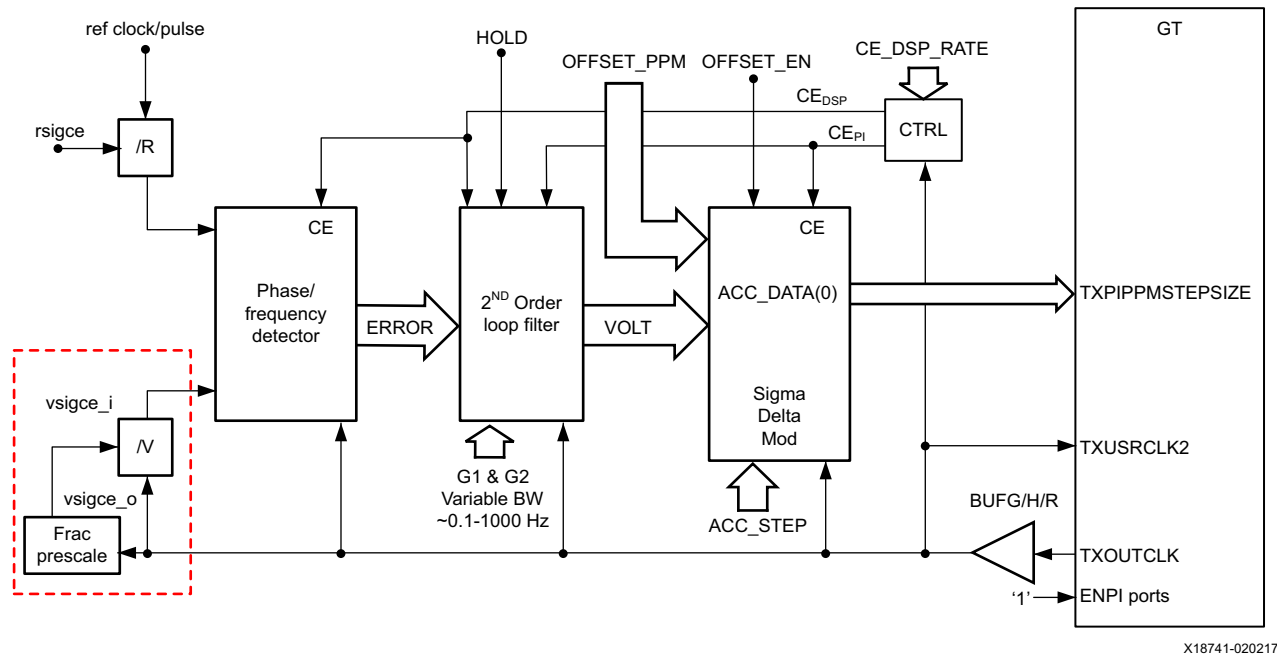


Figure 7: PICXO Architecture and Modifications to Support Fractional Division

Table 1: PICXO Loop Parameters

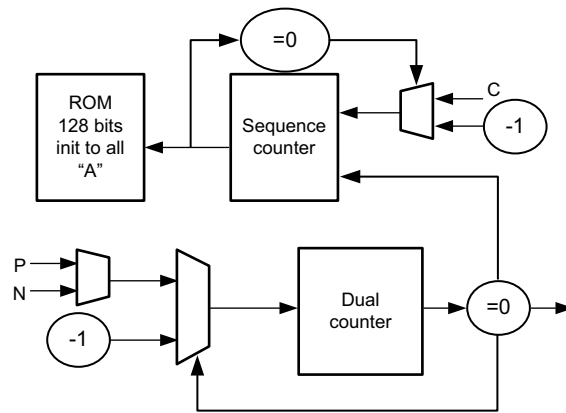
Signal Name	Directio	Description
VSIGCE_I	Input	Clock enable of the TXOUTCLK_I divider. Connects to 1 for normal operation.
VSIGCE_O	Output	Left unconnected for normal operation. For HSYNC mode, connects to VSIGCE_I (PICXO) and left floating.
C_I[7:0]	Input	Prescaler factor. (See Table 3 and Equation 1.)
P_I[9:0]	Input	Prescaler factor. (See Table 3 and Equation 1.)
N_I[9:0]	Input	Prescaler factor. (See Table 3 and Equation 1.)

The dual modulus counter architecture is represented in Figure 8. Inputs C\_I, N\_I, P\_I pre-scale the frequency with Equation 1.

$$\text{divide ratio} = ((N+1) * (\text{FLOOR}((C+1)/2,1)) + (P+1) * (\text{CEILING}((C+1)/2,1))) / (C+1) \quad \text{Equation 1}$$

where FLOOR and CELING represent MS Excel operators.

On reset, the sequence counter is loaded with C\_I and the dual counter is loaded with P or N, depending on the value of C. The dual counter counts down from P, then from N.



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Figure 8: Dual Modulus Counter

## Example Settings for NCO (NO\_GT PICXO)

Table 2 lists a range of possible settings that can be used in an HSYNC to SDI system. This frequency matrix describes the settings capable to generate a 27 MHz internal clock enable from a video HSYNC pulse.

Table 2: HSYNC to 27MHz NO\_GT Divider Settings

Standard	Frame Rate	Lines	HSYNC Freq	HSYNC-> 27 MHz	V'	R'	V - Hex	R	Compare (kHz)
480i (NTSC)	29.97003	525	15734.2657	1716/1	1716	1	D66	0	7.867
480p (NTSC)	59.9400599	525	31468.5315	858/1	858	1	6B2	0	15.734
576i (PAL)	25	625	15625	1728/1	1728	1	D7E	0	7.813
576p (PAL)	50	625	31250	864/1	864	1	6BE	0	15.625
720p 24	24	750	18000	1500/1	1500	1	BB6	0	9
720p 23.98	23.976024	750	17982.018	3003/2	3003	2	BB9	0	8.991
720p 25	25	750	18750	1440/1	1440	1	B3E	0	9.375
720p 30	30	750	22500	1200/1	1200	1	95E	0	11.25
720p 29.97	29.97003	750	22477.5225	6006/5	6006	5	1774	3	4.496
720p 50	50	750	37500	720/1	720	1	59E	0	18.75
720p 60	60	750	45000	600/1	600	1	4AE	0	22.5
720p 59.94	59.9400599	750	44955.045	3003/5	3003	5	BB9	3	8.991
1080i 50	25	1125	28125	960/1	960	1	77E	0	14.063
1080i 59.94	29.97003	1125	33716.2837	4004/5	4004	5	FA2	3	6.743
1080i 60	30	1125	33750	800/1	800	1	63E	0	16.875
1080p 24	24	1125	27000	1000/1	1000	1	7CE	0	13.5
1080p 23.98	23.976024	1125	26973.027	1001/1	1001	1	7D0	0	13.487
1080p 25	25	1125	28125	960/1	960	1	77E	0	14.063
1080p 30	30	1125	33750	800/1	800	1	63E	0	16.875
1080p 29.97	29.97003	1125	33716.2837	4004/5	4004	5	FA2	3	6.743



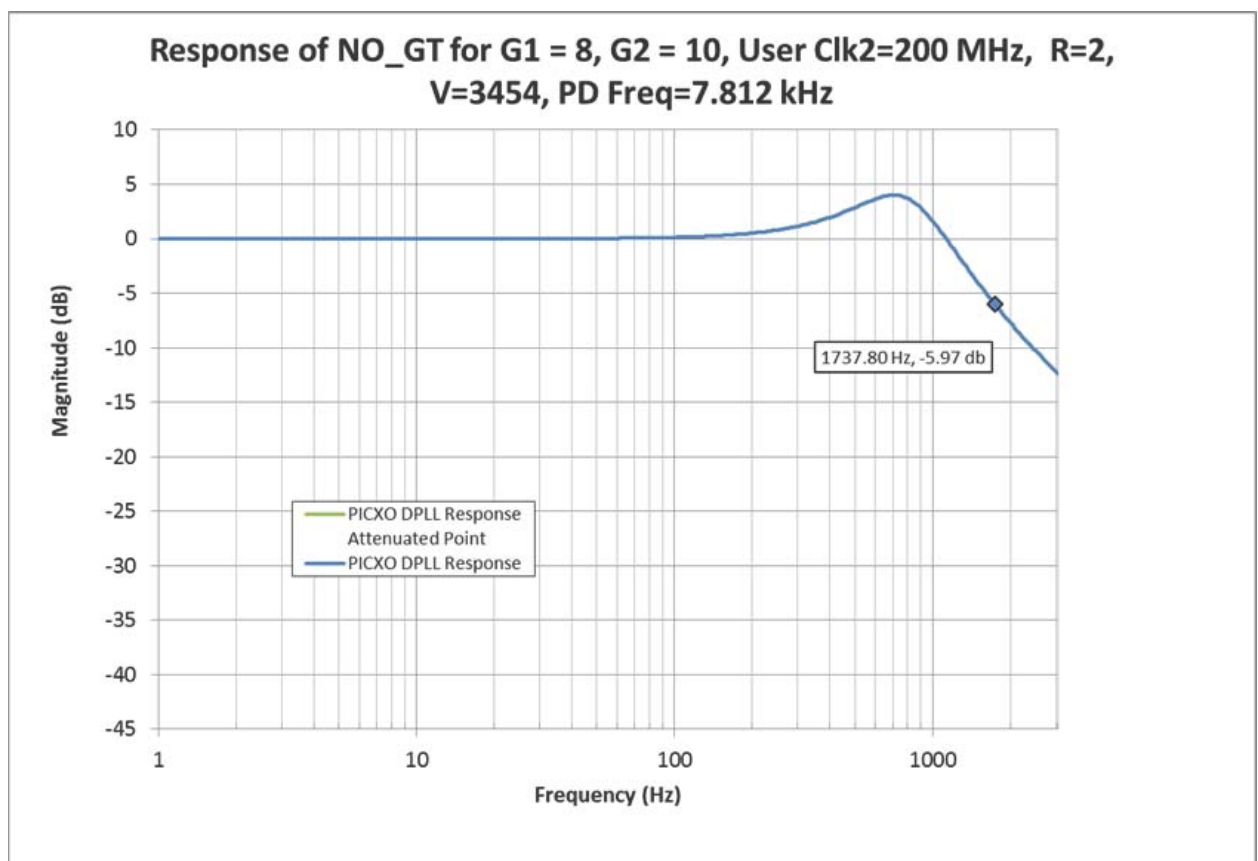
Table 2: HSYNC to 27MHz NO\_GT Divider Settings (Cont'd)

Standard	Frame Rate	Lines	HSYNC Freq	HSYNC-> 27 MHz	V'	R'	V - Hex	R	Compare (kHz)
1080p 50	50	1125	56250	480/1	480	1	3BE	0	28.125
1080p 59.94	59.9400599	1125	67432.5674	2002/5	2002	5	7D0	3	13.487
1080p 60	60	1125	67500	400/1	400	1	31E	0	33.75

The required ratio is listed in the **HSYNC > 27 MHz** column, and the **V'** and **R'** columns list the settings in hexadecimal that can be applied to the system. For reference, the phase detector compare rate is provided. Figure 9 shows the output from the frequency response estimator spread sheet using the settings from the simulation, where:

- G2=10d
- G1=8d
- CE\_DSP\_RATE=01FFh.

The estimator provides a guide for expected bandwidths in the system. The bandwidth and peak are user-defined and can be set based on requirements. If one gain setting is chosen for all HSYNC input settings, then stability should be verified for all NO\_GT PLL settings.



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Figure 9: Frequency Response

## Example Settings for Fractional Pre-scaler

The fractional pre-scaler is video specific and provides a clock enable to the V divider to effectively divide the TXOUT clock from the GT by an additional factor of 5.5 or 5.5/1.001. Use this feature when locking the SDI output to the 27 MHz generated by the NCO. The example is based on generating an SDI output signal using a 148.5 MHz clock. In this example, a pre-scale of divide by 5.5 is used so that the effective input rate to the V divider was 27 MHz. When generating an SDI output signal based on a 148.35 MHz clock, the pre-scale of divide by 5.5/1.001 is used; this means the is effective input clock to the V divider is also 27 MHz. The settings in [Table 3](#) are used.

**Table 3: Fractional Pre-scale Settings for SDI**

Pre-scale	P	N	C - decimal
5.5/1.000	4	5	89
5.5/1.001	4	5	90

The PICXO parameters can be set and the response estimated. See the *All Digital VCXO Replacement for Gigabit Transceiver Applications (UltraScale FPGAs) Application Note* [\[Ref 4\]](#) and the *All Digital VCXO Replacement for Gigabit Transceiver Applications (7 Series/Zynq-7000) Application Note* [\[Ref 5\]](#) for more information.

It is recommended the NO\_GT NCO DPLL be set with a faster loop bandwidth than the following PICXO GT DPLL so that the clock enable jitter can be filtered successfully on the output DPLL with its relatively low frequency response.

It is anticipated a typical system might have one NO\_GT NCO PLL providing a system 27 MHz to all the SDI output PICXO circuits, which can then generate the targeted SDI output rate independently. However, this does not prevent multiple NO\_GT NCO PLLs from being placed as required by the application.

## Clocking and Reset

Refer to the *All Digital VCXO Replacement for Gigabit Transceiver Applications (UltraScale FPGAs) Application Note* (XAPP589) [\[Ref 4\]](#) and the *All Digital VCXO Replacement for Gigabit Transceiver Applications (7 Series/Zynq-7000) Application Note* (XAPP1241) [\[Ref 5\]](#) for general information regarding PICXO reset and clocking.

The PICXO in NCO mode requires only one system clock as shown in [Figure 4](#).

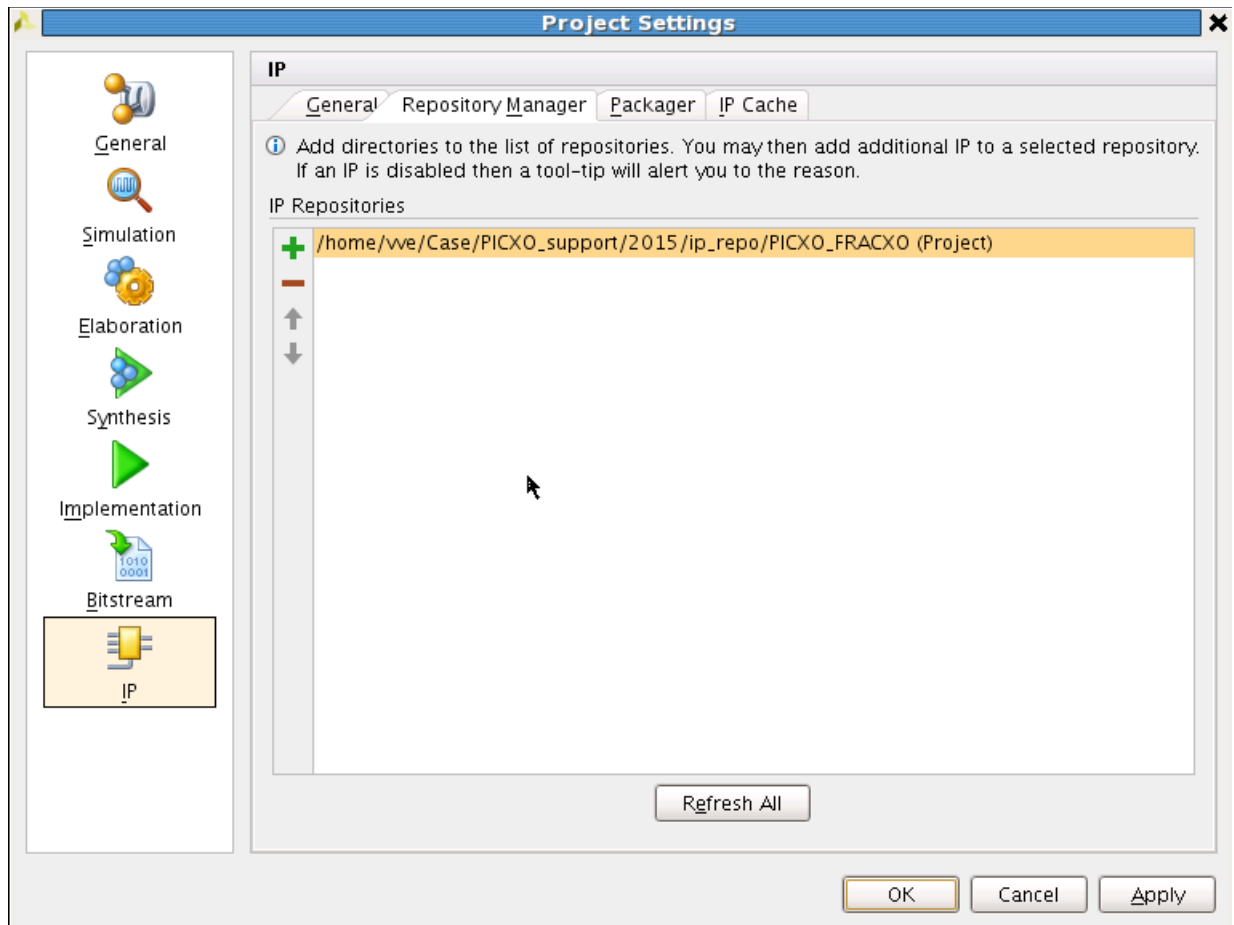
## Mandatory Conditions and Limitations

Refer to the *All Digital VCXO Replacement for Gigabit Transceiver Applications (UltraScale FPGAs) Application Note* (XAPP589) [\[Ref 4\]](#) and the *All Digital VCXO Replacement for Gigabit Transceiver Applications (7 Series/Zynq-7000) Application Note* (XAPP1241) [\[Ref 5\]](#) for conditions and limitations.

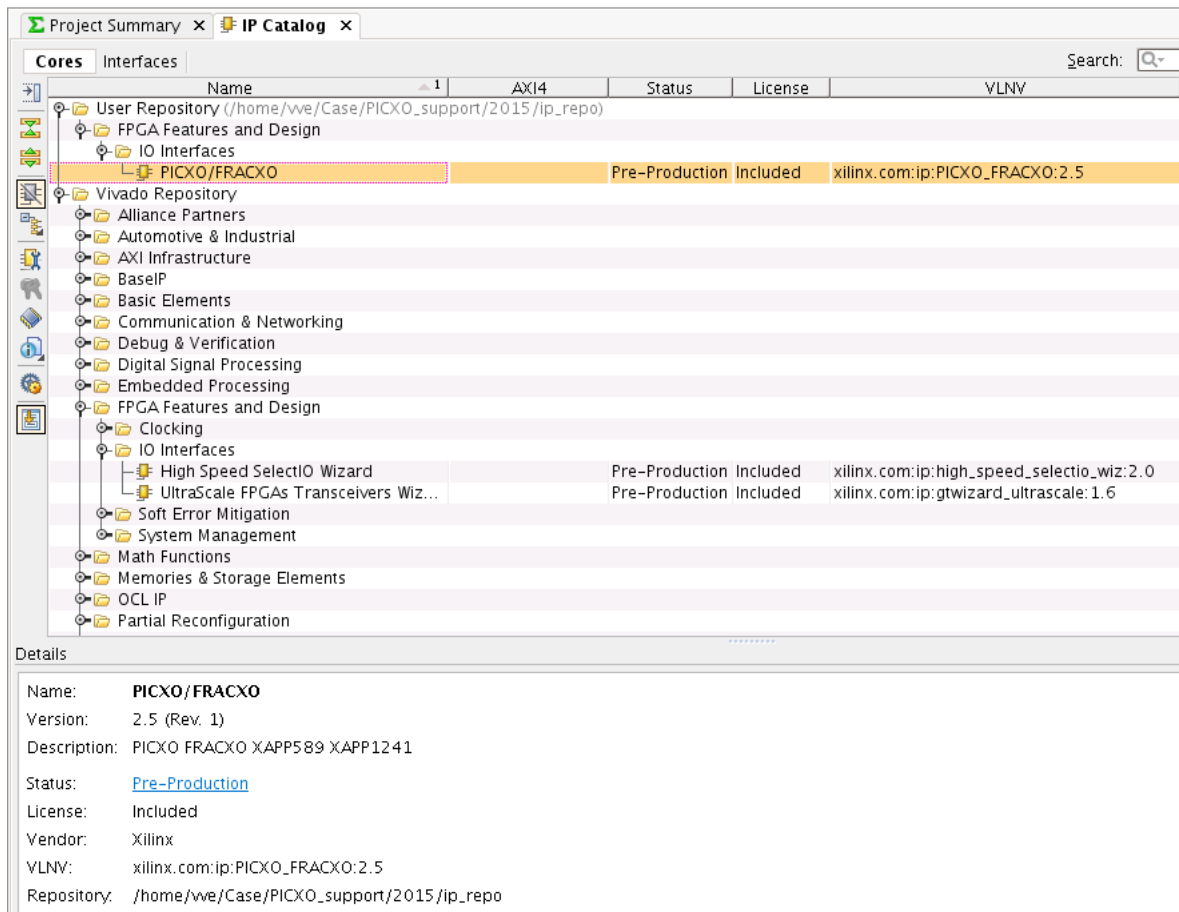
# Implementation

The PICXO design is delivered as a custom IP core. To add the PICXO in NCO mode to a project:

1. Unzip the file in a location.
2. Add the IP repository to the project: In **Tools > Project Options**, select **IP** on the left pane, click **Add Repository**, and select the **PICXO\_FRACXO** folder, shown below.



3. Select the **IP Catalog** tab. The PICXO/FRACXO IP is under **FPGA Features and Design > IO Interfaces** (shown below).



Name	AXI4	Status	License	VLNY
User Repository (/home/we/Case/PICXO_support/2015/ip_repo)				
FPGA Features and Design				
IO Interfaces				
PICXO/FRACXO		Pre-Production	Included	xilinx.com:ip:PICXO_FRACXO:2.5
Vivado Repository				
Alliance Partners				
Automotive & Industrial				
AXI Infrastructure				
BaseIP				
Basic Elements				
Communication & Networking				
Debug & Verification				
Digital Signal Processing				
Embedded Processing				
FPGA Features and Design				
Clocking				
IO Interfaces				
High Speed SelectIO Wizard		Pre-Production	Included	xilinx.com:ip:high_speed_selectio_wiz:2.0
UltraScale FPGAs Transceivers Wiz...		Pre-Production	Included	xilinx.com:ip:gtwizard_ultrascale:1.6
Soft Error Mitigation				
System Management				
Math Functions				
Memories & Storage Elements				
OCL IP				
Partial Reconfiguration				

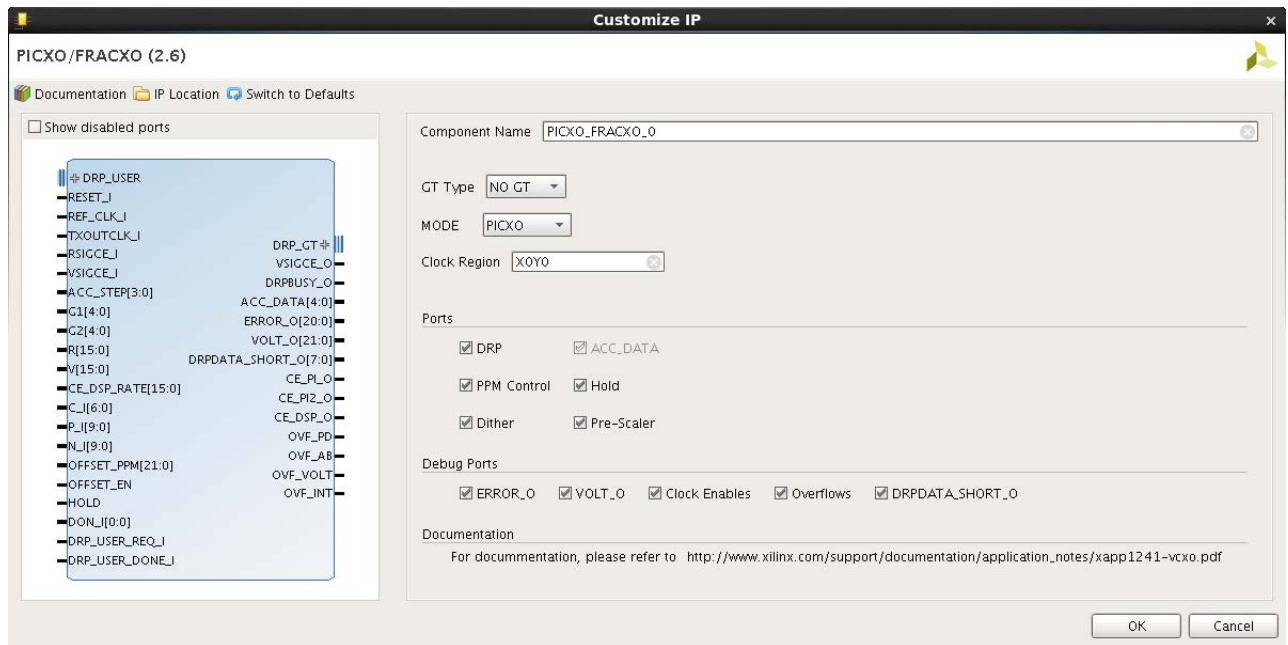
Details

Name: **PICXO/FRACXO**  
Version: 2.5 (Rev. 1)  
Description: PICXO FRACXO XAPP589 XAPP1241  
Status: [Pre-Production](#)  
License: Included  
Vendor: Xilinx  
VLNY: xilinx.com:ip:PICXO\_FRACXO:2.5  
Repository: /home/we/Case/PICXO\_support/2015/ip\_repo

4. Right-click **PICXO/FRACXO** and select **Customize IP**.
5. Select the IP module name, the Mode (**PICXO**), the GT type (**NO\_GT**), and Clock Region where the PICXO in NCO mode is located (**X0Y0**), then click **OK**.



**TIP:** For timing closure purposes, it is recommended to select the same clock region as the PICXO or an adjacent clock region.



- To generate the reference design, select the IP source, right click and select **Generate example design**.

## Reference Design

The reference design is a superset of the PICXO reference designs described in the *All Digital VCXO Replacement for Gigabit Transceiver Applications (UltraScale FPGAs) Application Note (XAPP589)* [Ref 4] and the *All Digital VCXO Replacement for Gigabit Transceiver Applications (7 Series/Zynq-7000) Application Note (XAPP1241)* [Ref 5]. When **NO GT** is selected as the GT type, the generated example design contains the PICXO in NCO mode driving a second PICXO. The NCO PICXO generates an output locked onto the recovered clock. Then, this recovered clock is used to lock the TXOUTCLK\_I signal of the second PICXO. The data received by the GT is simply looped back to the GT transmit side.

For evaluation purposes, both PICXOs are wired to independent VIOs and integrated logic analyzers (ILAs). As in the standard PICXO example design, the VOLT\_O and ERROR\_O signals can be captured when CE\_DSP\_O is High to monitor the PICXO response. The ERROR\_O signal should oscillate near 0 when locked.

You can download the reference design files for this application note at:

[www.xilinx.com/member/vcxoff/index.htm](http://www.xilinx.com/member/vcxoff/index.htm)

## Reference Design Tables

Table 5 shows the reference design matrix.

Table 4: Reference Design Matrix

Parameter	Description
<b>General</b>	
Developer names	David Taylor, Matt Klein, Vincent Vendramini
Target devices	Kintex <sup>®</sup> -7 XC7K325T FFG900-1 Virtex <sup>®</sup> -7 XC7VX690T FFG1761-2 Artix <sup>®</sup> -7 XC7A200T FBG676C-2 Zynq <sup>®</sup> -7000 AP SoC XC7Z045 FFG900-2 UltraScale™ XCKU040-2FFVA1156E and XCVU095-2FFVA2104E UltraScale+ XCZU9EG-2FFVB1156, XCKU5P-2, XCVU9P-2.
Source code provided	Yes
Source code format	VHDL/Verilog
Design uses code/IP from existing Xilinx application note/reference designs, or third party	Yes, ILA, VIO, GT wizard, <i>All Digital VCXO Replacement for Gigabit Transceiver Applications (7 Series/Zynq-7000) Application Note (XAPP589) [Ref 5]</i> , <i>All Digital VCXO Replacement for Gigabit Transceiver Applications (UltraScale FPGAs) Application Note (XAPP1241) [Ref 4]</i> .
<b>Simulation</b>	
Functional simulation performed	No
Timing simulation performed	No
Test bench used for functional and timing simulations	No
Test bench format	N/A
Simulator software tools/version used	N/A
SPICE/IBIS simulations	N/A
<b>Implementation</b>	
Synthesis software tools/version used	Vivado <sup>®</sup> Design Suite 2016.4
Implementation software tools/version used	Vivado Design Suite 2016.4
Static timing analysis performed	Yes
<b>Hardware Verification</b>	
Hardware verified	Yes
Hardware platform used for verification	AC701, KC705, VC709, ZC706, KCU105, VCU108, KCU116, VCU118, ZCU102.

Table 5 shows the device utilization table for the reference design.

**Table 5: Device Utilization and Performance for Reference Design**

	Artix-7 FPGA	Kintex UltraScale FPGA	Virtex UltraScale+ FPGA
	Full Design	Full Design	Full Design
LUTs	6859	5679	5671
Registers	9940	8265	8265
Occupied Slices/CLB <sup>(1)</sup>	3147	1548	1537
Block RAM	27	27	27
BUFG/BUFHCE	5	4	4
GTP/GTX/GTH/GTY	1	1	1
MMCM	1	0	0

1. The number of occupied slices can vary depending on packing results.

Table 6 shows the statistics and performance expectations for a standalone PICXO in NCO mode.

**Table 6: Statistics and Performance Expectations for a Standalone PICXO in NCO Mode**

Target Devices	Artix-7 FPGA	Kintex UltraScale FPGA	Virtex UltraScale+ FPGA
LUTs	790	796	796
Registers	945	945	945
SRLs	33	33	33
Maximum PICXO clock rate	Speed grade dependent, matches TXUSRCLK2 maximum frequency	Speed grade dependent, TXUSRCLK2 maximum frequency	

## Documentation Navigator and Design Hubs

Xilinx Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the [Design Hubs](#) page.

**Note:** For more information on Documentation Navigator, see the [Documentation Navigator](#) page on the Xilinx website.

## References

1. [A Guide to Standard and High-Definition Digital Video Measurements](#)
2. [Improving Video Clock Generation in Modern Broadcast Video Systems](#)
3. [Timing and Synchronization in Broadcast Video](#)
4. *All Digital VCXO Replacement for Gigabit Transceiver Applications (UltraScale FPGAs) Application Note (XAPP1241)*
5. *All Digital VCXO Replacement for Gigabit Transceiver Applications (7 Series/Zynq-7000) Application Note (XAPP589)*

## Revision History

The following table shows the revision history for this document.

Date	Version	Changes
04/25/2017	1.1	Updated Introduction to HSYNC in Modern Video Applications section.
04/12/2017	1.0	Initial Xilinx release.



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