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Interfacing to Mobile SDRAM with CoolRunner-II CPLDs

Summary

This document describes the VHDL design for interfacing CoolRunner™-II CPLDs with low power Mobile SDRAM memory devices. Mobile SDRAM is the ideal memory solution for wireless, handheld, and mobile computing applications, making this a perfect match with the Xilinx CoolRunner-II low power CPLD family. The VHDL code described here can be found in **VHDL Code**, page 6.

Introduction

CoolRunner-II CPLDs are the latest CPLD product offering from Xilinx. CoolRunner-II CPLDs combine high performance with low power operation. Standby current on CoolRunner-II CPLD devices is less than 100µA. More information on the CoolRunner-II CPLD family can be found at **http://www.xilinx.com/cr2**.

Key features of the CoolRunner-II CPLD family include DualEDGE triggered registers, a global clock divider, and voltage referenced I/O standards. These features provide the capability to interface a CoolRunner-II CPLD with low power memory devices such as Mobile SDRAM. Mobile SDRAM manufacturers include Micron and Samsung with data sheets available in **References**, page 6.

Signal Definitions

It is important to define the connections in this design before describing the CPLD logic to interface with the Mobile SDRAM. Table 1 defines the Mobile SDRAM interface signals described in this document.

Table 1: **Mobile SDRAM Signal Definitions**

Manufacturer Specification	Xilinx CPLD VHDL Code	Description
CLK	sdram_clk	Clock input to SDRAM. All input signals are referenced to positive edge of CLK.
CKE	sdram_cke	Clock enable.
CS#	sdram_cs	Command signals that define current operation.
RAS#	sdram_ras	
CAS#	sdram_cas	
WE#	sdram_we	
LDQM, UDQM	sdram_udqm, sdram_ldqm	Mask signal for write data operations (LDQM corresponds to DQ[7:0], while UDQM corresponds to DQ[15:8]).

Table 1: **Mobile SDRAM Signal Definitions**

Manufacturer Specification	Xilinx CPLD VHDL Code	Description
BA[1:0]	sdram_ba[1:0]	2-bit bank address bus.
A[12:0]	sdram_a[11:0]	13-bit row and column address bus.
DQ[15:0]	sdram_dq[7:0]	Bidirectional 16-bit data bus.

Mobile SDRAM

Mobile SDRAM devices feature low power technology to meet the needs of handheld electronics. Additional power savings are achieved with two self-refresh features, temperature-compensated self-refresh (TCSR) and partial-array self-refresh (PASR).

Read and write accesses to the Mobile SDRAM are burst-oriented, starting at a specific address. SDRAM is organized in banks, where each data location can be represented with a row and column address. Each access must begin with an ACTIVE command followed by the READ or WRITE operation. The ACTIVE command selects the bank and row address, while the individual READ or WRITE command select the column address. The Mobile SDRAM features AUTO PRECHARGE, in which the row being accessed is initiated with a PRECHARGE command at the end of the burst sequence.

The operation of the Mobile SDRAM device can be customized by writing different values to the mode register and extended mode register. Each register allows the designer to set parameters for interfacing with the memory device.

The following commands are available to execute with Mobile SDRAM devices:

- NOP (Deselect SDRAM device)
- ACTIVE (Opens row in specified bank for access)
- READ (Select bank and column, and start READ burst)
- WRITE (Select bank and column, and start WRITE burst)
- DEEP POWER DOWN (Maximum power savings, data is not retained)
- PRECHARGE (Deactivates open row in specified bank or all banks)
- AUTO REFRESH or SELF REFRESH (Retains data in SDRAM)
- LOAD MODE REGISTER (Defines operating mode of SDRAM)

More information on the Mobile SDRAM devices targeted in this design can be found in **References**, page 6.

CPLD Design

A CoolRunner-II CPLD is utilized as the controller for interfacing to the Mobile SDRAM memory device. The CPLD is responsible for interpreting the system level commands and creating the

interface requirements to the Mobile SDRAM. Figure 1 illustrates the main control logic in the CoolRunner-II CPLD.

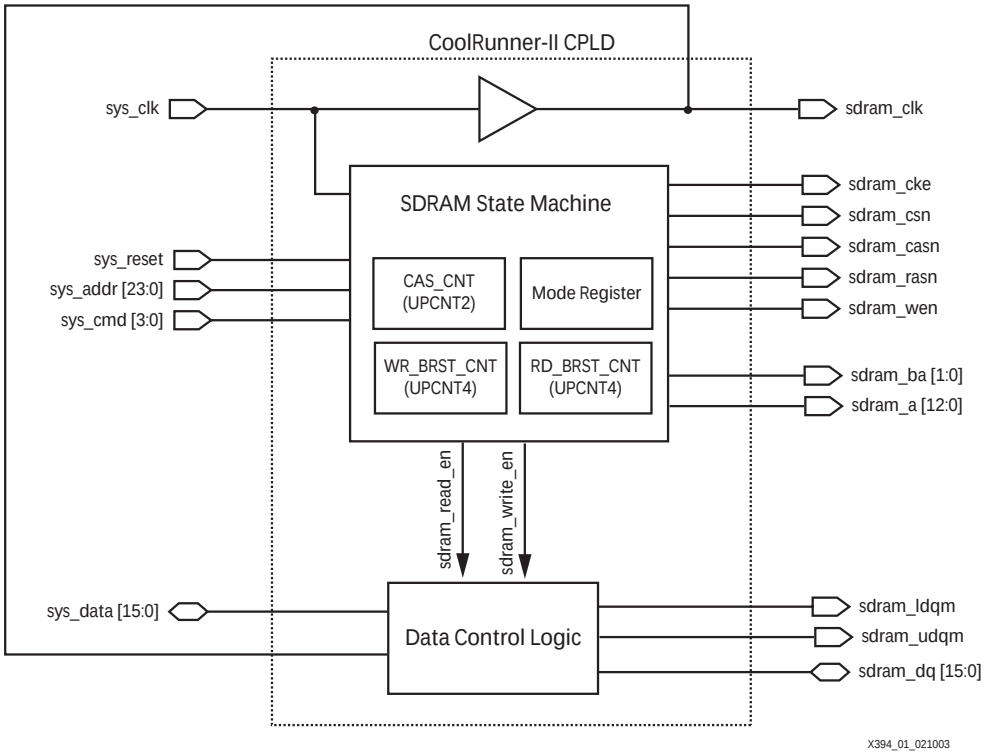

Figure 1: **CPLD Block Diagram**

The system level interface is illustrated in this design as an example interface. This system interface example is an asynchronous communication, with the signals registered in the CPLD. The SDRAM state machine is the main controller in this design and is responsible for generating the control, data, and address signals to the Mobile SDRAM device. The SDRAM state machine also asserts control signals that are used internally by the CPLD for reading/writing data and generating the SDRAM address signals. The SDRAM state machine in this design utilizes a 2-bit counter for waiting the CAS latency in a READ cycle, and two 4-bit counters, one for the length of a WRITE cycle burst and one for the length of a READ cycle burst.

A detailed description of the SDRAM state machine is illustrated in Figure 2. The SDRAM state machine remains in the IDLE state waiting for the next instruction to execute. The next instruction to execute is interpreted from the system command bus, sys_cmd. In this design,

AUTO PRECHARGE is utilized, where an ACTIVE command must be issued prior to any READ or WRITE operation.

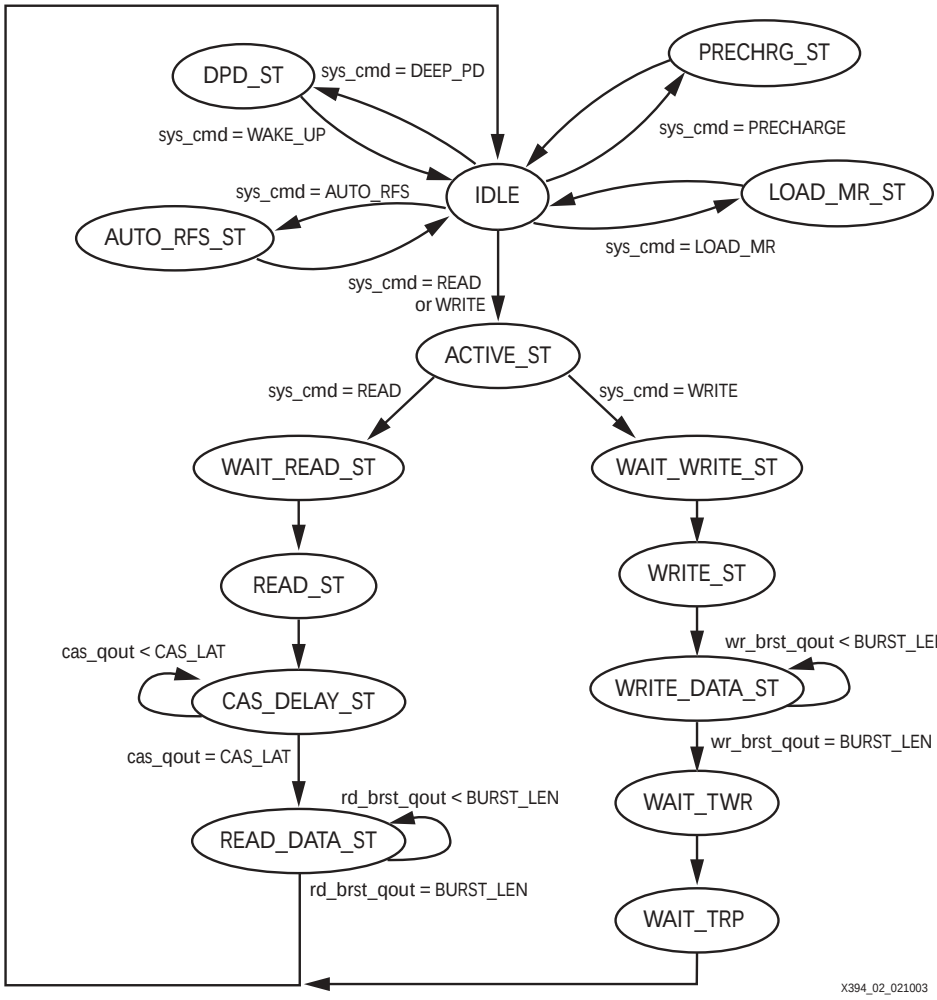

Figure 2: **SDRAM State Machine**

The function of each state in the SDRAM state machine is described in Table 2.

Table 2: **SDRAM State Machine State Description**

State Name	Function
IDLE	Assert NOP instruction control signals to SDRAM. Determines next operation to execute based on the value of sys_cmd signal.
AUTO_RFS_ST	Assign SDRAM command values to execute AUTO REFRESH instruction. Auto refresh retains data in SDRAM.
PRECHRG_ST	Assign SDRAM command values to execute PRECHARGE instruction. Precharge command deactivates specified row in one bank or all banks.
LOAD_MR_ST	Assign SDRAM command to execute LOAD MODE REGISTER. The mode register or extended mode register can be written to in this state, determined by bank address, sdram_ba signal.
DPD_ST	Executes DEEP POWER DOWN command. Data in SDRAM device is not retained in this state. Waits WAKE_UP for system command to return to IDLE state.

Table 2: **SDRAM State Machine State Description**

State Name	Function
ACTIVE_ST	Assign SDRAM command value to execute an ACTIVE command. Assign row address to SDRAM address bus.
WAIT_READ_ST	Execute NOP instruction. Necessary to meet timing specification for t_{RCD}.
READ_ST	Issue READ instruction by assigning SDRAM signals. Assign column address to address bus.
CAS_DELAY_ST	Wait for specified CAS latency of READ operation. Enable CAS latency counter, cas_cnt_en, is asserted.
READ_DATA_ST	Read data from SDRAM. Assert sdram_read_en signal to data control logic block. Enable rd_brst_qout counter. Remain in this state for length of specified burst to capture all data.
WAIT_WRITE_ST	Execute NOP instruction. Necessary to meet timing specification for t_{RCD}.
WRITE_ST	Assign WRITE command values to SDRAM to issue WRITE instruction. Assign column address to address bus.
WRITE_DATA_ST	Enable data write to SDRAM by asserting sdram_write_en signal to data control logic block. Enable wr_brst_qout counter. Wait for end of write burst length.
WAIT_TWR	Execute NOP instruction. Necessary to meet timing specification for write recovery, t_{WR}.
WAIT_TRP	Execute NOP instruction. Necessary to meet timing specification for precharge command period, t_{RP}.

Device Utilization

The SDRAM interface design utilizes a CoolRunner-II XC2C128-4TQ144 device. The system interface, SDRAM state machine, and SDRAM interface logic fits into this device with the utilization results shown in Table 3.

Table 3: **CoolRunner-II Design Utilization**

Parameter	Used	Available	% Utilization
I/O Pins	86	100	86%
Macrocells	102	128	80%
Product Terms	180	448	40%
Registers	100	128	78%
Function Block Inputs	126	320	39%

System Interface

The SDRAM design described in this document includes a generic system interface. The system interface illustrates the basic control signals needed for the SDRAM logic block. These signals include a system clock, reset, 24-bit address bus, 16-bit data bus, and 4-bit command bus. Excluding the system clock, all signals are asynchronous and registered in the CPLD.

Modeling of the system interface in this design is done with testbench logic. The testbench is responsible for generating the address, data and command signals for any operation with the

Mobile SDRAM device. The testbench controls the initialization requirements, single read/write operations, and tests the power down modes of the SDRAM.

VHDL Code

XAPP394 - **http://www.xilinx.com/products/xaw/coolvhdlq.htm**

Conclusion

CoolRunner-II CPLD devices are the perfect compliment to low power Mobile SDRAM memory. These two low power devices are targeted for handheld, mobile computing applications. CoolRunner-II CPLD devices feature low power consumption and create a seamless interface to Mobile SDRAM memory.

References

1. Micron Data Sheet. MT48V16M16LFFG 256Mb: x16 Mobile SDRAM. Micron Technology, Inc. 2002.
2. Micron Technical Note. TN-48-10. Mobile SDRAM Power-Saving Features. Micron Technology, Inc. 2002.
3. Samsung Data Sheet. K4S64163LF-RG/S 4Mx16 Mobile SDRAM. Rev 1.0. Samsung Electronics 2002.

Appendix A: CoolRunner-II Resources

Application Notes

http://www.xilinx.com/xapp/xapp375.pdf (Timing Model)
http://www.xilinx.com/xapp/xapp376.pdf (Logic Engine)
http://www.xilinx.com/xapp/xapp377.pdf (Low Power Design)
http://www.xilinx.com/xapp/xapp378.pdf (Advanced Features)
http://www.xilinx.com/xapp/xapp379.pdf (High Speed Design)
http://www.xilinx.com/xapp/xapp380.pdf (Cross Point Switch)
http://www.xilinx.com/xapp/xapp381.pdf (Demo Board)
http://www.xilinx.com/xapp/xapp382.pdf (I/O Characteristics)
http://www.xilinx.com/xapp/xapp383.pdf (Single Error Correction Double Error Detection)
http://www.xilinx.com/xapp/xapp384.pdf (DDR SDRAM Interface)
http://www.xilinx.com/xapp/xapp387.pdf (PicoBlaze Microcontroller)
http://www.xilinx.com/xapp/xapp388.pdf (On the Fly Reconfiguration)
http://www.xilinx.com/xapp/xapp389.pdf (Powering CoolRunner-II)
http://www.xilinx.com/xapp/xapp393.pdf (8051 Microcontroller Interface)

CoolRunner-II Data Sheets

http://direct.xilinx.com/bvdocs/publications/ds090.pdf (CoolRunner-II Family Datasheet)

http://direct.xilinx.com/bvdocs/publications/ds091.pdf (XC2C32 Datasheet)
http://direct.xilinx.com/bvdocs/publications/ds092.pdf (XC2C64 Datasheet)
http://direct.xilinx.com/bvdocs/publications/ds093.pdf (XC2C128 Datasheet)
http://direct.xilinx.com/bvdocs/publications/ds094.pdf (XC2C256 Datasheet)
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http://direct.xilinx.com/bvdocs/publications/ds096.pdf (XC2C512 Datasheet)

CoolRunner-II White Papers

http://www.xilinx.com/publications/products/cool2/wp_pdf/wp165.pdf (Chip Scale Packaging)
http://www.xilinx.com/publications/whitepapers/wp_pdf/wp170.pdf (Security)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/23/03	1.0	Initial Xilinx release.
12/01/03	1.1	Errata