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CompactFlash Card Interface for CoolRunner-II CPLDs

XAPP398 (v1.0) September 23, 2003

Summary

This application note describes the card-side implementation of an 16-bit CompactFlash (CF+) card interface using a CoolRunner™-II CPLD. Included in this implementation are the CIS, Attribute Memory Control and Status Registers, 16-bit Common Memory, and 8-bit I/O Interface. This design can be easily modified to interface to any memory, DSP or microcontroller. This application note does not describe the Host Bus Adapter (HBA) side of the CompactFlash interface, which is resident on a host system such as a Personal Computer or PDA.

Introduction

There are two types of CompactFlash devices: CompactFlash Storage Cards (CF), and CF+ Cards. CF consists only of common memory data storage whereas CF+ is expanded to include I/O devices or magnetic disk data storage, depending on the specific application. This application note targets the CF+ type of device. There are three basic modes of operation called for in the CF specification. Typically, CF+ devices operate in two of the three basic modes: PC Card ATA using I/O Mode, and PC Card ATA using Memory Mode. The third, optional mode is True IDE Mode. CF cards are required to operate in all three modes. This application note implements the CF+ card side interface utilizing PC Card ATA using I/O Mode and PC Card ATA using Memory Mode. True IDE Mode is not addressed in this application note, but can be implemented by the designer using the CoolRunner-II CPLD and this reference design.

The CompactFlash interface consists of two main components: the Host Bus Adapter (HBA) and the card side interface. The former resides on the host side of the interface, which typically is built into the socket of a personal computer or Personal Digital Assistant (PDA). The card side interface resides on the CF card itself. Described in this application note is the implementation of a controller which resides in the card side of the interface.

Within the card, there is Attribute Memory, Common Memory, and I/O Interface. Attribute memory consists of the Card Information Structure (CIS) and the Configuration and Control Registers. Common Memory, in this reference design, interfaces to the Intel StrataFlash 28F320J3 memory. The I/O logic interfaces to the Analog Devices, Inc. ADSP-218xN Series DSP using the 8 bit I/O Space of the DSP.

In this implementation, the CF+ interface is a 16-bit data bus. The I/O interface within the card consists of an 8-bit bus to the DSP.

It is necessary to refer to the CompactFlash Specification and the PCMCIA Specification to fully understand the discussion in this application note.

A free downloadable zip file containing the VHDL source code and a testbench for this reference design is available as described below in **Source Code Download**, .

Electrical Interface

Power Considerations

CoolRunner-II CPLDs are 1.8V core voltage devices with I/O banking features that allow for various I/O voltages and tolerances up to 3.3V. The CF+ specification calls for either 3.3V or

5.0V operation. The core power supply to the CPLD, therefore, must be regulated on the CF+ card to 1.8V while the I/Os must be configured to operate at 3.3V as described in the following section. For the specific application, if 1.8V regulation is not available or the I/Os will be subjected to 5.0V, consider using the CoolRunner XPLA3 CPLD, which is a 5V tolerant 3.3V device and therefore will not require the additional power regulation. I/O considerations for the CoolRunner-II CPLD are discussed in the following section.

To indicate to the host that the CF+ card is expecting 3.3V signaling, -VS1 must be held at GND. The signal -VS2 is reserved by PCMCIA for a secondary voltage and therefore must be left open. These two signals are not implemented in this application note and therefore must be electrically considered external to the CPLD on the PCB by the designer.

CF+ devices that are configured for 3.3V operation are limited to 75mA max (Power Level 0) or 500mA max. (Power Level 1). Further, during power up and after reset, the CF+ card is limited to Power Level 0. To assist the designer with more efficiently utilizing the CF+ power budget, CoolRunner-II CPLDs are the perfect choice since these devices exhibit very low static and dynamic current consumption.

I/O Considerations

Inputs

The CompactFlash specification calls for three basic types of input configurations in the Pin Assignments and Pin Type description: IxZ, IxU and IxD. "I" represents the pin is an input, "Z" represents an input with no resistive termination, "U" represents a weak pullup termination, and "D" represents a weak pulldown termination. These three configurations are also specified with one of three electrical characteristics which is denoted by a number 1, 2 or 3 in the "x" position of the designation. The three numbers correspond to various input threshold levels for the type of input required. Details of these values and configurations can be found in the CompactFlash specification.

Outputs

Similarly, the CF+ specification calls for three basic types of output configurations: OTx, OZx, OPx, and ONx. "O" designates the signal to be an output, "T" represents a totem pole type output, "Z" a CMOS P-channel/N-channel output with 3-state capabilities, "P" a PMOS only output, and "N" an NMOS only output. These also have three electrical characteristics denoted by 1, 2, or 3 in the "x" position of the designation. These three values represent V_{OH} and V_{OL} levels under certain test conditions. All output types also have a 3-state characteristic and, together with the voltage levels, are described in the CompactFlash Specification.

Implementation

The CF specification calls for 3.3V or 5.0V for the card power supply and I/O signals. CoolRunner-II devices are 1.8V devices, but have I/O banking capabilities. To implement the CF+ interface, the CoolRunner-II CPLD I/Os should be configured as 3.3V LVCMOS. CoolRunner-II CPLDs are not 5V tolerant. However, external circuitry can be used to interface to 5V systems. See XAPP364. Alternately, CoolRunner XPLA3 CPLDs are 3.3V devices with 5.0V tolerance. If these voltage requirements are an issue for the application, the CF+ implementation can target the CoolRunner XPLA3 CPLD. Since the CF+ card tells the HBA what voltage it expects, 5.0V is not present on the I/O pins until the HBA determines the required voltage. CoolRunner-II CPLDs are therefore acceptable for CF+ applications since 5.0V will never be applied to its I/Os, as long as -VS1 and -VS2 are configured correctly.

Since this application note describes the implementation of the two modes PC Card ATA using I/O Mode and Memory Mode, the I/Os are required to be configured as I1Z, I2Z, I1U, I3U, OZ3, OT1, and OT3. The CoolRunner-II CPLD can be configured to support all I/O modes with the following caveats.

I/O configuration I2Z requires that V_{IH} be at a lower voltage than the CoolRunner-II CPLD is specified in the data sheet. The signal of interest is RESET whose V_{IH} should be analyzed for the particular application of this CF+ design. If it is determined that the supplied signal is always

high enough to meet the V_{IH} value of CoolRunner-II devices, then this CPLD should be sufficient. If not, an external buffer with these characteristics must be supplied to satisfy the system requirements.

I/O configurations OT1 and OT3 require a totem pole type of driver. CoolRunner CPLDs only provide CMOS type output buffers and therefore cannot explicitly meet these requirements. Therefore, an external buffer of totem pole type should be implemented to satisfy the CF+ specification. However, CoolRunner-II CPLDs can meet the I/O drive requirements of V_{OH} and V_{OL} at the specified I_{OH} and I_{OL} test conditions respectively, regardless of CMOS or totem pole type configuration. Analysis of the particular application is necessary to determine if CoolRunner-II CPLD I/Os can be used without the use of external totem pole buffers.

Fixed Level and Unused I/Os

Nomenclature of all signals in the VHDL source code matches that of the CF+ specification for PC Card I/O Mode.

The signals -CD1 and -CD2 are card detect pins which indicate to the host that the card is fully inserted when it detects both signals are low. This application note does not implement these signals within the CPLD, but instead relies on the system designer to hold these two signals at GND external to the CPLD.

The signal -CSEL is not used by this application as described by the CF+ specification.

-SPKR, binary audio, is not used in this reference design, but can be added if required.

-VS1 and -VS2, voltage sense signals, are also not used in this implementation, but must be hardwired on the PCB so the host system can correctly determine the card's required voltage levels. For this reference design, it is assumed that -VS1 is held LOW while -VS2 is left floating. These two signals are held HIGH by the host system, thereby allowing -VS2 to be read as a logic HIGH when the card leaves it in a floating state.
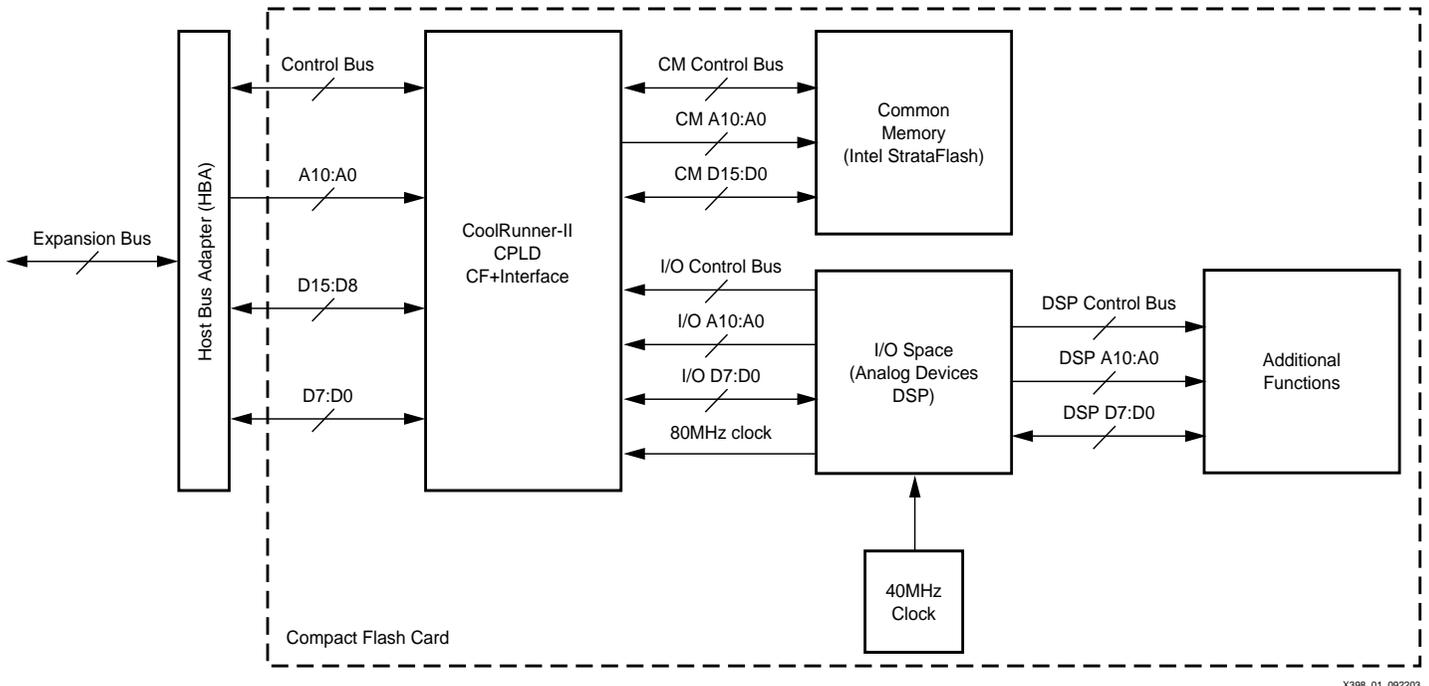
Block Diagram

CF+ Card

Figure 1 shows a block diagram of the CF+ card where the major components are the CoolRunner-II CPLD, Intel StrataFlash and the Analog Devices DSP.

The CoolRunner-II CPLD implements the direct interface to the CF+ slot, an interface to the Common Memory space and an interface to the I/O Space. Control logic is included to synchronize data between the three interfaces. The Attribute memory as a whole is realized in the CPLD which includes control and status registers as well as the CIS. External ROM is not needed for the CIS since it has been compactly implemented in the CPLD as a lookup table constructed of product terms.

The Intel StrataFlash is used for the Common Memory space and is limited to 2 kB due to the 11 available address lines of the CF+ interface. To access further memory space, the CF+ card must be configured to utilize the I/O Space or redesigned to implement the True IDE mode. The Common Memory space is configured with a 16-bit data bus.

The I/O Space, for this implementation, consists of an Analog Devices DSP. In Figure 1, there is a reference to Additional Functions. This is included for illustrative purposes and can be any function, such as a GPS device. An 8-bit data bus is used to interface to the DSP.

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Figure 1: **CompactFlash Card General Block Diagram**

CPLD Implementation

Figure 2 represents an overview of the CF+ controller reference design contained in the CPLD (as described in this application note). There are two controllers for the three interfaces: CF+ Address Decode and Control Logic (CF+ Card Controller), and I/O Space Address Decode and I/O Control Logic (I/O Space Controller).

The former controls transactions with the CompactFlash interface and directs data to the correct locations—more specifically, the Attribute Memory, Common Memory, and the I/O Space Controller. It also provides the necessary status and control signals required by the HBA to effectively communicate with the card.

The I/O Space controller interfaces the CF+ card controller with the devices connected to the I/O Space bus, which is in this case the DSP. To interface more effectively and synchronously with the DSP, there are three I/O register banks: Address Register, Data Register, and Status Register.

As mentioned earlier, the Attribute memory is included in the CPLD reference design. The Attribute Memory, in this case includes the CIS, COR, CSR and PRR, whose functionality is described later in this document.
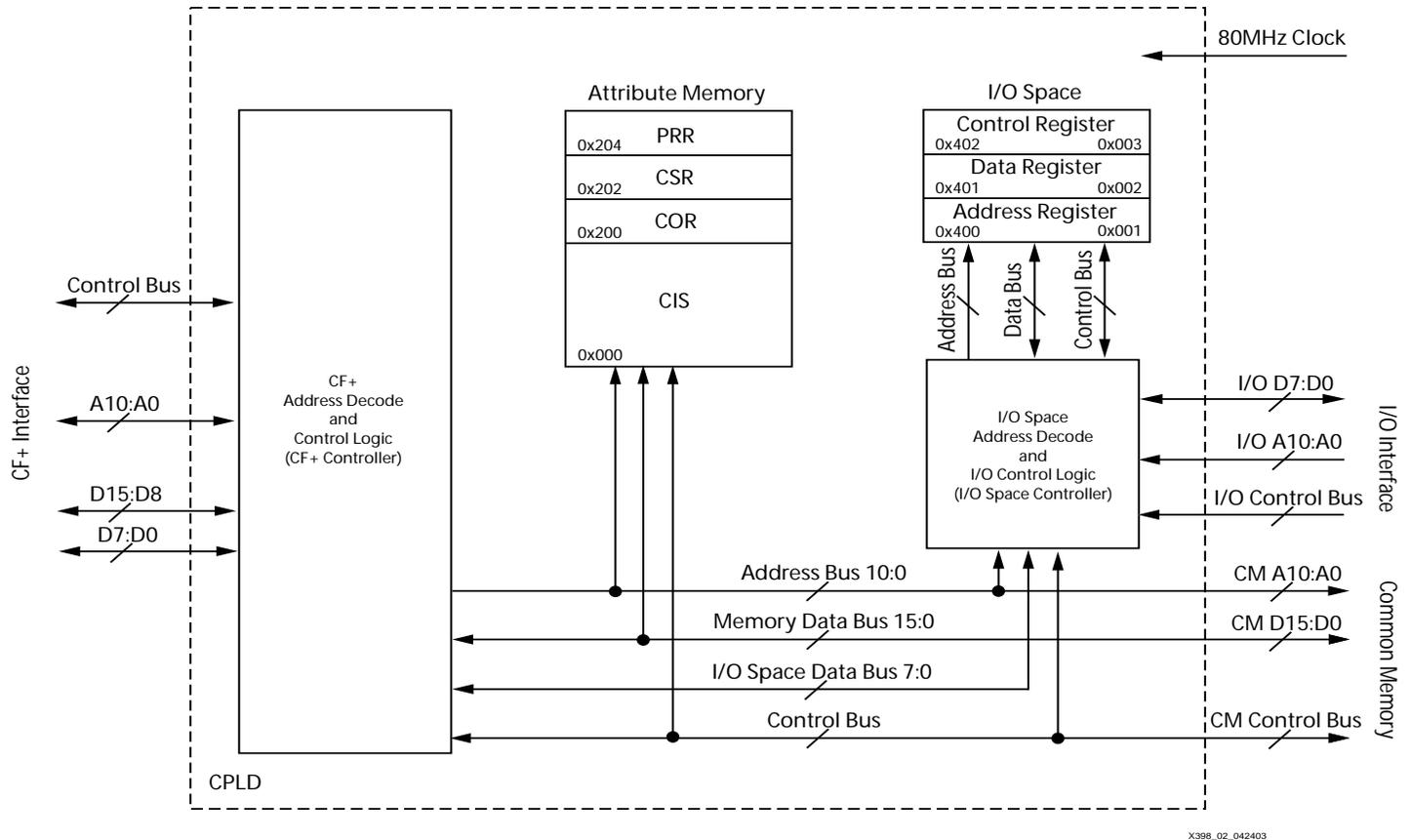
Figure 2: **CPLD Controller General Block Diagram**

Signal Descriptions

Table 1 displays the pin descriptions of the CoolRunner-II CF+ Interface. Note that according to the CompactFlash specification, some pin names change depending on the card configuration mode. For these signals, the I/O Mode nomenclature is used in the table, throughout this document, and in the VHDL source code.

Table 2 describes the pins of the Common Memory Interface to the Intel StrataFlash device.

Similarly, Table 3 indicates pin names and their functions for the I/O Space Interface to the Analog Devices DSP.

No pin assignments have been forced, leaving it up to the user to custom fit the design per their requirements.

Table 1: **CF+ Interface Pin Descriptions**

Name	Direction	Description
host_addr(10:0)	Input	A10:A0 in the Compact Flash Specification which are address lines from the HBA.
ce1_n	Input	Active LOW card select signal. Together with ce2_n and host_addr(0), selects between 16/8-bit data transfers and odd/even byte transfers. See Table 4 for details.
ce2_n	Input	Active LOW card select signal. When ce1_n is LOW, selects the odd or even byte of the data word depending on host_addr(0). See Table 4 for details.
iord_n	Input	Used in I/O Mode, this is an active LOW I/O read strobe from the host. Data is placed on the CF+ bus by the CF+ card.
iowr_n	Input	Also used in I/O Mode, this signal clocks data into the CF+ card when the host has placed valid data on the data bus of the CF+ interface. iowr_n is active LOW.
oe_n	Input	In Memory mode, this signal is used as a strobe by the host to read data from Common Memory or Attribute Memory including the CIS. In I/O Mode, this signal is used to read data from the Attribute Memory and CIS. oe_n is active LOW.
reg_n	Input	Active LOW signal that distinguishes between Common Memory (HIGH) and Attribute Memory (LOW). When in I/O Mode, this signal must be LOW to access I/O Space.
reset	Input	This is an active HIGH signal to initialize and reset all registers in the CF+ card.
we_n	Input	Active LOW signal to strobe data into the Attribute memory and the Common Memory.
stschg_n	Output	If enabled in the CSR, this active LOW pin indicates the status of the rdy/-bsy pin. When in I/O Mode, rdy/-bsy is renamed to ireq_n and its functionality no longer reflects the ready/busy condition. For the host to see ready/busy conditions, stschg_n is available. When in Memory Mode, stschg_n is always HIGH.
inpack_n	Output	When configured in I/O Mode, the CF+ card uses this active LOW signal to indicate the card is responding to an I/O Space read cycle at the address present on the host_addr bus.

Table 1: **CF+ Interface Pin Descriptions** *(Continued)*

Name	Direction	Description
ireq_n	Output	ireq_n is active LOW.
		In Memory Mode, this signal indicates a ready/busy state (rdy/-bsy) where a LOW signal indicates a busy state. The CompactFlash specification requires this signal to be LOW during power up. During power up/configuration, the CoolRunner-II 3-states the I/Os with weak pullup, making it impossible to meet this requirement. However, the specification requires the HBA not access the card until >1ms after power has stabilized after which the HBA must assert the reset signal for 10µs. Since configuration times for CoolRunner-II CPLDs is much less than 1ms, this allows the card to have a HIGH rdy/-bsy signal during power up without adverse effects.
		The rdy/-bsy signal in Memory Mode is LOW during a reset, either a reset directed by the reset pin or a soft reset when the SRESET bit has been written in the COR. This signal also reflects the status of the Common Memory pin, cm_sts.
		During I/O Mode, this pin takes on the ireq_n functionality and masks the rdy/-bsy functionality. This active LOW signal now indicates that data is ready to be read from the I/O Space (DSP) Address or Data registers.
		To obtain the status of rdy/-bsy, the PRR bit 1 must be read. A change in status of this bit is reflected on the stschg_n pin, if enabled.

Table 1: **CF+ Interface Pin Descriptions** *(Continued)*

Name	Direction	Description
wait_n	Output	As an active LOW signal, wait_n tells the HBA to extend the current memory or I/O cycle. This signal has been implemented such that the I/O Space and Common Memory have control over this signal. The dsp_ioms_n signal is sampled when accessing the I/O Space and indicates the DSP is reading or writing to the I/O Space. As implemented with the Analog Devices DSP, the signal ioms_n is used to drive dsp_ioms_n. Since the DSP has configured with three wait states, this assists the HBA to wait the appropriate length of time during an I/O Space access. The Common Memory uses cm_wait to drive wait_n during this type of memory access. However, as implemented with the Intel StrataFlash, this memory has no wait signal and therefore cm_wait must be driven HIGH external to the CPLD or removed from the source code.
host_data_low(7:0)	Bidirectional	D7:D0 in the CompactFlash specification. These are the lower data signals to/from the HBA. This corresponds to the even byte described in the CompactFlash specification.
host_data_high(7:0)	Bidirectional	D15:D8 in the CompactFlash specification. These are the upper data signals to/from the HBA.This corresponds to the odd byte described in the CompactFlash specification.

Table 2: **Common Memory Interface Pin Descriptions**

Name	Direction	Description
cm_sts	Input	Effectively a ready/busy signal for the Intel StrataFlash. This implementation assumes the memory is configured with level mode sts signalling and therefore supplies the CF+ rdy/-bsy logic (named ireq_n) a busy state (LOW) when the memory is busy performing a lengthy operation. cm_sts is active LOW.
cm_wait	Input	Available for Common Memory wait type status inputs. As the Intel StrataFlash memory used in this implementation does not contain a wait signal, cm_wait is unused and driven high in the test bench. The user must either permanently drive this signal HIGH or remove it from the source code so as to allow proper functionality of wait_n. cm_wait is active LOW.
cm_byte_n	Output	Active LOW, cm_byte_n selects the 8-bit or 16-bit data bus access modes of the Intel StrataFlash as requested by the HBA. When in 8-bit mode, cm_addr(0) selects the high or low byte of the addressed memory location. When in 16-bit mode, cm_addr(0) is ignored and cm_addr(1) becomes the LSB of the Common Memory address bus.
cm_addr(0)	Output	Byte-select address for the Intel StrataFlash. This signal selects the high or low byte of the addressed memory location. A high byte from Common Memory corresponds to an odd byte with respect to the CF+ interface. Similarly, a low byte from Common Memory corresponds to an even byte on the CF+ interface. High bytes are accessed when cm_addr(0) is HIGH and low bytes are accessed when cm_addr(0) is LOW.
cm_addr(10:1)	Output	Address bus for the Common Memory.
cm_reset	Output	Active LOW reset for the Common Memory
cm_read_n	Bidirectional	Active LOW output enable signal to read data from the Common Memory.
cm_data(15:0)	Bidirectional	Data bus for the Common Memory.
cm_ce_n	Bidirectional	Active LOW chip enable signal for the Common Memory.
cm_write_n	Bidirectional	Active LOW write enable signal for the Common Memory.

Table 3: **I/O Space Interface Pin Descriptions**

Name	Direction	Description
dsp_clk	Input	This clock input to the CPLD must be 80MHz
dsp_addr(10:0)	Input	11-bit address bus from the DSP. Most of these pins can be removed from the design to obtain more I/Os as needed. This implementation only utilizes the two LSBs since there are only three registers accessed by the DSP.
dsp_ioms_n	Input	I/O memory select from the DSP. This active LOW signal enables the I/O Space from the DSP side of the CF+ interface. The CF+ interface signal wait_n samples this signal, and when low, indicates the DSP is either reading or writing to the I/O Space interface.
dsp_rd_n	Input	Active low-read strobe from the DSP which accesses data contained in the I/O Space registers.
dsp_wr_n	Input	Active low-write strobe from the DSP which accesses data contained in the I/O Space registers.
dsp_data(7:0)	Bidirectional	8-bit bidirectional data bus from the DSP.

CF+ Controller

All primary control functions for the CF+ interface are contained in the CF+ controller (cf_plus_control.vhd). The following subsections describe the CF+ controller's functionality.

Addressing Modes

This CF+ interface consists of a 16-bit data bus, which may or may not be used to its fullest capabilities, depending on the architecture of the HBA and the host system. Some host systems can only support 8-bit transfers which therefore requires the HBA to request 8-bit data bytes from the CF+ card. It is the card controller's responsibility to provide 8 bits of data to the HBA. In the case of the 8-bit host, it is the HBAs responsibility to request the upper or lower byte of a 16-bit data word from the CF card using specific control signals and then sending that data to the host over the 8-bit data bus in the correct order.

The CF+ implementation in the CPLD reads the control signals (host_addr(0), ce1_n and ce2_n) from the interface and interprets them in the correct order for providing data over the 8-bit or 16-bit data bus as required by the HBA. Table 4 describes in detail this interpretation, which is compliant to the CompactFlash specification. This table references Odd and Even bytes as described in the CompactFlash specification. The Intel StrataFlash maintains a nomenclature of High and Low bytes. Table 4 conveniently shows the correlation between Odd/Even and High/Low nomenclatures.

Currently, I/O Space access is limited to 8-bit in this implementation. If-16 bit I/O Space access is required, comments have been added throughout the source code to assist the user to this end. However, 16-bit I/O Space access has not been tested.

Table 4: **Addressing Even and Odd Bytes from CF+ Interface**

Addressing Mode	ce1_n	ce2_n	host_addr(0)	host_data_high	host_data_low
No access	1	1	X	3-State	3-State
8/16-bit Mode (even byte)	0	1	0	3-State	Even Byte (Low Byte)
8-bit Mode (odd byte)	0	1	1	3-State	Odd Byte (High Byte)
16-bit Mode (odd byte only)	1	0	X	Odd Byte (High Byte)	High-Z
16-bit Mode (even & odd bytes)	0	0	X	Odd Byte (High Byte)	Even Byte (Low Byte)

Memory and I/O Space Access

The HBA gains access to the different memory spaces via a few control pins. The signal reg_n allows the HBA to write or read from Common Memory when this signal is HIGH. Note that when reg_n is LOW, the HBA has access to either the Attribute Memory or the I/O Space, dictated by the state of iord_n, iowr_n and, of course, the address.

When reg_n is LOW, the HBA can perform read and write operations on the I/O Space registers. To perform a read, iord_n is held LOW. Similarly, holding iowr_n LOW will access the I/O space registers in a write mode.

All memory spaces (Attribute Memory, Common Memory and I/O Space) are read and write capable. There are two exceptions: The CIS is read-only, and the I/O Space Status Register, which is read-only as well.

Interrupt Request and Ready/Busy

A CF+ card can be configured for several modes of operation, as mentioned earlier. Two of these modes are supported in this implementation: Memory Mode and I/O Mode. Each mode has unique I/O signal descriptions as described in the CompactFlash specification. In other words, when the card is configured in Memory Mode, the I/Os are defined to have a specific set of I/O functions and names. But when the card has been reconfigured for I/O Mode, some of these pins take on a new name and functionality. Of interest is the rdy/−bsy pin named ireq_n in this implementation. The CompactFlash specification names this pin rdy/−bsy for Memory Mode and changes it to −ireq in I/O Mode. See Table 1, page 6.

In Memory Mode, this signal indicates a ready/busy state (rdy/-bsy) where a LOW signal indicates a busy state. The CompactFlash specification requires this signal to be LOW during power up. During power up/configuration, the CoolRunner-II 3-states the I/Os with weak pullup, making it impossible to meet this requirement. However, the specification requires the HBA not access the card until >1ms after power has stabilized, after which the HBA must assert the reset signal for 10µs. Since the configuration time for CoolRunner-II CPLDs is much less than 1ms, this allows the card to have a HIGH rdy/-bsy signal during power up without adverse effects.

The rdy/−bsy signal in Memory Mode is LOW during a reset, either a reset directed by the reset pin or a soft reset when the SRESET bit has been written in the COR. This signal also reflects the status of the Common Memory pin, cm_sts. The Intel StrataFlash provides a signal named STS which, in level mode, acts as a ready/busy signal. This CF+ implementation uses this STS signal to reflect the ready/'busy status of the Common Memory when it is being accessed.

During I/O Mode, this pin takes on the ireq_n functionality and masks the rdy/−bsy functionality. This active LOW signal now indicates that data is ready to be read from the I/O Space (DSP) Address or Data registers. When new data is placed in the Address or Data registers by the DSP, ireq_n goes LOW. Once data has been read from these registers by the HBA, ireq_n returns to its inactive HIGH state.

Since rdy/−bsy status is masked during I/O Mode, the PRR bit 1 must be read to determine the status of the Common Memory. A change in status of this PRR bit is reflected on the stschg_n pin, if enabled.

Attribute Memory

The Attribute Memory is divided into two basic sections: The CIS and the Configuration Registers. There are at least six optional Configuration Registers, but this implementation integrates three of these registers. The CIS may be found in the reference design source file named cis.vhd. The Attribute Memory may be found in attribute_memory.vhd, but some associated control signals for this memory space are found in cf_plus_control.vhd.

Addressing Attribute Memory

The CIS is found at memory location 000h per the CompactFlash specification and is read-only. The CompactFlash specification states that for CompactFlash and other cards with data storage, the configuration registers must reside at a base offset (BASE) of 200h. Conversely, non-data storage cards BASE can be located anywhere and is found by parsing the CIS tuples. This implementation, since data storage is used, sets BASE to 200h. Table 5 describes the addressing scheme of the Attribute Memory.

Table 5: **Attribute Memory Registers**

Address	Register	Description
000h	CIS	Card Information Structure
BASE + 00h	COR	Configuration Option Register
BASE + 02h	CSR	Card Configuration and Status Register
BASE + 04h	PRR	Pin Replacement Register

Card Information Structure

The Card Information Structure (CIS) is maintained in the Attribute Memory as a read-only memory space and is intended as nonvolatile memory. In this CoolRunner-II implementation, the CIS is built using product terms and therefore retains its nonvolatile properties without using external memory.

This data structure is comprised of tuples which tell the software driver of the host system what characteristics the CF+ card contains, such as size, speed and resources required. The host then configures the card and the HBA to efficiently take advantage of the card's features. The structure of the tuples and the definitions of the values within the tuples is not described here. It is up to the user to investigate this information as found in the CompactFlash specification and the PCMCIA specification.

Included in this implementation is an example CIS which must be modified to the user's application. To modify the CIS, edit the source file cis.vhd.

Configuration Option Register

The Configuration Option Register (COR) is one of the registers included in the Attribute Memory and is used to configure the card. Configuration options include soft reset, interrupt types and address decoding.

The COR is comprised of 8 bits as shown in Table 6.

Table 6: **Configuration Option Register**

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevelReq	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

SRESET - Soft Reset

When this bit is written by the HBA, a soft reset of the card will occur. To obtain this functionality, the HBA must write a HIGH then a LOW where the reset is performed during the HIGH cycle. A soft reset differs from a hard reset in that this bit is not cleared by a soft reset. Otherwise, both types of reset have the same functionality. All registers and state machines in the card will be reset to zero upon hard or soft reset, including registers in the I/O space. A reset condition is also presented to the Common Memory. This bit is initially set LOW by a hardware reset condition when driven by the reset pin.

LevelReq

ireq_n can be set to indicate interrupts on a level or pulse mode basis. Setting this bit HIGH enables level mode interrupts, whereas setting this bit LOW enables pulse mode interrupts. Pulse mode is set to 0.5μs per the CompactFlash specification and uses a 6-bit binary up counter (upcnt6.vhd) to implement the pulse width. This bit is set to zero by reset.

Conf

These 6 bits select the operation mode of the card. The specification states that for CompactFlash Cards these bits are used for Memory Mapping or I/O Mapping, depending on the application. But since this implementation is of a CF+ card, the specification states that these bits specify either Memory Mapping where I/O cycles are ignored (all bits zero), or the bits are user-defined. The specification also states that multiple function CF+ cards bits 0 through 2 have specific functionality and bits 3 through 5 are reserved for user implementation.

This CF+ implementation handles the Conf bit functionality where an all zeros condition disables the I/O space and effectively allows for memory mapping only. Also, since single function CF+ cards use these bits optionally, and since this implementation is of a single function CF+ card, these bits are not required. However, they have been included for convenience. All Conf bits are set to zero when a reset condition occurs.

Conf0 enables the I/O space when set HIGH, and disables the I/O function if LOW.

Conf1 is used for Base and Limit Registers, but since these registers are not used in this implementation, Conf1 is non-functional.

Conf2 enables ireq_n routing. Its functionality depends on the state of Conf0. If Conf0 is HIGH and Conf2 is HIGH, interrupts from the I/O Space are routed to the ireq_n pin. If Conf0 is HIGH and Conf2 is LOW, interrupts are disabled. If Conf0 is LOW, Conf2 is undefined.

Conf3 through Conf5 are reserved for user implementation.

Card Configuration and Status Register

Another register in the Attribute Memory, the Card Configuration and Status Register (CSR) contains information regarding the card's condition.

The CSR is comprised of 8 bits as described in Table 7.

Table 7: **Card Configuration and Status Register**

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOis8	XE_n	Audio	PwrDwn	Int	0
Write	0	SigChg	IOis8	XE_n	Audio	PwrDwn	0	0

Changed

This bit reflects the status of CRdy_Bsy_n and CWProt in the PRR. Note that the functionality of CWProt is not implemented since WProt (Write Protect) is not supported by the CompactFlash specification.

When CRdy_Bsy_n is HIGH, indicating Rdy_Bsy_n has changed state, the Changed bit goes HIGH. Additionally, this bit will drive the stschg_n pin LOW indicating Rdy_Bsy_n has changed states, but only if the SigChg bit is HIGH and the card is configured to function in the I/O mode.

The Changed bit is reset to zero by a reset condition. Note that this bit is read-only.

SigChg

As a readable and writable bit, SigChg controls whether the stschg_n pin reflects the Changed bit status. If SigChg is HIGH, the stschg_n pin indicates the status of the Changed bit when the card is configured with I/O Space. If SigChg is LOW, the stschg_n pin will be held HIGH when the card is configured with I/O Space.

This bit is reset LOW during a reset condition.

IOis8, XE_N, Audio, and PwrDwn

These bits are unused in this implementation of the CF+ card. If the user desires to enable the functionality of these bits, code must be added to the source files. If a read is performed on the CSR, all of these bits will be LOW with the exception of IOis8, which will be HIGH.

A reset has no effect on these bits.

Int

The Int bit reflects the status of an interrupt request from the I/O Space, regardless of the setting of Conf2, the interrupt enable/disable bit. When HIGH, this bit indicates an interrupt is pending. The bit will clear when the interrupt has been serviced. This bit is read only and is reset to zero during a reset condition.

Pin Replacement Register

Located in the Attribute Memory space, this is an optional register that indicates the status of pins that have been remapped during I/O Space configuration. Some pins lose their functionality during I/O Space configuration, compared to Memory Mode configuration. Specifically, the rdy/–bsy pin from Memory Mode becomes ireq_n during I/O Mode. This register is 8 bits wide and is described in Table 8.

Table 8: **Pin Replacement Register**

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CRdy_Bsy_n	CWProt	1	1	Rdy_Bsy_n	WProt
Write	0	0	Host_CRdy_Bsy_n	CWProt	0	0	MRdy_Bsy_n	MWProt

Bits D2, D3, D6 and D7 are not writable. Bits D2 and D3 will be read as logic HIGH, whereas bits D6 and D7 will be read as a logic LOW.

CRdy_Bsy_n

When Rdy_Bsy_n changes state, this bit is set to a logic HIGH. This bit may also be written to by the host and is designated as Host_CRdy_Bsy_n in the source files. This bit is set LOW during a reset.

CWProt

Since write protect is not used as detailed in the CompactFlash specification, CWProt is unused in the source files and will read logic LOW.

Rdy_Bsy_n

This bit represents the internal state of the rdy/−bsy pin when it has been reallocated as ireq_n when the card has been configured for I/O Mode. When rdy/−bsy changes states (due to the cm_sts pin in this implementation), this bit reflects that state. When written HIGH by the host, this bit acts as a mask so that Host_CRdy_Bsy_n may be written by the Host. Writing to this bit is by using the MRdy_Bsy_n bit in the source code. This bit is set LOW during a reset condition.

WProt

Since write protect is not used as specified by the CompactFlash specification, this bit and MWProt are unused in this implementation. This bit is read as a logic LOW.

Common Memory

The functionality for the Common Memory space may be found in the reference design source file named cf_plus_control.vhd.

Common Memory has been implemented assuming an Intel StrataFlash 28F320J3 flash memory is used. Since there are only 11 address lines on the CF+ interface, there are only 2 kB of addressable common memory for the card. Common Memory is typically used as a working memory space which contains mapping of the larger memory arrays found in the I/O Space using True IDE Mode. Larger memory arrays are not included in this implementation, but can be added by the user.

The CF+ controller implements all functionality when interfacing the Common Memory. This includes addressing, byte mode select, reset, memory status, chip select and reset.

Addressing

The Intel StrataFlash memory can be accessed in either 16-bit or 8-bit modes. This works well with the CompactFlash specification since the interface is accessed by the HBA in either 16-bit or 8-bit modes. To access the Common Memory, reg_n must be HIGH. By using ce1_n and ce2_n the 16-bit or 8-bit modes can be selected as required. When in 16-bit mode, cm_addr(0) is driven HIGH or LOW depending on host_addr(0). When in 8-bit mode with cm_addr(0) HIGH, the high (odd) byte is accessed from Common Memory. Conversely, when in 8-bit mode, cm_addr(0) is LOW accessing the low (even) byte of Common Memory. When in 16-bit mode, cm_addr(0) is ignored by the flash memory. Addresses cm_addr(10:1) are used to specify the location of the byte or word in memory. Table 9 describes this relationship.

Table 9: **Common Memory Addressing Modes**

Addressing Mode	cm_addr(10:1)	cm_addr(0)	cm_byte_n
8-bit	host_addr(10:1)	host_addr(0)	0
16-bit	host_addr(10:1)	1	1

The signal cm_byte_n is used to indicate to the memory that byte mode is selected and is active LOW.

Memory status is reflected on the ireq_n pin, acting as rdy/−bsy in Memory Mode. This status is also available in the Rdy_Bsy_n bit of the PRR. The state of rdy/−bsy is directly related to the cm_sts pin of the Common Memory Interface.

I/O Space

Most I/O Space functionality is found in the reference design source file named dsp_interface.dsp. The interface state machine is located in this file. Some control signals are located in cf_plus_control.vhd. The pulse mode IRQ requires use of the counter found in upcnt6.vhd.

For the I/O Space, the CF+ specification states that either 8-bit or 16-bit I/O access is allowable. This application note describes the implementation of an 8-bit I/O Space as provided in the reference design. If 16-bit access is required, the reference design can easily be modified to

support this requirement. There are comments placed throughout the source files (VHDL) to convert the I/O Space to 16-bit access, although 16-bit I/O Space access has not been tested.

Clock

This Compact Flash implementation requires an 80 MHz clock signal to be supplied to the CPLD. This particular implementation with the Analog Devices ADSP-218xN series DSP, uses the CLKOUT signal found on the DSP as the clock source. CLKOUT is a signal provided by the DSP and is double the input clock signal to the DSP found on pin CLKIN. This implementation assumes a 40 MHz clock on CLKIN of the DSP which subsequently becomes 80 MHz on CLKOUT. The CPLD requires this 80 MHz signal on the dsp_clk pin to function correctly. If a different clock speed is required for another implementation, it is recommended that a functional and post-route simulation be performed to ensure correct functionality is retained.

Although the CF+ interface itself contains no clock, this 80 MHz clock can be used to ensure proper timing of the interface signals.

Addressing I/O Space Registers

Three registers are provided as the communications venue to/from the I/O Space interface: Address Register, Data Register, and Status Register. There is no direct communication with the I/O Space—the communication is instead provided indirectly through these three registers. Their functionality is described in the following sections.

To gain access to these registers, there are two sets of addresses: one for the DSP and one for the HBA. This is intended to provide access to the same registers using two different memory maps. Table 10 describes this addressing scheme.

Table 10: **Addressing I/O Space Registers**

DSP Address	HBA Address	Register	Description
001h	400h	io_addr_reg	Address Register
002h	401h	io_data_reg	Data Register
003h	402h	io_status_reg	Status Register

Address Register

An 8-bit register is provided to pass address data to the DSP from the HBA, or in the reverse direction, from the DSP to the HBA.

Data Register

Similarly, the Data Register is an 8-bit register that is used to pass data to/from the I/O Space. It is read/write capable from both the DSP and the HBA.

Status Register

As a read-only register, Status Register contains information regarding the current Data Register and Address Register transactions. Table 11 describes the relationship of the bits in the register. All unused bits (D5:D2) are available for user implementation, as in the case of inserting additional I/O Space registers.

Table 11: **I/O Space Status Register**

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	IRQ_CF	IRQ_DSP	0	0	0	0	DataReg	AddrReg
Write	0	0	0	0	0	0	0	0

IRQ_CF

When new data is available in the Data Register or the Address Register given by the DSP, this bit supplies an interrupt request to the HBA. A HIGH condition triggers an active LOW interrupt on ireq_n, provided interrupts are enabled in Conf(0) of the COR. An interrupt condition is recorded in the Int bit of the CSR regardless of the Conf(0) bit state.

To safeguard data in the Address and Data Registers prior to the HBA reading the new data, the HBA is not permitted to write to these registers until the IRQ_CF bit has cleared. This bit is cleared when the HBA reads data from either the Address or Data Registers or a card reset has been performed.

The IRQ_CF bit is found in the reference design source files as io_status_reg(7).

IRQ_DSP

When new data is available in the Data Register or the Address Register given by the HBA, this bit, in a HIGH state, indicates an interrupt request is pending to the DSP. This reference design does not utilize an interrupt request pin for the DSP, and therefore, this bit is unused throughout this implementation. This bit is available only for the purposes of the user if an interrupt request pin is desired to be added for a specific application.

To safeguard data in the Address and Data Registers prior to the DSP reading the new data, the DSP is not permitted to write to these registers until the IRQ_DSP bit has cleared. This bit is cleared when the DSP reads data from either the Address or Data Registers or a card reset has been performed.

This bit is found in the reference design source files as io_status_reg(6).

DataReg

When the Data Register has been written by either the DSP or the HBA, this bit is set HIGH. This bit is used to indicate the Data Register has been written when an interrupt has been detected by the system monitoring interrupts. This bit is cleared when the Data Register has been read by the target system, or a card reset has been issued.

This bit is found in the reference design source files as io_status_reg(1).

AddrReg

When the Address Register has been written by either the DSP or the HBA, this bit is set HIGH. This bit is used to indicate the Address Register has been written when an interrupt has been detected by the system monitoring interrupts. This bit is cleared when the Address Register has been read by the target system, or a card reset has been issued.

This bit is found in the reference design source files as io_status_reg(0).

State Machine

The I/O Space interface state machine synchronizes the communication between the DSP and the HBA and relies on the 80MHz clock provided to the CPLD. This state machine consists of seven states, including the IDLE state. Two basic paths in the state machine are available: communication initiated by the DSP and communication initiated by the HBA. Figure 3 displays the flow as described in the following paragraphs.
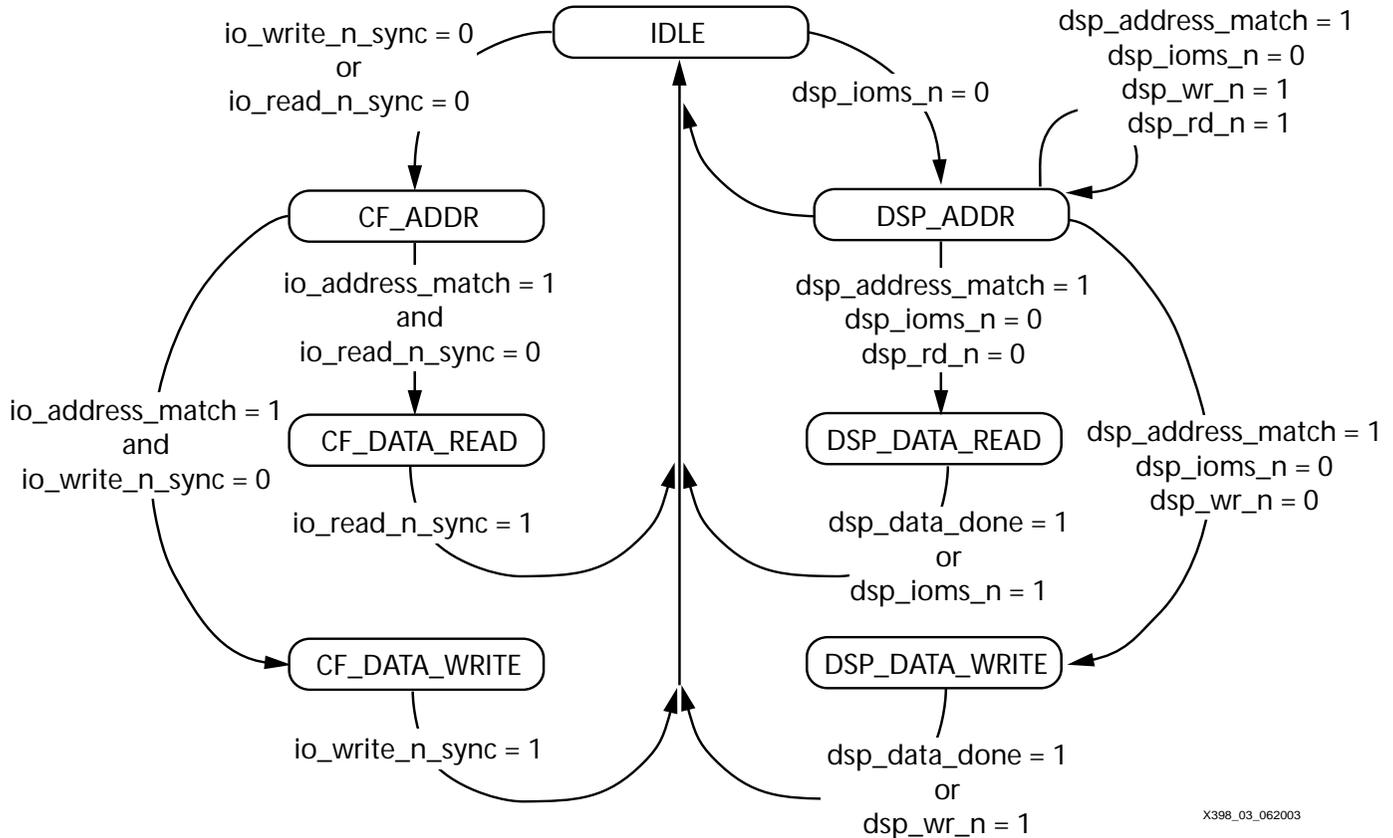
Figure 3: **I/O Space State Machine**

IDLE State

The default state upon reset, is the IDLE state. In this state, the machine waits for either the DSP or the HBA to initiate communications with the I/O Space registers. For a DSP initiated data transfer, the state machine follows the right hand branch shown in Figure 3, whereas an HBA data transfer is contained in the left hand path of Figure 3. The signal dsp_ioms_n represents the ioms_n pin as it is driven by the DSP. The signals io_write_n_sync and io_read_n_sync are the active low write and read request conditions as driven by the HBA. The latter two are synchronized to the state machine using the 80 MHz clock.

DSP Read/Write

When a chip select condition has been detected as found on the ioms_n pin, the state machine transitions to the DSP_ADDR state. During this branch of the machine, no HBA transactions can occur with the I/O Space registers. The DSP_ADDR state waits for a valid address for one of the registers in the I/O space. Once a valid address has been detected, the state machine transitions to the DSP_DATA_READ or DSP_DATA_WRITE state, depending on the status of the dsp_rd_n and dsp_wr_n pins.

The DSP_DATA_READ state allows data from the I/O space registers to be placed on the DSP data bus. Once the data has been transferred to the DSP, the state machine transitions to the IDLE state.

The DSP_DATA_WRITE state permits the DSP to transfer data from the data bus to the register being addressed. Once data has been captured in these registers, the state machine transitions to the IDLE state.

HBA Read/Write

When the HBA issues a request for data from the I/O space, as indicated using the io_write_n_sync and io_read_n_sync signals, and the state machine is in the IDLE state, the machine branches to the CF_ADDR state. It is in this state that the machine waits for a valid address from the HBA to access the I/O space registers. Once a valid address has been detected from the HBA as indicated with io_address_match at a HIGH level, the state machine transitions to either the CF_DATA_READ_STATE or CF_DATA_WRITE_STATE state. The signals io_read_n_sync and io_write_n_sync direct the state machine to the respective state when one of these signals is LOW.

Once in the CF_DATA_READ_STATE state, data is placed from the addressed I/O Space register to the HBA data bus. Once the HBA has received the data and removed the read condition from the CF+ interface, the state machine transitions to the IDLE state.

The CF_DATA_WRITE_STATE state allows data to be written to the addressed I/O Space register from the HBA data bus. After the HBA has written the data and removed the write condition from the CF+ interface, the state machine moves to the IDLE state.

Source Code Download

The VHDL source code and test benches are available for this design. THE DESIGN IS PROVIDED TO YOU "AS IS". XILINX MAKES AND YOU RECEIVE NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, STATUTORY OR OTHERWISE, AND XILINX SPECIFICALLY DISCLAIMS ANY IMPLIED WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR A PARTICULAR PURPOSE. This design has not been verified on hardware (as opposed to simulations), and it should be used only as an example design, not as a fully functional core. XILINX does not warrant the performance, functionality, or operation of this Design will meet your requirements, or that the operation of the Design will be uninterrupted or error free, or that defects in the Design will be corrected. Furthermore, XILINX does not warrant or make any representations regarding use or the results of the use of the Design in terms of correctness, accuracy, reliability or otherwise.

XAPP398 - http://www.xilinx.com/products/xaw/coolvhdlq.htm

To simulate the files included in the download, it is necessary to obtain the VHDL model of the Intel StrataFlash 28F320J3 memory from the Intel website. To obtain this VHDL model, visit **http://appzone.intel.com/toolcatalog/listtools.asp?pid=5319&cid=683&pfamily=**

Disclaimer

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Conclusion

The CoolRunner-II CPLD is the perfect device to use as an interface to a CompactFlash host. These CPLDs exhibit low power consumption as well as other features that are beneficial to these cards. Features such as 3.3V I/Os, Schmitt Triggers and DualEDGE clocking allow easy integration to this type of system as well as provide flexibility to other functions on a CompactFlash card.

Further Reading

Application Notes

http://www.xilinx.com/xapp/xapp371.pdf (Galois Field GF (2^m) Multiplier)

http://www.xilinx.com/xapp/xapp372.pdf (Smart Card Reader)

http://www.xilinx.com/xapp/xapp373.pdf (Avoiding CPLD Brownout)

http://www.xilinx.com/xapp/xapp374.pdf (CryptoBlaze)

http://www.xilinx.com/xapp/xapp375.pdf (Timing Model)

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http://www.xilinx.com/xapp/xapp394.pdf (Interfacing with Mobile SDRAM)
http://www.xilinx.com/xapp/xapp395.pdf (Using DataGATE)
http://www.xilinx.com/xapp/xapp398.pdf (CompactFlash Card Interface)

CoolRunner-II Data Sheets

http://direct.xilinx.com/bvdocs/publications/ds090.pdf (CoolRunner-II Family Datasheet)
http://direct.xilinx.com/bvdocs/publications/ds091.pdf (XC2C32 Datasheet)
http://direct.xilinx.com/bvdocs/publications/ds092.pdf (XC2C64 Datasheet)
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CoolRunner-II White Papers

http://www.xilinx.com/publications/products/cool2/wp_pdf/wp165.pdf (Chip Scale Packaging)
http://www.xilinx.com/publications/whitepapers/wp_pdf/wp170.pdf (Security)
http://www.xilinx.com/publications/whitepapers/wp_pdf/wp197.pdf (Cipher Stream Protocol)
http://www.xilinx.com/publications/whitepapers/wp_pdf/wp198.pdf (Cell Phone Handsets)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/23/03	1.0	Initial Xilinx release.