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Implementing DDR2-400 Memory Interfaces in Spartan-3A FPGAs

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Summary

High-performance consumer products and their requirement for low-cost, high-bandwidth memory create demand for high-performance DDR2 memory interfaces. Xilinx offers a Memory Interface Generator (MIG) integrated in the CORE Generator™ software for ultimate design flexibility and ease-of-use. MIG is a free, user-friendly tool designed to create memory interfaces in unencrypted RTL. This tool supports multiple memory architectures across a variety of FPGA selections, providing system designers with the flexibility to easily customize their own design.

Spartan®-3A FPGAs with the higher speed grade (-5) have been specified for operation up to DDR2-333 using a 166 MHz clock, while lower speed grade (-4) devices have been specified for operation up to DDR2-266 using a 133 MHz clock. Based on demand for even higher performance, Xilinx has validated a DDR2-400 (200 MHz clock) memory interface in Spartan-3A FPGAs with the higher speed grade (-5). The validation results also apply to Spartan-3AN and Spartan-3A DSP FPGAs with the higher speed grade (-5).

The DDR2-400 memory interface discussed in this application note is derived from the default output of MIG. The design is fully verified in hardware using Spartan-3A FPGAs with the higher speed grade (-5) assembled on Spartan-3A Starter Kits. The validation effort includes characterization at different process corners, as well as temperature and voltage variations that meet commercial grade requirements.

Purpose

The goal of this application note is to thoroughly document all aspects of the DDR2-400 memory interface to allow customers to leverage it in their own applications, drastically reducing development time. This document has the following organization:

- Memory Interface
  - Component Configuration
  - Changes to Standard MIG Output
  - Timing Budgets for 200 MHz
- Verification Platform
  - Reference Clock Quality
  - Signal Termination and Signal Integrity
  - Component Placement and Routing
- Verification Design and Process
  - Functional Description
  - Error Checking via Frame CRC
  - Power Supply Control via the RS-232 Interface
  - Reference Clock Generation
  - Verification Plan
  - Results

The information presented in this application note applies to implementation of similar DDR2-400 memory interfaces with point-to-point connections and JEDEC compatible DDR2 memory devices.

Memory Interface

A wide variety of DDR2 components are available from a number of memory vendors. The DDR2-400 memory component selection is made while keeping two important project goals in mind.

The first goal is to leverage existing memory interface source code from MIG. By avoiding substantial changes or redesign, the need for logical reverification of the memory interface is eliminated. Currently, the MIG-based memory interface for Spartan-3A FPGAs supports DDR2 devices with a CAS latency of three. Therefore, a device offering DDR2-400 performance with CL = 3 is required.

The second goal is to verify the design in hardware, a task that requires a test board. While it is possible to build a unique board specifically for test, the existing Spartan-3A Starter Kit is already populated with a memory device offering DDR2-400 performance with CL = 3. The use of the Spartan-3A Starter Kit for hardware verification eliminates the expense of designing a unique board for verification.

Component Configuration

The selected DDR2-400 capable memory device with CL = 3 is a Micron Technology MT47H32M16BN-3:D, a 512 Mb device organized as 8 Meg x 16 bits x 4 banks. This device is standard on production Spartan-3A Starter Kits. It has superior AC performance characteristics compared to the lower performance MT47H32M16BN-5E:D but is priced similarly. The device interfaces to the Spartan-3A FPGA using point-to-point connections as shown in Figure 1.

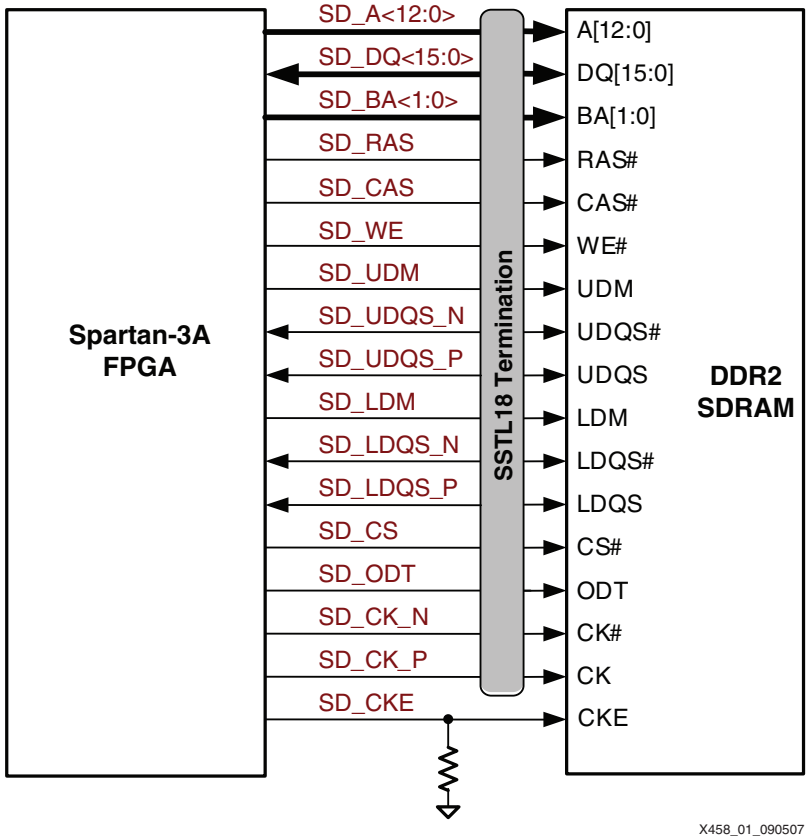

Figure 1: **Point-to-Point Memory Interface**

The Spartan-3A FPGA, which is a Xilinx XC3S700A-5FG484C, is a higher speed grade (-5) device that accommodates the higher performance memory interface. This device is not standard on production Spartan-3A Starter Kits. The test boards for hardware verification are reworked to replace the lower speed grade (-4) devices with higher speed grade (-5) devices.

Changes to Standard MIG Output

The memory interface realized in this application note is derived from MIG output but is not available directly from MIG. The memory interface is initially created using MIG with the parameter settings shown below. For more information on MIG and how to use it, refer to UG086, *Memory Interface Solutions User Guide*. Some minor modifications are made to accommodate the Spartan-3A Starter Kit, operation at 200 MHz, and the needs of the verification design.

```
****************************************
Part                      : XC3S700A-FG484
Frequency in MHz          : 133
Speed grade               : 4
No of controllers         : 1
DCM used                  : 1
Add test bench            : 1
Number of write pipes     : 4
****************************************
Memory type               : MT47H32M16XX-5E
  Bits per strobe         : 8
  Banks for data          : 3
  Data bits               : 16
  Banks for addr & ctrl   : 1
  Row address bits        : 13
  Column address bits     : 10
  Bank address bits       : 2
****************************************
Mode Register
  Burst Length            : 4(010)
  Burst Type              : Sequential(0)
  CAS Latency             : 3(011)
  Mode                    : Normal(0)
  DLL Reset               : Yes(1)
  Write Recovery          : 3(010)
  PD Mode                 : Fast Exit(0)
Extended Mode Register
  DLL Enable              : Enable-Normal(0)
  Output Drive            : Full Strength(0)
  RTT (nominal)           : RTT Disabled(00)
  Additive Latency        : 0(000)
  OCD Operation           : OCD Exit(000)
  DQS# Enable             : Enable(0)
  RDQS Enable             : Disable(0)
  Outputs                 : Enable(0)
****************************************
```

The scope of the changes is small enough that it is not necessary to logically reverify the interface code for correctness. The modified memory interface is assumed to function correctly, which is a valid assumption, based on the system functional simulation and the ultimate hardware verification.

Changes Specific to the Spartan-3A Starter Kit (RTL and UCF)

In addition to providing a generic DDR2 memory interface, MIG also provides a design customized specifically for the Spartan-3A Starter Kit. The design is known good, materially the

same as the generic design, and has a few modifications noted in the documentation provided with the files. Relevant modifications are summarized below for reference:

- The sys_clk reference clock input is modified from differential to single ended.
- The input data capture FIFOs are modified to support routing requirements of the pinout.
- The UCF is modified to reflect these RTL modifications and pinout of this board.

Users of MIG who are targeting a configuration that differs from the Spartan-3A Starter Kit should be aware that the memory interface used in the verification design is intended for the Spartan-3A Starter Kit and contains these modifications. However, the changes specific to the Spartan-3A Starter Kit are not required for general DDR2-400 operation.

Changes Specific to 200 MHz (RTL and UCF)

Minor modifications to the baseline Spartan-3A Starter Kit memory interface are required to accommodate operation at 200 MHz. The code changes are described in the documentation provided with the source code to the verification design. The RTL modifications and their purposes are summarized here:

- The initialization counter is modified to increase the time-out value to guarantee a 200 µs interval with a 200 MHz system clock. Without this change, the memory interface begins the initialization process too early. This particular modification is made in the counter code itself, because the time-out value is not a parameter.
- The refresh counter is modified to increase the time-out value (the max_ref_cnt parameter) to reduce the refresh rate. Without this change, the memory interface issues substantially more refresh cycles than necessary.
- The refresh-to-active counter is modified to increase the time-out value (the rfc_count_value parameter) to satisfy the memory timing requirements with a 200 MHz system clock. Without this change, the memory interface does not wait enough cycles for the refresh-to-active interval, thereby violating this specification.
- For experimental purposes, an additional control input is added to the memory interface to allow the user to disable the refresh counter. In general use cases, this feature has limited utility and is not required for DDR2-400 operation.
- The system clock generation is modified to accept a 50 MHz input and multiply it up to 200 MHz before feeding it into the memory interface. This modification allows the use of the 50 MHz oscillator on the Spartan-3A Starter Kit, with a penalty of extra jitter. While a direct 200 MHz differential clock signal is preferred, the Spartan-3A Starter Kit has limited provisions to connect such a signal source.

The UCF also has modifications to support operation at 200 MHz. The timing specifications are scaled, and additional placement and routing constraints are added to ensure consistent results. The modifications and their purposes are summarized below:

- Timing specifications are scaled for 200 MHz operation. The PERIOD constraint is reduced below 5.000 ns, and the MAXDELAY constraints are also scaled, where appropriate.
- Location constraints are added to the Digital Clock Managers (DCMs) and Global Clock Buffers (BUFGs). Signals between these primitives not routed on dedicated resources are constrained with Directed Routing (DIRT) constraints in the UCF, which eliminate variability in the clocking circuits that might result from automatic placement and routing. The result is shown in Figure 2.

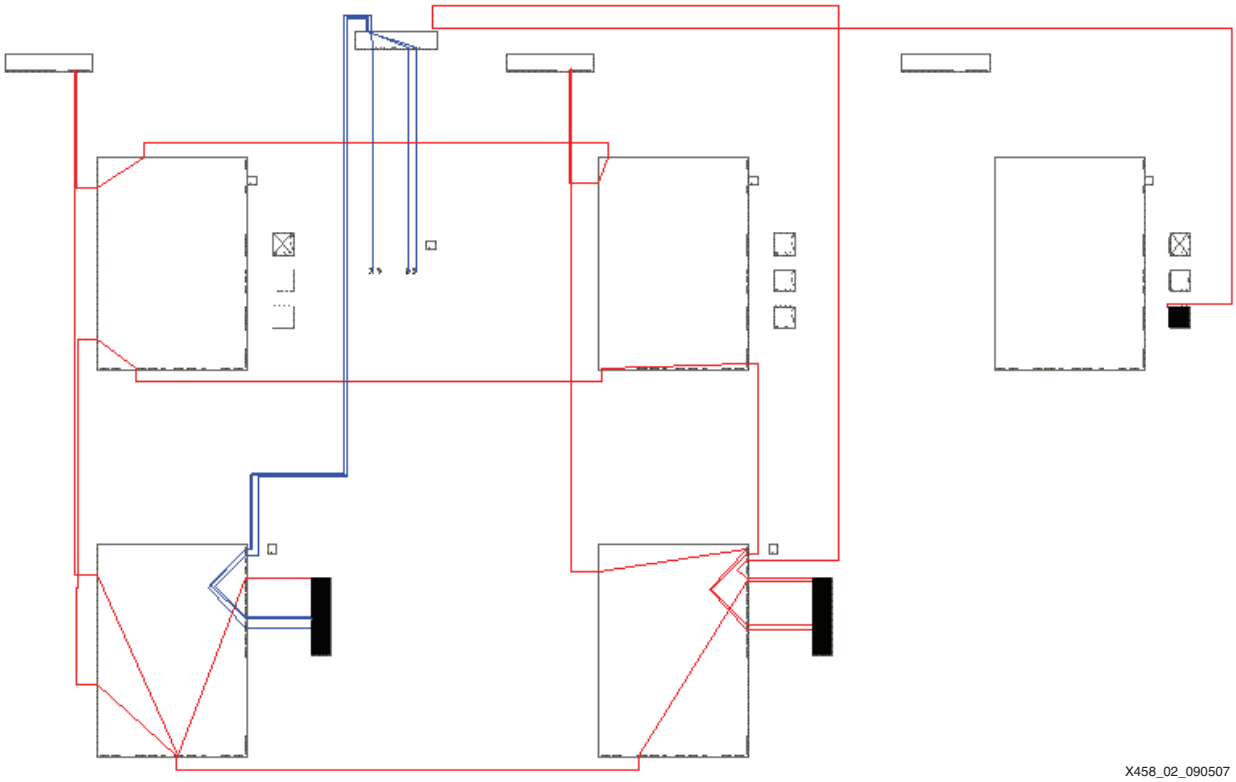

Figure 2: **Global Clock Resources with Placement and Routing Constraints**

- All logic involved in the input capture circuit is placed in the standard constraint file. To ensure consistent results, all critical routes in the input capture circuit are given DIRT constraints in the UCF. These circuits are discussed in detail in XAPP768c, *Interfacing Spartan–3 Devices With 166 MHz or 333 Mb/s DDR SDRAM Memories*. The input capture logic for the top byte is shown in Figure 3, page 6, and the input capture logic for the bottom byte is shown in Figure 4, page 7.

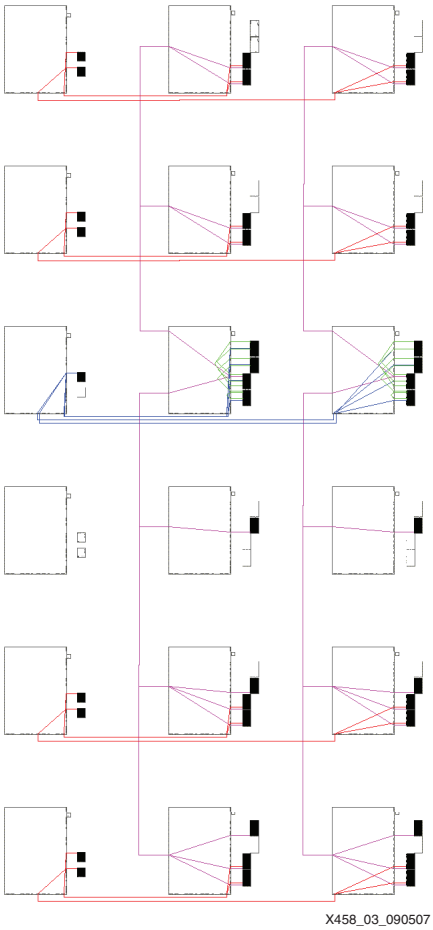

Figure 3: **Top Byte Input Capture with Placement and Routing Constraints**

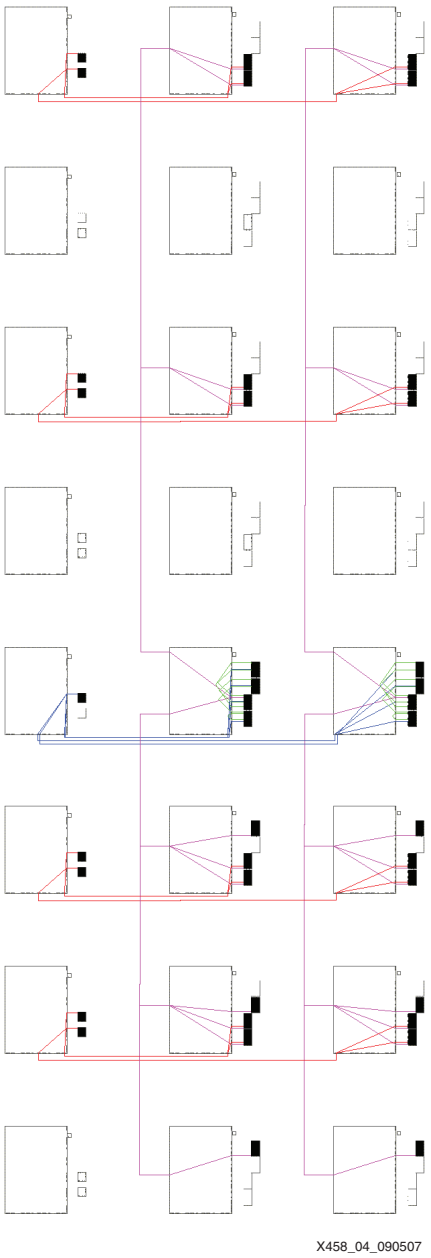

Figure 4: **Bottom Byte Input Capture with Placement and Routing Constraints**

DIRT constraints are not required in generic MIG designs. The location constraints in the generic design place the I/O and input capture logic in an arrangement that is recognized by the router. Upon recognizing this arrangement, the router uses a “template” to route signals with low skew and low delay. However, if the arrangement is not recognized, or low-skew and low-delay routing channels are unavailable, the router does not issue a warning.

In the DDR2-400 design, DIRT constraints are applied to ensure that the same low-skew and low-delay routes are used in every route attempt. The success of the DIRT constraints are verified in the place-and-route report. The DIRT constraints cover additional intermediate routes that are drawn in green in Figure 3 and Figure 4. In this manner, the timing results for the input capture are 100% reproducible.

Hierarchy and Implementation

MIG output for the Spartan-3A Starter Kit is generated with clocking resources and a test bench; no option is provided to eliminate the clocking resources or the test bench. The test

bench includes a small hardware test application that generates and checks a sequence of memory accesses.

For small designs, it is easy to replace the hardware test application with the desired user application. For larger designs, it is desirable to use the memory interface as a sub-module. The hardware test application is therefore removed from “main_0”, and the exposed memory interface signals are exported. The resulting structure has clocking resources but no test bench, which is one of the four generation options available for the generic MIG design.

The synthesis, mapping, and place-and-route options for the DDR2-400 design on the Spartan-3A Starter Kit are similar to the generic MIG design, but employ higher effort levels for better performance.

Timing Budgets for 200 MHz

Evaluation of the PERIOD and MAXDELAY constraints by the static timing analyzer is not sufficient to determine if the memory interface is functional at a particular frequency. The PERIOD constraint covers the internal timing between synchronous elements, and the MAXDELAY constraints cover portions of other critical paths.

XAPP768c, *Interfacing Spartan–3 Devices With 166 MHz or 333 Mb/s DDR SDRAM Memories*, and XAPP454, *DDR2 SDRAM Memory Interface for Spartan-3 FPGAs*, both discuss the concept of timing budgets for the interface between the FPGA and the memory device. Five timing budgets are to be considered. All timing budgets must pass; otherwise the memory interface cannot be expected to function at the DDR2-400 performance level. The timing budgets are:

- DDR Read
- DDR Write
- SDR Output
- Loopback
- Clock to Memory

Most timing data used in these budgets is obtained from the device data sheets. Additional data is obtained from Xilinx ISE® software. Assumptions and other important notes are discussed with each budget.

The DDR Read timing budget pertains to the input data capture scheme when the Spartan-3A FPGA is receiving data from the memory device. The input capture scheme is discussed in detail in XAPP768c, *Interfacing Spartan–3 Devices With 166 MHz or 333 Mb/s DDR SDRAM Memories*. Table 1 through Table 3 show the DDR Read timing budget for DDR2-400 operation.

Package skew data for Spartan-3A FPGAs is not published; internal Xilinx data is used instead. For designs in other Spartan-3A FPGA selections, the user should file a support case with Xilinx Technical Support. The board layout skew between signals in each signal group (data and strobe, address and control) is assumed to be 50 ps or less, which is a realistic amount in a point-to-point connection, provided that some attention is paid to delay matching during board routing.

Table 1: **DDR Read Timing Budget**

Parameter	Value	Leading-Edge Uncertainties	Trailing-Edge Uncertainties	Meaning
Master Clock Frequency in MHz	200	0	0	Master clock frequency
Tclock	5000	0	0	Master clock period
Tclock_phase	2500	0	0	Clock phase (half period)

Table 1: **DDR Read Timing Budget *(Cont'd)***

Parameter	Value	Leading-Edge Uncertainties	Trailing-Edge Uncertainties	Meaning
Tclock_duty_cycle_dist	240	0	0	DCM/BUFG duty cycle distortion from the FPGA data sheet
Tdata_period	2260	0	0	Total data period, Tclock_phase - Tclock_duty_cycle_dist
Tdqsq	350	350	0	Strobe to data distortion from memory data sheet
Tpackage_skew	60	60	60	Package skew for XC3S700A-FG484
Tds	-70	-70	0	Setup time for RAM16X1D from the FPGA data sheet, parameter Tds
Tdh	130	130	0	Hold time for RAM16X1D, from FPGA data sheet, parameter Tdh
Tjitter	0	0	0	Common clock means all signals jitter together; this is zero
Tlocal_clock_skew	64	64	64	Skew on local clock as reported in PAR clock summary
Tqhs	450	0	450	Hold skew for DQ from the memory data sheet
Tpcb_layout_skew	50	50	50	Skew between data and strobes on the board (assumed)
Total Uncertainties		584	624	Worst case for leading and trailing can never happen simultaneously
Window for DQS Position	**1052**	**584**	**1636**	

The duty cycle distortion of the global clock resources at 200 MHz is listed here as 240 ps although the device data sheet indicates the value is 350 ps. Based on extensive data, Xilinx tightened the duty cycle distortion specification for the circuits used in this particular application, specifically at 200 MHz. While this gain seems immaterial here, it plays a significant role in a subsequent timing budget.

Table 2: **Delay Details for DDR Read Timing Budget**

Parameter	Value	Meaning
Data Delay (IOB to FIFO)	386	Measured in FPGA Editor
Local Clock Route Delay	421	As reported in the PAR summary
DQS Delay from IOB to LUT	418	Measured in FPGA Editor
LUT Delay for DQS	620	LUT delay from the FPGA data sheet
Total DQS Delay	**839**	

The total extra DQS delay must be within the lower and upper bounds of the data valid window, and the total result is PASS (see Table 3).

Table 3: **LUT Delay Derating Values**

Parameter	100%	90%	80%	70%	60%	50%	40%
Data Delay	386	347	309	270	232	193	154
LUT Delay	620	558	496	434	372	310	248
Number of LUTs in a Clock Phase	4	4	5	6	7	8	10
Number of LUTs to Delay DQS	1	2	2	3	3	4	5
Total DQS Delay	1459	1871	1663	1889	1619	1660	1576
Total Extra DQS Delay	1073	1524	1354	1619	1388	1467	1421
Data Valid Window (Lower Bound)	584	566	547	529	510	492	474
Data Valid Window (Upper Bound)	1636	1648	1661	1673	1686	1698	1710
	PASS	**PASS**	**PASS**	**PASS**	**PASS**	**PASS**	**PASS**

The DDR Write timing budget pertains to the output data generation scheme when the Spartan-3A FPGA is transmitting data to the memory device using DDR output flip-flops. Table 4 shows the DDR Write timing budget for DDR2-400 operation.

Table 4: **DDR Write Timing Budget**

Parameter	Value	Leading-Edge Uncertainties	Trailing-Edge Uncertainties	Meaning
Tclock	5000	0	0	Master clock period
Tclock_phase	2500	0	0	Clock phase (half period)
Tclock_duty_cycle_dist	240	0	0	DCM/BUFG duty cycle distortion from the FPGA data sheet
Tdata_period	2260	0	0	Total data period, Tclock_phase - Tclock_duty_cycle_dist
Tds	400	400	0	DQ and DM input setup time relative to DQS from the memory data sheet, Tds
Tdh	400	0	400	DQ and DM hold time relative to DQS from the memory data sheet, Tdh
Tpackage_skew	60	60	60	Package skew for XC3S700A-FG484
Clock_tree_skew	87	87	87	Clock tree skew for DDR signals measured in the FPGA Editor

Table 4: **DDR Write Timing Budget *(Cont'd)***

Parameter	Value	Leading-Edge Uncertainties	Trailing-Edge Uncertainties	Meaning
Tjitter	0	0	0	Common clock means all signals jitter together; this is zero
Tclock_out_phase	200	200	200	Phase offset between outputs of DCM from the FPGA data sheet
Tpcb_layout_skew	50	50	50	Skew between data and strobes on the board (assumed)
Data Valid Window Edges		797	797	Includes 2 * Tjitter
Margin	**666**	**Budget PASS**		

The SDR Output timing budget pertains to the output address and control generation scheme when the Spartan-3A FPGA is accessing the memory device using output flip-flops. Table 5 shows the SDR Output timing budget for DDR2-400 operation.

Table 5: **SDR Output Timing Budget**

Parameter	Value	Leading-Edge Uncertainties	Trailing-Edge Uncertainties	Meaning
Tclock	5000	0	0	Master clock period
Memory Address and Control Input Setup Time (Tis)	375	375	0	Address and control input setup from the memory data sheet
Memory Address and Control Input Hold Time (Tih)	375	0	375	Address and control input hold time from the memory data sheet
Tpackage_skew	60	60	60	Package skew from packaging team for XC3S700A-FG484
Tjitter	0	0	0	Common clock means all signals jitter together; this is zero
Tclock_tree_skew	78	78	78	Clock tree skew for SDR signals measured in FPGA Editor
Tpcb_layout_skew	50	50	50	Skew between address and control signals on the board (assumed)
Tclkout_phase	200	200	200	Phase offset between outputs of the DCM from the FPGA data sheet
Data Valid Window Edges		763	763	Includes 2 * Tjitter
Margin	**3474**	**Budget PASS**		

The Loopback timing budget pertains to the input data capture scheme when the Spartan-3A FPGA is receiving data from the memory device. This additional budget supplements the DDR

Read timing budget and is related to the write-enable generation for the input capture scheme. Table 6 shows the Loopback timing budget for DDR2-400 operation.

Table 6: **Loopback Timing Budget**

Parameter	Leading-Edge Delays	Trailing-Edge Delays	Meaning
Tclock	5000	0	Master clock period
Tclock_phase	2500	0	Clock phase (half period)
Delay Details for DQS			
DQS Delay from IOB to LUT	418	418	The delay of the DQS line from the input buffer to the LUT
DQS Local Clock Route Delay	421	421	The delay of the DQS line from the output of LUT delay element
Total DQS Delay	839	839	The LUT delay on DQS is not considered, since both DQS and rst_dqs_div signals are delayed the same amount
Delay Details for Loopback			
rst_dqs_div Delay from IOB to LUT	668	668	Constrained using MAXDELAY constraints; value from the PAR report
delayed_rst_dqs_div Delay to LUT	871	871	Constrained using MAXDELAY constraints; value from the PAR report
LUT delay (OR gate)	620	620	Implemented in a single LUT
fifo_1_wen Delay from LUT	1041	1041	Constrained using MAXDELAY constraints; value from the PAR report
Total Loopback Signal Delay	3200	3200	Sum of all delays listed
Margin	**2639**	**2639**	**Budget PASS**

The Clock-to-Memory timing budget evaluates the path from the system clock source, through the Spartan-3A FPGA, to the memory device clock input. The revised duty cycle distortion specification for the global clock resources is essential in this budget for DDR2-400 operation, shown in Table 7.

Table 7: **Clock-to-Memory Timing Budget**

Parameter	Leading-Edge Delays	Trailing-Edge Delays	Meaning
Tclock	5000	0	Master clock period
Tclock_phase	2500	0	Clock phase (half period)
CLKIN_CYC_JITT_DLL_HF	150	150	Cycle-to-cycle jitter of the oscillator (Max set by CLKIN_CYC_JITT_DLL_HF from the Spartan-3A data sheet)
CLKOUT_DUTY_CYCLE_DLL	240	240	DCM/BUFG duty cycle distortion from the FPGA data sheet

Table 7: **Clock-to-Memory Timing Budget *(Cont'd)***

Parameter	Leading-Edge Delays	Trailing-Edge Delays	Meaning
Clock Phase from DCM plus BUFG	2185	2815	Derived after duty cycle distortion and jitter values are subtracted from clock
Memory Clock Jitter	150	150	From the DDR memory data sheet
Memory Duty Cycle Distortion	2250	2750	From the DDR memory data sheet
Memory Input Clock Timing	2183	2833	Derived after jitter and duty cycle distortion parameters are applied to the input clock
Margin	**3**	**18**	**Budget PASS**

All five timing budgets in consideration pass, as do the PERIOD and MAXDELAY constraints. The memory interface is expected to function at the DDR2-400 performance level. The verification process takes the design into the lab to verify the conclusion drawn from the timing budgets.

Verification Platform

The Spartan-3A Starter Kit is used as the verification platform, avoiding the need to design a unique board for the verification of the DDR2-400 memory interface. As an additional convenience, the use of this board allows technical information generated during its design to be leveraged in the project documentation as reference material.

The test boards for hardware verification are reworked to remove the existing lower speed grade (-4) devices, which are replaced with the higher speed grade (-5) devices. Otherwise, the verification platforms use the same board as the kits currently available on the Xilinx website, part numbers HW-SPAR3A-SK-UNI-G, HW-SPAR3AN-SK-UNI-G, and HW-SPAR3ADDR2-DK-UNI-G.

Reference Clock Quality

The DDR2-400 memory interface requires a 200 MHz reference clock. Per the Clock-to-Memory timing budget shown in Table 7, the 200 MHz reference clock must have a cycle-to-cycle jitter of 150 ps or less. This generally requires the direct input of a 200 MHz reference clock from a good source. For new designs, an appropriate 200 MHz reference clock source (typically differential) should be used.

The Spartan-3A Starter Kit has flexible clocking options, but they become limited when the desired frequency exceeds 125 MHz. Most +3.3V, single-ended clock sources are not available at 200 MHz. As a result, a compromise is used for verification purposes. It is discussed later with the verification design.

Signal Termination and Signal Integrity

DS529, *Spartan-3A FPGA Family: Complete Data Sheet*, and UG086, *Memory Interface Solutions User Guide*, indicate the following recommended termination scheme:

- Selection of SSTL18_I versus SSTL18_II for the Spartan-3A FPGA SelectIO™ mode is at the discretion of the user, based on the topology of the board design.
- For single-ended, unidirectional signals: One 50Ω termination to V_{TT}, within 1 inch of the load device.

- For single-ended, bidirectional signals: Two 50Ω terminations, each to V_{TT}, within 1 inch of each device.
- For differential, unidirectional signals: One 100Ω differential termination, between the signal pair, or one 50Ω termination to V_{TT} on each signal of the pair, within 1 inch of the load device.
- For differential, bidirectional signals: Two 100Ω differential terminations, each between the signal pair, or two 50Ω terminations to V_{TT} on each signal of the pair, within 1 inch of each device.
- Where terminations are used, they can be implemented with external resistors and/or the on-die termination feature of the memory device, where appropriate.

In practice, there are a variety of valid termination techniques that cover a spectrum of cost/performance points. In addition to the component cost, another cost to consider is the complexity of placement and routing on a board. Ultimately, the designer is responsible for making sure the selected termination scheme properly addresses the overall system requirements. This involves simulation of any proposed termination scheme and subsequent evaluation of the final result.

The termination scheme in use on the Spartan-3A Starter Kit is a good compromise that yields respectable performance while reducing the component count and board complexity. It is suitable for a point-to-point connection between devices where the signal length is low and the signal loading is light:

- SSTL18_I is selected for the Spartan-3A FPGA SelectIO mode. The memory device uses full strength drivers with on-die termination disabled.
- For single ended, unidirectional and bidirectional signals: One 50Ω termination to V_{TT}, in the middle of the trace, which is roughly 1 inch from both devices.
- For differential, unidirectional and bidirectional signals: One 50Ω termination to V_{TT} on each signal in the pair, in the middle of the trace, which is roughly 1 inch from both devices. Differential signals are effectively treated as two single-ended signals.

The Revision A prototype of the Spartan-3A Starter Kit had additional terminator component footprints to enable the designer to experiment with the termination scheme. Several termination schemes were initially validated through simulation using IBIS models. Subsequent experimentation with the prototype confirmed that the less expensive termination scheme described above produced satisfactory results.

Component Placement and Routing

Placement of relevant devices on the Spartan-3A Starter Kit is shown in Figure 5. The pinout for the memory interface in the Spartan-3A FPGA is located in I/O Bank 3, which is on the left side of IC1. This relative placement is easy to route, given the pinout generated by MIG.

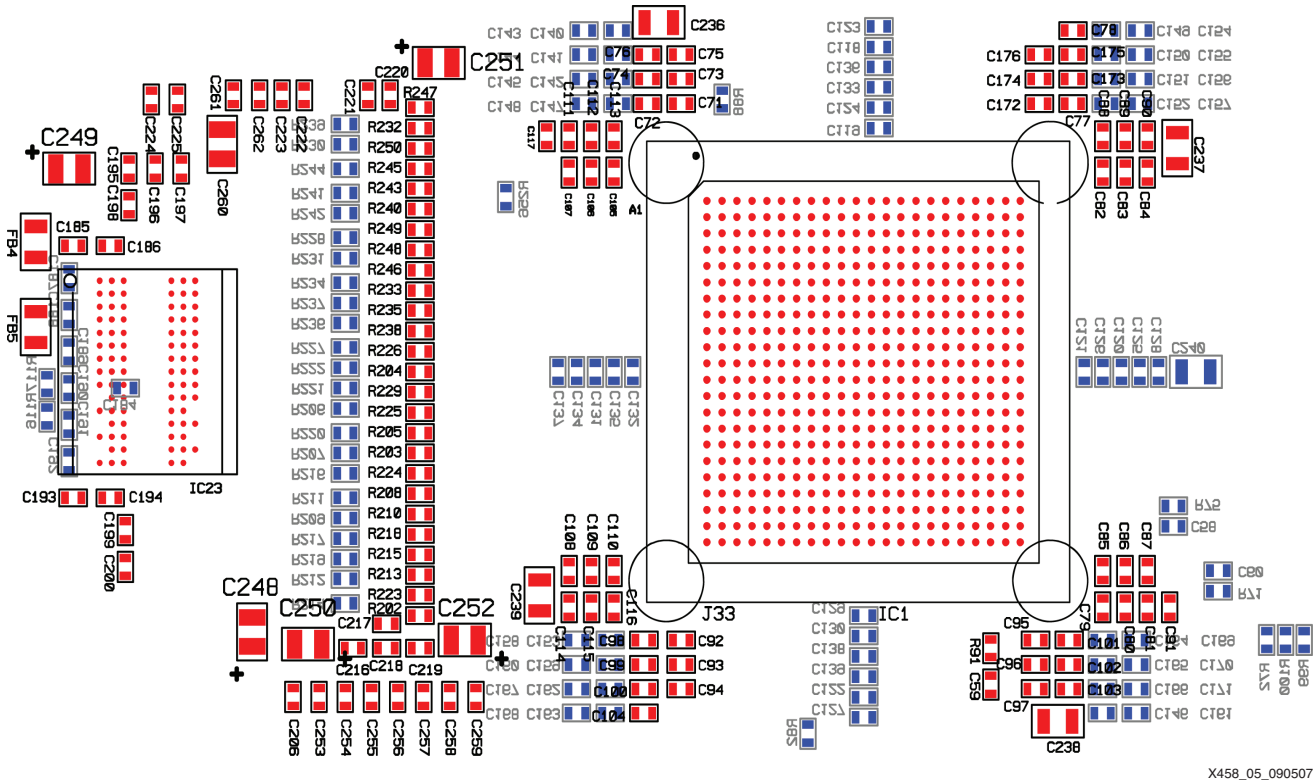

Figure 5: **Component Placement**

Some space is needed to accommodate serpentine traces for delay matching of the routes. However, what is shown in Figure 5 is far from an aggressive placement and could be optimized. The Revision A prototype of the Spartan-3A Starter Kit had additional terminator component footprints that were removed after evaluating the signal integrity on the prototypes, freeing up considerable space. However, the placement of the memory device and the Spartan-3A FPGA was not changed. In theory, this placement could be compressed, with further space savings achieved using resistor packs, smaller resistor packages, or staggering the placement of the termination devices to reduce average trace length.

Figure 6 and Figure 7 show the signal routing. The data and strobe signals form a source synchronous bus (governed by the read and write timing budgets) and are routed with an average length of 2.5 inches and less than 50 ps of skew. The address and control signals form another bus and are routed similarly.

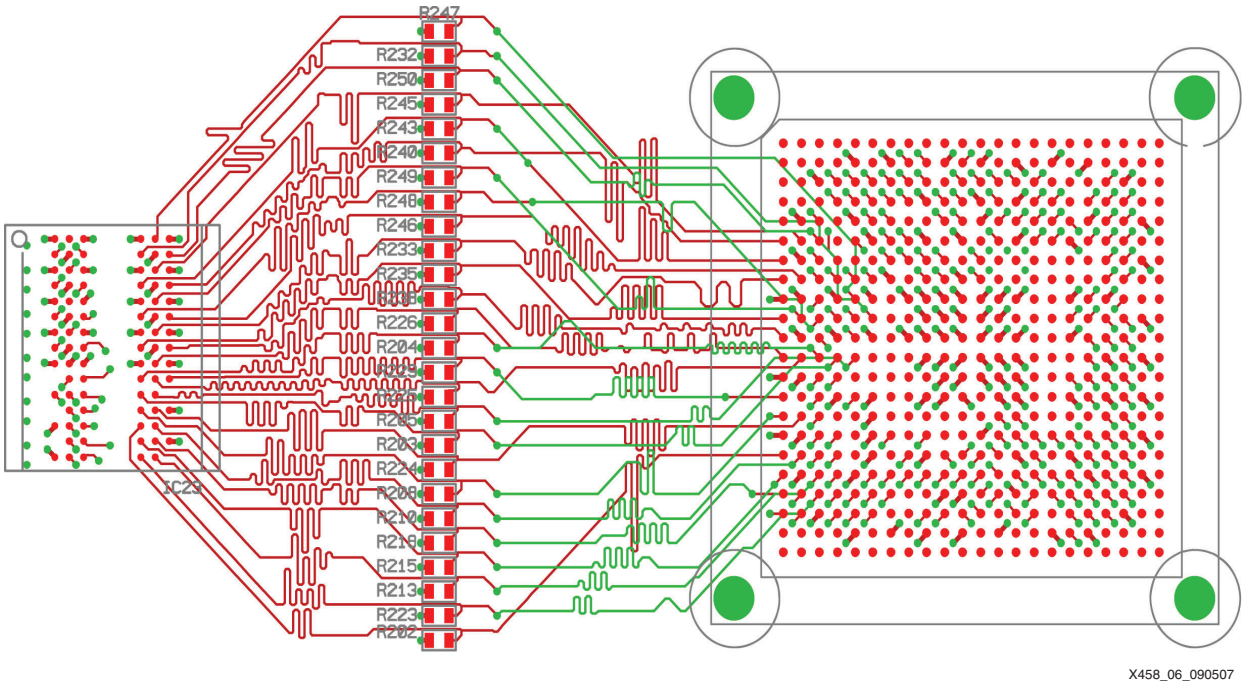

Figure 6: **Top/Mid Layer Routing**

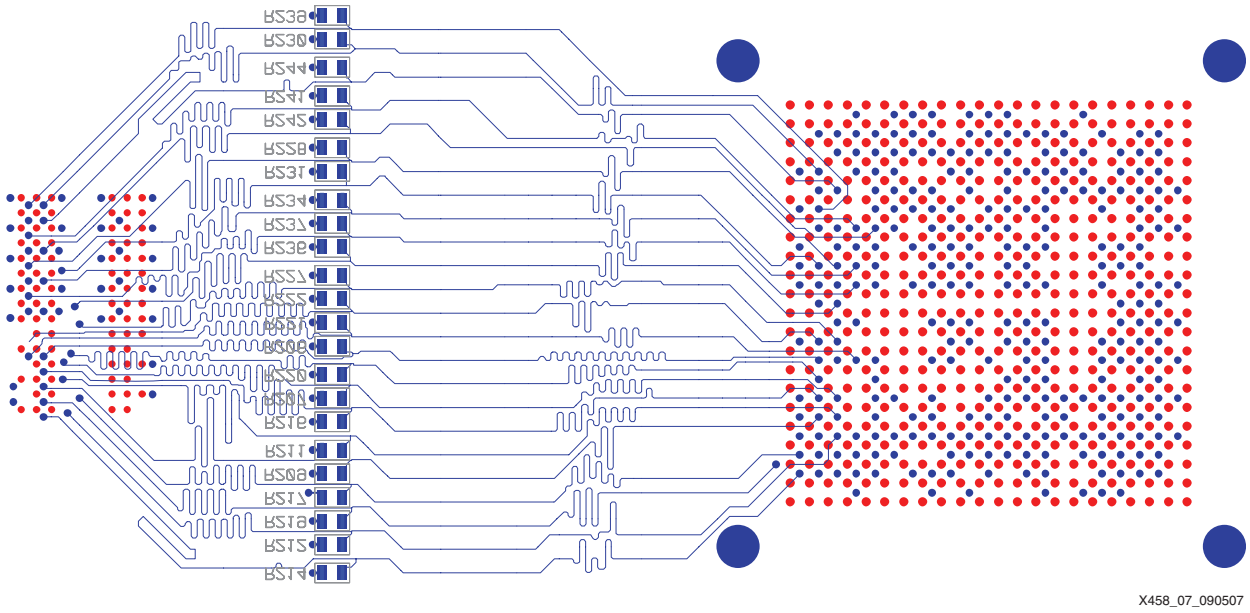

Figure 7: **Bottom Layer Routing**

The MIG-based memory interface in the Spartan-3A FPGA also requires a properly tuned loopback signal. This signal is used by the memory interface to generate an enable for the input capture scheme. The trace delay of the loop should be the sum of the trace delays of the clock forwarded to the memory and the average DQS trace delay. For more information on this topic, refer to UG086, *Memory Interface Solutions User Guide*.

Verification Design and Process

The verification design integrates the DDR2-400 memory interface with an application that implements a frame buffer. In addition to the frame buffer, additional functions exist to facilitate the verification process, including data error checking and power supply control. The verification process involves evaluating the behavior of multiple units of the verification platform, programmed with the verification design, across process, voltage, and temperature variations.

Functional Description

A frame buffer is an output device that drives a video display. An integral part of any frame buffer is a memory. The memory must have enough capacity to contain at least one entire display frame worth of data and must have enough bandwidth to provide data at or above the rate required by the display. In this implementation, the frame buffer is designed to drive a standard UXGA-capable display with a 1600 pixel by 1200 pixel frame at a frame rate of 75 Hz (1600x1200@75). Each pixel is represented by 12 bits of information, 4 bits for each color channel, providing 4096 possible colors.

This frame buffer configuration is selected to facilitate data movement between the memory interface and the display generator. The design requires a system clock of 200 MHz for the DDR2-400 memory interface, and it is desirable (for simplicity) to clock the display generator with the same clock to form a fully synchronous system. Standard 1600x1200@75 display timing uses a 202.5 MHz clock (which is close to 200 MHz) and, with a minor change to the horizontal timing, a 200 MHz clock can be used.

Another simplification from the frame buffer configuration is the elimination of pixel packing and color indexing. The Spartan-3A Starter Kit has a provision for driving a VGA output with 12-bit color, but the memory device has a 16-bit interface with byte enables. At the cost of storage efficiency, pixels are considered as 16-bit quantities with a 12-bit field that represents color information and a 4-bit field that is not displayed. More efficient systems are possible when pixels are packed together, avoiding unused bits. It is also possible to further reduce storage and bandwidth requirements by using color indexing. In the case of the verification design, however, the goal is to consume as much bandwidth as possible! Figure 8 shows a simplified block diagram.

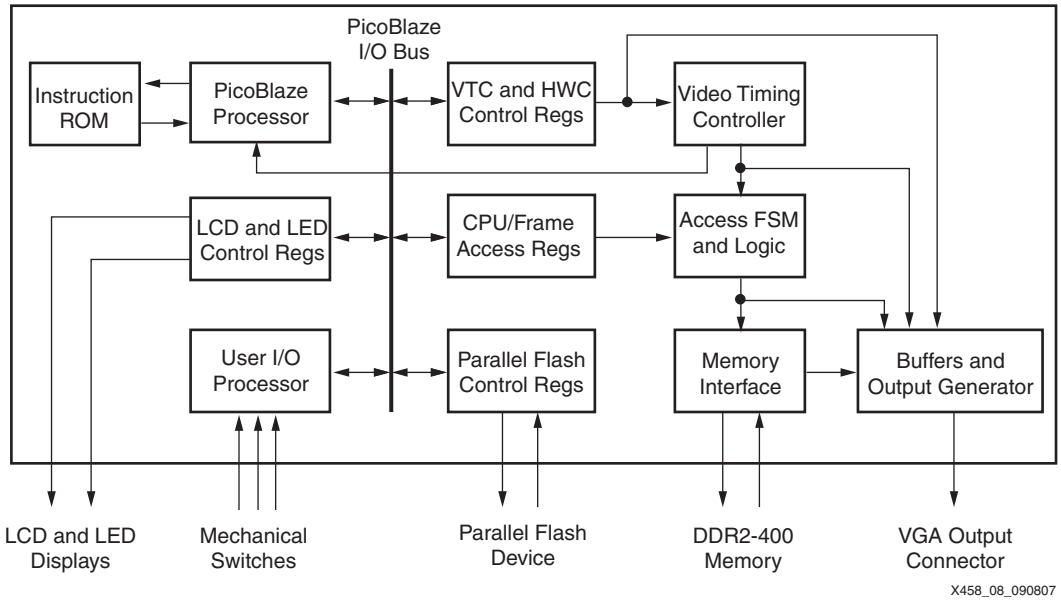

Figure 8: **Simplified Block Diagram of the Verification Design**

Besides the DDR2-400 memory interface, the other significant block is the Memory Access FSM which sits between the PicoBlaze™ processor, the line buffers, and the DDR2-400

memory interface. The FSM monitors the PicoBlaze processor ports and the video timing controller to determine what type of memory access should be requested from the memory interface. The PicoBlaze processor can move data into the frame buffer as memory writes. The video timing controller can move data out of the frame buffer and into a selected line buffer as memory reads.

A very simple arbitration scheme is used: writes initiated by the PicoBlaze processor always have priority over the display fetch. For this reason, writes by the PicoBlaze processor should only be performed before the display fetch is enabled or during periods when no display fetch is taking place, such as horizontal and vertical blanking periods. Failure to observe this does not corrupt the data stored in the frame buffer, but it causes transient corruption of pixels on the display. The PicoBlaze processor receives a vertical blanking interrupt to facilitate synchronization with the display fetch process.

The display fetch process consists of 1200 line fetches, with each line fetch taking place one line earlier than used on the display. This prefetching increases the buffering requirements compared to a flow-through implementation, but eliminates the concern about the frequency and duration of periodic memory refresh cycles, as long as the average available bandwidth during a line fetch is adequate.

Each line fetch reads 1600 words of data, and the process of reading those 1600 words can involve one, two, or three burst reads from the memory interface. The number of burst reads depends on the initial read address relationship to memory row boundaries and the number of words to be fetched. The data is placed in a line buffer.

The display generation circuits obtain data from a line buffer, optionally scale the intensity, and overlay six programmable hardware cursors. The intensity scale and hardware cursors are not directly relevant to the operation of the DDR2-400 interface, but serve to demonstrate that the video data can be digitally processed in real time. Figure 9 shows a photograph of the system operation.

Figure 9: **Verification Design Operation**

Error Checking via Frame CRC

During initialization, the data for display is read from the parallel Flash as bytes and written to the frame buffer as words. One complete frame (approximately four megabytes) is copied in this manner. During the copy, a CRC-32 is computed across each “nibble lane” of the words to be written, resulting in four CRC-32 values. The computation is done in hardware. The “nibble lanes” correspond to the three color channels (red, green, and blue) plus an additional channel that is not displayed but contains a pattern to ensure all 16 bits of the memory interface are exercised. This is illustrated in Figure 10.

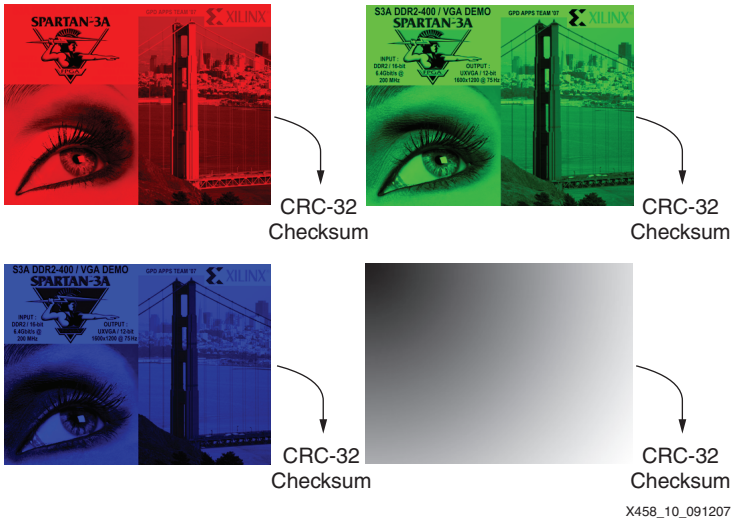

Figure 10: **Frame CRC-32 Calculation on Color Channels**

After initialization has completed, the display fetch process begins. Prior to the start of a new frame, another set of four CRC-32 values are initialized. As the frame is displayed, CRC-32 values are computed in real time on the data using the hardware CRC circuits. Here, running four parallel CRC-32 circuits with 4-bit data inputs is an advantage over a single CRC-32 circuit with a 16-bit input for performance reasons because the calculations need to take place at the pixel clock rate. The computation is identical to the one used during the initialization process.

At the end of each frame, after the CRC-32 values are compared, the green LD3, LD2, LD1, and LD0 indicators are updated to indicate CRC-32 comparison errors for each of the four channels. These indicators help diagnose which data channels (nibbles) have errors, and also provide a qualitative indication of how many errors are occurring based on the perceived intensity of the indicator illumination. If no errors take place, the indicators are off. If errors take place occasionally, the indicators flicker, transitioning to a steady glow as the error rate increases.

At the first detection of any error, the yellow LD13 indicator is illuminated until the design is reset or the power is cycled. This serves as a pass/fail indicator used to quickly assess the cumulative test results at a given point in time. As long as LD13 is off, no errors have been detected during operation.

Power Supply Control via the RS-232 Interface

The verification design enables interactive control of the output voltage levels of the power supplies on the Spartan-3A Starter Kit via the RS-232 interface. For more information on the power supply design of the Spartan-3A Starter Kit, refer to Chapter 17 of UG334, *Spartan-3A Starter Kit Board User Guide*. This interactive control is of particular use when performing verification at different supply voltages.

Commands to change the output voltage levels are entered into an ASCII terminal, received by the verification design, and converted into I^2C accesses to the power supply devices. Each

device has four independently adjustable regulators: two linear regulators and two switching regulators. All regulators are ±3%, with adjustment steps of 0.05V for the switching regulators and 0.1V for the linear regulators. There are eight power rails, five of which are relevant to the operation of the memory interface:

- VCCAUX, nominally +3.3V, powers certain auxiliary circuits in Spartan-3A FPGAs, including digital clock managers (DCMs), which are used in the memory interface.
- VCCINT, nominally +1.2V, powers internal logic in Spartan-3A FPGAs, including configurable logic blocks (CLBs), which implement the bulk of the memory interface including the lookup table (LUT) based delay lines used in the input capture scheme.
- VREF1V8, nominally +1.8V, powers the Spartan-3A FPGA voltage reference for the 1.8V signaling interface with the memory device.
- DDR1V8, nominally +1.8V, powers the memory device, as well as the Spartan-3A FPGA pins that form the interface with the memory device.
- DDR0V9, nominally +0.9V, powers the termination network for the signals between the Spartan-3A FPGA and the memory device.

The design also accepts a set of abbreviated single-keystroke commands as “shortcuts” for desired voltage conditions used in the verification plan.

Reference Clock Generation

The reference clock must be a 200 MHz clock signal with 150 ps of cycle-to-cycle jitter or less. Because there is no reasonably priced option to directly apply a 200 MHz clock from an external source, the on-board 50 MHz oscillator is used with a DCM inside the Spartan-3A FPGA to multiply the 50 MHz signal up to 200 MHz. This setup introduces additional jitter into the 200 MHz reference clock which is undesirable and violates the Clock-to-Memory timing budget. This approach must not be used for production designs.

For verification purposes, this approach is acceptable provided that the verification process yields a passing result. It simply means that more design margin exists than can be proven with the verification platform.

Verification Plan

The verification process involves evaluating the behavior of multiple units of the verification platform, programmed with the verification design, across process, voltage, and temperature variations. Confirming proper operation of the design in this three-dimensional space, particularly in regions where the devices exhibit worst-case (slowest) performance, verifies the conclusion drawn from the timing budgets. Consider the following variables:

- Silicon Process: The Spartan-3A Starter Kits are reworked to replace the existing lower speed grade (-4) devices with the higher speed grade (-5) devices screened to specific performance levels. One set of units is built with slow devices from the higher speed grade, and another set of units is built with typical devices from the higher speed grade. The memory devices are considered “sample tested”.
- Supply Voltage: The component data sheets indicate the allowed supply voltage range for each component, and the programmable power supplies allow easy output voltage adjustments to enable exploration of the functional ranges for the verification design. Due to the accuracy of the power supply devices and the resolution of the output voltage steps, the usable settings within the allowed supply voltage range are limited.
- Temperature: The component data sheets also indicate the allowed temperature range for each component. The Spartan-3A FPGAs with the higher speed grade (-5) are available only in the commercial temperature grade, with allowed junction temperatures between 85°C and 0°C. During the verification process, a Thermonics T-2420 temperature forcing machine is used to evaluate operation at 85°C, 25°C, and 0°C.

The process for each unit consists of forcing the temperature to each of the desired values and allowing a three minute “soak time” to ensure the junction temperature is as close as possible to the case temperature. Once the temperature is stable, the error indicator is monitored while the supply voltages are set at different levels within the allowed voltage ranges.

Results

The design is robust across process variations and the commercial temperature range, provided the power supplies are regulated within the ranges shown in Table 8. The results in Table 8 have been “cleaned up” to ease understanding and incorporate additional margin.

Table 8: **Power Supply Specifications**

	Nominal	Tolerance
VCCAUX	3.300V	±5%
VCCINT	1.200V	±3%
VREF1V8	1.800V	±3%
DDR1V8	1.800V	±3%
DDR0V9	0.900V	±3%

The programmable power supplies allow adjustment, but they have fairly coarse steps. The tolerances in Table 8 reflect available output voltage settings that exhibit robust operation, are within the device data sheet specifications, and are achievable with the programmable power supply solution.

For example, V_{CCINT}, the Spartan-3A FPGA supply, is specified at 1.2V±5% in DS529, *Spartan-3A FPGA Family: Complete Data Sheet*. The programmable power supply was capable of generating a nominal V_{CCINT} voltage with the next steps at +3.5% and -4.2%. Larger steps from nominal are outside the operational range of V_{CCINT} for the Spartan-3A FPGA and were not tested. The reported result is simplified to ±3% in Table 8.

While these power supply specifications are moderately tighter than otherwise required by the individual component data sheets, they are not difficult to meet. Many commercially available, reasonably priced power solutions exist, including the power solution designed into the Spartan-3A Starter Kit.

Design Files

The design files for this application note, which are available in Verilog-HDL only, are located on the Xilinx website at https://secure.xilinx.com/webreg/clickthrough.do?cid=91539.

This design is compatible with the Spartan-3A Starter Kit and derivative kits (HW-SPAR3A-SK-UNI-G, HW-SPAR3AN-SK-UNI-G, and HW-SPAR3ADDR2-DK-UNI-G) but requires the replacement of the existing lower speed grade (-4) device with the higher speed grade (-5) device. Xilinx does not provide this service.

The design can be downloaded into a standard Spartan-3A Starter Kit with the lower speed grade (-4) device for evaluation purposes only. The design may operate correctly, operate with data errors, or not operate at all. Xilinx does not guarantee the operation of this design in lower speed grade (-4) devices.

Conclusion

System designers may take advantage of Spartan-3A, Spartan-3AN, or Spartan-3A DSP FPGAs with the higher speed grade (-5) to incorporate robust, low-cost, and high-performance DDR2-400 memory interfaces in applications operating over the commercial temperature range. A successful implementation for a point-to-point connection requires the use of moderately tighter voltage regulation coupled with a DDR2-400 capable memory device with CL = 3, such as a Micron Technology MT47H32M16BN-3:D. The increased performance of DDR2-400 memory interfaces is a compelling advantage and can be used to enable new applications or optimize and enhance existing applications.

References

The following documents and links provide additional information useful to this application note:

- DS529, *Spartan-3A FPGA Family: Complete Data Sheet*
  http://www.xilinx.com/support/documentation/data_sheets/ds529.pdf
- MT47H32M16 (32M x 16) DDR2 SDRAM Data Sheet
  http://download.micron.com/pdf/datasheets/dram/ddr2/512MbDDR2.pdf
- UG086, *Xilinx Memory Interface Generator User Guide*
  http://www.xilinx.com/support/documentation/ip_documentation/ug086.pdf
- UG334, *Spartan-3A Starter Kit Board User Guide*
  http://www.xilinx.com/support/documentation/boards_and_kits/ug334.pdf
- Spartan-3A Starter Kit Board Schematics
  http://www.xilinx.com/support/documentation/boards_and_kits/s3astarter_schematic.pdf
- Spartan-3A Starter Kit Board Photoplots
  http://www.xilinx.com/support/documentation/boards_and_kits/s3a_starter_gerbers.pdf
- XAPP454, *DDR2 SDRAM Memory Interface for Spartan-3 FPGAs*
  http://www.xilinx.com/support/documentation/application_notes/xapp454.pdf
- XAPP768c, *Interfacing Spartan–3 Devices With 166 MHz or 333 Mb/s DDR SDRAM Memories*
  http://www.xilinx.com/support/software/memory/protected/XAPP768c.pdf
- Xilinx ISE 9.2i Service Pack 1, Spartan-3A speed file “PRODUCTION 1.37 2007-06-02”
  http://www.xilinx.com/tools/designtools.htm

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
09/19/07	1.0	Initial Xilinx release.
07/09/09	1.0.1	Updated URLs and trademark usage throughout.

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