



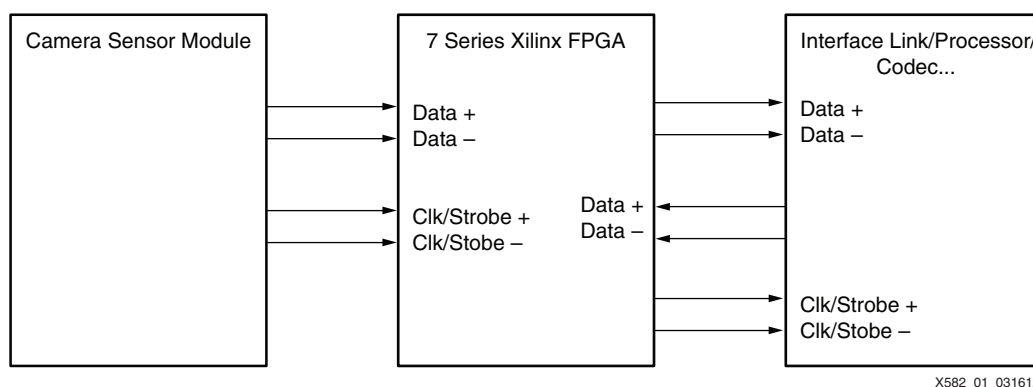
XAPP582 (v1.0) January 31, 2013

# Compact Camera Port 2 SubLVDS with 7 Series FPGAs High-Range I/O

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## Summary

The Compact Camera Port 2 (CCP2) protocol is used to interface between camera sensors and receivers. The signaling scheme uses SubLVDS. [Figure 1](#) shows an example topology where a Xilinx 7 series FPGA fits into a CCP2 system.



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**Figure 1: Example Topology of a 7 Series FPGA Interfacing to a Camera Sensor and Other Components**

This application note describes the SubLVDS electrical specifications. It includes a reference design to implement resistor topology that emulates the electrical characteristics of a SubLVDS transmitter and also covers the FPGA receiver.

## SubLVDS Transmitter

SubLVDS is a differential low-voltage signal that is a subset of the LVDS in IEEE Standard 1596.3 [\[Ref 1\]](#). SubLVDS operates at either 1.8V or 1.5V. A 1.8V  $V_{CCO}$  is used for the receiver. [Table 1](#) lists the parameters necessary to implement SubLVDS.

**Table 1: SubLVDS Transmitter Specifications**

Parameter	Minimum	Nominal	Maximum	Unit
$V_{CMF}$ fixed common mode	0.8	0.9	1.0	V
$V_{OD}$ differential voltage swing	100	150	200	mV
$I_{OD}$ drive current range	0.833	1.5	2	mA
Drive current variation			15%	
$R_o$ output impedance	40		140	$\Omega$

[Figure 2](#) and [Figure 3](#) show how the parameters listed in [Table 1](#) are measured.

### $V_{CMF}$

The fixed common mode voltage,  $V_{CMF}$ , is one of the key differentiators between SubLVDS and LVDS. For SubLVDS, the nominal common mode is 0.9V compared to 1.25V for LVDS. [Figure 2](#)

shows two single-ended signals  $V_{INP}$  and  $V_{INN}$  toggling. The dark line at the bottom of the figure shows the reference ground. The average of  $V_{INP}$  and  $V_{INN}$  is  $V_{CMF}$ .

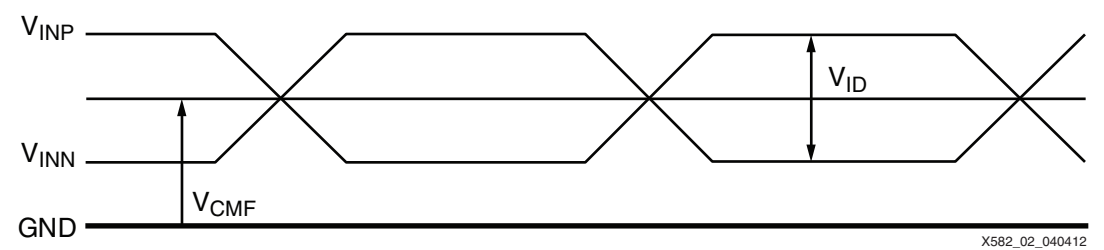


Figure 2: Single-Ended Signaling Showing Where the  $V_{CMF}$  is Measured From

$V_{CMF}$  is defined in Equation 1.

$$V_{CMF} = (V_{INP} + V_{INN}) / 2 \quad \text{Equation 1}$$

**$V_{OD}$**

The differential voltage swing,  $V_{OD}$ , is another key differentiator between SubLVDS and LVDS. The maximum differential swing for SubLVDS is 200 mV. Figure 3 shows the differential signal for SubLVDS and the measurement points that are used. The dark black line represents ground. It is apparent that this is a differential signal, not a single-ended signal, because the signal is centered around ground instead of  $V_{CMF}$ .

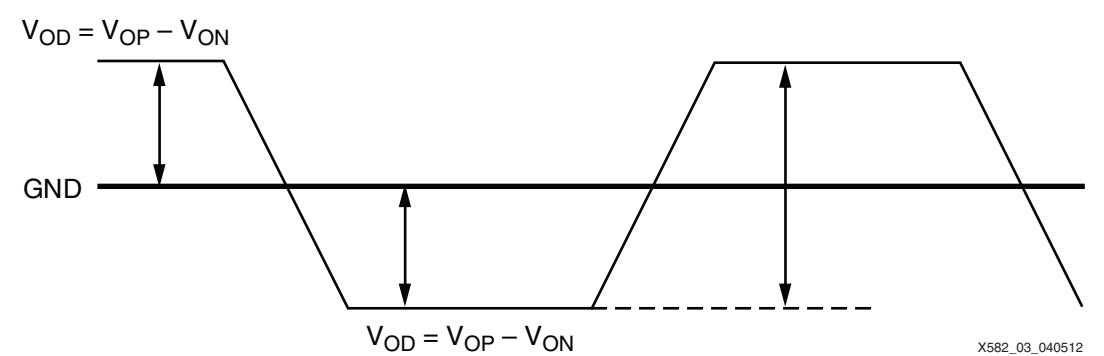


Figure 3: Differential Signal for SubLVDS

The  $V_{OD}$  of the differential signal is defined in Equation 2.

$$V_{OD} = V_{OP} - V_{ON} \quad \text{Equation 2}$$

When measuring  $V_{OD}$ ,  $V_{OP}$  is equal to the top line of the signal and  $V_{ON}$  is equal to the base line of the signal.

**SubLVDS Receiver**

The SubLVDS receiver is a differential self-biasing receiver. The SubLVDS receiver specifications are listed in Table 2.

Table 2: SubLVDS Receiver Specifications

Parameter	Minimum	Typical	Maximum	Unit
Input voltage range	$(V_{CMF}) - 0.4$	$V_{CMF} (0.9V)$	$(V_{CMF}) + 0.4$	V
Receiver input high threshold $V_{THH}$			25	mV
Receiver input low threshold $V_{THL}$	-25			mV
Termination resistance value	80	100	120	$\Omega$

Table 2 lists four parameters: Input voltage range,  $V_{THH}$ ,  $V_{THL}$ , and termination resistance value. The input voltage range is self-explanatory in that the common mode voltage can range from 0.5V to 1.3V.  $V_{THH}$  and  $V_{THL}$  are explained in more depth in [V<sub>THH</sub>, V<sub>THL</sub>, and Eye Width](#). The termination resistance value is the parallel termination placed at the input of the receiver. The termination resistance value should not be confused with the series termination value mentioned later in this application note.

### $V_{THH}$ , $V_{THL}$ , and Eye Width

The receiver eye has two thresholds,  $V_{THL}$  and  $V_{THH}$ , that are  $-25\text{ mV}$  and  $+25\text{ mV}$ , respectively, as shown in Table 2. This is a  $50\text{ mV}$  differential or  $\pm 25\text{ mV}$ . In Figure 4, the dark black line represents ground, and the dashed lines above and below ground show the measurement points for  $V_{THL}$  and  $V_{THH}$ .

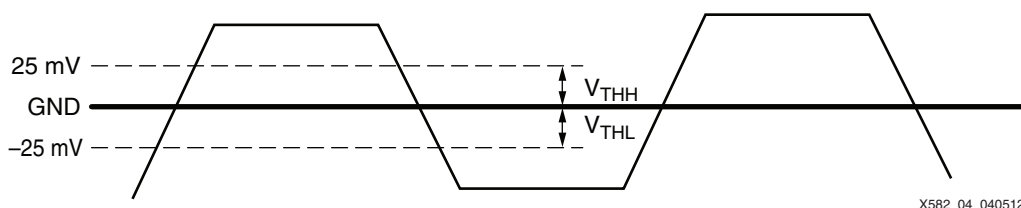


Figure 4: Differential Signal Showing  $V_{THH}$  and  $V_{THL}$  Measurement Points Relative to Ground

There is no strict eye mask for SubLVDS. Therefore, Figure 5 shows an eye diagram that has several markers on it to represent an eye mask based on  $V_{THH}$  and  $V_{THL}$ . The eye diagram is a differential signal as denoted by the signal swinging above and below the dark black line that represents ground (GND). The unit interval of the eye is represented by the total unit interval. For example, if the interface is running at  $200\text{ Mb/s}$ , the total unit interval would be  $5\text{ ns}$ . At  $25\text{ mV}$  above ground and  $25\text{ mV}$  below ground, a box is drawn wherever the signal is open or no crossing occurs. The region within the box is where the differential measured unit interval is defined. Figure 5 shows how this application note defines the SubLVDS receiver eye.

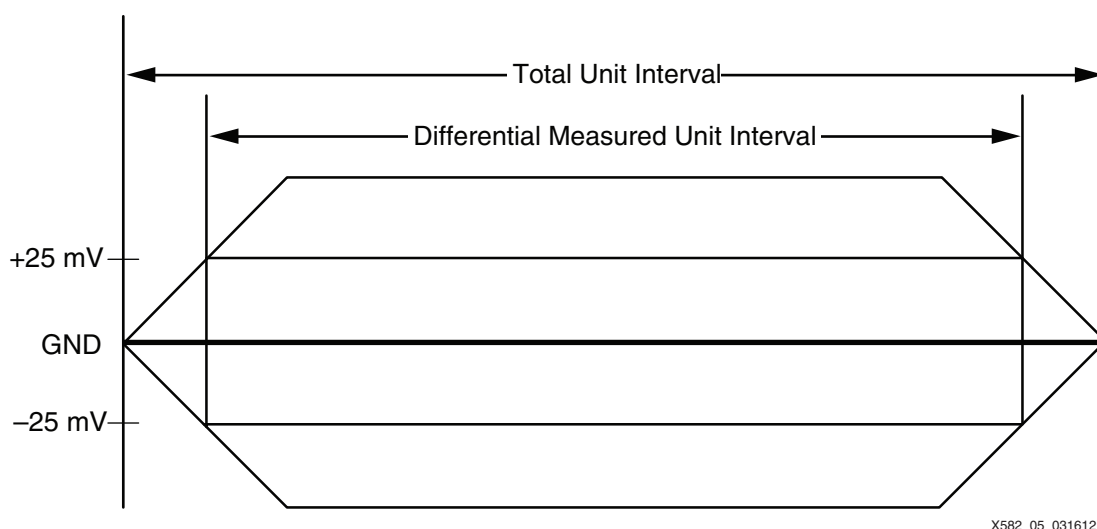


Figure 5: Example SubLVDS Eye Mask

### Using DIFF\_HSTL\_II\_F\_18 for SubLVDS Transmitter

The DIFF\_HSTL\_II\_F I/O standard was chosen for the SubLVDS transmitter because it has a common mode of  $0.9\text{V}$  nominal. DIFF\_HSTL\_II\_F\_18 has too large of a swing to be used for the SubLVDS signal. A series termination is placed in-line to reduce the signal swing and thus

meet the SubLVDS specifications while keeping the common mode in the correct range. Figure 6 shows the reference design topology used in this application note to implement the SubLVDS circuit.

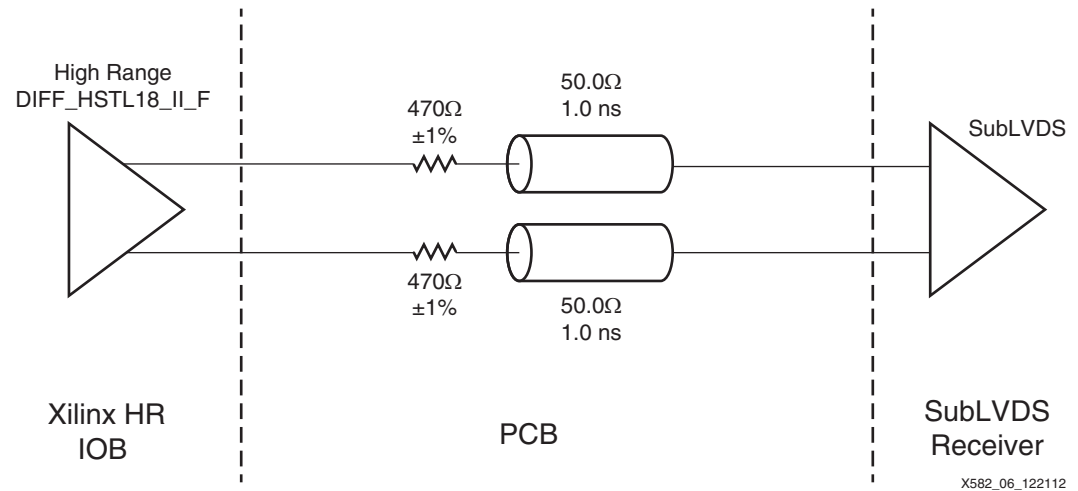


Figure 6: DIFF\_HSTL18\_II\_F Reference Design Topology Used to Implement SubLVDS

## Reference Design Topology

When designing systems, it is important to select a model that actually reflects the board and system. This section provides some general guidelines for selecting a model.

### Transmitter

Starting at the left side of Figure 6, the transmitter used in the reference design is the Xilinx-supplied Input/Output Buffer Information Specification (IBIS) simulation model. The actual I/O standard used from the IBIS model is DIFF\_HSTL\_II\_F. This model should be selected when setting up the simulation.

### Package Capacitance

The package capacitance is part of the simulation. In this application note, the package files provided with the IBIS and SPICE models are used. As a real example, the FBG900\_7K325T.pkg file with pin AB20 is a part of the Bare Die Flip Chip packaging. Other packages and pins can be used but this pin, part, and package were chosen as a somewhat typical option.

For the IO\_L6N\_T0\_VREF\_12 pin, the RLC is:

- $R = 0.173453\Omega$
- $L = 1.46861 \text{ nH}$
- $C = 1.39896 \text{ pF}$

### Series Resistor

A series resistor of  $470\Omega$  with a 1% tolerance is placed on the board near the transmitter. The reasons why this  $470\Omega$  value is used are:

- Strong enough to get the  $V_{OD}$  below the 200 mV range
- A common value that can be found from many vendors
- Can be found in the 0204 and 0102 packages
- Can be found in 1% tolerance

The small package is often a key factor in CCP2 designs. There is a range of resistance values that could work. This application note provides a guideline for selecting those other values.

Board Trace

CCP2 is commonly used for less than 6 inches of trace with 50Ω impedance. The same guidelines have been used for these simulations. If the user’s board is shorter than 6 inches or has a different impedance profile, the board’s impedance profile should be used for simulation.

SubLVDS Receiver

The SubLVDS receiver is placed at the end of the line. This is where the user can place their particular SubLVDS receiver.

Electrical  
Simulations and  
Reference  
Design

Simulation Tools

Xilinx provides two methods of SelectIO™ technology simulation: IBIS and SPICE. Examples of both of these have been provided using the Mentor Graphics HyperLynx Simulation method and Synopsis HSPICE. There are other simulators, but these are two most common ones.

Simulation Corners

The IBIS models that Xilinx provides are text format models that are generated from the SPICE models. Xilinx IBIS models are generated from three corners: MIN, MAX, and TYP (Table 3).

Table 3: IBIS Simulation Model Corners

IBIS Corner Condition (HyperLynx)	Silicon Process Corner	Temperature (°C)	Voltage
MIN (Slow-Weak)	Slow	85	–5%
TYP (Typical)	Typical	25	Nominal Voltage
MAX (Fast-Strong)	Fast	0	+5%

Figure 7 shows the layout for the HyperLynx simulation because the IBIS file contains the package for which the IBIS model was manually edited to match the package for the AB20 pin. A 50Ω V<sub>TT</sub> termination is used in place of another IBIS model to match the SPICE model.

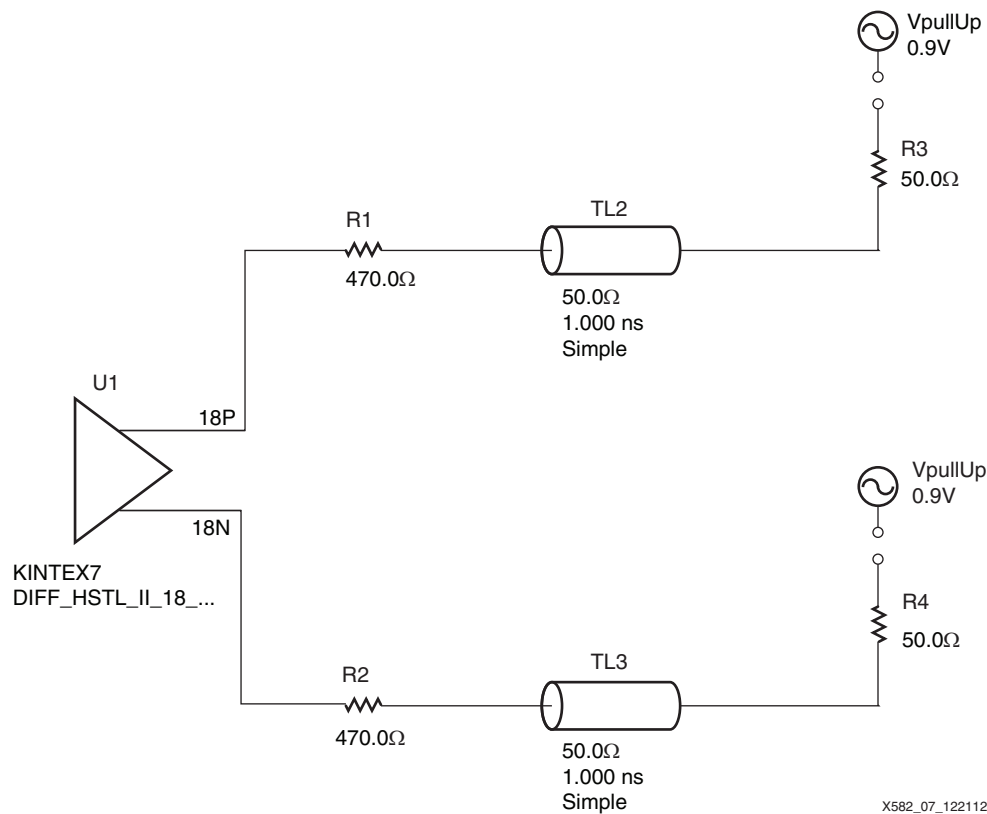


Figure 7: IBIS Simulation Model Using 50Ω V<sub>TT</sub>

When probing using an IBIS model with Mentor Graphics, **At DIE** should be selected instead of **At PIN**. This gives a better simulation result. The differential output should be used to measure the eye opening. For this simulation, a differential probe was inserted at R4.1 and R3.1. The result was thus differential.

The SPICE models provided by Xilinx are encrypted transistor models generated from the circuit design. These models are generated with three process corners but allow for voltage and temperatures to be set for each simulation. For this application note, the settings shown in Table 4 were used.

Table 4: SPICE Simulation Model Corners

SPICE Corner Condition	Silicon Process Corner	Temperature (°C)	Voltage
MIN	Slow	125	-5%
TYP	Typical	25	Nominal Voltage
MAX	Fast	-40	+5%

Figure 8 shows what is built in the SPICE deck example provided in the reference design. For the SPICE deck example, the same RLC package setting as the IBIS model was used. In the SPICE deck, a 50Ω V<sub>TT</sub> termination is used. The SPICE deck is set up to use the PTN3700 IBIS model so the code can be modified to use this IBIS model instead of the 50Ω V<sub>TT</sub> termination.

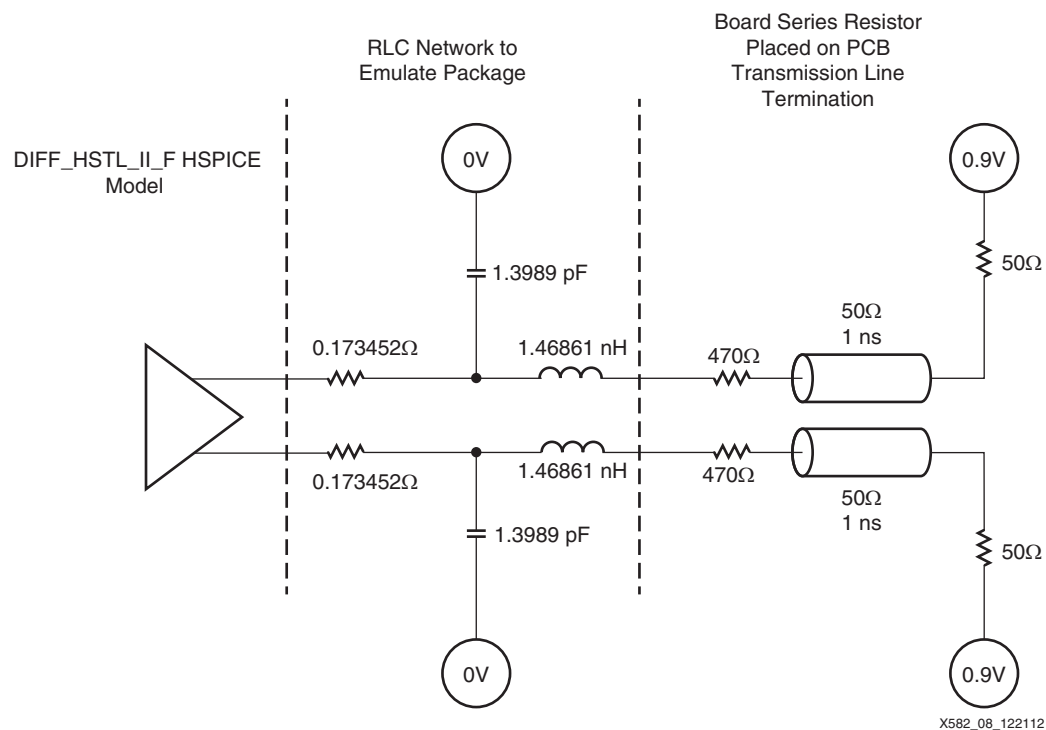


Figure 8: HSPICE Deck Topology Provided in Reference Design

When probing the transit response file (.tr0), the probe point t\_right\_p and t\_right\_n should be used for the single-ended points. When measuring the eye width, t\_right\_p – t\_right\_n should be used. This will give the differential results.

Results of  
Electrical  
Simulation

The results of electrical simulation are shown in Table 5. There are two headers, one with the SubLVDS specifications and one with DIFF\_HSTL18\_II\_F as implemented in this application note. In reviewing the parameters line by line, the results show that the electrical specifications are met.

Table 5: DIFF\_HSTL18\_II\_F\_HR with 470Ω Termination Results

Parameter	SubLVDS Specification			DIFF_HSTL18_II_F as Implemented in this Application Note			Unit
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum	
V <sub>CMF</sub> fixed common mode	0.8	0.9	1.0	0.8		1.0	V
V <sub>OD</sub> differential voltage swing	100	150	200	100		200	mV
I <sub>OD</sub> drive current range	0.833	1.5	2	0.833		2.0	mA
Drive current variation			15%			15%	

Differential  
Measured Eye

The performance range for SubLVDS is based on the eye diagram as defined in Figure 8 of a ±25 mV aperture or eye mask applied to an HSPICE slow simulation at 125°C with –5% voltage.

Figure 9 shows 1.62 ns of a 1.66 ns possible window or 0.978 UI opening. This closes more as package effects of the receiver are added to the simulation.

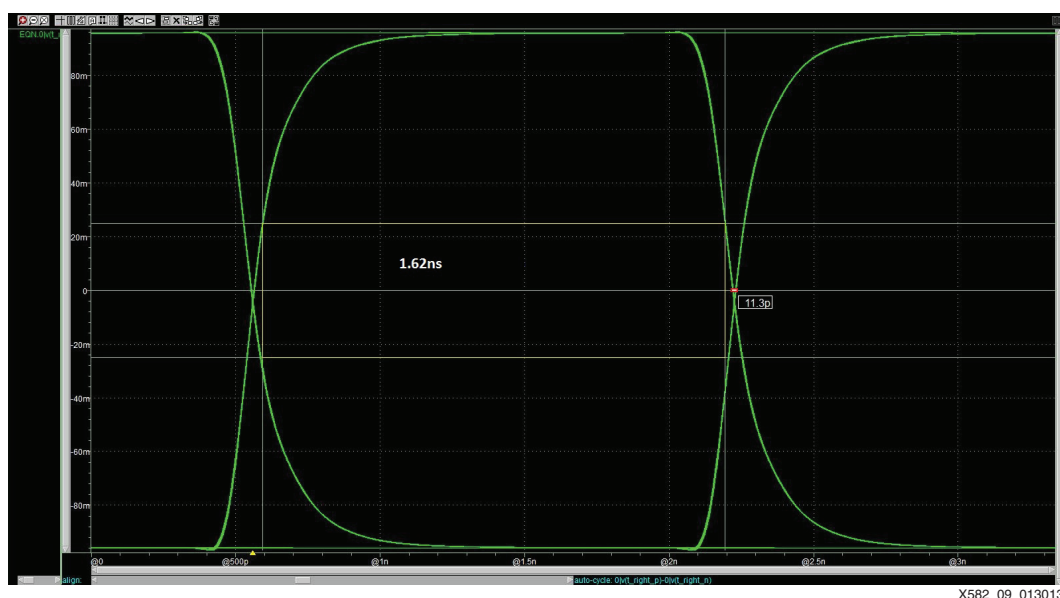


Figure 9: 600 Mb/s Differential Eye Measurement of Figure 8 at M Corner

Figure 10 shows the PRBS15 simulation results for the IBIS model. The eye measurement was taken with two cursors placed at approximately 25 mV. The eye width is 1.63 ns of 1.66 ns, or a 0.98 UI opening. The eye opening closes as the receiver package is added to the simulation.

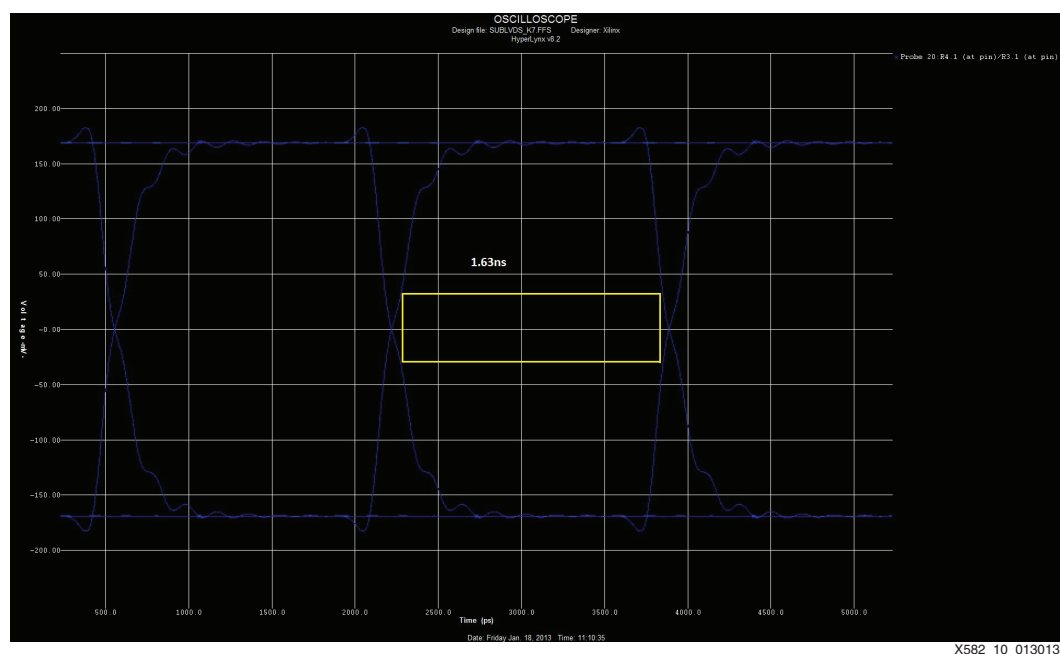


Figure 10: 600 Mb/s Differential Eye Simulation Result of Figure 7 at Slow-Weak corner

The IBIS and SPICE simulation track within the range of margin for two different simulation models at different temperatures.

## Performance

Timing closure must be performed on every particular board and application using a 0.70 UI differential measured eye as a guideline (see Table 6). This is only a guideline for the given simulations. The user is responsible for simulating and closing timing on any given system.

**Table 6: Guideline for Performance of Xilinx-implemented SubLVDS with DIFF\_HSTL18\_II\_F**

Speed Grade	Performance (Mb/s)
3	600
2/2L	600
1	600
-2L/0.9V	600

## Reference Design

The reference design files for this application note can be downloaded from:

<https://secure.xilinx.com/webreg/clickthrough.do?cid=202234>

The reference design matrix is shown in Table 7.

**Table 7: Reference Design Matrix**

Parameter	Description
<b>General</b>	
Developer name	Brandon Day
Target devices (stepping level, ES, production, speed grades)	7 series FPGAs
Source code provided	Yes
Source code format	SPICE decks and free-form schematics
Design uses code/IP from existing Xilinx application note/reference designs, CORE Generator software, or third party	No
<b>Simulation</b>	
Functional simulation performed	N/A
Timing simulation performed	N/A
Test bench used for functional and timing simulations	N/A
Test bench format	N/A
Simulator software/version used	HSPIICE versions 2010.03-SP1, 2010.12-SP1, 2010.12-SP2, 2011.09, 2011.09-SP1, 2011.09-SP2. HyperLynx v8.2 64-bit.
SPICE/IBIS simulations	Yes
<b>Implementation</b>	
Synthesis software tools/version used	N/A
Implementation software tools/versions used	N/A
Static timing analysis performed	N/A
<b>Hardware Verification</b>	
Hardware verified	No
Hardware platform used for verification	N/A

Table 8 shows the device utilization information.

Table 8: Device Utilization

Parameters	Specification/Details	
Maximum frequency (by speed grade)	-1	600 Mb/s
	-2	600 Mb/s
	-3	600 Mb/s
Device utilization without testbench (mandatory)	Slices	N/A
	GCLK buffers	N/A
	IOB pins	2 per pair
Bus width		N/A
I/O standard		HSTL18_II_F
HDL language support		N/A
Target memory device for verification	Simulation	N/A
		N/A
	Hardware	N/A
		N/A

## Conclusion

The SubLVDS I/O standard can be used in the 7 series FPGA high-range (HR) input/output block at high data rates by using a DIFF\_HSTL\_18 I/O standard and series termination as a transmit source. When the FPGA is used as a receiver of SubLVDS, LVDS\_25 or DIFF\_HSTL\_II\_18 can be used as a receiver with a 100Ω parallel termination on the board. Xilinx strongly recommends that users perform their own system validation to close timing for their applications.

## References

This application note uses the following references:

1. IEEE Std. 1596.3-1996 - *IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)*, IEEE Standard  
<http://standards.ieee.org/findstds/standard/1596.3-1996.html>

## Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
01/31/2013	1.0	Initial Xilinx release.

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