



XAPP591 (v1.0)
July 27, 2012

Implementing Triple-Rate SDI Pass-Through Using an All-Digital VCXO Replacement Technique in Virtex-6 FPGAs

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Summary

Triple-rate serial digital interface (SDI) pass-through is a key function typically found in multichannel broadcast video equipment such as switchers, routers, and multiviewers. The video equipment is required to process and pass the SDI video signal through with a locked frequency between its receiver and transmitter.

This application note discusses how to use a novel all-digital voltage-controlled crystal oscillator (VCXO) replacement technique to implement a frequency-locked triple-rate SDI pass-through design using Virtex®-6 FPGAs.

Introduction

Conventionally, the frequency lock in the pass-through is done using an external VCXO, which takes an input from the SDI receiver's recovered clock. The VCXO cleans the clock and feeds it back to the FPGA as a new reference for its SDI transmitter. Thus the video transmitter is operating at a frequency identical to its receiver.

Advantages

Compared to the conventional approach, the new method delivers several major application advantages:

- The method uses complete internal clock management with no need for an external VCXO.
- The same reference clock is shared between receiver (RX) and transmitter (TX).
- A maximized gigabit transceiver (GT) utilization ratio allows implementation of one RX/TX channel on a per GT basis.

These combined advantages provide the broadcast video industry with benefits including much better system integration and reduced overall system cost.

The conventional triple-rate SDI pass-through design has been thoroughly discussed in the Xilinx application note *Implementing Triple-Rate SDI with Virtex-6 FPGA GTX Transceivers* [Ref 1]. [Figure 1](#) illustrates the design architecture.

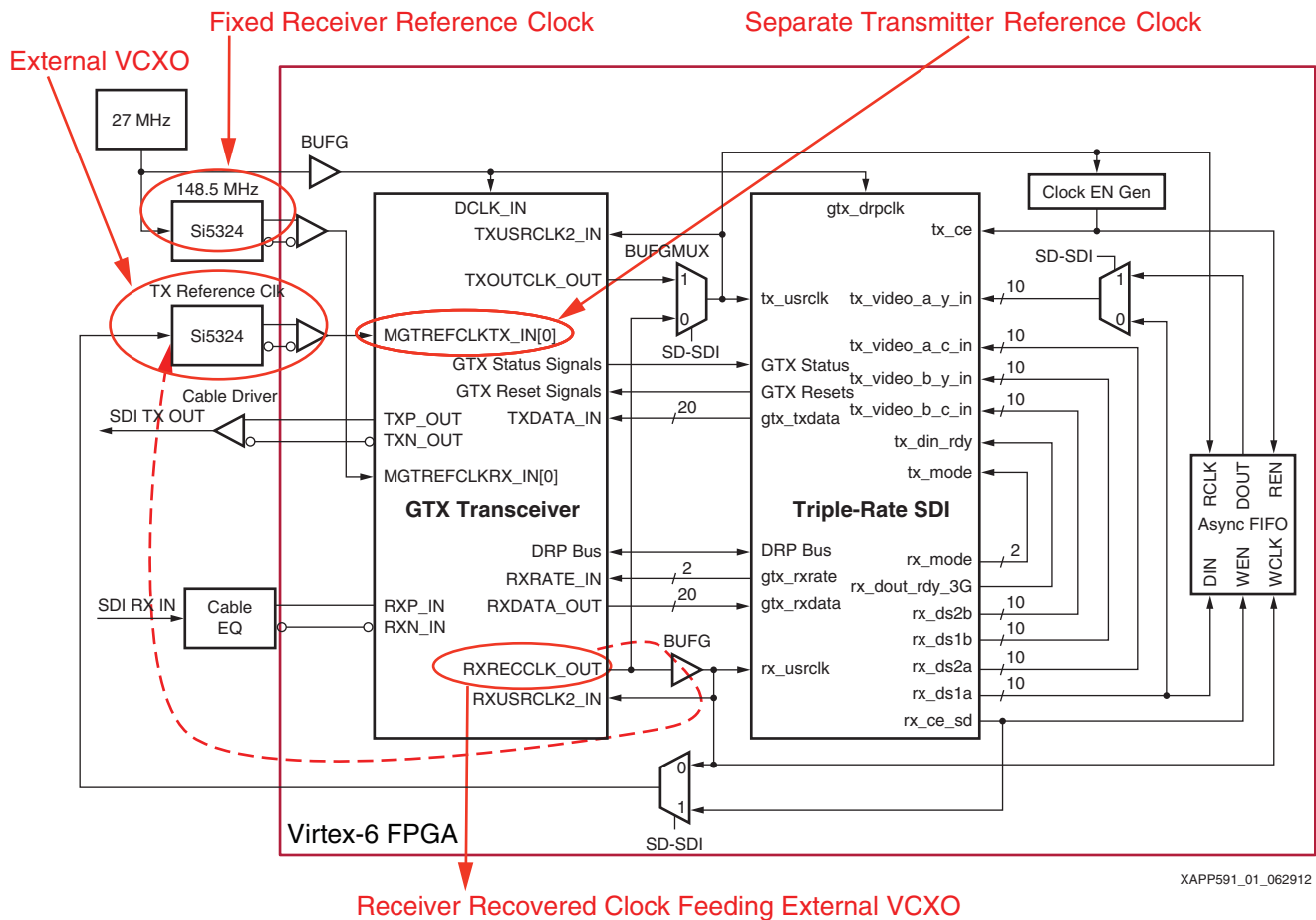


Figure 1: **Conventional Frequency-Locked Triple-Rate Pass-Through Implementation**

In addition to passing the SDI video data through from the RX to TX using the triple-rate SDI LogiCORE™ block, the key challenge is to achieve a frequency lock between RX and TX.

In each RX/TX channel, the SDI receiver's recovered clock RXRECCLK is generated by the Virtex-6 FPGA GTX transceiver clock and data recovery (CDR) circuit using a fixed 148.5 MHz external reference. An external Silicon Labs Si5324 VCXO is applied to clean the recovered clock jitter and feed it back to the FPGA as a separate GTX transmitter reference.

For an N channel video system, N external VCXOs are required to feed N reference clocks for all transmitters. This requirement results in linearly increased system costs and also requires more PCB space and power consumption.

In addition, the Virtex-6 FPGA comes with a group of four GTX transceivers in a Quad architecture. See *Virtex-6 FPGA GTX Transceivers User Guide* [Ref 2]. Each GTX Quad shares two external reference clock pins [Ref 2]. With one pin serving the receiver, the remaining reference clock can only be implemented as a one channel pass-through. This worst case scenario delivers only a 25% GT utilization ratio. For a multichannel implementation, this approach causes an inefficiency that often requires larger devices with higher GT counts.

A better and more efficient method is highly desired to:

- Eliminate the need for an external VCXO.
- Realize a 100% GT utilization ratio.

New Implementation Using the All-Digital VCXO Replacement Technique

The application note *All Digital VCXO Replacement for Gigabit Transceiver Applications* discloses a new method to effectively replace the external VCXOs using a combination of unique Xilinx GT features and a high performance FPGA logic-based digital PLL (DPLL) design [Ref 3]. In Virtex-6 FPGAs, each GTX transceiver has a phase interpolator (PI) circuit in its transmitter physical medium attachment (PMA) circuit that provides an ability to phase- and frequency-modulate the transmit clock operating the GTX transceiver [Ref 2]. This essentially allows the DPLL to phase- or frequency-modulate the GTX transceiver data output directly locking into an input reference clock or pulse, while providing a built-in clock cleaning function [Ref 3].

All Digital VCXO Replacement for Gigabit Transceiver Applications releases an easy-to-use soft macro named *phase interpolator controlled oscillator (PICXO)*. Figure 2 shows all major ports from the PICXO macro.

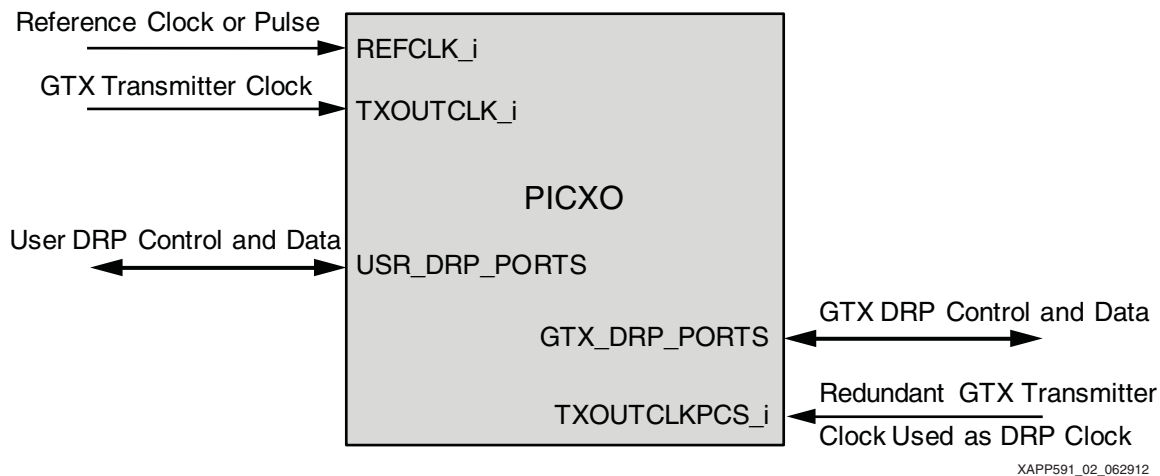


Figure 2: PICXO Macro

The PICXO macro takes a reference clock or pulse and locks up to the reference with as many as ± 160 PPM offset from the current GTX transmitter clock [Ref 3]. The modulation of the transmitter clock's phase and frequency is controlled through the GTX transceiver DRP ports [Ref 2]. Combined with its phase detection logic, loop filter, and sigma delta modulator [Ref 3], the PICXO performs all necessary jitter cleaning functions and tunes the transmitter line rate on the fly to match the incoming reference.

In the triple-rate SDI pass-through case, the PICXO REFCLK_i port is multiplexed between the GTX receiver recovered clock RXRECCLK and an SD-SDI data enable pulse rx_ce_sd [Ref 1]. The GTX transmitter clock is fed into the PICXO macro's TXOUTCLK_i port. These two critical connections allow the PICXO macro to understand the rate difference between the transmitter and the receiver, and to subsequently make adjustments through the DRP ports to lock them. This internal design completely eliminates the need for using the external Silicon Labs Si5324 VCXO to clean the RXRECCLK.

The PICXO implements a DRP arbiter to allow the user application to issue DRP port accesses [Ref 3]. In this SDI pass-through design, the SDI LogiCORE block connects to this DRP arbiter and conducts line rate changes.

The GTX transceiver only needs a pair of fixed frequency reference clocks at 148.5 MHz and 148.5/1.001 MHz. In the receiver direction, the 148.5 MHz is used to provide reference for receiving various line rates, that is, 270 Mb/s, 1.485 Gb/s, 1.4835 Gb/s, 2.97 Gb/s, and 2.967 Gb/s [Ref 1]. The 148.5/1.001 MHz clock, on the other hand, is used to accommodate the 1.4835 Gb/s and 2.967 Gb/s line rates in the transmitter direction. The transmitter is automatically switched between the two reference clocks by the triple-rate SDI LogiCORE block [Ref 1].

Other than these PICXO-related changes and additions, the rest of the pass-through design remains the same as the original design described in *Implementing Triple-Rate SDI with Virtex-6 FPGA GTX Transceivers* [Ref 1]. Figure 3 illustrates the new triple-rate SDI pass-through design based on the PICXO macro.

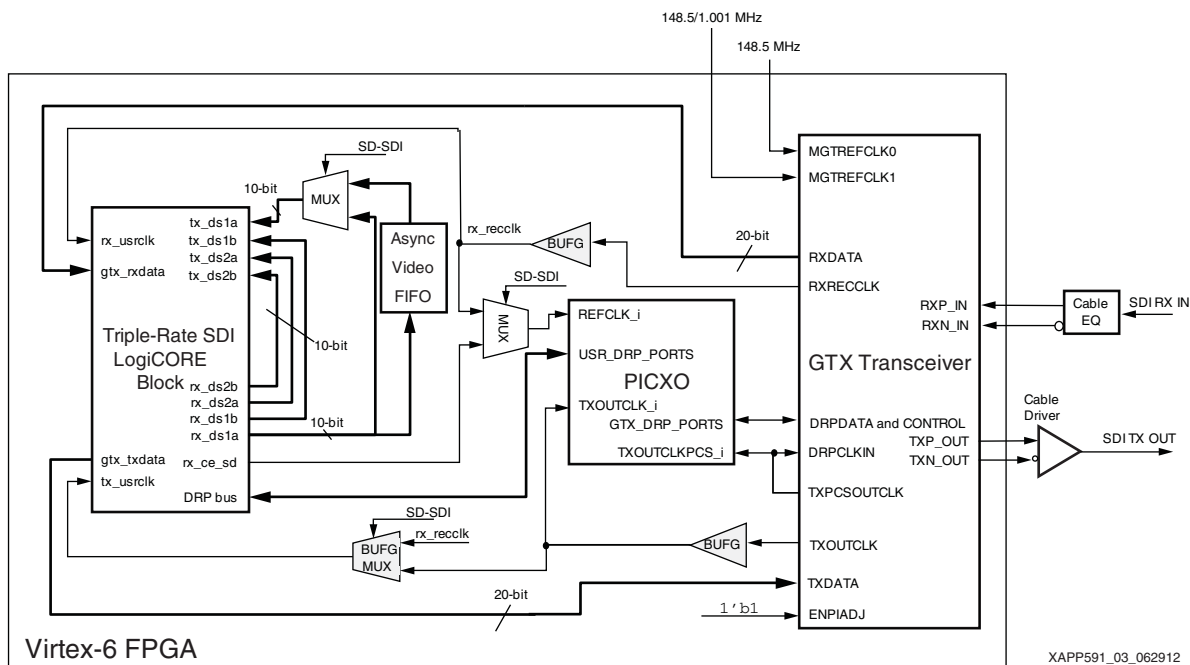


Figure 3: PICXO-Based Triple-Rate SDI Pass-Through Design

Demonstration Design Architecture

To best explain the benefits of using the new PICXO method, a four channel triple-rate SDI pass-through reference demonstration design is built. This design showcases the great simplification of the multichannel design by using the new clocking infrastructure. Figure 4 shows the four channel demonstration design architecture.

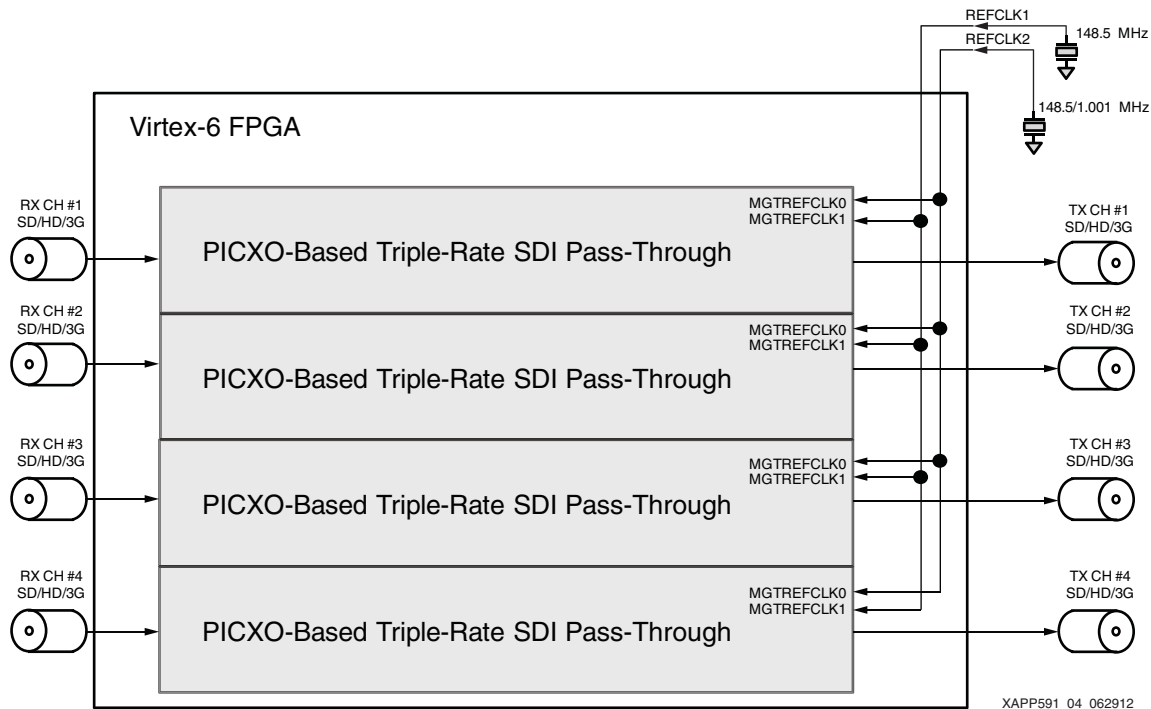


Figure 4: **Four-Channel Triple-Rate SDI Pass-Through Demonstration**

The single channel PICXO-based SDI pass-through instance (Figure 3) is instantiated four times. Each of them is connected to its corresponding SDI input and output ports. All four instances share two fixed reference clocks from outside (these clocks can be as simple as two relevant oscillators). Without using an external VCXO, all necessary jitter cleaning function is still provided on a per channel basis.

Demonstration Design Setup

The demonstration design is targeted to a Virtex-6 FPGA Broadcast Connectivity Kit [Ref 5]. The kit includes a Cook Technologies CTXIL671 SDI FMC daughter card that provides four channels of RX and TX, respectively [Ref 6]. Each CTXIL671 card comes with two clock modules capable of serving up to four reference clocks. Using the conventional approach, a maximum two channel pass-through can be implemented.

This demonstration design showcases four channel pass-through using only one clock module with two fixed reference clocks. Figure 5 illustrates the hardware setup.

The hardware required for the demonstration includes:

- One Virtex-6 FPGA Broadcast Connectivity Kit [Ref 5], including the ML605 evaluation card and the Cook Technology CTXIL671 daughter card
- A compact flash card formatted in FAT file system
- One mini-USB cable (included in the ML605 Evaluation Kit)
- Eight SDI 75Ω coax cables (or at least two cables for input and output, respectively)
- Four SDI video sources with various line rates covering SD, HD, and 3G SDI standards (or at least one programmable source with all the line rates supported)
- Four input SDI monitors or multiviewers (or at least one SDI monitor or multiviewer that supports all the line rates)
- A laptop PC with Xilinx® ISE® Design Suite 14.1 installed

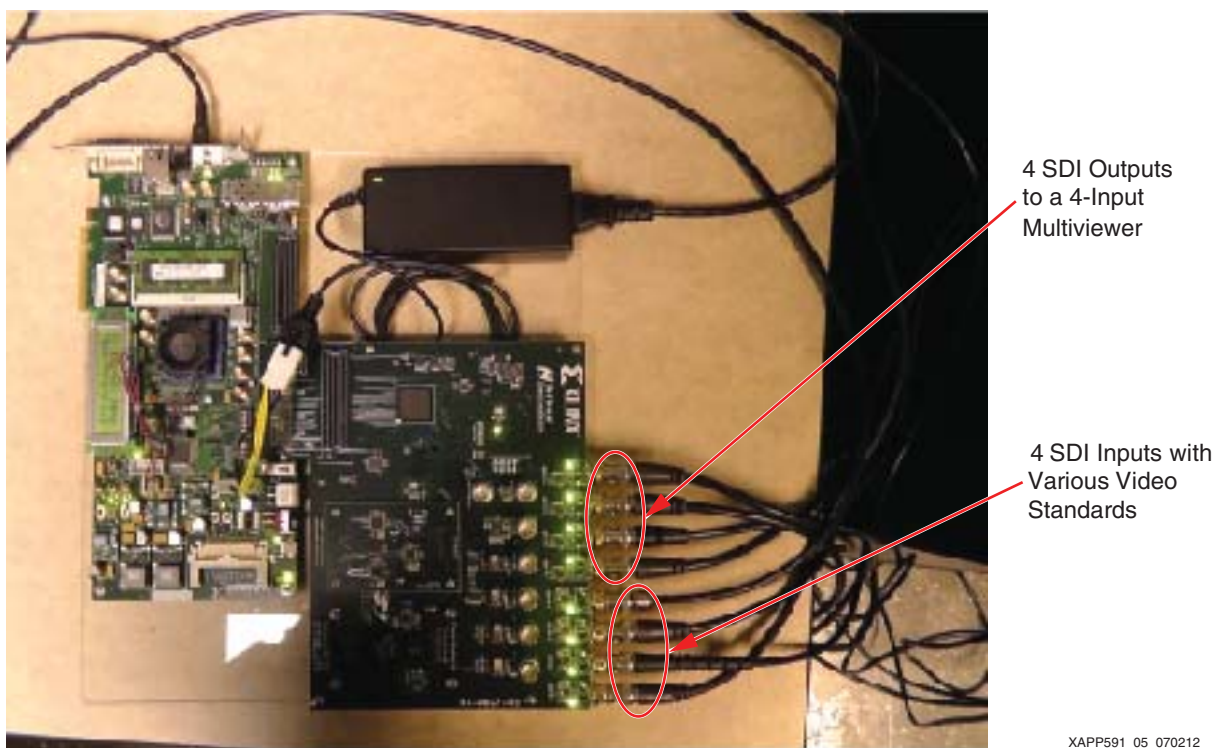


Figure 5: Four Channel Demonstration Hardware Setup

Figure 6 shows four different video standards concurrently passed through and displayed through the multiviewer. The four standards are:

- 3G-SDI 1080p60 Hz
- HD-SDI 1080i59.94 Hz
- HD-SDI 720p60 Hz
- SD-SDI 480i59.94 Hz



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Figure 6: Four Video Standards Passed Through and Displayed

Limited Characterization and Test

To further validate the performance of the PICXO-based pass-through design, some limited jitter tests have been conducted. Figure 7 illustrates the test setup.

An Omnitek OTM-1000 Waveform Monitor [Ref 4] is used to provide both video signal generation and eye jitter measurement. The video signal is programmed to cover all popular line rates including 270 Mb/s, 1.485 Gb/s, 1.4835 Gb/s, 2.97 Gb/s, and 2.967 Gb/s. All test results are illustrated in Table 1 and Table 2.

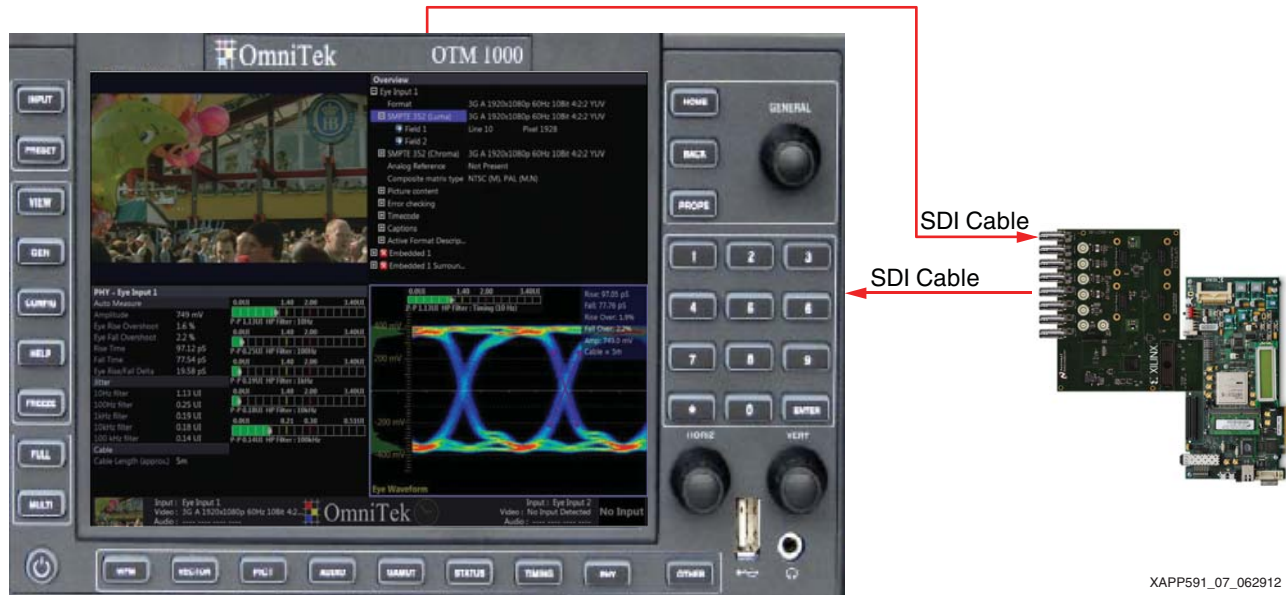


Figure 7: Triple-Rate SDI Pass-Through Transmitter Jitter Hardware Test Setup

Table 1: PICXO Triple-Rate SDI Pass-Through Transmitter Jitter Test Result for SD SDI

Video Format (Generated by OTM-1000)	Bit Rate (Mb/s)	SMPTE Timing Jitter Limit 10 Hz (UI)	SMPTE Alignment Jitter Limit 1 kHz (UI)	Demo Design RX Timing Jitter 10 Hz (UI)	Demo Design RX Alignment Jitter 1 kHz (UI)	Demo Design TX Timing Jitter 10 Hz (UI)	Demo Design TX Alignment Jitter 1 kHz (UI)
NTSC (480i59.94)	270	0.2	0.2	0.13	0.05	0.13	0.05
PAL (576i50)	270	0.2	0.2	0.14	0.05	0.14	0.05

Table 2: PICXO Triple-Rate SDI Pass-Through Transmitter Jitter Test Result for HD SDI and 3G SDI

Video Format (Generated by OTM-1000)	Bit Rate (Gb/s)	SMPTE Timing Jitter Limit 10 Hz (UI)	SMPTE Alignment Jitter Limit 100 kHz (UI)	Demo Design RX Timing Jitter 10 Hz (UI)	Demo Design RX Alignment Jitter 100 kHz (UI)	Demo Design TX Timing Jitter 10 Hz (UI)	Demo Design TX Alignment Jitter 100 kHz (UI)
HD 720p60	1.485	1	0.2	0.57	0.11	0.5	0.08
HD 720p50	1.485	1	0.2	0.61	0.11	0.55	0.08
HD 720p59.94	1.4385	1	0.2	0.61	0.09	0.52	0.06
HD 1080i60	1.485	1	0.2	0.57	0.1	0.5	0.08
HD 1080i50	1.485	1	0.2	0.54	0.11	0.49	0.06
HD 1080i59.94	1.4385	1	0.2	0.54	0.09	0.49	0.08
3G A 1080p60	2.97	2	0.3	1.36	0.23	1.3	0.15
3G A 1080p50	2.97	2	0.3	1.51	0.22	1.33	0.15
3G A 1080p59.94	2.967	2	0.3	1.58	0.19	1.2	0.11

It is clear that the PICXO-based triple-rate SDI pass-through not only successfully locks to any incoming SDI video standard but also offers a substantial amount of jitter cleaning on a per channel basis. With all the benefits provided by this innovative design, the broadcast industry

can now realize much easier system integration and lower cost (N external VCXO are eliminated).

Timing Constraints and Analysis

The demonstration design requires all relevant GTX transceiver clocks to run at 150 MHz. These clocks include TXOUTCLK, TXPCSOUTCLK, RXRECCLK, MGTREFCLK0, and MGTREFCLK1. The included project user constraints file (UCF) reflects this.

In addition, for any -1 speed grade Virtex-6 device, a specially screened device is required to allow the GTX transceiver DRP port to be clocked at a rate of up to 150 MHz. For more information on ordering these devices, please contact your Xilinx sales representative. In this design, the DRP port is clocked directly from the TXPCSOUTCLK clock.

All constraints recommended by *All Digital VCXO Replacement for Gigabit Transceiver Applications* [Ref 3] must be followed, including cross clock domain and U_SET constraints.

By following the above constraints and running the design through the standard Xilinx ISE design tools, the design yields zero setup or hold violations and hits exactly four component switching limits as listed in the section [Timing Summary](#).

Timing Summary

The following information is generated from the ISE design tools TRCE report.

Note: Using the specially screened devices, the errors from the report (the negative slack numbers) can safely be ignored.

Timing errors: 4 Score: 4104 (Setup/Max: 0, Hold: 0, Component Switching Limit: 4104)

Slack: -1.026 ns (period – min period limit)

Period: 6.666 ns

Min period limit: 7.692 ns (130.005 MHz) (Tgtxper_DCLK)

Physical resource: SDI1/SDIGTX/gtx0_v6sdi_wrapper_i/gtxe1_i/DCLK

Logical resource: SDI1/SDIGTX/gtx0_v6sdi_wrapper_i/gtxe1_i/DCLK

Location pin: GTXE1_X0Y7.DCLK

Clock network: SDI1/tx_pcsoutclk

Slack: -1.026 ns (period – min period limit)

Period: 6.666 ns

Min period limit: 7.692 ns (130.005 MHz) (Tgtxper_DCLK)

Physical resource: SDI2/SDIGTX/gtx0_v6sdi_wrapper_i/gtxe1_i/DCLK

Logical resource: SDI2/SDIGTX/gtx0_v6sdi_wrapper_i/gtxe1_i/DCLK

Location pin: GTXE1_X0Y6.DCLK

Clock network: SDI2/tx_pcsoutclk

Slack: -1.026 ns (period – min period limit)

Period: 6.666 ns

Min period limit: 7.692 ns (130.005 MHz) (Tgtxper_DCLK)

Physical resource: SDI3/SDIGTX/gtx0_v6sdi_wrapper_i/gtxe1_i/DCLK

Logical resource: SDI3/SDIGTX/gtx0_v6sdi_wrapper_i/gtxe1_i/DCLK

Location pin: GTXE1_X0Y5.DCLK

Clock network: SDI3/tx_pcsoutclk

Slack: -1.026 ns (period – min period limit)

Period: 6.666 ns

Min period limit: 7.692 ns (130.005 MHz) (Tgtxper_DCLK)

Physical resource: SDI4/SDIGTX/gtx0_v6sdi_wrapper_i/gtxe1_i/DCLK

Logical resource: SDI4/SDIGTX/gtx0_v6sdi_wrapper_i/gtxe1_i/DCLK

Location pin: GTXE1_X0Y4.DCLK

Clock network: SDI4/tx_pcsoutclk

Reference Design

The reference design files for this application note can be downloaded from:

<http://www.xilinx.com/member/vcxoff/>

Reference Design Checklist

The reference design checklist is shown in [Table 3](#).

Table 3: Reference Design Checklist

Parameter	Description
General	
Developer name	Xilinx
Target devices (stepping level, ES, production, speed grades)	Virtex-6 FPGAs
Source code provided	Yes
Source code format	Verilog
Design uses code/IP from existing Xilinx application note/reference designs, CORE Generator™ tool, or third party	Yes
Simulation	
Functional simulation performed	No
Timing simulation performed	No
Test bench used for functional and timing simulations	No
Test bench format	N/A
Simulator software/ version used	N/A
SPICE/IBIS simulations	N/A
Implementation	
Synthesis software tools/version used	ISE Design Suite 14.1
Implementation software tools/versions used	ISE Design Suite 14.1
Static timing analysis performed	Yes
Hardware Verification	

Table 3: Reference Design Checklist (Cont'd)

Parameter	Description
Hardware verified	Yes
Hardware platform used for verification	Virtex-6 Broadcast Connectivity Kit

Resource Utilization

The reference design utilization summary is listed in Table 4.

Table 4: Resource Utilization

Parameters	Specification/ Details	
Maximum frequency (by speed grade)	-1	150 MHz
Device utilization without test bench (mandatory)	Slices	8002
	GCLK buffers	14
	Block RAM	20
	GTX transceivers	4
HDL Language Support	Verilog	

Reference Design Directory Setup

Figure 8 shows the file structure of the demonstration design.

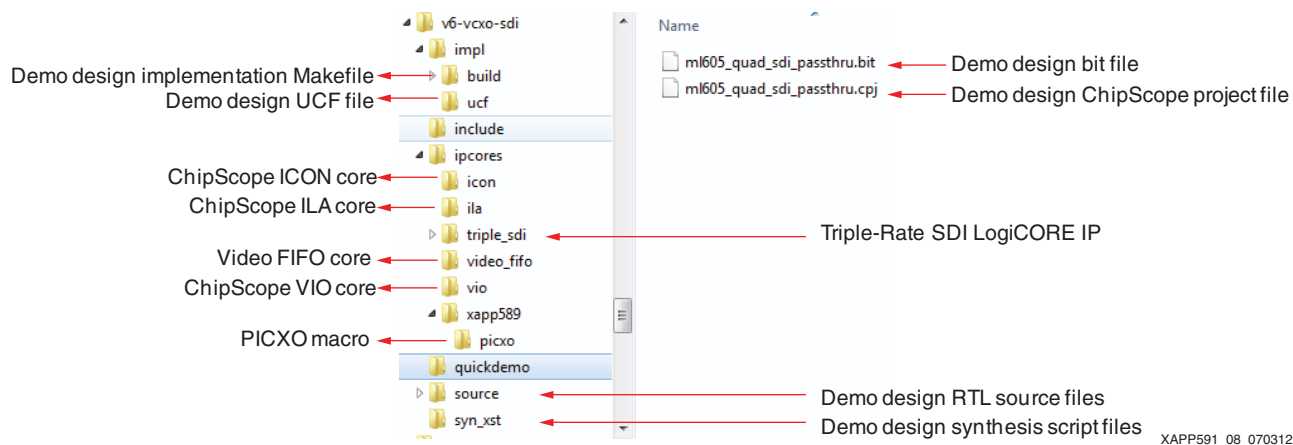


Figure 8: Demonstration Design File Structure

References

This document uses the following references:

- [XAPP1075](#), *Implementing Triple-Rate SDI with Virtex-6 FPGA GTX Transceivers*
- [UG366](#), *Virtex-6 FPGA GTX Transceivers User Guide*
- [XAPP589](#), *All Digital VCXO Replacement for Gigabit Transceiver Applications*
- OmniTek Product page
www.omnitek.tv/products/video-test-measurement/otm-1000.html
- Virtex-6 FPGA Broadcast Connectivity Kit
www.xilinx.com/products/boards-and-kits/DK-V6-BCCN-G.htm
- Cook Technologies CTXIL671 board page
www.cook-tech.com/ctxil671.php

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
07/27/2012	1.0	Initial Xilinx release.

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