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Virtex-II Pro / Virtex-II Pro X 3.3V I/O Design Guidelines

Summary

This application note describes guidelines on interfacing 3.3V I/O standards (PCI, LVTTL, and LVCMOS) in a Virtex™-II Pro / Virtex-II Pro X system design. Topics include overshoot/undershoot considerations, external regulator and bus switch solutions, device configuration, and other board level design techniques. For guidelines applicable to other FPGA families, refer to their respective user guides or data sheets.

Introduction

New system I/O standards continue the trend of lowering supply voltage to gain higher throughput performance. Still, many 3.3V I/O standards, including LVTTL, LVCMOS, and PCI, are prevalent to accommodate legacy requirements. To support all popular design requirements, Virtex-II Pro / Virtex-II Pro X devices offer a range of 3.3V to 1.5V I/O standards. Despite internal device power of 1.5V, the I/Os are designed to meet every system design challenge.

To achieve maximum performance and get the best the Virtex-II Pro / Virtex-II Pro X devices have to offer, several 3.3V I/O designs and techniques are highlighted in this application note. This includes managing overshoot/undershoot with termination techniques, regulating V_{CCO} at 3.0V with a voltage regulator, using external bus switches, reviewing configuration methods, and other design considerations.

I/O Standard Design Rules

Overshoot / Undershoot

Undershoot and overshoot voltages on I/Os operating at 3.3V should not exceed the absolute maximum ratings of –0.3V to 4.05V, respectively, when V_{CCO} is 3.75V. These absolute maximum limits are stated in the absolute maximum ratings table in Table 1 of the **Virtex-II Pro and Virtex-II Pro X Platform FPGA Complete Data Sheet**, Module 3. However, the maximum undershoot value is directly affected by the value of V_{CCO}. Table 1 describes the worst-case undershoot and overshoot at different V_{CCO} levels.

The voltage across the gate oxide at any time must not exceed 4.05V. Consider the case in which the I/O is either an input or a 3-stated buffer as shown in Figure 1. The gate of the output PMOS transistor P_o and NMOS transistor N_o is connected essentially to V_{CCO} and ground, respectively.

The amount of undershoot allowed without overstressing the PMOS transistor P_o is the gate voltage minus the gate oxide limit, or V_{CCO} – 4.05V.

Likewise, the absolute maximum overshoot allowed without overstressing the NMOS transistor N_o is the gate voltage plus the gate oxide limit, or Ground + 4.05V.

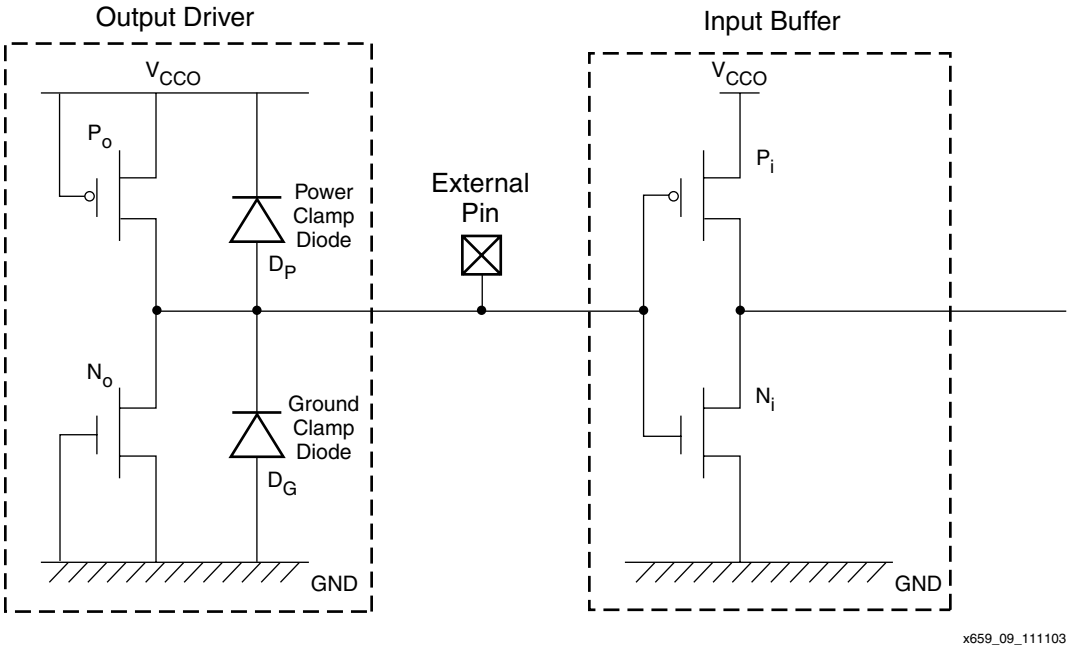

Figure 1: **Virtex-II Pro / Virtex-II Pro X I/O: 3-Stated Output Driver**

The lower absolute maximum has a direct relationship with V_{CCO}. It is further extended as V_{CCO} drops below 3.75V. Table 1 summarizes the absolute maximum undershoot and overshoot at different V_{CCO} levels. Note the absolute maximum overshoot value does not change with the V_{CCO} level.

Table 1: **Absolute Maximum Undershoot and Overshoot**

V_{CCO} (V)	Maximum Undershoot (V)	Maximum Overshoot (V)
3.75	–0.30	4.05
3.6	–0.45	4.05
3.45	–0.60	4.05
3.3	–0.75	4.05
3.0	–1.05	4.05

The clamp diodes offer protection against transient voltage beyond approximately V_{CCO} + 0.5V and Ground – 0.5V. Note the voltage across the diode increases proportionally to the current going through it. Therefore the clamped level is not fixed and can vary depending on the board design. The absolute maximum I/O limits might be exceeded even if the clamp diode is active.

The IBIS models contain the voltage-current characteristics of the I/O drivers and clamp diodes.

To verify overshoot and undershoot are within the I/O absolute maximum specifications, Xilinx recommends proper I/O termination and performing IBIS simulation. "Appendix A: Termination" summarizes the needs for and methods of termination.

LVTTL / LVCMOS

In general, the LVTTL and LVCMOS drivers should match the board trace impedance to within ±10% to minimize overshoot and undershoot. Source termination is often used for unidirectional interfaces. The Virtex-II Pro / Virtex-II Pro X digitally controlled impedance (DCI) feature has built-in source termination on all user output pins. It compensates for impedance changes due to voltage and/or temperature fluctuations, and can match the reference resistor values. Assuming the reference resistor values are the same as the board trace impedance, the output impedance of the driver will closely match with the board trace.

The LVDCI_33 standard is used to enable the DCI features for 3.3V I/O operations. As shown in Figure 2, the OBUF_LVDCI_33 primitive is used to implement the source termination function in Virtex-II Pro / Virtex-II Pro X output drivers. The pull-up resistor connected to VRN and the pull-down resistor connected to VRP determine the output impedance of all the output drivers in the same bank. For more details on using DCI, see **UG012**, *Virtex-II Pro and Virtex-II Pro X FPGA User Guide*.

Since the LVDCI_33 standard does not offer input termination, source termination must be implemented on the driver side. Figure 2 shows the recommended external source termination resistors to be incorporated on the external device side.

The total impedance of the LVTTL/LVCMOS driver added to the series termination resistor R_0 must match the board trace impedance ±10 percent to minimize overshoot and undershoot. An IBIS simulation is advised for calculating the exact value needed for R_0.

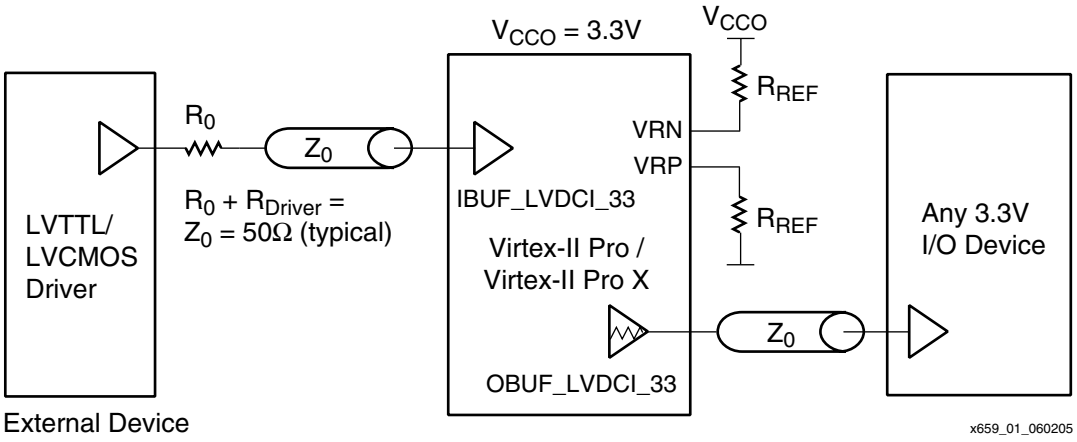

Figure 2: **Connecting LVTTL or LVCMOS Using the LVDCI_33 Standard**

The connection scheme shown in Figure 3 is for a bidirectional bus scenario. The signal performance may be degraded by R_0. Therefore, it is also recommended to verify the R_0 value and performance with an IBIS simulation.

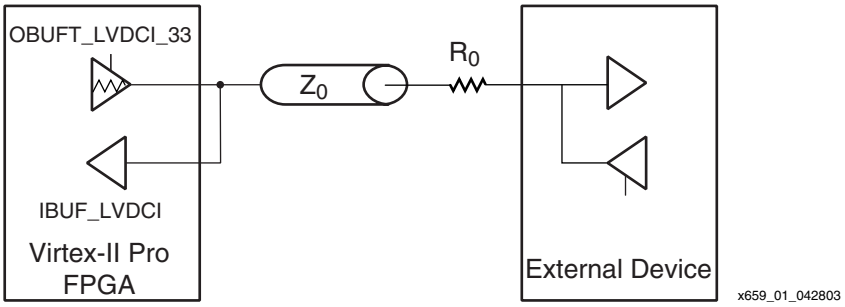

Figure 3: **3.3V I/O Configuration**

The following list contains helpful information for designing with the LVDCI_33 standard:

- The output drive strength and slew rates are not programmable. The output impedance references the VRP and VRN resistors, and the output current is determined by the output impedance.
- If only LVDCI_33 inputs are used, it is not necessary to connect VRP and VRN to external reference resistors. The implementation pad report does not record VRP and VRN being used. External reference resistors are required only if LVDCI_33 outputs are present in a bank.
- LVDCI_33 is compatible with LVTTL and LVCMOS standards only.
- Refer to **UG012** on how to use DCI. The user guide shows an HDL example as well as other DCI design considerations.

In addition, changing the slew rate from fast to slow and/or reducing the current drive could significantly reduce overshoot and undershoot.

The Xilinx **Signal Integrity Central** website contains additional design information to assist PCB designers and signal integrity engineers.

PCI Interface

Some interfaces such as PCI do not allow terminations. This section discusses alternatives for managing overshoot and undershoot for such applications.

As stated in Table 1, when V_{CCO} is lowered to 3.0V, the absolute maximum level remains at 4.05V. The *power clamp diode* limits overshoot at about 3.5V, preventing the upper absolute maximum level from being exceeded.

Similarly, the lower absolute maximum limit is –1.05V when V_{CCO} is 3.0V. In this case, the *ground clamp diode* clips undershoot at around –0.5V, preventing the lower absolute maximum level from being exceeded.

Therefore, lowering V_{CCO} to 3.0V addresses the PCI overshoot and undershoot specifications. Refer to **XAPP653**, *3.3V PCI Design Guidelines*, for more implementation details.

External Bus Switch

Another alternative to address overshoot and undershoot uses an external bus switch. **XAPP646**, *Connecting Virtex-II Devices to a 3.3V/5V PCI Bus*, discusses using IDT QuickSwitch devices to buffer between Virtex-II Pro / Virtex-II Pro X I/Os and external device driving signals between 3.3V to 5V.

Device Configuration

Virtex-II Pro / Virtex-II Pro X devices can be configured through a JTAG interface port, a serial PROM, or by a System ACE controller.

Dedicated configuration pins such as CCLK, PROG_B, DONE, M2, M1, and M0 are powered by V_{CCAUX} at 2.5V, including the PWRDWN_B and HSWAP_EN pins. Dual-purpose configuration pins such as DIN, D1:D7, CS_B, RDWR_B, BUSY/DOUT, and INIT_B can be either 2.5V or 3.3V. See Table 2 for details.

This section describes 3.3V I/O interface considerations for each configuration method. For further information on configuration, refer to **UG012**.

Table 2: **Virtex-II Pro / Virtex-II Pro X Pins and Bias Voltages**

Pin Name	Direction	Bias Voltage (V)	Comments
CCLK	Input/ Output	2.5	Pin is biased by V_{CCAUX}. Input should not be driven by a 3.3V signal unless a 100Ω series resistor is used. Output is LVCMOS25 and compatible with LVTTL.
PROG_B	Input	2.5	Pin is biased by V_{CCAUX} (2.5V). It should not be pulled up to 3.3V unless a 100Ω resistor is used.
DONE	Open-drain output	2.5	Pin is biased by V_{CCAUX} (2.5V). It should not be pulled up to 3.3V unless a 470Ω pull-up resistor is used.
M2, M1, M0	Input	2.5	Pin is biased by V_{CCAUX} (must be 2.5V). These pins should not connect to 3.3V unless 100Ω series resistors are used.
HSWAP_EN	Input	2.5	Pin is biased by V_{CCAUX} (must be 2.5V). This pin should not connect to 3.3V unless a 100Ω series resistor is used.
TDI	Input	2.5/3.3	Powered by V_{CCAUX}. Although pin is 3.3V tolerant.
TMS	Input	2.5/3.3	Powered by V_{CCAUX}. Although pin is 3.3V tolerant.
TCK	Input	2.5/3.3	Powered by V_{CCAUX}. Although pin is 3.3V tolerant.
TDO	Open-drain Output	2.5/3.3	Pin is open-drain and can be pulled to 3.3V. The external pull-up is recommended to be greater than 200Ω. There is no internal pull-up.
PWRDWN_B	Input	2.5	Pin is biased by V_{CCAUX} (2.5V). It has an internal pull-up. Do not pull up externally to 3.3V unless a 100Ω series resistor is used. This pin does not support the power-down feature.
DIN/D0-D7	Input/ Output	2.5/3.3	Pins are biased by V_{CCO}
CS_B	Input	2.5/3.3	Pins are biased by V_{CCO}
RDWR_B	Input	2.5/3.3	Pins are biased by V_{CCO}
BUSY/DOUT	Input	2.5/3.3	Pins are biased by V_{CCO}
INIT_B	Input/ Output	2.5/3.3	Pins are biased by V_{CCO}
VRP	Input	N/A	Reference resistor pulled to GND
VRN	Input	2.5/3.3	Reference resistor must be pulled to V_{CCO}
V_{REF}	Input	2.5/3.3	Depends on the I/O standard used.
DXN, DXP	N/A	N/A	These are the cathode and anode of the temperature diode
V_{BATT}	Input	3.0	Battery supply for the encryption keys
User I/O	Input/ Output	Various	All regular user I/Os support the following 3.3V signaling standards: LVTTL, LVCMOS, PCI33, PCI66, PCIX, LVDCI33

Dedicated Configuration Pins

Dedicated configuration pins such as CCLK, PROG_B, DONE, M2, M1, and M0 are powered by V_{CCAUX} at 2.5V, so they must not be exposed to 3.3V signals. However, in those cases in which these pins must be connected to 3.3V, Xilinx highly recommends either one of the following courses of action:

- Connect the pins to 42Ω series resistors before they connect to 3.3V.
- Ensure that no more than 8 mA of current goes through these pins at any time.

The DONE pin can connect through a 470Ω series resistor to 3.3V. If the DONE pins of multiple FPGAs are connected together and the pull-up resistor values recommended by the other FPGA family are larger than 470Ω, use the larger value for the connected DONE pin.

JTAG Configuration

Although JTAG pins are powered by V_{CCAUX} (2.5V), all JTAG input pins are 3.3V compatible and operate between 2.5V and 3.3V TTL levels. The JTAG output pin, TDO, is an open-drain output. It does not have an internal pull-up resistor and must be pulled up with an external resistor on the PCB. The maximum pull-up voltage is 3.3V. It is recommended to use an external pull-up resistor greater than 200Ω. Different resistor values yield different JTAG performance. Perform IBIS simulation to verify the speed. Series resistors are not needed for JTAG pins because they do not have clamp diodes.

Serial PROM Configuration

Xilinx recommends using the XCFxxP/XCFxxS series of Platform Flash In-System Programmable Configuration PROMs. The XC18Vxx configuration PROMs also can be used. These families provide 3.3V or 2.5V output capabilities. When interfacing to the Virtex-II Pro / Virtex-II Pro X device in master serial mode, the V_{CCO} of the PROM and the V_{CCO} of the Virtex-II Pro / Virtex-II Pro X device should connect to the same voltage level (2.5V or 3.3V). Figure 4 shows the Virtex-II Pro / Virtex-II Pro X FPGA and the configuration PROM in master serial configuration.

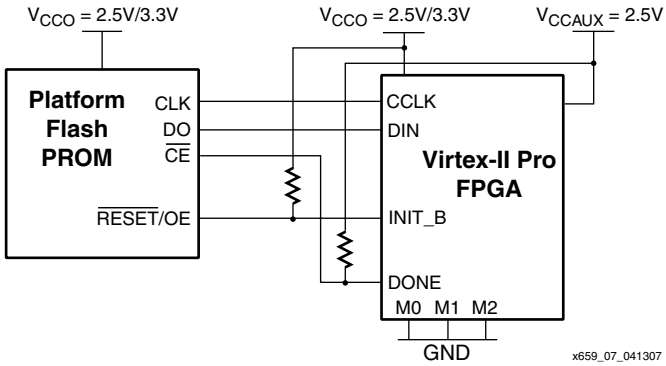

Figure 4: **Virtex-II Pro / Virtex-II Pro X FPGA and PROM in Master Serial Configuration**

Although the noise margin of LVCMOS_25 driving LVTTL is 100 mV, the LVCMOS25 driver will drive from rail-to-rail if the devices are connected as shown in Figure 4.

In slave serial mode, the V_{CCO} of the FPGA can be either 2.5V or 3.3V. However, ensure the CCLK pin of the FPGA is not exposed to 3.3V unless a 100Ω series resistor is used or the current is less than 3 mA.

System ACE Configuration

When interfacing a System ACE controller to a Virtex-II Pro / Virtex-II Pro X FPGA, set the V_{CCO} of the System ACE controller to either 1.8V or 2.5V, depending upon system DC power availability. For more information, see the **System ACE** website.

Further System Design Considerations

Supported 3.3V I/O Standards

The Virtex-II Pro / Virtex-II Pro X family supports the following 3.3V I/O standards:

- LVTTL: 24 mA, 16 mA, 12 mA, 8 mA, 6 mA, 4 mA, and 2 mA
- LVCMOS_33: 24 mA, 16 mA, 12 mA, 8 mA, 6 mA, 4 mA, and 2 mA
- PCI_33, PCI_66, and PCI_X
- LVDCI_33

DC Power Distribution System

Designers need to consider power distribution in their system designs. Many systems have 5V, 3.3V, 2.5V, 1.8V, 1.5V, and other DC power requirements. Use **XAPP623**, *Power Distribution System (PDS) Design: Using Bypass/Decoupling Capacitors*, as a guide to determine board level decoupling requirements for a successful system design

Package Thermal Management

The absolute maximum junction temperature (T_J) is 125°C for 3.3V I/O operation for the Virtex-II Pro / Virtex-II Pro X FPGA. Use Xilinx package guide **UG112**, *Device Package User Guide*, as a design resource for thermal measurement techniques, package thermal characteristics, and options for power management in a system environment. The document also contains some references for heat-sink and interface material suppliers.

LVDS

Although the Virtex-II Pro / Virtex-II Pro X Platform FPGA does not support LVDS_33, its input and output specifications are compatible with LVDS_25. It is acceptable to use LVDS_25 in place of LVDS_33.

Choosing Solutions

Both **XAPP653** and **XAPP646** have been fully verified. Xilinx recommends **XAPP653** for designing Virtex-II Pro / Virtex-II Pro X systems in a PCI 3.3V environment, as it is PCI-compliant and provides a lower cost solution than **XAPP646**.

Table 3 lists application notes to consult for guidance, based on the PCI signaling environment.

Table 3: **Reference Application Notes**

Signaling Environment	Virtex-II Devices	Virtex-II Pro / Virtex-II Pro X Devices
PCI 3.3V	Not Required	XAPP653 or XAPP646
PCI 5.0V	XAPP646	XAPP646
LVTTL/LVCMOS33	Not Required	XAPP659

Mixing Techniques

Either using LVDCI_33 standard or lowering the V_{CCO} to 3.0V is a good approach to address overshoot and undershoot. It is also acceptable to combine both methods. When V_{CCO} is lowered to 3.0V, it is not necessary to adjust the reference resistors VRP and VRN. The VRP and VRN values should always be the same as the board trace impedance.

Conclusion

Virtex-II Pro / Virtex-II Pro X devices support 3.3V I/O standards (LVTTL, LVCMOS33, LVDCI33, PCI33/66, and PCI-X) when the following guidelines are met:

1. Keep signal overshoot and undershoot within the absolute maximum FPGA device specifications. Four methods are discussed:
   a. Source termination using LVDCI_33
   b. Slow slew rate and/or reduced drive current
   c. Voltage regulation at 3.0V for PCI
   d. External high-speed bus switches for PCI
2. For PCI bus solutions, use either **XAPP653** or **XAPP646**.
3. Dedicated I/O pins are restricted to 2.5V only.
4. The absolute maximum junction temperature (T_J) is 125°C for 3.3V I/O operation.

Appendix A: Termination

Transmission line effects can cause voltage deviations at both the driver and receiver. The worst of these effects causes voltage doubling. For example, a 3.3V I/O standard signal can double to 6.6V at the load when termination effects are ignored. *Clock frequency is not a parameter of interest. Transmission line effects cannot be ignored simply because a design uses a relatively slow clock frequency.*

Transmission line effects become prevalent when the time it takes a signal to propagate from the driver to the receiver and back to the driver is longer than 1/6th the I/O rise or fall time. Typical transmission speeds on a printed circuit board (PCB) are 200 ps per inch. Figure 5 shows the difference between the LVCMOS 24mA fast slew rate driver (24F) and LVCMOS 2mA slow slew rate driver (2S) when driving into an unterminated load. The respective rise times are approximately 1 ns vs. 7 ns, or a 7:1 variation.

The maximum trace length before transmission line effects become prominent for a 1 ns rise time is (1/6) * (1 ns) * (1/2) * (1 inch/0.2 ns), or 0.42 inches. For a 7 ns rise time, the result is (1/6) * (7 ns) (1/2) (1 inch/0.2 ns), or 2.9 inches.

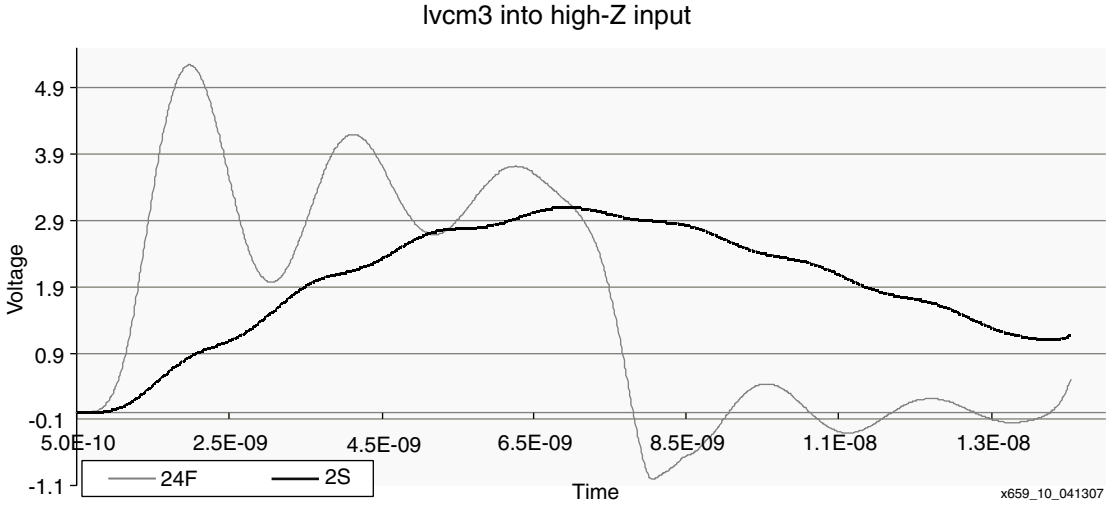

Figure 5: **Rise Time Comparison between Slowest and Fastest LVCMOS I/O Selections**

To satisfy high-speed memory design requirements, faster I/O drivers typically are chosen. Typical memory, processor, and FPGA device packages exceed 0.4 inches in size. Therefore, it is realistic to expect transmission line effects for virtually all practical memory PCB layouts.

Xilinx recommendeds that the slowest I/O speed possible is used for a given application, which might contradict the high-speed memory application requirements above. Nevertheless, serious consideration must given to using the slowest slew rate possible.

Figure 6 depicts the receiver signals for two different slew rate selections with the same 50Ω, 0.5 ns long transmission line interconnect. From the figure, the slower slew rate does not suffer the same magnitude overshoot and undershoot issues at the receiver.

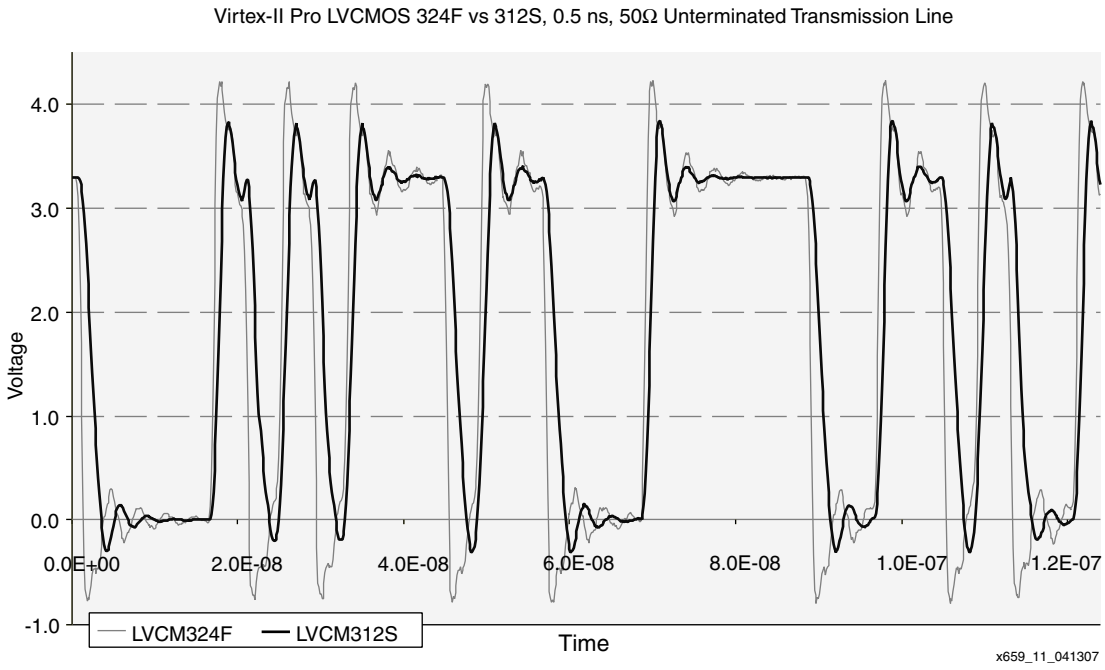

Figure 6: **Example Slew Rate Impact at the Receiver on Overshoot and Undershoot**

Transmission line effects are captured by the reflection equation that states the voltage excursion at the load follows the relationship:

$$(R_{LOAD} - Z_0)/(R_{LOAD} + Z_0)$$

An unterminated high-impedance condition at the receiver causes voltage doubling at the receiver. In this situation, R_{LOAD} (load input impedance) is very high—much greater than the transmission line impedance, Z_0. Because typical transmission line impedances range from 45 to 65Ω and receiver input impedances are in the mega-ohms, large voltage overshoots and undershoots can occur easily in unterminated situations. The undershoot condition suffers the same consequence, that is, simply a negative overshoot.

The impact of implementing LVCMOS versus LVTTL drivers into an unterminated receiver is illustrated in Figure 7.

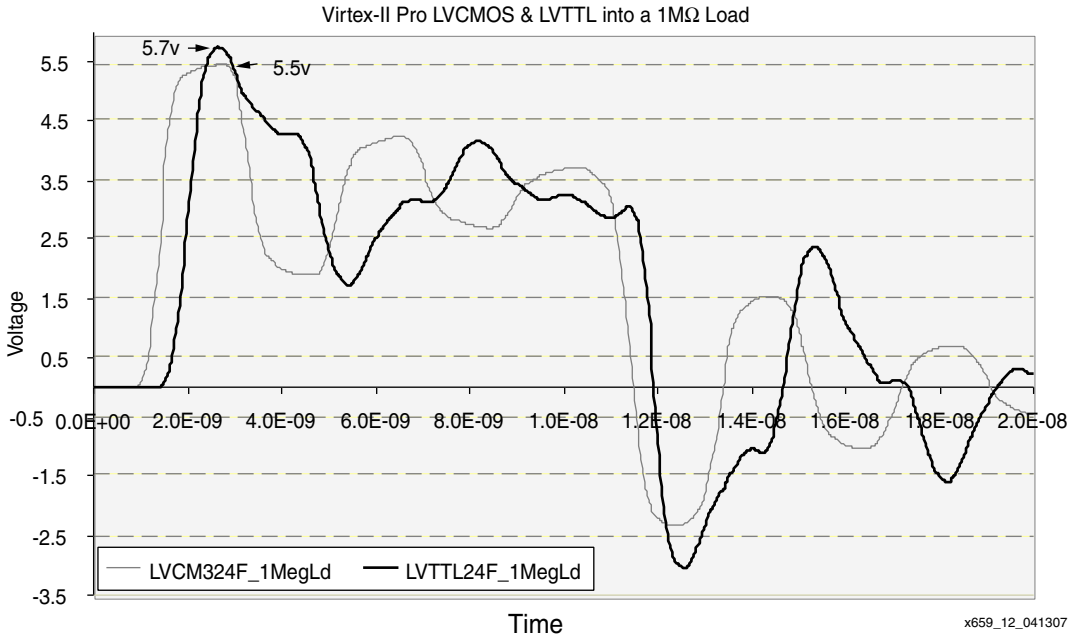

Figure 7: **Overshoot and Undershoot Effects**

Various configurations of passive components, referred to as terminations, can significantly reduce overshoot and undershoot voltage excursions. Some of the most basic configurations are Series, Parallel, and Split Parallel. These three configurations are described below along with their subsequent impact.

Series Source Termination

Series Resistor (R_S) Source Termination is accomplished by placing a resistor in series with the driver pin. PCB trace having impedance Z_0. The resistor should be placed close to the driver to minimize the effect of reflections between the driver and the resistor.

Figure 8 depicts the classic series termination technique.

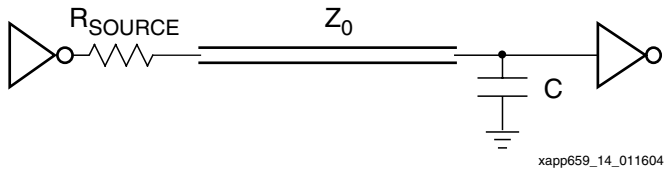

Figure 8: **Series Source Termination Topology**

As indicated previously, Z_0 represents the impedance of the PCB trace and is assumed to be one uniform value over the trace length. The capacitor in the schematic represents the connection capacitance from the receiver to the driver reference and is composed mainly of the component package connection and receiver die capacitance. Using one capacitance value is a low frequency approximation, which is valid as long as the rise time of the arriving signal is significantly less than the propagation time from the package pin to the die. Many rules of thumb exist, but one in common practice is 1/6th of the package propagation time. Overshoot and undershoot are minimized by choosing the series resistor's value in the following manner:

$$R_{SOURCE} = Z_0 - \text{Driver Output Impedance}$$

Driver Output Impedance varies with the SelectIO™ resource, but typically ranges between 15 and 45Ω. Using an IBIS simulation in conjunction with Xilinx IBIS models is the recommended way to optimize driver impedance determination and subsequent selection of R_{SOURCE}.

By following this technique, the transmitted I/O standard voltage high state is reduced to half. The technique relies on the assumption that the receiver input impedance is very high. Therefore, by the reflection equation, the transmitted voltage doubles at the receiver. Subsequently, this doubled voltage reflects back toward the driver. But, in choosing R_{SOURCE} as indicated above, the load impedance matches Z_0 and the reflection ceases at the driver.

This technique works best for unidirectional interfaces. In particular, clocks, address, and control signals benefit from this topology. Figure 9 shows a 25Ω series termination example with Virtex-II Pro / Virtex-II Pro X LVCMOS 324F drivers.

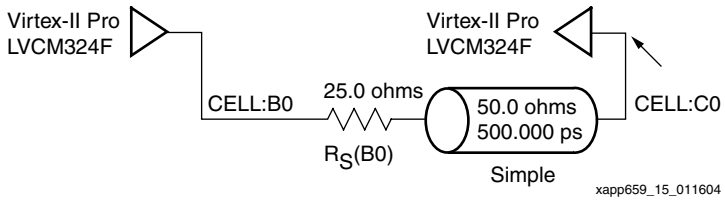

Figure 9: **Series Termination Schematic**

Figure 10 shows the effects of R_{SOURCE} in this circuit, comparing R_{SOURCE} values of 0Ω and 25Ω. A distinct advantage of Series Source Termination is that the resistor limits trace current, which helps in reducing overall power consumption and electromagnetic emissions (EMI).

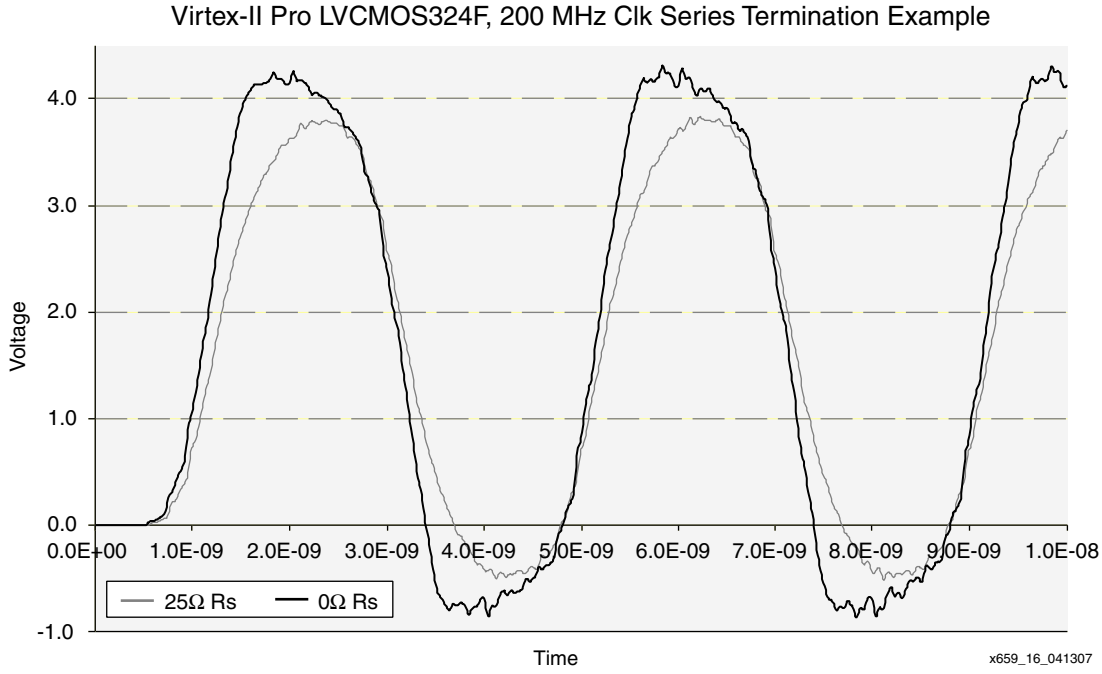

Figure 10: **Waveforms Generated by the Series Termination Schematic**

Parallel Termination

Figure 11 shows the parallel termination topology, where a terminating resistor (R_L) is placed at the receiver to an AC voltage reference. The resistor needs to be placed as closely to the receiver as feasible to minimize reflections between the receiver and the resistor. The simplest reference for the terminating resistor is ground. The I/O standard driving waveform propagates at full magnitude toward the receiver. If R_L is matched with Z_0, the reflection equation produces a result of zero, indicating that a reflection is not produced. Check V_{OH}/ R_L for current drain and power consumption to ensure that neither the driver or resistor specifications are violated.

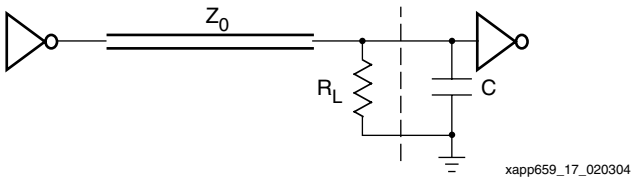

Figure 11: **Parallel Termination Topology**

Figure 12 shows the schematic for Parallel termination.

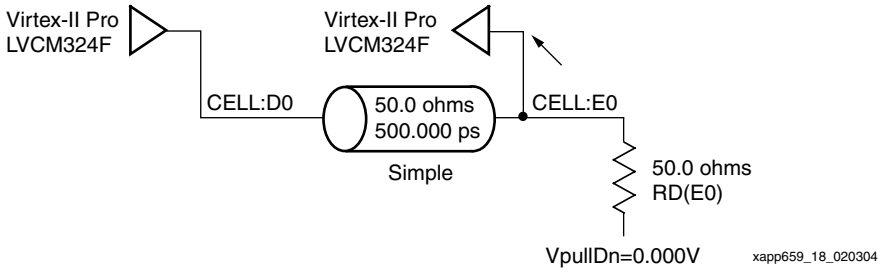

Figure 12: **Parallel Termination Schematic**

Figure 13 presents waveforms for two Parallel termination schematic cases: matched termination and unterminated instances are shown (R_L is absent). A pseudo random bitstream (PRBS) pattern is shown instead of the clock pattern to better represent this technique's application, which typically is an address bus.

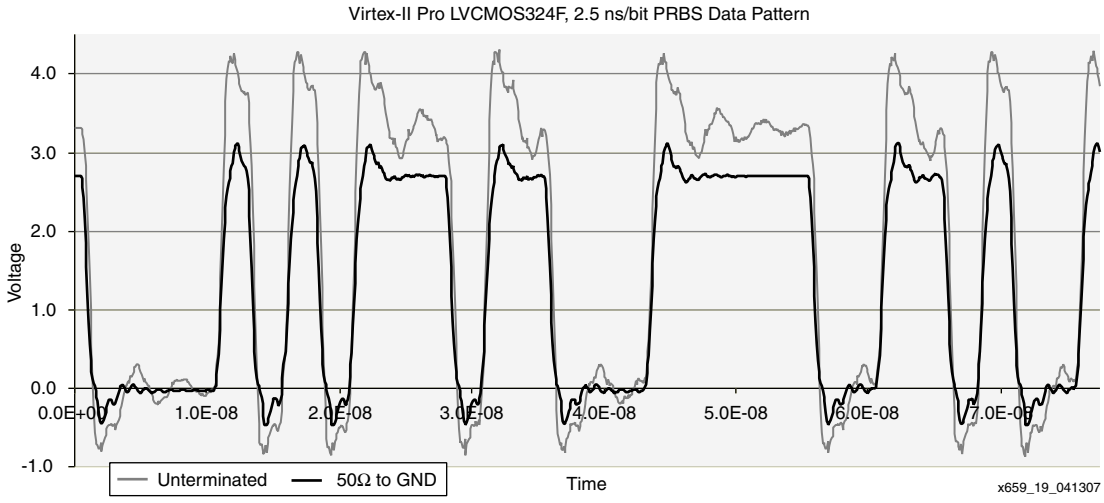

Figure 13: **Waveforms Generated by the Parallel Termination to Ground Schematic**

Split Parallel Termination

Figure 14 shows the Split Parallel Termination topology. The additional resistor offers adjustment of a driver's high versus low output impedance. If this impedance is symmetrical, then $R_1 = R_2$. Further, the parallel combination of R_1 and R_2 must match Z_0.

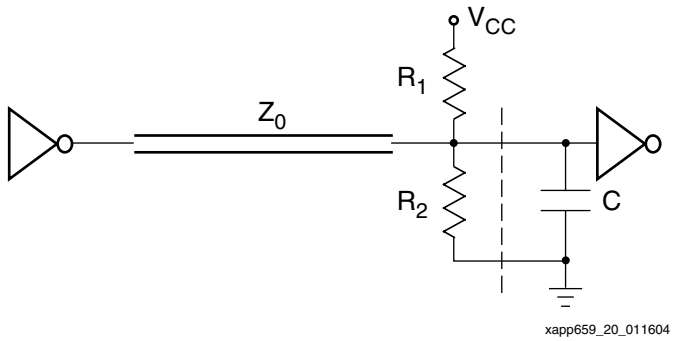

Figure 14: **Split Parallel Termination Topology**

V_{CC} may be chosen to center the driver output swing near the receiver logic switch level threshold, thereby minimizing terminator power consumption, maximizing frequency of operation, and minimizing duty cycle distortion. This termination technique creates a more symmetrical waveform at the receiver and should be used when duty cycle is critical. Power consumption of the V_{CC} supply as well as the power dissipated in the termination resistors and driver must be considered.

Figure 15 shows a schematic of this termination technique.

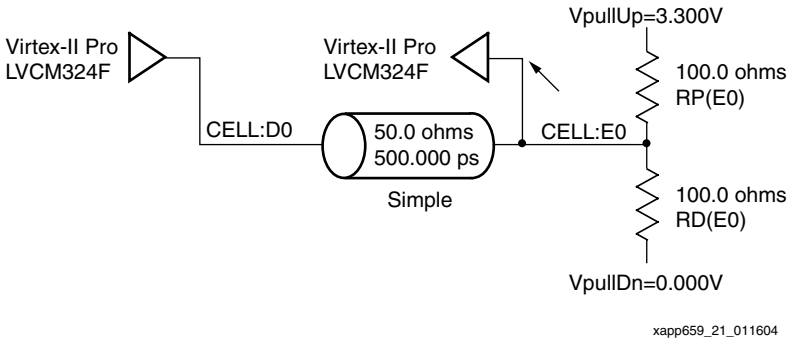

Figure 15: **Split Parallel Termination Schematic**

Figure 16 shows example waveforms generated by the schematic in Figure 15 using a PRBS pattern was used. Note that undershoot must be reduced compared to the simple parallel termination technique.

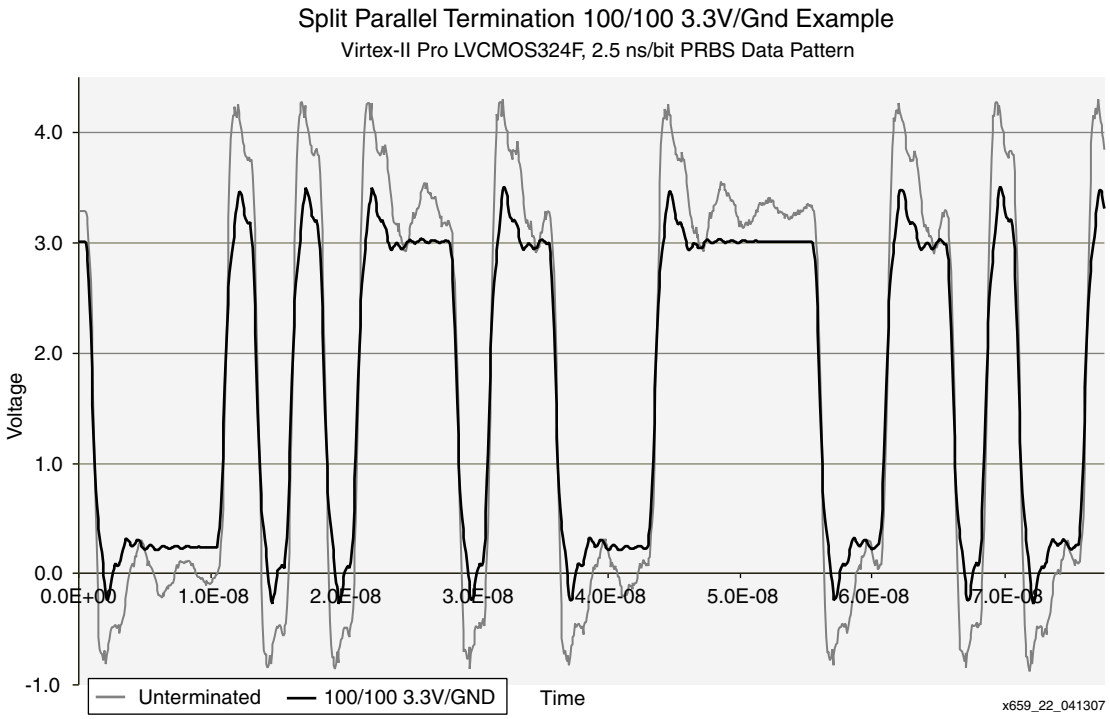

Figure 16: **Waveforms Generated by the Split Parallel Termination Schematic**

Xilinx offers an integrated solution for SSTL and HSTL technologies. This solution is referred to as DCI and effectively creates a split parallel termination or series termination associated with the SSTL and HSTL standards. An SSTL example is depicted in Figure 17.

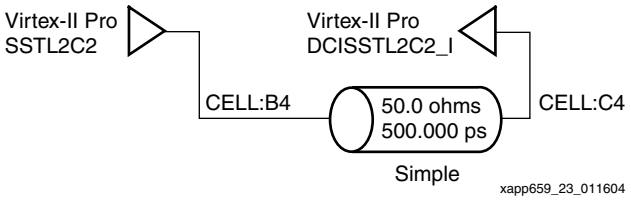

Figure 17: **SSTL Schematic**

The waveforms generated by this schematic are shown in Figure 18.

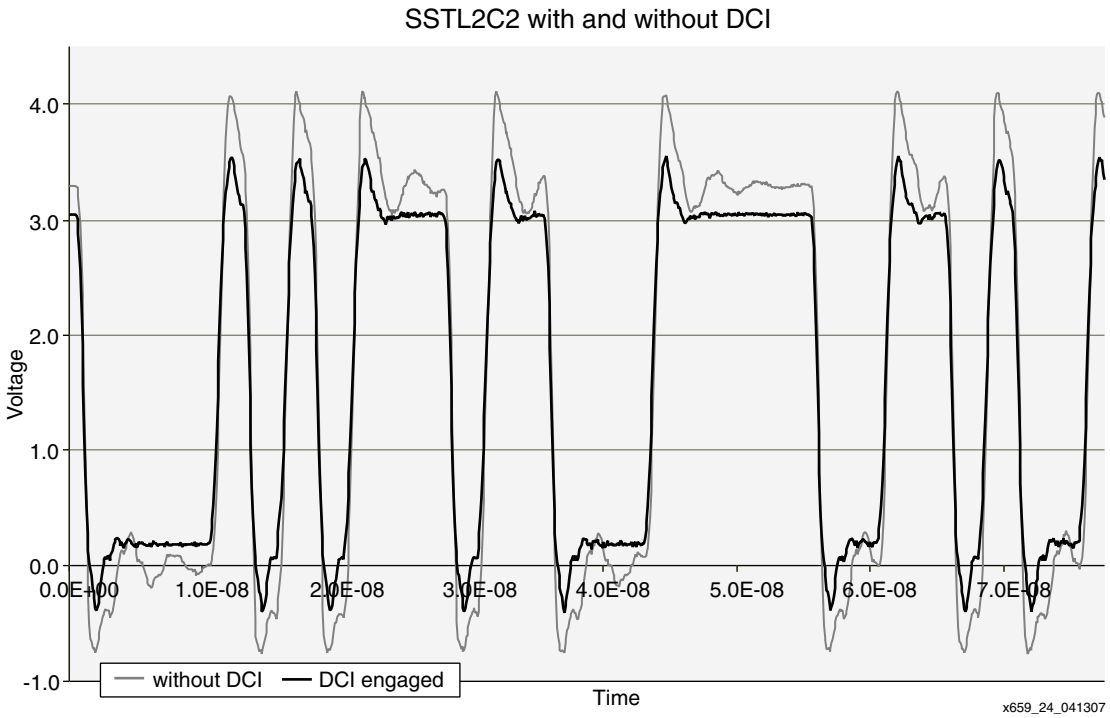

Figure 18: **Waveforms Generated by SSTL2C2 Schematic**

DCI is an effective mechanism to prevent unwanted overshoot and undershoot. Refer to **UG012** to view all DCI options.

Additionally, parasitics such as vias, lead wires, solder bumps and packaging as well as temperature and silicon process variations affect the exact nature of reflections. Therefore, a safety margin is recommended when dealing with overshoot and undershoot.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/25/02	1.0	Initial Xilinx release.
01/06/03	1.1	Add PCIX, LVTTL_33 and LVCMOS_33 support. Removed 3.3V banking restrictions
01/07/03	1.2	Added new sub-section on supported 3.3V I/O standards.
05/06/03	1.3	Revised "Serial PROM Configuration" section. Added Table 2. Removed implementation support section since the tools have been updated. Revised "Further System Design Considerations". Clarified 100°C for 3.3V I/O operation in "Package Thermal Management".
12/01/03	1.4	Revised "Overshoot / Undershoot", "PCI Interface", and "Serial PROM Configuration" sections. Updated series and pull-up resistor information for Table 2. Added "Dedicated Configuration Pins" sections describing series resistor requirements for dedicated configuration pins. Revised absolute maximum junction temperature to 125•C. Added slow slew rate and/or reduced drive current bullet to "Conclusion". Added **Appendix A** containing voltage-current characteristics for I/O protection diodes.

Date	Version	Revision
02/04/04	1.5	Replaced "Appendix A: Termination" with transmission line and termination information. Moved "Conclusion" above the appendix.
06/09/05	1.6	• Corrected all references to Virtex-II Pro devices to include Virtex-II Pro X devices. • Deleted redundant material already covered in XAPP653 and XAPP646, replacing it with references to these application notes.
04/24/07	1.7	• Revised Table 2. • Revised "Dedicated Configuration Pins" section. • Revised "Package Thermal Management" section.