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Using Digitally Controlled Impedance: Signal Integrity vs. Power Dissipation Considerations

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Summary

On-die termination (ODT) promises higher signaling rates for printed circuit board (PCB) inter-chip interfaces through improved signal integrity. However, when using ODT, there is sometimes an associated power penalty. This application note explains the reason for the power penalty and suggests a simulation technique for comparing the signal integrity and power dissipation of internally and externally terminated versions of an interface. The termination architecture that is most appropriate to a product's requirements can be chosen intelligently in advance, thus saving valuable engineering design cycles.

Introduction

With the advent of Digitally Controlled Impedance (DCI) in Xilinx FPGAs comes the promise of implementing higher speed interfaces through superior Signal Integrity (SI) as well as reduced Bill of Materials (BOM) part count and, therefore, lower production cost in electronic designs. However, DCI (often referred to as ODT in electronic trade publications and component data sheets) should not be considered a panacea for every electronic design challenge. Like most aspects of engineering, DCI represents an inherent compromise between two or more desirable goals, and its use must be evaluated in a system-level architectural analysis to decide whether DCI should be used in any particular design.

This application note begins by introducing the concept of SI quantification, which allows signal quality to be expressed in a less qualitative, more meaningful way. It then shows how to calculate input/output (I/O) power dissipation (PD) for several common circuit topologies in both DCI and non-DCI cases. With these two pieces of information, intelligent choices can be made regarding the system-level trade-offs between PD and SI. Finally, these techniques are applied to two specific design examples that are typical of current electronic design activity: the SSTL18 (see [Ref 1]) termination standards applied to DDR2 SDRAM address/control and data lines.

SI Quantification

A proper and conclusive evaluation of several different termination topologies requires their behavior to be described quantitatively. This section discusses one way of doing this.

Eye Diagram Construction

Eye diagrams are used to analyze the quality of interfaces because they provide an aggregate view of the interface's performance. The interface cannot be designed to perform well for only a single bit in a particular data stream. Rather, it must be ensured to perform well for every bit of any data stream (subject to the design limitations of the chosen interface). The aggregate signal represented in the eye diagram is an ideal vehicle for achieving this goal and so is used exclusively in this work.

Eye Diagram SI Metrics

It is necessary to define and justify the SI metrics to be applied to the measured eye diagrams. The following three metrics of eye diagram quality are used in this application note.

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Overshoot/Undershoot

This is a measure of the extent to which the maximum and minimum voltages recorded in the eye fall outside the I/O cell's power supply range, $0-V_{CCO}$, or $0-1.8V$ for the two specific design examples used later in this application note. This metric is an important characteristic of the signal impinging upon an input. Input voltages that lie too far outside the power supply range can damage gate oxides and/or cause increased system PD due to increased average protection diode current flow. This application note reports overshoot/undershoot *margin* to remain consistent with the other two metrics for which higher positive numbers imply a better eye.

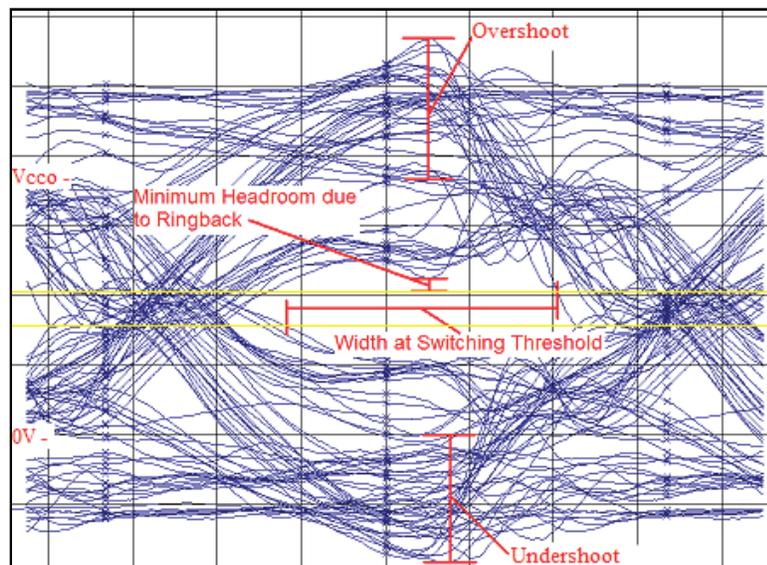
Eye Width at Switching Thresholds

This is a measure of the duration in time during which the voltage at an input lies either above the minimum High input level or below the maximum Low input level, whichever is shorter. This metric is an important characteristic of the signal impinging upon an input; it determines how much timing margin is available to accommodate such things as clock jitter/skew, signal skew, input buffer delay variation, etc., while still allowing for correct data capture.

Minimum Headroom Due to Ringback

This metric is a measure of the vertical clearance between the switching threshold and the point of maximum negative reflection in the data valid window. It is an important characteristic of the signal impinging upon an input because it determines how much voltage margin is available to accommodate noise while still allowing for correct data capture.

Figure 1 illustrates these three eye metrics and was generated by simulating an unterminated Virtex™-5 SSTL18_II 1 ns delay link in HyperLynx. As shown, the performance of such a link is very poor. The horizontal yellow lines represent the input switching thresholds for this standard. The bottom reference for the overshoot measurement is V_{CCO} , which is 1.8V for this I/O standard.



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Figure 1: Sample Eye Showing Three Chosen Metrics

Power Dissipation Calculations

This application note is only concerned with those components of system PD that change depending upon whether or not DCI is used. Therefore, all internal switching currents are ignored when calculating PD, and instead, only the currents flowing through the following components are considered:

- I/O totem pole transistors
- External termination network
- Internal DCI termination network, when enabled
- Any capacitive loads driven

Furthermore, the PD analysis is divided into the following two categories:

- The static (DC or quiescent) power dissipated due to the continuous current that flows through the termination network (external or internal) when the output has settled into its new state.
- The dynamic (AC or active) power dissipated due to the transient current that must flow immediately after the output switches state in order to charge any capacitance attached to the output node to the new steady-state level.

Static vs. Dynamic I/O Power Dissipation

Because the static PD is a function only of the average DC voltage level of the output and of the DC characteristics of the particular termination network chosen, it is not frequency dependent. While this is not strictly true (it ignores the effect of finite rise and fall times), the distinction being made between static and dynamic power dissipation remains valid. The dynamic PD, however, is frequency dependent since it must charge and discharge the output node capacitance through the output voltage range with every cycle of the output state. To show the frequency dependence of the results, it is necessary to differentiate between the static and dynamic PD.

The static PD is easily calculated by taking the average of the power dissipation due to the effective resistance of the termination network that occurs for the High and Low output states. It is assumed, for the sake of simplicity, that the output spends an equal amount of time in its High and Low states.

Calculating the dynamic PD is more complicated. [Ref 2] provides a detailed treatment of this topic. Equation 1 is taken from [Ref 2] and gives the dynamic power, P, dissipated by a driver connected to a capacitive load, which is being continually charged and discharged over the full extent of the power supply voltage range:

$$P = f \times C \times V^2 \quad \text{Equation 1}$$

Where:

- f = cycling frequency of the load capacitor (fclk/2 for randomly changing DDR data lines; fclk/4 for SDR data lines)
- C = capacitance of the load capacitor
- V = output driver's supply voltage (V_{CCO} in this case)

However, Equation 1 overestimates the dynamic power dissipated when the capacitive load is not being charged and discharged through the full supply voltage range, as is the case with the specific examples considered later. Figure 2 shows an output driver stage driving a capacitive load.

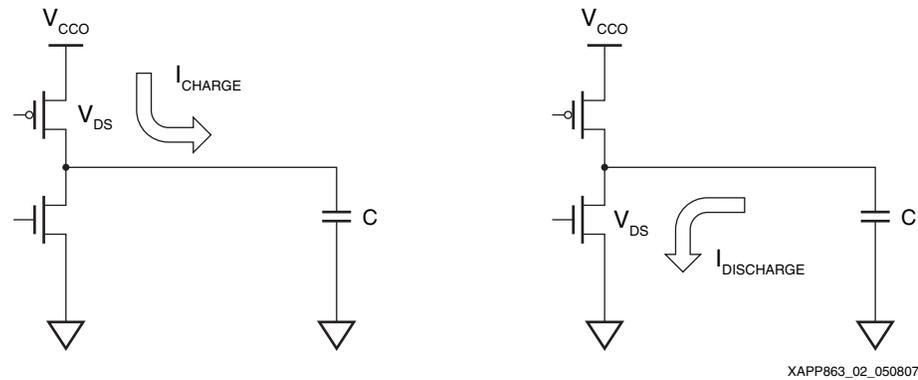


Figure 2: Schematic Showing Charge and Discharge of Capacitive Load

A typical drive cycle proceeds as follows:

1. At time $t = 0$, the upper transistor turns on and the lower transistor turns off. Also at this time, the voltage across the capacitor is V_1 .
2. Current flows from the V_{CCO} supply through the upper transistor into the capacitor, gradually charging it to some final voltage, V_2 .
3. At time $t = T/2$, the upper transistor turns off and the lower transistor turns on.
4. Current now flows out of the capacitor through the lower transistor into ground, discharging the capacitor to voltage V_1 at time $t = T$, at which point the cycle begins again.

The power dissipated by the upper and lower transistors during the charging and discharging phases of the cycle is calculated as follows. Taking the charging phase first, at any time, t , the voltage across the upper transistor is given by Equation 2.

$$V_{DS}(t) = V_{CCO} - V_C(t) \quad \text{Equation 2}$$

The instantaneous power dissipated by the upper transistor is given by Equation 3.

$$P(t) = V_{DS}(t) \times I(t) \quad \text{Equation 3}$$

So, the increment of energy dissipated by the transistor can be defined by Equation 4 as:

$$\begin{aligned} dE(\text{charge}) &= P(t)dt = V_{DS}(t) \times I(t)dt \\ &= [V_{CCO} - V_C(Q_C)]dQ_C \\ &= [V_{CCO} - V_C] \times CdV_C \end{aligned} \quad \text{Equation 4}$$

Where the independent variable has changed from t to Q_C and then to V_C . Equation 5 integrates the energy differential over the voltage range of interest to give the total energy dissipated by the upper transistor during the charging phase of the cycle.

$$E(\text{charge}) = C \left[V_{CCO} \int_{V_1}^{V_2} dV_C - \int_{V_1}^{V_2} V_C dV_C \right] = C \left[V_{CCO}(V_2 - V_1) - \frac{V_2^2 - V_1^2}{2} \right] \quad \text{Equation 5}$$

The energy dissipated by the lower transistor during the discharging phase of the cycle is given by Equation 6:

$$dE(\text{discharge}) = V_C(Q_C) \times (-dQ_C) = -C \times V_C dV_C \quad \text{Equation 6}$$

Where the sign inversion on dQ_C is necessary to accommodate the fact that energy dissipated in the lower transistor is accompanied by a reduction in the charge stored in C. Equation 7 integrates dE to give:

$$E(\text{discharge}) = -C \int_{V_2}^{V_1} V_C dV_C = -C \times \frac{V_1^2 - V_2^2}{2} = C \times \frac{V_2^2 - V_1^2}{2} \quad \text{Equation 7}$$

Equation 5 and Equation 7 are added to get the total energy dissipated per charge/discharge cycle as shown in Equation 8.

$$E_{CYC} = C \times V_{CCO} \times (V_2 - V_1) \quad \text{Equation 8}$$

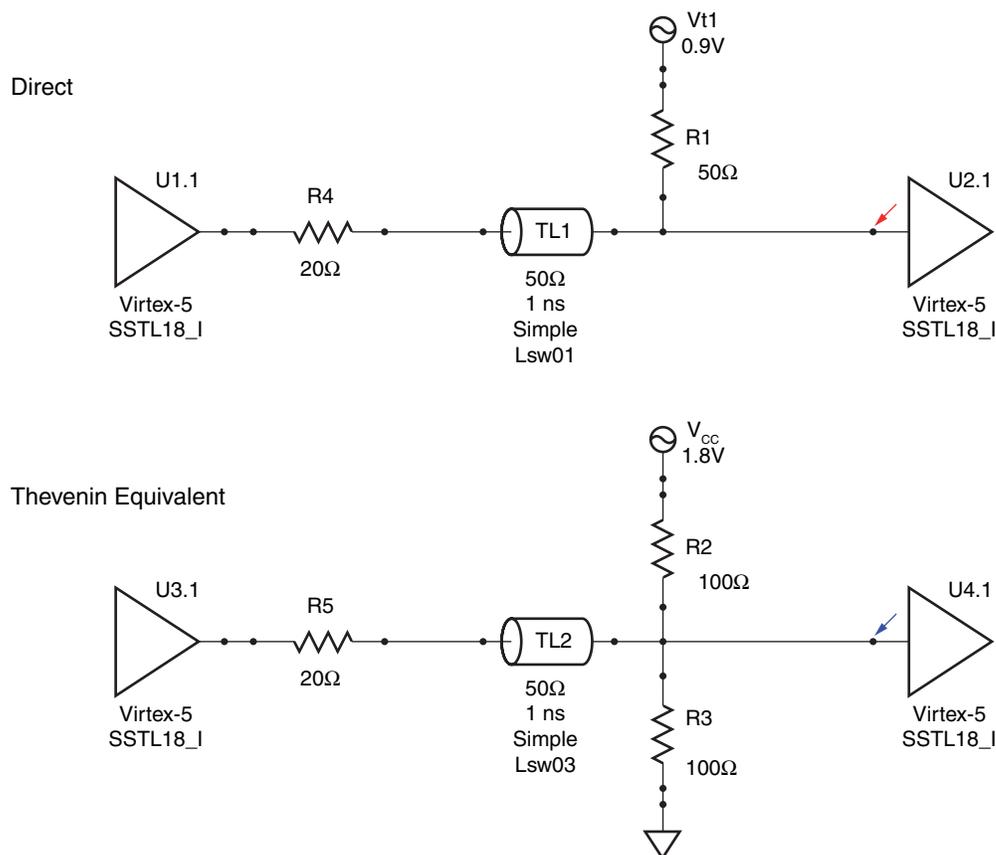
Multiplying E_{CYC} by the cycle repetition rate gives the *average dynamic power dissipation* (Equation 9) for any arbitrary values of High and Low settling voltages:

$$P_{DYNAMIC} = f \times C \times V_{CCO} \times V_{DCpp}(\text{in}) \quad \text{Equation 9}$$

Where $V_{DCpp}(\text{in})$ is the DC peak-to-peak voltage swing at the receiver's input node, i.e., the peak-to-peak voltage swing ignoring any switching transient ringing. Setting $V_{DCpp}(\text{in})$ equal to V_{CCO} reduces Equation 9 to Equation 1, which is correct.

Direct vs. Thevenin Equivalent Termination

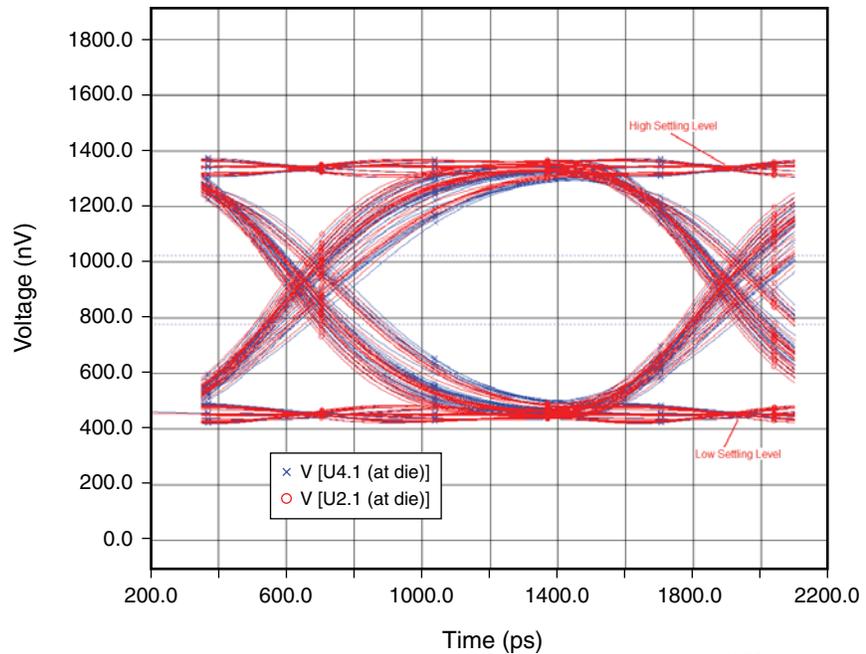
When parallel terminating the receiving end of a transmission line resistively, two basic topologies tend to be used in the majority of real-world design examples: direct and Thevenin equivalent. These two termination schemes are depicted schematically in Figure 3. Both schemes use series termination at the driving end of the line.



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Figure 3: Direct vs. Thevenin Equivalent Termination

Both termination schemes shown in Figure 3 present the incoming switching transients with an effective termination of 50Ω to $0.9V$. The SI at the inputs of U2 and U4 are, therefore, expected to be the same, and the two waveforms are plotted in Figure 4. The plots in Figure 4 show the eyes predicted by HyperLynx for the signals at the inputs of receivers U2 and U4, when probed at the die, and when the two drivers, U1 and U3, are set to produce a 2^7 PRBS pattern at 800 Mb/s.



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Figure 4: Superimposed Eyes Showing Equivalent SI for Direct and Thevenin Termination

As shown in Figure 4, both direct and Thevenin equivalent termination yield the same SI at the receiver's input, as expected. This does not imply that external and internal (i.e., DCI) termination provide the same SI. Other differences between external and internal termination, besides topology, affect SI (see "Example 1: SSTL18 Class I").

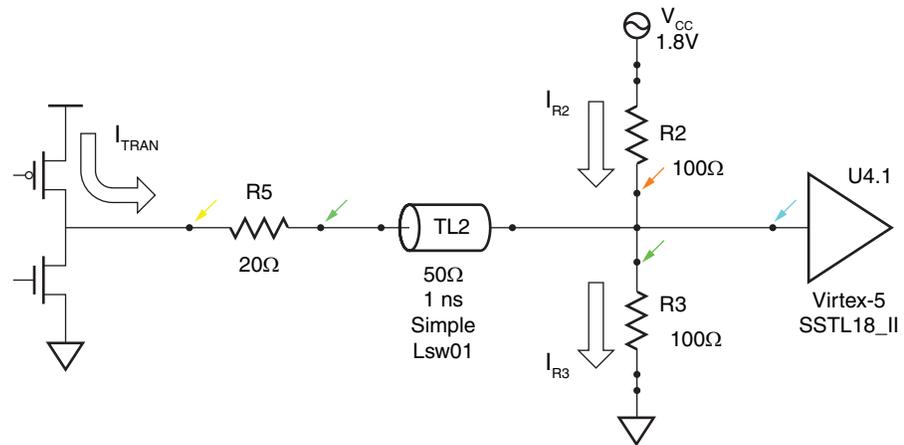
The dynamic PD is the same for both termination schemes because they are both driving the same capacitive load. The High and Low state static PD for the directly terminated case is straightforward and is obtained by calculating the current flowing through the 50Ω termination resistor (because no current flows into the receiver input in the non-DCI case) and multiplying that current by the total voltage drop through which it falls, which is $0.9V$ ($V_{CCO} - V_{CCO}/2 = V_{CCO}/2 = 0.9V$) in either case. It is necessary to include the entire voltage drop that the current falls through, including the drop across the output driver's pass transistor and the 20Ω series termination resistor, in order to calculate the total power dissipated. In general, average static power dissipation is given by Equation 10:

$$\begin{aligned} \bar{P}_{STATIC(Direct)} &= \frac{V_{CCO}}{2} \times \frac{1}{2} \left[\frac{\left(V_{IN(hi)} - \frac{V_{CCO}}{2} \right) + \left(\frac{V_{CCO}}{2} - V_{IN(low)} \right)}{Z_0} \right] \\ &= \frac{V_{CCO}}{4Z_0} \times V_{DCpp}(in) \end{aligned} \quad \text{Equation 10}$$

Where Z_0 is the characteristic impedance of the transmission line (and, therefore, assuming the line is terminated properly, the termination resistance). Equation 10 actually gives the worst-

case bound on average static power dissipation because it ignores the finite rise and fall times of the input signal, which tend to reduce average static power dissipation.

For the Thevenin equivalent case, the total power is obtained by adding the power dissipated by the three components that draw current; namely, the top and bottom parallel termination resistors (R2 and R3 in Figure 3) and the on transistor in the driver output's totem pole (the upper PMOS transistor in the High case, and the lower NMOS transistor in the Low case). This is shown schematically in Figure 5, which is similar to Figure 3 except that U3 is replaced with a schematic depiction of its output totem pole structure. The High case has been shown in Figure 5.



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Figure 5: Schematic for Deriving Thevenin Static Power Dissipation

Solving for the general case yields equations in terms of V_{CC0} , V_{in} , and Z_0 . The power dissipated by the two termination resistors, R2 and R3, in the High case is given by Equation 11 and Equation 12, respectively.

$$P_{STATIC_R2}(hi) = \frac{V^2}{R} = \frac{(V_{CC0} - V_{IN}(hi))^2}{2Z_0} \quad \text{Equation 11}$$

$$= \frac{V_{CC0}^2 - 2V_{CC0}V_{IN}(hi) + V_{IN}(hi)^2}{2Z_0}$$

$$P_{STATIC_R3}(hi) = \frac{V_{in}(hi)^2}{2Z_0} \quad \text{Equation 12}$$

The power dissipated by the on transistor and its series terminator, R5, is obtained by first determining what current is flowing through them, and then using $P = VI$ to determine their total PD. $P = V^2/R$ cannot be used because the transistor's on resistance is unknown and is not constant. To determine the current flowing through the on transistor and R5, it is seen that (Equation 13):

$$I_{R3} = I_{R2} + I_{TRAN} \quad \text{Equation 13}$$

That is, the current flowing through the upper totem pole transistor adds to the current flowing through the upper resistor in the termination network and the resultant total current is what flows through the lower resistor. Furthermore, it is known that I_{R2} and I_{R3} are given by [Equation 14](#) and [Equation 15](#), respectively.

$$I_{R2} = \frac{V_{CCO} - V_{in}(hi)}{2Z_0} \quad \text{Equation 14}$$

$$I_{R3} = \frac{V_{in}(hi)}{2Z_0} \quad \text{Equation 15}$$

Rearranging [Equation 13](#) gives [Equation 16](#):

$$I_{TRAN} = I_{R3} - I_{R2} = \frac{2V_{in}(hi) - V_{CCO}}{2Z_0} \quad \text{Equation 16}$$

and [Equation 17](#):

$$\begin{aligned} P_{STATIC_Qon+R5}(hi) &= V \times I = (V_{CCO} - V_{in}(hi)) \times \frac{2V_{in}(hi) - V_{CCO}}{2Z_0} \\ &= \frac{-V_{CCO}^2 - 2V_{in}(hi)^2 + 3V_{CCO}V_{in}(hi)}{2Z_0} \end{aligned} \quad \text{Equation 17}$$

Adding [Equation 11](#), [Equation 12](#), and [Equation 17](#) gives the total static PD in the Thevenin equivalent case for the High state ([Equation 18](#)).

$$\begin{aligned} P_{STATIC}(\text{Thevenin_hi}) &= \\ &= P_{STATIC_R2}(hi) + P_{STATIC_R3}(hi) + P_{STATIC_Qon+R5}(hi) \\ &= \frac{V_{CCO}^2 - 2V_{CCO}V_{in}(hi) + 2V_{in}(hi)^2 - V_{CCO}^2 - 2V_{in}(hi)^2 + 3V_{CCO}V_{in}(hi)}{2Z_0} \quad \text{Equation 18} \\ &= \frac{V_{CCO}V_{in}(hi)}{2Z_0} \end{aligned}$$

This result could have been easily determined by noticing that all the current in [Figure 5](#) flows through R3 and experiences a voltage drop equal to V_{CCO} . [Equation 19](#) provides a similar analysis for the Low case.

$$P_{STATIC}(\text{Thevenin_low}) = \frac{V_{CCO}(V_{CCO} - V_{in}(low))}{2Z_0} \quad \text{Equation 19}$$

[Equation 20](#) gives the average static PD in the Thevenin equivalent case.

$$\begin{aligned} \bar{P}_{STATIC}(\text{Thevenin}) &= \frac{P_{STATIC}(\text{Thevenin_hi}) + P_{STATIC}(\text{Thevenin_low})}{2} \\ &= \frac{V_{CCO}^2 + V_{CCO} \times V_{DCpp}(in)}{4Z_0} = \frac{V_{CCO}^2}{4Z_0} + \frac{V_{CCO}}{4Z_0} \times V_{DCpp}(in) \end{aligned} \quad \text{Equation 20}$$

Comparing [Equation 10](#) and [Equation 20](#) confirms that the average static power dissipated in the Thevenin equivalent case should be greater than that in the directly terminated case by exactly the power dissipated by the two termination resistors, R2 and R3, being placed across the power supply rails. Substituting the particular values for V_{CCO} , V_{in} , and Z_0 into [Equation 10](#) and [Equation 20](#) gives [Equation 21](#) and [Equation 22](#), respectively.

$$\bar{P}_{STATIC}(\text{Direct}) = 8.1 \text{ mW} \quad \text{Equation 21}$$

$$\bar{P}_{STATIC}(\text{Thevenin}) = 24.3 \text{ mW} \quad \text{Equation 22}$$

[Equation 21](#) and [Equation 22](#) show that a 200% static power penalty is incurred for choosing the Thevenin equivalent style termination scheme for this particular I/O standard and circuit

topology. The significance of this penalty is unknown until the ratio of static PD to total PD (i.e., Total PD = static PD + dynamic PD) is determined.

Assuming that the receiver has 10 pF of input capacitance and that the link is running at 800 Mb/s (i.e., $f_{CLK} = 400$ MHz) as shown in Figure 4, then, inferring a value of 0.9V for $V_{DCpp(in)}$ from Figure 4 and referring to Equation 9, the dynamic PD is given by Equation 23:

$$P_{DYNAMIC} = 200 \text{ MHz} \times 10 \text{ pF} \times 1.8 \text{ V} \times 0.9 \text{ V} = 3.24 \text{ mW} \quad \text{Equation 23}$$

Which is the same for either termination scheme. Combining this result for the dynamic PD with the static PD results for direct and Thevenin equivalent termination, respectively, gives the total PD for both termination schemes (Equation 24 and Equation 25).

$$P_{TOTAL(Direct)} = P_{STATIC(Direct)} + P_{DYNAMIC} \quad \text{Equation 24}$$

$$P_{TOTAL(Thevenin)} = P_{STATIC(Thevenin)} + P_{DYNAMIC} \quad \text{Equation 25}$$

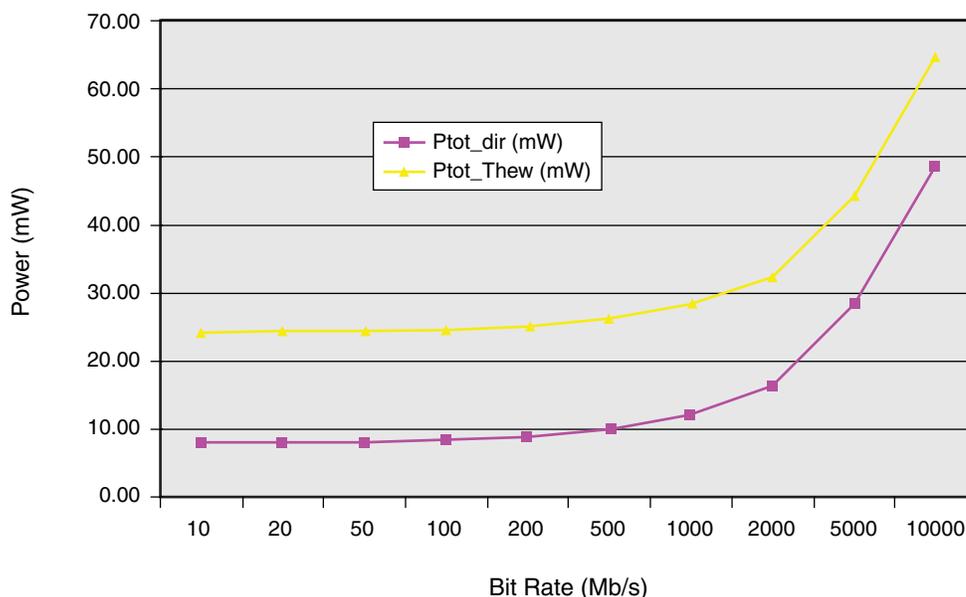
This yields 11.3 mW and 27.5 mW for the total PD in the direct and Thevenin equivalent cases, respectively. From a total PD perspective, the actual penalty for using Thevenin equivalent termination is an additional 143%, which is a severe penalty but not as severe as a static PD analysis alone would have been. In addition to increasing the total PD over that of the externally, directly terminated case, all of the PD is moved inside the FPGA.

There are three main reasons to use the Thevenin equivalent termination style:

- Sometimes, using an asymmetric split termination is the only way a line can be properly terminated while still providing a sufficient voltage swing at the receiver's input.
- When DCI is chosen as an alternative to external termination components, the choice of termination style is relinquished and the style is dictated by the DCI topology for a particular I/O standard. In the case of the two standards used here as examples, that style is Thevenin equivalent.
- Sometimes, it is cost prohibitive to include a direct termination voltage source in a design.

Finally, Figure 6 shows how the total PD comparison between direct and Thevenin equivalent termination schemes varies as a function of data bit rate.

The data is synthesized simplistically. The value of f in Equation 9 ranges from 2.5 MHz to 2,500 MHz, and it is incorrectly assumed that this does not change the value of $V_{DCpp(in)}$. The plot thus generated in Figure 6 is not very accurate.



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Figure 6: Total Power Dissipation Comparison for Direct vs. Thevenin Termination

At bit rates below about 1 Gb/s, the PD difference between the Thevenin equivalent and direct termination styles is fairly constant and represents a significant power penalty when considered relative to the total PD.

Example 1: SSTL18 Class I

The first example is a DDR2 SDRAM address/control line using SSTL18 Class I signaling and includes a comparison of the SI and PD of several different topologies. The schematic used to run the simulation in HyperLynx is shown in Figure 7. The transmission lines are assumed to be six inches of FR4 at 180 ps/in. A 0.9V supply rail is also provided so that direct external termination can be used. If this supply rail had not been provided, no power penalty would have been paid for using DCI termination since direct external termination would not have been available as an option. That is, external termination would have to be Thevenin equivalent as well.

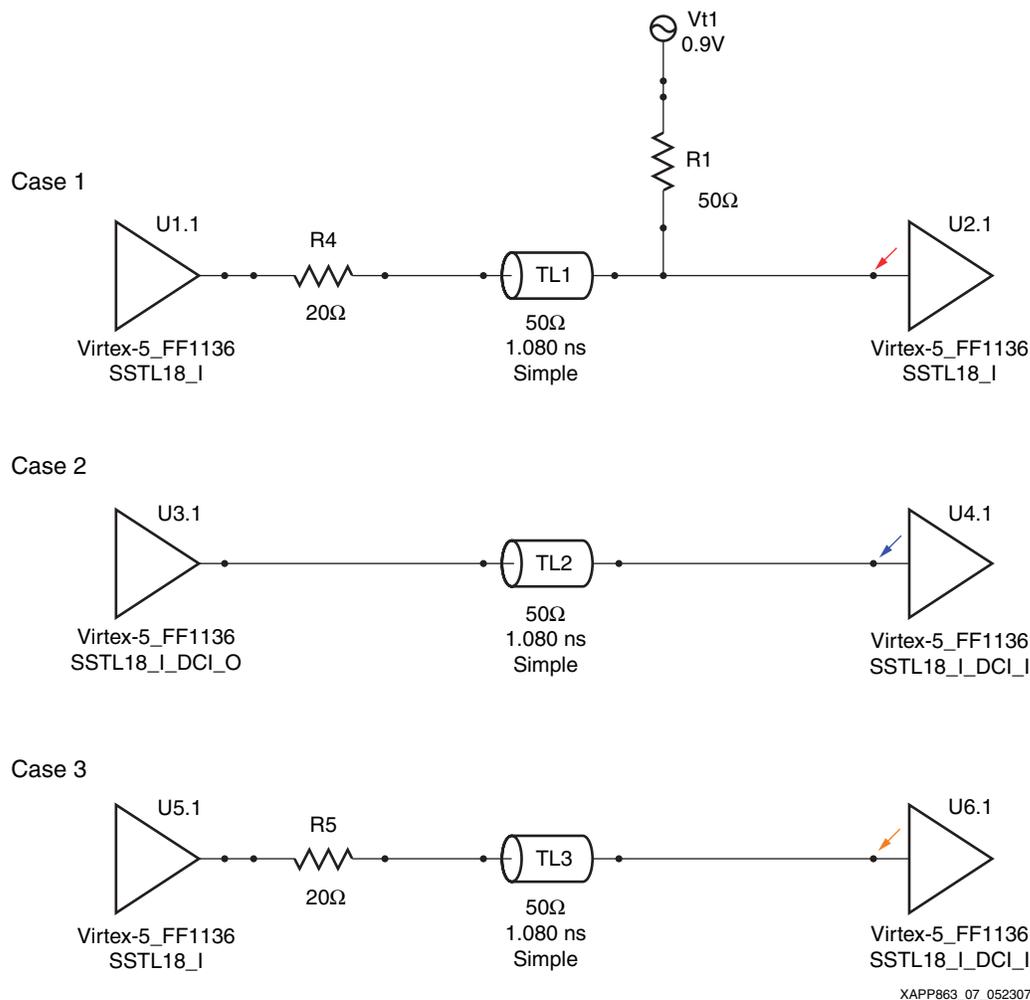


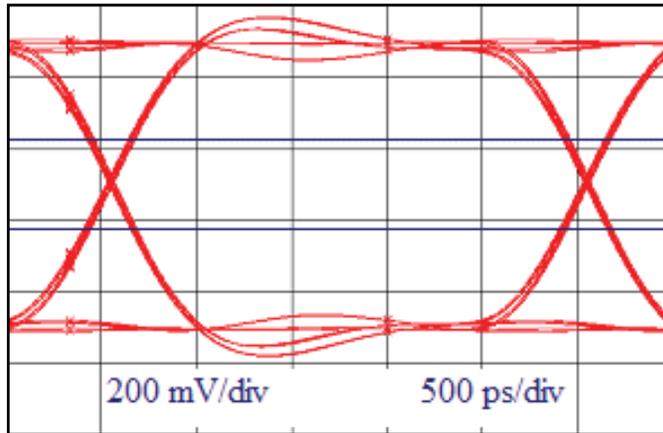
Figure 7: Topologies Compared for SSTL18_I

Case 1 and Case 2 correspond to the Xilinx external and DCI recommended use models, respectively, given in [Ref 3] (see the SSTL18 Class I (1.8V) section). Case 3 is a hybrid consisting of external series termination at the driver combined with DCI parallel termination at the receiver.

Figure 8, Figure 9, and Figure 10 show the eye patterns at the inputs of receivers U2, U4, and U6, respectively. The simulation is configured as follows:

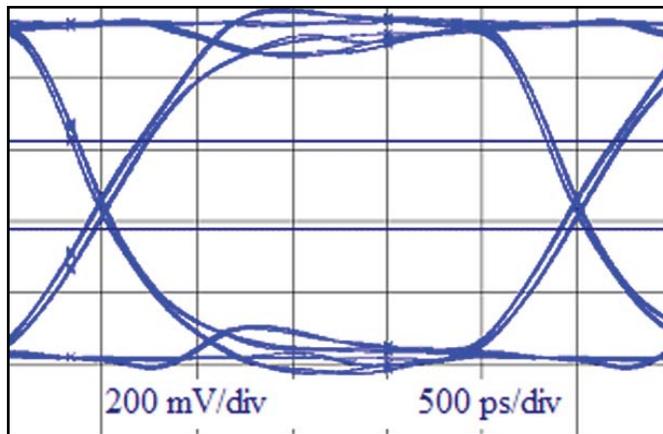
- standard eye, with:
 - ◆ 2^7 PRBS, initially High
 - ◆ 2.5 ns bit period
 - ◆ 1 pattern repetition
 - ◆ first 8 bits (i.e., 20 ns) skipped
 - ◆ 0 added jitter
- slow-weak IC modeling (FF1136 package. This causes HyperLynx to use the worst-case package models.)
- probes located at die

The corresponding metrics are tabulated in Table 1.



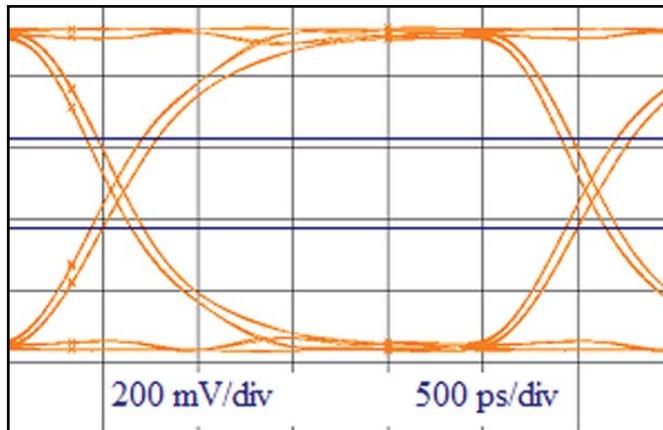
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Figure 8: Eye at U2 - Case 1



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Figure 9: Eye at U4 - Case 2



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Figure 10: Eye at U6 - Case 3

Table 1: Metrics for SSTL18_I Eye Diagrams

Case	Type	Width at Threshold (ns)	Headroom from Ringback (mV)	Overshoot Margin (mV)
1	External	2.20	219	415
2	DCI	2.06	225	373
3	Hybrid	2.10	265	429

The eyes for Case 1 and Case 2 (i.e., the waveforms in [Figure 8](#) and [Figure 9](#)) appear very different than the eye in [Figure 4](#). It was the intent of [Figure 4](#) to show that a Thevenin equivalent termination produces an eye that is identical to that produced by its direct termination counterpart, all other things being equal. There are two main reasons for the difference:

- When using DCI (i.e., Case 2 and [Figure 9](#)), the termination is provided by active devices that are nonlinear and exhibit effective impedances that have a larger tolerance than the typical resistors used for external termination. This larger tolerance results in an impedance mismatch at the ends of the transmission line that is worse than in the externally terminated case and varies with the voltage at the end of the line.
- When the source series termination (i.e., R4 of Case 1 in [Figure 7](#)) is pulled inside the driver IC as in Case 2, the transmission line becomes directly exposed to the parasitic capacitance of the driver output. Thus, any energy reflected from the receiver has to see that capacitance before it passes through the source series termination. Consequently, the high frequency components of that reflected energy are reflected back toward the receiver rather than being damped along with the low frequency components as in Case 1. The removal of the resistive isolation between the transmission line and the parasitic capacitance of the driver output when using DCI at the driver effectively creates a completely unterminated line at high frequencies. This is due to the low impedance exhibited by the parasitic capacitances at both ends of the line at high frequencies.

The total PD is given by [Equation 24](#) for Case 1 and by [Equation 25](#) for Case 2 and Case 3. SSTL18_I/II_DCI inputs use a Thevenin equivalent topology. $P_{\text{STATIC}}(\text{Direct})$, $P_{\text{STATIC}}(\text{Thevenin})$, and P_{DYNAMIC} are given by [Equation 10](#), [Equation 20](#), and [Equation 9](#), respectively. $V_{\text{CCO}} = 1.8\text{V}$, $f = 100\text{ MHz}$ (the address/control lines are SDR and a 50% probability of switching is assumed), and $Z_0 = 50\Omega$ throughout. C is the total capacitance formed by the driver output capacitance (given by C_{COMP} in the IBIS file as 6 pF), the total transmission line capacitance ($\tau/Z_0 = 21.6\text{ pF}$), and the receiver input capacitance (also given by C_{COMP} as 6 pF), and equals 33.6 pF. $V_{\text{DCpp}}(\text{in})$ is inferred from the plots in [Figure 8](#), [Figure 9](#), and [Figure 10](#).

The numbers given in [Table 2](#) and [Table 3](#) for the various SI metrics, the total PD, and the PD breakdown by component can now be used to select the best link topology for any particular application.

Table 2: Power Dissipation for Three Class I Cases

Case	$V_{\text{DCpp}}(\text{in})$ (V)	P_{STATIC} (mW)	P_{DYNAMIC} (mW)	Total Power (mW)
1	0.80	7.2	4.84	12.0
2	0.96	24.8	5.81	30.6
3	0.90	24.3	5.44	29.7

Table 3: Power Dissipation Breakdown by Component

Case	$P_{\text{DRVR_IC}}$ (mW)	$P_{\text{EXT_TERM}}$ (mW)	$P_{\text{RCVR_IC}}$ (mW)
1	5.06	6.98	0
2	9.81	0	20.8
3	5.66	3.78	20.3

Notes:

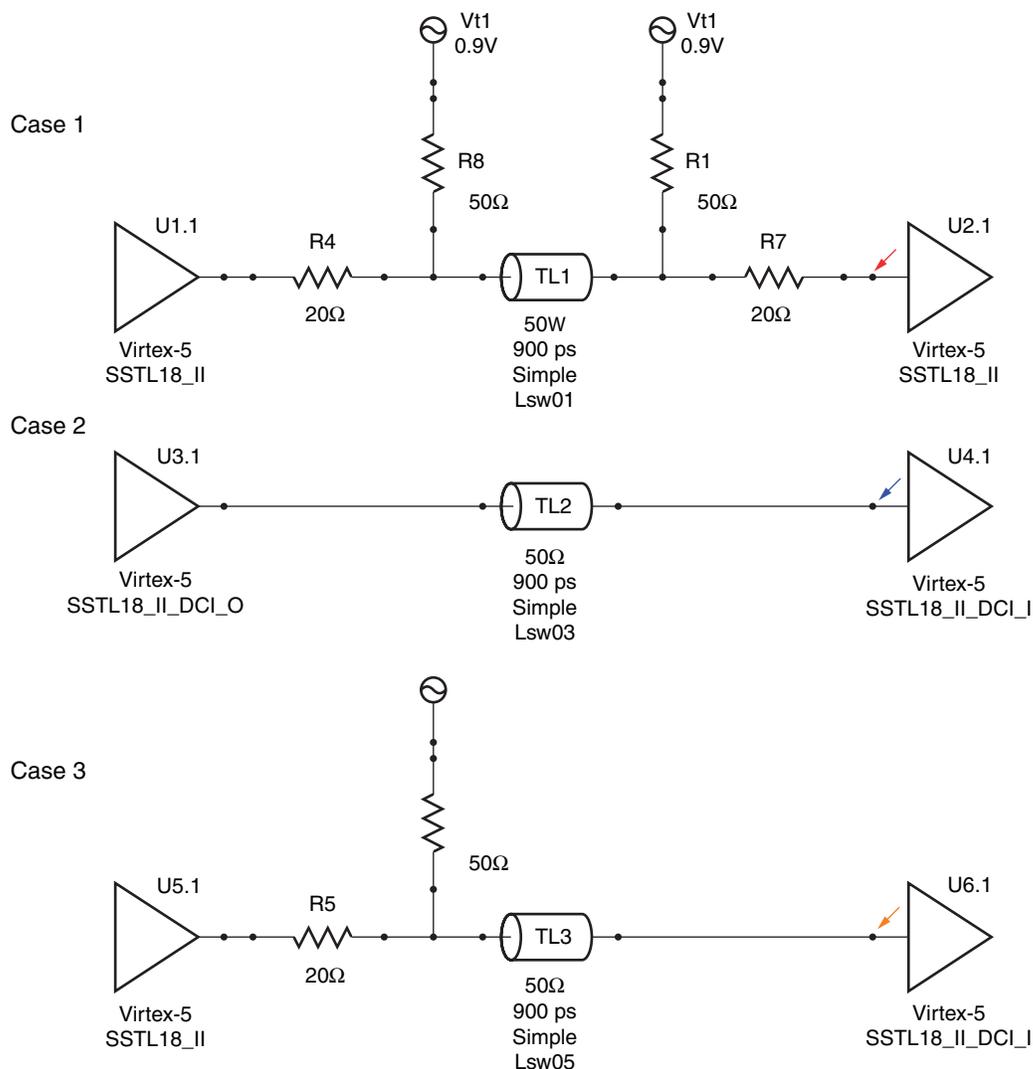
1. Numbers are based on an estimate of 30Ω for non-DCI driver output impedance.

The hybrid model provides an attractive alternative when little room is left to increase driver power dissipation. In the specific example discussed here, when the hybrid model is chosen, the driver power dissipation is increased by only 12% and superior performance in both the Headroom from Ringback and Overshoot Margin SI metrics is gained. Only 5% of the Width at

Threshold is sacrificed compared to the externally terminated case. A 148% penalty in total power dissipation is incurred for the link when using the hybrid model as compared to the externally terminated case, which offers the lowest total power dissipation.

Example 2: SSTL18 Class II

A typical data line of the same DDR2 interface using SSTL18 Class II signaling as well as the SI and PD of several different topologies is considered. Two of these topologies correspond to the Xilinx recommended use models for the external and DCI termination schemes and the third is a hybrid of the previous two (see SSTL18 Class II (1.8V) section in [Ref 3]). The schematic used to run the simulation in HyperLynx is shown in Figure 11.



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Figure 11: Test Case Topologies for SSTL18 Class II

Figure 12, Figure 13, and Figure 14 show the eye patterns at the inputs of receivers U2, U4, and U6, respectively. The simulation configuration is identical to the previous case with the following exceptions:

- 1.25 ns bit period
- first 16 bits (i.e., 20 ns) skipped

The eye metrics are given in Table 4.

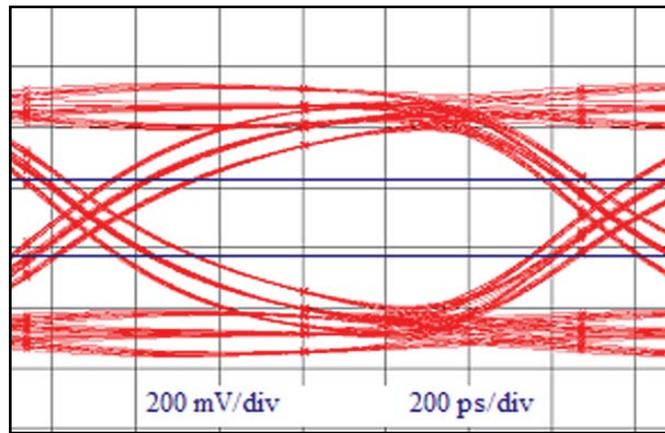


Figure 12: Eye at U2 - Case 1

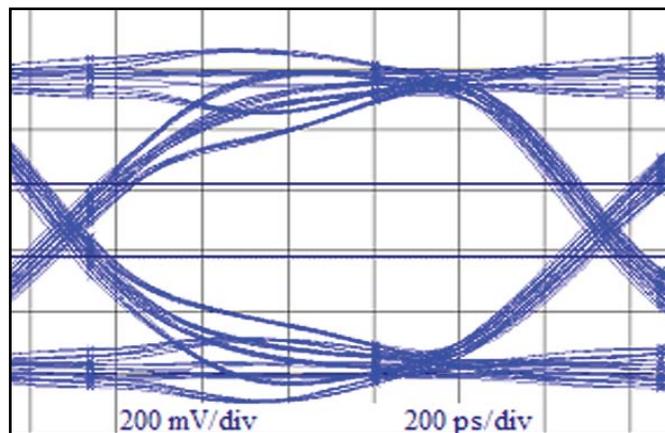


Figure 13: Eye at U4 - Case 2

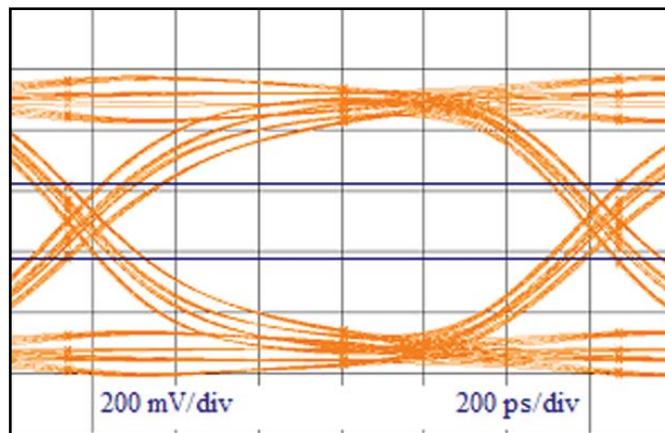


Figure 14: Eye at U6 - Case 3

Table 4: Metrics for SSTL18_II Eye Diagrams

Case	Type	Width at Threshold (ps)	Headroom from Ringback (mV)	Overshoot Margin (mV)
1	External	780	167	434
2	DCI	947	227	300
3	Hybrid	902	195	390

Power dissipation calculations for these three Class II cases are explained here on a case by case basis. In all cases, $f = 200$ MHz since these are data lines (DDR) and toggle at twice the rate of address/control lines. The values of C and V_{CCO} are the same as in the previous case, and the values for $V_{DCpp(in)}$ are inferred from the plots in [Figure 12](#), [Figure 13](#), and [Figure 14](#).

- Case 1 and Case 2 can be handled simply by substituting 25Ω for Z_0 in [Equation 10](#) and [Equation 20](#), respectively. Reducing Z_0 by a factor of two doubles each of the additive terms in [Equation 10](#) and [Equation 20](#), and therefore, simultaneously accounts for the two 50Ω terminations in parallel as well as an extra Thevenin correction factor (i.e., the additive $V_{CCO}^2/4Z_0$ factor in [Equation 20](#)). This correction factor is required because the parallel termination at the driver output is also Thevenin equivalent in the DCI case (Case 2).
- Case 3 requires that 50Ω is used for the first Z_0 in [Equation 20](#) and 25Ω is used for the second. Even though one Thevenin correction is needed, there are still two 50Ω terminations in parallel.

The results are given in [Table 5](#) and [Table 6](#).

Table 5: Power Dissipation for Three Class II Cases

Case	Type	$V_{DCpp(in)}$ (V)	P_{STATIC} (mW)	$P_{DYNAMIC}$ (mW)	Total Power (mW)
1	External	0.74	13.3	8.95	22.3
2	DCI	0.98	45.7	11.9	57.6
3	Hybrid	0.82	29.5	9.92	39.4

Table 6: Power Dissipation Breakdown by Component

Case	Type	P_{DRVR_IC} (mW)	P_{EXT_TERM} (mW)	P_{RCVR_IC} (mW)
1	External	4.21	18.0	0
2	DCI	36.6	0	21.0
3	Hybrid	4.55	15.3	19.6

Notes:

1. Numbers are based on an estimate of 10Ω for non-DCI driver output impedance.

[Table 6](#) shows the trade-off between SI and PD. Moving from the externally terminated case through the hybrid model to the full DCI case, SI gets consistently better while PD increases steadily. Minimal weighting is given to the overshoot margin metric when assessing overall SI quality since there is 300 mV in even the worst case. The hybrid model can be very useful in cases where the improved SI of the DCI model is desired, but little margin is left to increase the driver power dissipation. In fact, the hybrid model also saves appreciably on total power dissipation for the link. The recommended-use models are taken from the generic Virtex-5 user guide ([\[Ref 3\]](#)). A more accurate representation of the current state-of-the-art in Xilinx memory interface design can be found in [\[Ref 4\]](#) and [\[Ref 5\]](#).

Reference Design

The reference design package, including HyperLynx simulation schematics, is available on the Xilinx website at: <http://www.xilinx.com/bvdocs/appnotes/xapp863.zip>.

Conclusion

This application note discusses the general means for quantitatively assessing both the signal integrity and the power dissipation of data transmission lines terminated with two of the most common methodologies in use today: direct and Thevenin equivalent termination. These general techniques are applied to two specific examples that are common to one of the most ubiquitous interface technologies today: DDR2 memory interfaces using SSTL18_I/II signaling standards. The signal integrity and power dissipation of several different candidate topologies

are compared for each example, including cases that make use of DCI. A hybrid approach using external termination at one end of the link and DCI termination at the other often provides the best compromise; however, the decision of which topology to use must be made separately for each design based upon particular design priorities.

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/01/07	1.0	Initial Xilinx release.