XAPP895 (v1.0) February 4, 2014

Adapt Lock Design for 7 Series FPGAs GTX/GTH Transceivers

Author: Jayesh Patil

Summary

This application note describes the Adapt Lock design targeted for the GTX/GTH transceivers in the Xilinx® 7 series FPGAs. This design speeds up the automatic gain control (AGC) convergence in decision feedback equalizer (DFE) mode, and the low and high frequency loop compensation (KL and KH) loop convergence in lower power mode (LPM) by changing the bandwidth while maintaining a dynamic error-free operation on the link. The Adapt Lock design uses the channel dynamic reconfiguration port (DRP) to set AGC, KL, and KH bandwidth values at specific time intervals based on user clock and line rate. The design is integrated into the wizard and the Verilog files can be generated from the tool.

Introduction

In 7 series FPGAs RX physical medium attachment (PMA) DFE mode, the AGC is the ultimate outer loop on top of all other adaptation loops. Consequently, it is the slowest loop. However, the recommended settings for the AGC make the AGC loop convergence increases the settling time. Similarly, in LPM mode, the KL and KH loops are set to the slowest bandwidth. Based on the line rate, adding an Adapt Lock design improves the convergence speed. The Xilinx ISE® Design Suite 14.1 was used to design, compile, and simulate the Adapt Lock design. The design was verified in hardware using ChipScope™ and the integrated logic analyzer (ILA).

Implementation Details

Figure 1 shows the top-level implementation of the Adapt Lock design. It consists of a down shifter, which generates signals at specific count values, a read modify write finite state machine (FSM) that only modifies the bandwidth attributes, and a DRP access module.

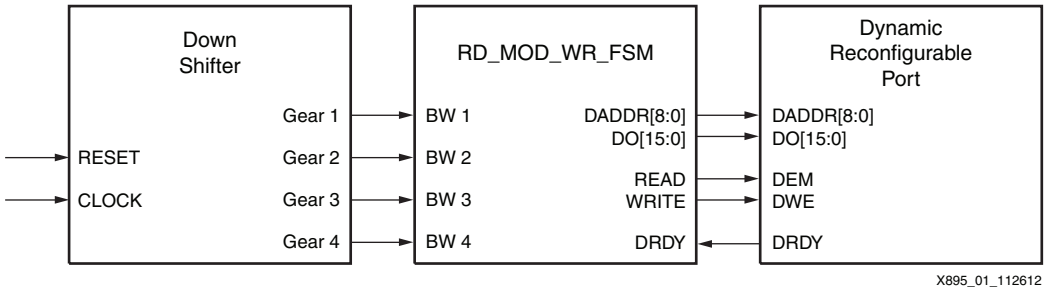

Figure 1: **Adapt Lock Block Diagram**

These blocks are described in the following sections.

© Copyright 2014 Xilinx, Inc. Xilinx, the Xilinx logo, Artix, ISE, Kintex, Spartan, Virtex, Vivado, Zynq, and other designated brands included herein are trademarks of Xilinx in the United States and other countries. All other trademarks are the property of their respective owners.

Down Shifter

The down shifter consists of a 32-bit counter and generates four signals at count values that are based on the user clock, mode of operation (DFE/LPM), and line rate. The count is calculated as shown in Equation 1:

$$\text{Timer} = \text{DCLK Frequency (in MHz)} \times \frac{12.5}{\text{Line Rate in Gb/s}} \qquad \textit{Equation 1}$$

You specify the value based on Equation 1 in the wizard during the initial setup.

RD_MOD_WR_FSM

The finite state machine (FSM) is executed every time the gear signals are asserted by the gear shifter. The gear signals 1 through 4 trigger the FSM to modify the bandwidths starting from the highest setting to the lowest, respectively. The FSM reads the contents from the DRP address of the loop, modifies bandwidth related ports without changing other user specific information, and writes it back to the same address. If there are multiple loops, (for example, LPM, KL, and KH) the same sequence must be executed sequentially for each loop under consideration. The read-modify-write state machine is shown in Figure 2.

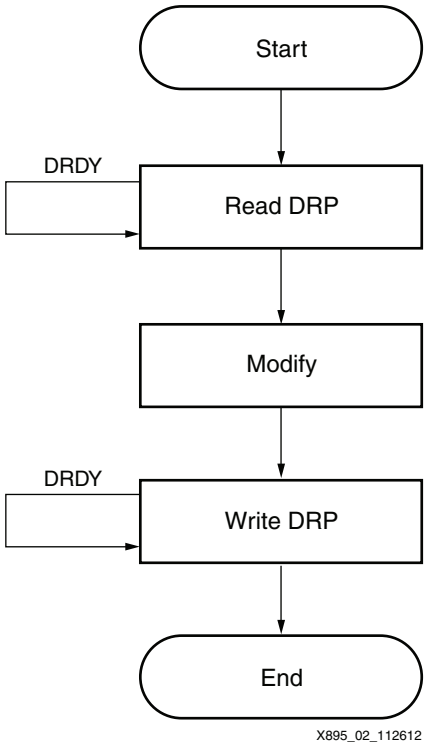

Figure 2: **Read-Modify-Write State Machine for Bandwidth Adjustment**

Start State

In the start state, the state machine asserts the hold signal on KL and KH loops when operating in DFE mode.

Read DRP State

In the read DRP state, the state machine initiates the read sequence for the DRP. It pulses the DEN signal and waits for the DRDY signal from the DRP to be asserted. After the signal is asserted, the contents of the DRP are stored in a local register for modification. The read DRP sequence is outlined in the *7 Series FPGAs Configuration User Guide* (UG472).

Modify DRP State

In the modify DRP state, the contents from the local register are modified to retain the user information and only the bits that control the bandwidth are changed.

Write State

In the write state, the write sequence to the DRP is initiated. It pulses the DWE signal and waits for the DRDY signal from the DRP to be asserted. After the signal is asserted, the contents from the local register are written to the DRP. The write DRP sequence is outlined in the *7 Series FPGAs Configuration User Guide* (UG472).

End State

In the end state, the holds are asserted for the RXAGCHOLD after the AGC loop has converged and for the KL and KH loops. The DFE mode FSM is shown in Figure 3 and the LPM mode FSM is shown in Figure 4.

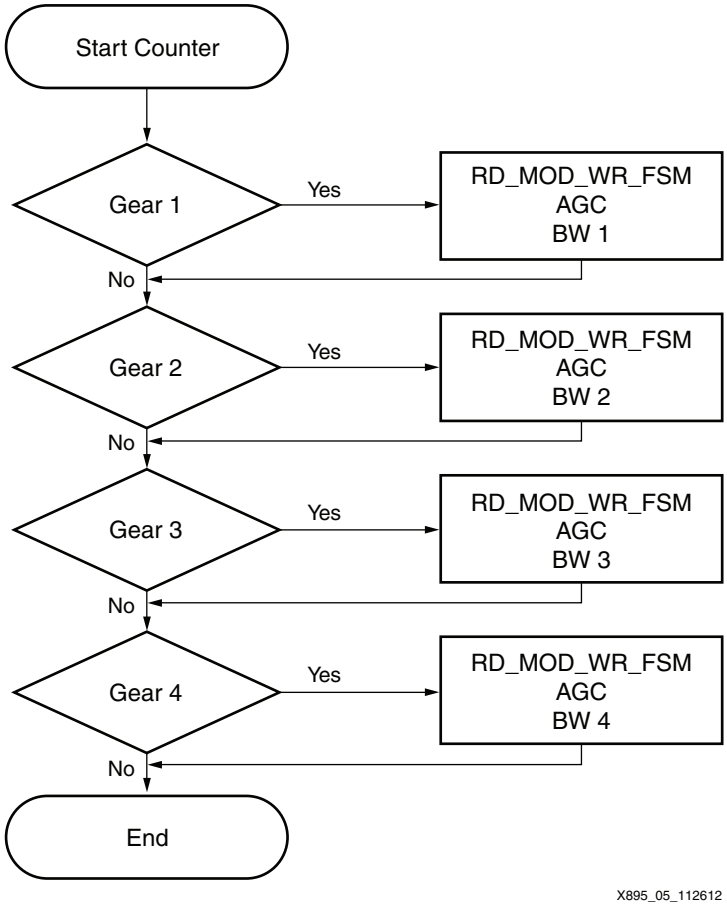

Figure 3: **DFE Mode FSM**

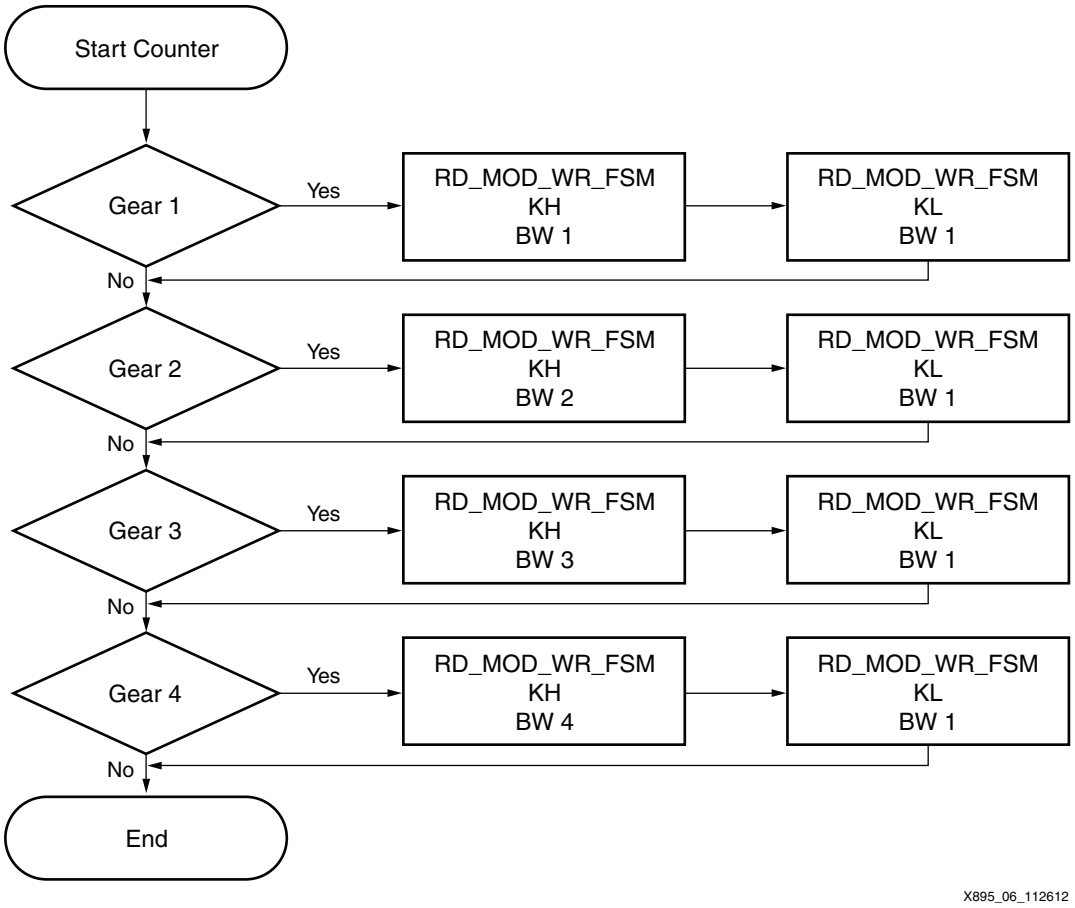

Figure 4: **LPM Mode FSM**

Physical Interface

The design is currently incorporated in the Wizard. The FPGA resources used depends on how many GTX/GTH Quads are used and the chosen mode (LPM/DFE).

Characteristics

The design characteristics are summarized in Table 1.

Table 1: **Design Matrix**

Parameter	Description
General	
Developer name	Jayesh Patil
Target device	7 series devices with GTX/GTH transceivers
Source code provided	Yes
Source code format	Verilog
Simulation	
Functional simulation performed	Yes
Timing simulation performed	Yes
Test bench format	Verilog/ChipScope
Simulator software and version	ISE Design Suite 14.1 or later

Table 1: **Design Matrix *(Cont'd)***

Parameter	Description
SPICE/IBIS simulations	No
Implementation	
Synthesis tool/version	ISE Design Suite 14.1 or later
Implementation tool/version	ISE Design Suite 14.1 or later
Static timing analysis performed	Yes
Hardware Verification	
Hardware verified	Yes
Hardware platform used for verification	VC7203

Conclusion

The design was verified in logic simulations and during lab tests. The design is integrated into the wizard and the Verilog files can be generated from the tool. The logic provides a four times increase from the original time of 2.9 ms at 10G in DFE mode and a two times increase in LPM mode from 10 ms at 10G. Table 2 and Table 3 summarize the results. The first column shows the bandwidth multiplier where 1x is the lowest bandwidth setting and 64x the maximum. N1 represents the number of DRP clock cycles.

Table 2: **DFE Mode—AGC Loop Results**

Speed	Cycles	Time (seconds)
64x	N1 = 100	4.00×10^{-5}
16x	4 x N1 = 400	1.60×10^{-4}
4x	16 x N1 = 1600	6.40×10^{-4}
1x	Infinite	∞

Table 3: **LPM Mode—KL or KH Loop Results**

Speed	Cycles	Time (Sec)
16x	N1 = 4500	1.80×10^{-3}
8x	2 x N1 = 9000	3.60×10^{-3}
4x	3 x N1 = 13500	5.40×10^{-3}
1x	Infinite	∞

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
02/04/2014	1.0	Initial Xilinx release.

Notice of Disclaimer

The information disclosed to you hereunder (the “Materials”) is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx’s limited warranty, please refer to Xilinx’s Terms of Sale which can be viewed at www.xilinx.com/legal.htm#tos; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx’s Terms of Sale which can be viewed at www.xilinx.com/legal.htm#tos.

Automotive Applications Disclaimer

XILINX PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS APPLICATIONS RELATED TO: (I) THE DEPLOYMENT OF AIRBAGS, (II) CONTROL OF A VEHICLE, UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE (WHICH DOES NOT INCLUDE USE OF SOFTWARE IN THE XILINX DEVICE TO IMPLEMENT THE REDUNDANCY) AND A WARNING SIGNAL UPON FAILURE TO THE OPERATOR, OR (III) USES THAT COULD LEAD TO DEATH OR PERSONAL INJURY. CUSTOMER ASSUMES THE SOLE RISK AND LIABILITY OF ANY USE OF XILINX PRODUCTS IN SUCH APPLICATIONS.