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Interfacing Virtex-6 FPGAs with 3.3V I/O Standards

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Introduction

All the devices in the Virtex®-6 family are compatible with and support 3.3V I/O standards. This application note describes methodologies for interfacing Virtex-6 devices to 3.3V systems. It covers input, output, and bidirectional busses, as-well-as signal integrity issues and design guidelines.

The Virtex-6 FPGA I/O is designed for both high performance and flexibility. Each I/O is homogenous, meaning every I/O has all features and all functions. This high-performance I/O allows the broadest flexibility to address a wider range of applications. A range of options can be deployed to interface Virtex-6 FPGA I/O to 3.3V devices.

Interfacing Options

There are different options for interfacing depending on performance needs, function, and signal type (input, output, bi-directional). This application note explores options ranging from no external components, to added resistors, to FET switches, to level translators.

No External Components

Depending on the load capacitance and V_{IH} levels of the 3.3V receivers, Virtex-6 FPGAs can drive most 3.3V logic with no additional components shown in Figure 1. To minimize overshoot/undershoot, one option is to match the FPGA output drive impedance to the characteristic impedance of the transmission line. In Virtex-6 FPGAs, an LVCMOS25 6 mA or 8 mA driver or an LVDCI25 driver with a 50Ω resistor on VRN and VRP is matched to a 50Ω characteristic impedance. With a driver matched to the transmission line, the FPGA drives V_{OH} to V_{CCO} (2.5V) with a 5KΩ load. The V_{IH} threshold for a standard LVCMOS 3.3V type receiver is 2.0V. With a V_{OH} of 2.5V and a V_{IH} of 2.0V, there is a 500 mV margin left for simultaneous switching noise (SSN), reflections from impedance discontinuity, crosstalk, and inter-symbol interference. Increasing V_{CCO} can achieve extra margin, but it also requires a tighter output tolerance on the power regulator. If a regulator is chosen that has a maximum tolerance of ±2% then V_{CCO} can be set to 2.575V. With this tolerance and V_{CCO} setting, the regulator remains below the recommended operating voltage of 2.625V. By increasing V_{CCO} an additional 75 mV of margin is added to the system.

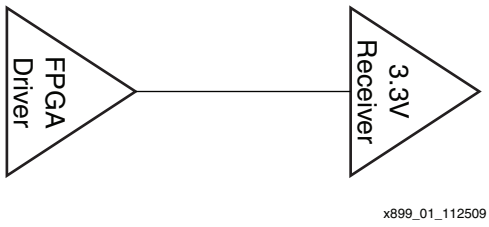

Figure 1: **Example: No External Components Topography**

The charge time of the transmission line is based on the load capacitance of the receiver and the output impedance of the driver. This application note assumes the output impedance matches the transmission line characteristic impedance. If the driver is not matched, use HSPICE or IBIS models to calculate the charge time and overshoot/undershoot.

The charge time is defined in Equation 1.

$$\tau = Z_{DRIVER} \times C_{RECEIVER} \quad \text{Equation 1}$$

After 5τ, the voltage at the receiver reaches 99% of V_{CCO} (2.5V). Using the formula in Equation 1 and assuming the output impedance of the driver is 50Ω and the receiver capacitance is 9 pF, the edge rate at the receiver is 2.25 ns. If these options do not produce enough margin or the input capacitance of the receiver is too large to meet the timing requirements, a different solution is required.

Resistive Pull-Down Divider

A simple resistor load can truncate excessive signal swing to tolerable levels for the FPGA. By placing a resistor from the transmission line to GND, as show in Figure 2, only the driving high-voltage is attenuated. This solution can lead to less than ideal signal integrity because the pull-down resistor is not typically matched to the transmission line. Placing this pull-down resistor close to the receiver helps reduce unwanted reflections.

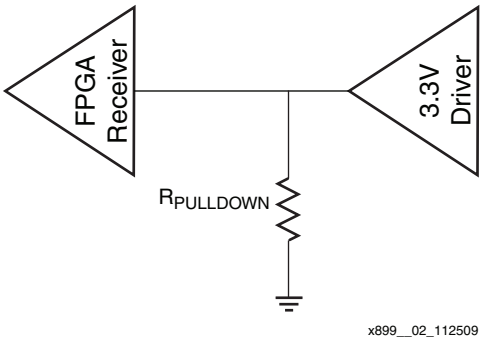

Figure 2: **Example: Pull-Down Resistor Topography**

To calculate the correct pull-down resistor, knowledge of the driver's output impedance is required. To find the driver's output impedance, place a known resistance at the output of the driver. Probe the output of the driver at the resistor node, shown in Figure 3, and measure the DC voltage level while driving a logic 1.

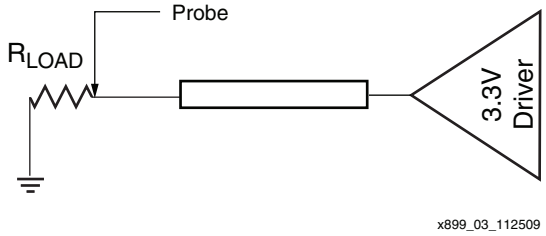

Figure 3: **Example: Probing Circuit Topography**

The driver and load can be described as a voltage divider (Figure 4) where the output impedance is defined by Equation 2.

$$Z_{DRIVER} = R_{LOAD} \times \left(\frac{(V_{CC} - V_{PROBE})}{V_{PROBE}} \right) \quad \text{Equation 2}$$

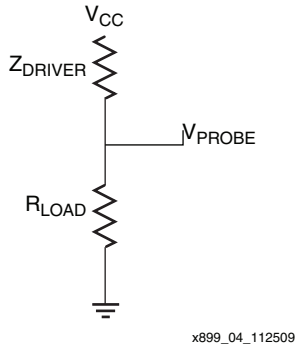

Figure 4: **Schematic of Driver Driving Logic-1 with Probing Load**

After the output impedance of the driver is calculated, the correct pull-down resistor can be calculated using Equation 3. The circuit is shown in Figure 5.

$$R_{PULLDOWN} = \left(\frac{V_{RECEIVER} \times Z_{DRIVER}}{V_{CC} - V_{RECEIVER}}\right) \quad \text{Equation 3}$$

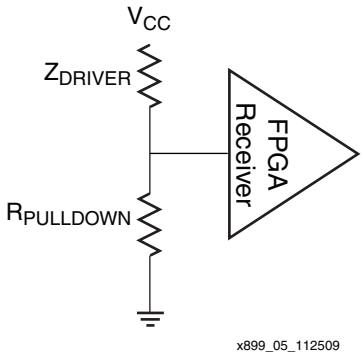

Figure 5: **Schematic of Driver Driving Logic-1 with Pull-Down Resistor**

For example, if $V_{RECIEVER}$ for the FPGA is 2.625V and Z_{DRIVE} is 50Ω, the $R_{PULLDOWN}$ is 194Ω. This method results in a close approximation of the correct pull-down resistor required to limit the line voltage to $V_{RECIEVER}$. There can be discrepancies between the calculated value and the actual value due to the non-linearity in the driver. The best design practice is to simulate with an HSPICE model which will take the non-linearity into account. IBIS models assume accuracy at the simulated termination value.

Totem-Pole Resistive Divider

The two resistor totem-pole solution shown in Figure 6 allows the termination to match the transmission line. This effect minimizes reflections. Although the pull-up and pull-down resistors can be placed anywhere along the transmission line, they need to be grouped to the same location. Minimum reflections occur when the pull-up and pull-down resistors are close to the receiver.

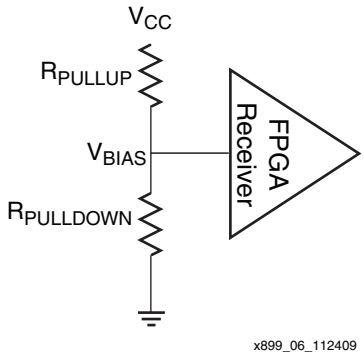

Figure 6: **Example: Totem-Pole Resistor Topography**

Compared to the single pull-down solution, a totem-pole solution requires a DC bias current for each I/O. Assuming the driver's output impedance is balanced between rising and falling edges, the optimal voltage bias is when V_{OH} and V_{OL} have the same amount of margin about V_{IH} and V_{IL} of the receiver. Using the topography in Figure 7, the bias point can be calculated using Equation 4.

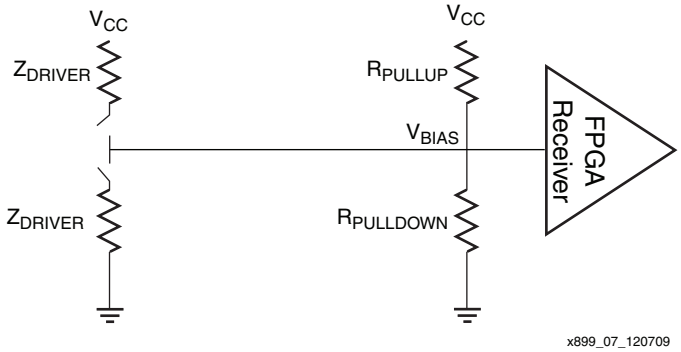

Figure 7: **Schematic of Driver with Thevenin Parallel Termination**

$$V_{BIAS} = \frac{V_{CCDRIVER} \times (V_{IL} - margin)}{V_{CCDRIVER} + (V_{IL} - margin) - (V_{IH} + margin)} \qquad \textit{Equation 4}$$

In this example, assume a 3.3V driver and an LVCMOS25 receiver that has a V_{IH} = 1.7V and the V_{IL} = 0.7V. Presuming 300 mV of margin is needed, a voltage bias of 0.776V is optimal. This bias point enables a symmetrical margin for both logic 1 and logic 0 at the minimum output impedance as shown in Equation 5.

$$\frac{3.3 \times (0.7 - 0.3)}{3.3 + (0.7 - 0.3) - (1.7 + 0.3)} = 0.776 \qquad \textit{Equation 5}$$

After the voltage bias is obtained, the pull-up and pull-down resistor values are determined as shown in Equation 6.

$$R_{PULLUP} = \frac{V_{CC} \times Z_0}{V_{BIAS}} \qquad R_{PULLDOWN} = \frac{Z_0 \times R_{PULLUP}}{R_{PULLUP} - Z_0} \qquad \textit{Equation 6}$$

Where Z_0 is the characteristic impedance of the transmission line.

Continuing the example, the pull-up and pull-down resistor values are calculated, assuming a V_{CC} of 2.5V and a 50Ω transmission line, to be 158Ω and 73Ω, respectively (Equation 7).

$$158 = \frac{2.5 \times 50}{0.776} \qquad 73 = \frac{50 \times 158}{158 - 50} \qquad \text{Equation 7}$$

Using the above topography, the output impedance must be small enough to reach the V_{IH} and V_{IL} thresholds of the receiver. In addition, the output impedance must be large enough not to overdrive the recommended operating voltage (V_{IHMAX}) of the receiver. In Virtex-6 FPGAs the V_{IHMAX} is 2.625V.

$$Z_{DRIVER(MAX)} \leq \left(\frac{(V_{CCDRIVER} - V_{BIAS}) \times Z_0}{(V_{IH} + margin) - V_{BIAS}}\right) - Z_0 \qquad \text{Equation 8}$$

$$Z_{DRIVER(MIN)} \leq \left(\frac{(V_{CCDRIVER} - V_{BIAS}) \times Z_0}{V_{IHMAX} - V_{BIAS}}\right) - Z_0 \qquad \text{Equation 9}$$

In this example, the maximum driver impedance is 53Ω and the minimum drive impedance is 18Ω.

$$Z_{DRIVER(MAX)} \leq \left(\frac{(3.3 - 0.776) \times 50}{(1.7 + 0.3) - 0.776}\right) - 50 = 53\Omega \qquad \text{Equation 10}$$

$$Z_{DRIVER(MIN)} \leq \left(\frac{(3.3 - 0.776) \times 50}{2.625 - 0.776}\right) - 50 = 18\Omega \qquad \text{Equation 11}$$

At 53Ω, there is exactly 300 mV of margin for logic1 and logic 0. As the output impedance is reduced, the logic 1 margin grows faster then the logic 0 margin. Use Equation 12 and Equation 13 to calculate the exact margin for each logic state.

$$\text{Logic 1 Margin} = \frac{(V_{CCDRIVER} - V_{BIAS}) \times Z_0}{Z_0 + Z_{DRIVER}} + V_{BIAS} - V_{IH} \qquad \text{Equation 12}$$

$$\text{Logic 0 Margin} = V_{IL} + \frac{V_{BIAS} \times Z_0}{Z_0 + Z_{DRIVER}} - V_{BIAS} \qquad \text{Equation 13}$$

Where Z_{DRIVER} is the output impedance of the driver.

Continuing the example and assuming the output impedance of the driver is 53Ω, the logic margins are calculated in Equation 14 and Equation 15.

$$\text{Logic 1 Margin} = \frac{(3.3 - 0.776) \times 50}{50 + 53} + 0.776 - 1.7 = 0.301 \text{ mV} \qquad \text{Equation 14}$$

$$\text{Logic 0 Margin} = 0.7 + \frac{0.776 \times 50}{50 + 53} - 0.776 = 300 \text{ mV} \qquad \text{Equation 15}$$

The bias power consumed per I/O from the totem pole termination is calculated using Equation 16.

$$Power = \frac{V_{CC}^2}{R_{PULLDOWN} + R_{PULLUP}} \qquad \text{Equation 16}$$

The bias power is calculated to be 27 mW per I/O.

$$Power = \frac{2.5^2}{73 + 158} = 27\text{mW} \qquad \text{Equation 17}$$

By using a parallel termination to V_{BIAS}, the same performance can be achieved with no DC bias at the cost of an additional power rail shown in (Figure 8). If the application has a large number of inputs, this solution could be a more power-efficient option.

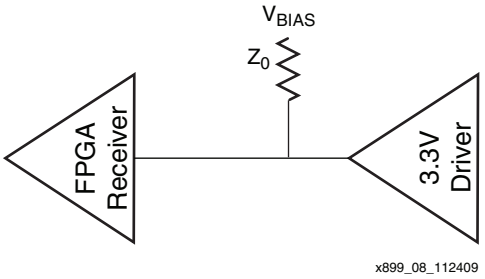

Figure 8: **Example: Parallel Termination to V_{BIAS} Topology**

Series FET Switch

The field-effect transistor (FET) bus switch (Figure 9) is a guaranteed drop-in unidirectional solution. With simulation and minor adjusting, it can work in a bidirectional case as well. The FET bus switch is used to isolate the 3.3V logic from the 2.5V FPGA. This device performs like a NMOS transistor in series with the transmission line. As shown in Figure 10, the source is connected to the FPGA, the drain connected to the 3.3V logic, and the gate is connected to a supply voltage.

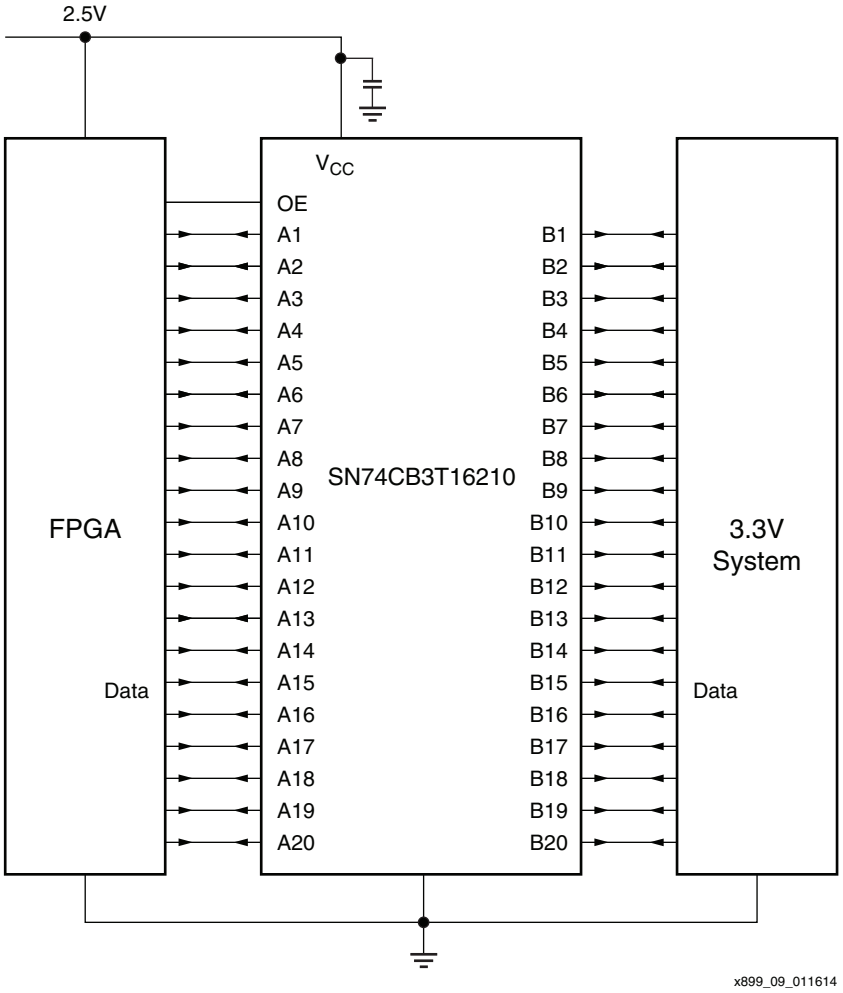

Figure 9: **FET Switch Topography**

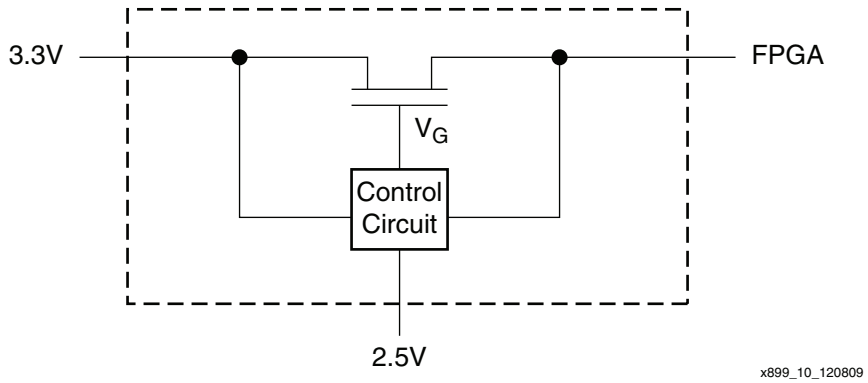

Figure 10: **Simplified Schematic of FET Switch**

When the transistor is in the liner region, $V_{GS} > V_{TH}$ and $V_{DS} < (V_{GS} – V_{TH})$, the signal is allowed to propagate through the device. V_{TH} is the threshold voltage of transistor. Once $V_{GS} < V_{TH}$ the transistor is in cutoff and prevents the FPGA I/O pins from excessive voltage. In the SN74CB3T16210, a charge pump sets the gate voltage to $V_{CC} + V_{TH}$. This causes the signals passing through the device to be truncated to V_{CC} as shown in Figure 11. If the signal is below V_{CC}, it passes through the device.

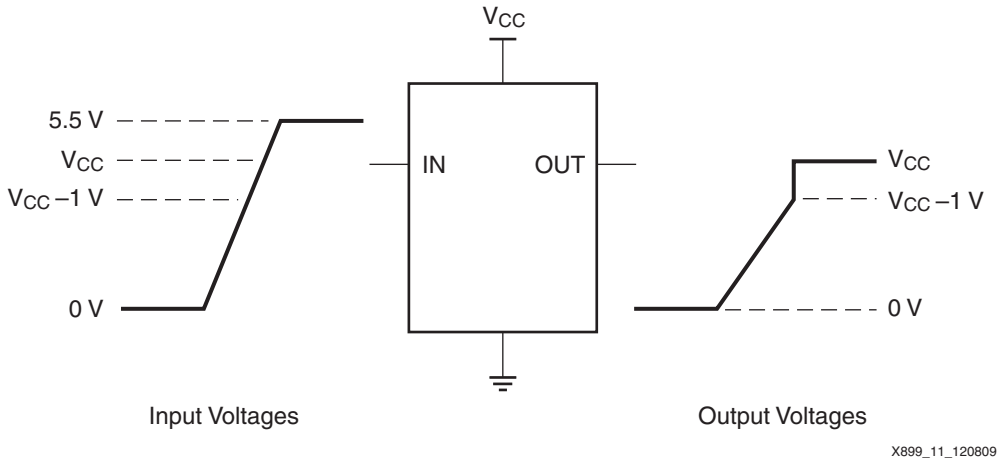

Figure 11: **Schematic and Operation of SN74CB3T16210**

Bidirectional Interface with an FET Switch

When building a bidirectional interface, simulation and measurement against two metrics, timing margin and voltage margin, need to be verified at each receiver. A good start is matching the driver's output impedance to the characteristic impedance of the transmission line. This process minimizes the amount of overshoot/undershoot. With a driver matched to the transmission line, the FPGA drives V_{OH} to V_{CCO} (2.5V) with a 5KΩ load. Since the V_{IH} threshold of an LVCMOS 3.3V receiver is 2.0V, The $V_{OH} – V_{IH}$ equation leaves 500 mV of voltage margin left for SSN, reflections from impedance discontinuity, crosstalk and inter-symbol interference. In Virtex-6 FPGAs, an LVCMOS25 6 mA or 8 mA driver or an LVDCI25 driver with a 50Ω resistor on VRN and VRP is matched to a 50Ω characteristic impedance. Increasing V_{CCO} can achieve extra margin, but requires tighter output tolerance on the power regulator. If a regulator is chosen that has a maximum tolerance of ±2%, then V_{CCO} can be set to 2.575V. With this ±2% tolerance and V_{CCO} setting, the regulator remains below the recommended operating voltage of 2.625V. This increase in V_{CCO} voltage adds an additional 75 mV of margin to the system. After using the previous two techniques, if enough margin has not been produced, use a pull-up resistor on the 3.3V receiver side to help increase margin (as shown in Figure 12).

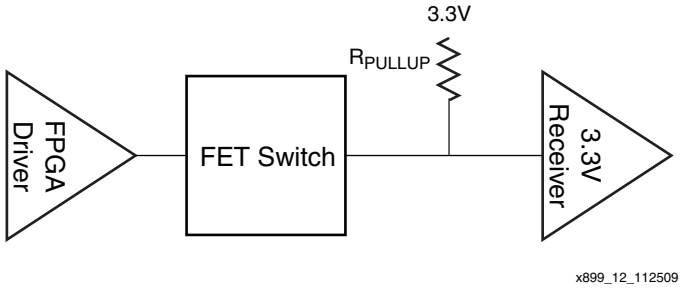

Figure 12: **FET Switch with Pull-Up Topography**

The weaker the pull-up resistor, the longer the time to charge the 3.3V side of the transmission line. While the margin on a driven logic 1 increases due to the pull-up resistor, it will adversely affect the margin on a driven logic 0. A pull-up resistor needs to be large enough to meet the logic 0 requirements and small enough to meet the voltage and timing margin on the logic 1. The speed that the line charges, using the topography shown in Figure 13, is calculated in Equation 18. τ is 63% of $V_{CC} - V_{OH}$ of the FPGA (2.5V).

$$\tau = R_{PULLUP} \times (C_{FET} + C_{LOAD}) \qquad \text{Equation 18}$$

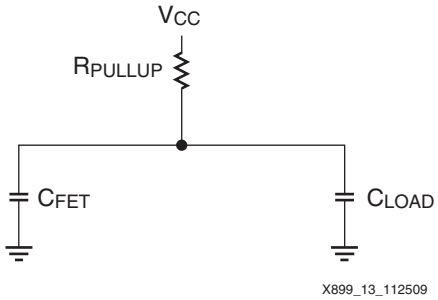

Figure 13: **Schematic Representation of the 3.3V Side of the FET**

This example uses a 360Ω pull-up resistor, 3.3V V_{CC}, 4.47 pF C_{FET}, and a 4 pF load. An additional 500 mV of voltage margin is obtained in 3.05 ns. After the pull-up resistor is defined, the driver impedance needs to be calculated to meet the V_{IL} requirements of the I/O standard. The topography in Figure 14 and Equation 19 calculates the driver output impedance.

$$Z_{DRIVER} = \frac{(V_{IL} - margin) \times R_{PULLUP}}{V_{CC} - (V_{IL} - margin)} \qquad \text{Equation 19}$$

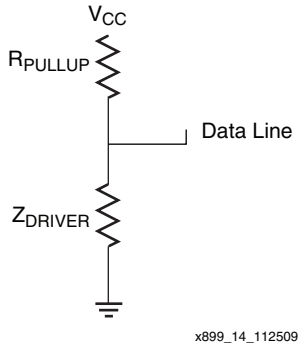

Figure 14: **Schematic of Driver Driving Logic 0 with Pull-Up Resistor**

Using the previous case, to meet the V_{IL} (800 mV) requirement with 400 mV of margin, both drivers' output impedance are required to be 50Ω or less. Equation 18 through Equation 19 give a starting point for simulation. The pull-up resistor can have adverse effects on margin depending on its location in the transmission line. The closer the termination can be placed to the FET switch typically helps reduce reflections.

Automatic Level Translator

The TXB0108 block diagram in Figure 15 is an automatic direction sensing level translator. The ability to automatically sense the direction of traffic makes an automatic level translator easy to drop into a bidirectional system. There are no additional control signals as each bit has an independent directional sensor. Several independent/asynchronous signals interfaced to a 3.3V logic system can all be routed through the same device. This device adds up to 5.6 ns of propagation delay to the circuit. The TXB0108 in a DC state drives a weak pull-up/pull-down to maintain the logic state. The device is capable of being over-driven by external logic when bus directions change. When the device detects a transition, the appropriate PMOS/NMOS is turned on to increase edge rate. The driver then turns off and the logic level is maintained by a weak pull-up/pull-down. If a termination or other heavy loading is present on the line, the weak pull-up/pull-down could cause logic faults. Termination resistors and bus loads must be larger then 50kΩ to avoided logic level interruption. If the bus load is less then 50kΩ, then the weak pull-up/pull-down is not able to maintain the logic state. For these reasons, open drain busses such as I2C and 1Wire are not compatible with this type of level translator.

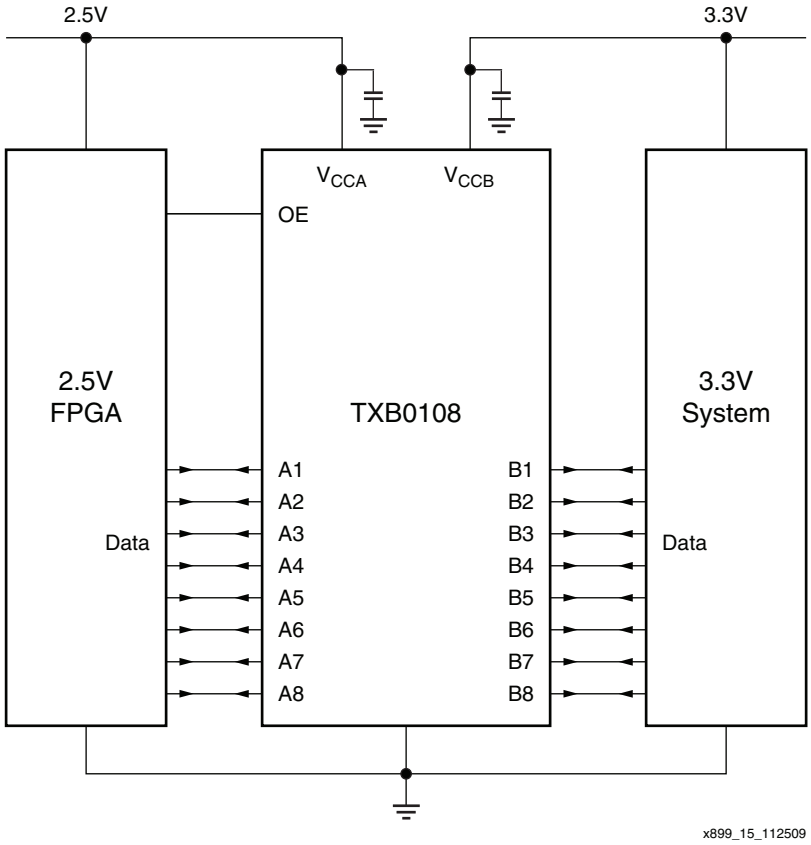

Figure 15: **Automatic Level Translator Topography**

CPLDs and Spartan FPGAs

A variety of Xilinx devices are 3.3V tolerant and can be fitted for bidirectional level-shifting applications. CPLDs are available with up to 117 I/O to support up to a 58-bit bus. Spartan devices are available with up to 530 I/O. Both devices have a few advantages over traditional level shifters. Programmable logic can also off-load tasks previously dedicated to the Virtex-6 FPGA. While still requiring control signals to identify direction, the CPLD or Spartan devices (compared to a dedicated directional level shifter), can be programmed to support any number of traffic to control signal ratios. A pin-to-pin propagation delay of 5 ns exists through the CPLD devices while the pin-to-pin propagation delay is dependent on routing within the Spartan device.

Inside a CPLD or Spartan device, an IOBUF is instantiated on the Virtex-6 FPGA side as well as the 3.3V logic for each port on the bus shown in Figure 16. A signal is brought into the device from either the FPGA or the 3.3V logic to identify the direction (DIR) of traffic.

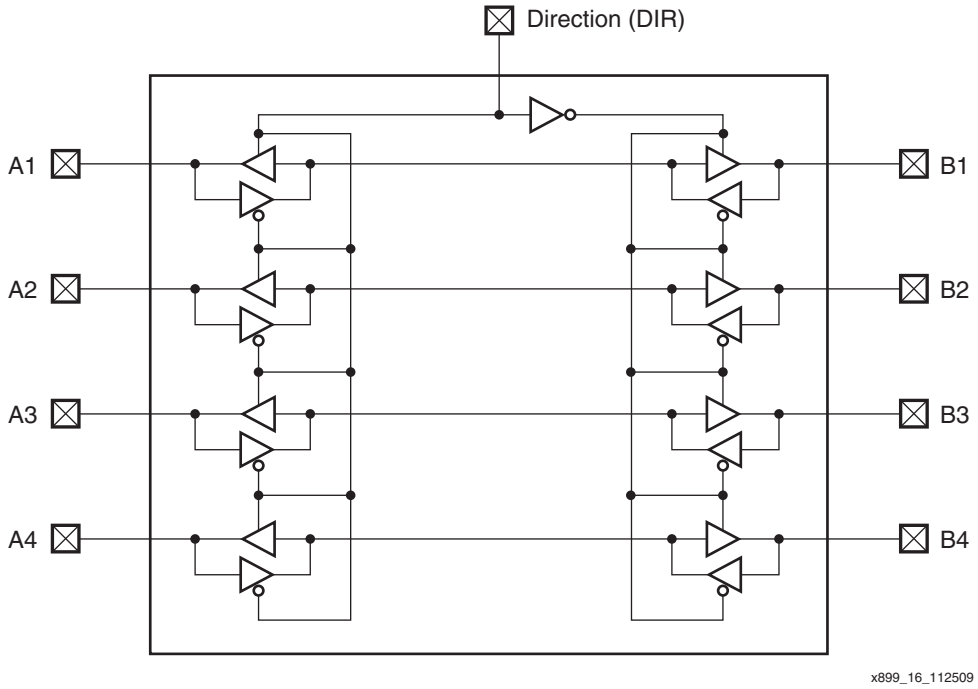

Figure 16: **Example Schematic of CPLD or FPGA Design**

Directional Level Translator

The SN74AVC20T245 is a 20-bit bidirectional level translator that level-shifts data from A to B or B to A (Figure 17) depending on the logic of DIR. Logic is required to generate a DIR signal to control the direction of the bus. This signal can be generated from the FPGA or from external 3.3V logic.

The SN74AVC20T245 is broken into two 10-bit busses, each with independent controls. All signals into the 10-bit block must share direction in accordance with the DIR signal (Figure 18). There is also an output enable for each block that isolates port A from B. A pin-to-pin propagation delay of 3.4 ns exists through the device.

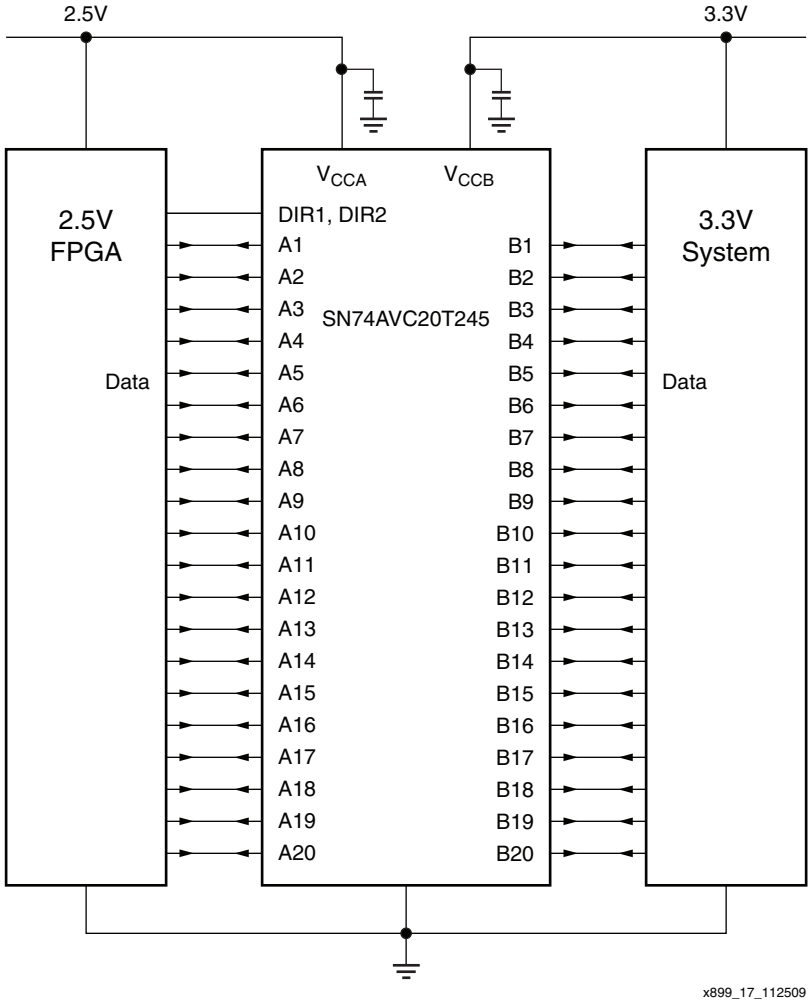

Figure 17: **20-bit Bidirectional Level Translator Topography**

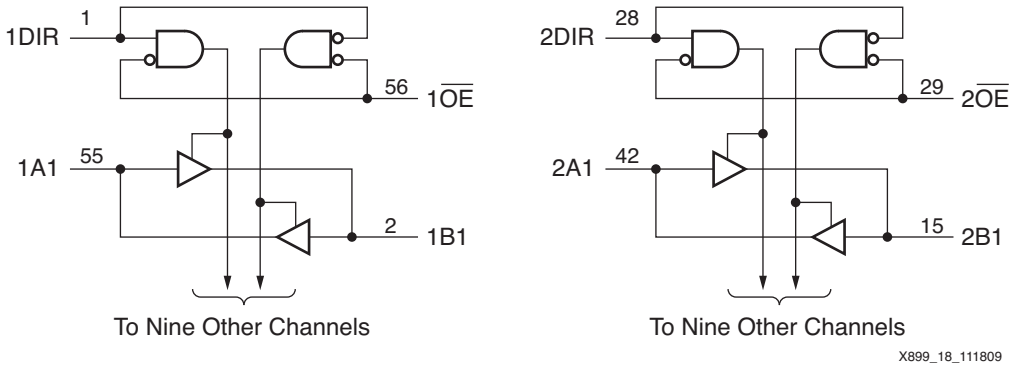

Figure 18: **Schematic of Level Translator**

Design Guidelines

Table 1 compares solutions for interfacing 3.3V systems to Virtex-6 FPGAs. There are many approaches with several metrics of interest when choosing the right solution.

Table 1: **Comparison of Design Guidelines**

Type	External Part Numbers	Bit Width	Bi-directional	Input	Output	Bus Must Be Aligned to Directional Signal (DIR)	Supports Open Drain Drivers	Supports Termination	Number of Components	Propagation Delay
No External Components	N/A	N/A	No	No	Yes(5)	No	N/A	No(1)	0	N/A
Resistive Pull-Down Divider	N/A	N/A	No	Yes	No	No	Yes	Yes	1	N/A
Totem-Pole Resistive Divider	N/A	N/A	No	Yes	No	No	Yes	Yes	2	N/A
Series FET Switch	SN74CB3T16210	20	Yes(2)	Yes	Yes(2)	No	Yes	Yes	1(4)	0.25 ns
Automatic Level Translator	TXB0108	8	Yes	Yes	Yes	No	No	No	1	5 ns
CPLDs and Spartan FPGAs	XC9536XL	16(3)	Yes	Yes	Yes	Yes(3)	Yes	Yes	1	5 ns
Directional Level Translator	SN74AVC20T245	20	Yes	Yes	Yes	Yes	Yes	Yes	1	3.4 ns

Notes:

1. Terminations can be used but reduce margin.
2. Has capability of bidirectional support, 500 mV of margin exists with a 5 KΩ load.
3. Bit widths are dependent on device size
4. Two component can be required if a pull-up resistor is need for additional margin.
5. 500 mV of margin exists with a 5 KΩ load.

Conclusion

Virtex-6 devices are compatible with and support 3.3V I/O standards. Device reliability and proper interface operation are ensured by following the design guidelines found in this application note. The DC and AC input voltage specification must be met when designing interfaces with the Virtex-6 devices.

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
01/05/2010	1.0	Initial Xilinx release.
02/05/2014	1.1	Updated the FET switch in Figure 9 to remove the 3.3V supply, which changed V_{CCA} to V_{CC}.

DISCLAIMER