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Reference System: OPB Ethernet MAC

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Abstract

This application note describes a reference system illustrating how to build an embedded MicroBlaze™ system using the On-Chip Peripheral Bus Ethernet Media Access Controller (OPB EMAC) processor IP core. This reference system has all the main performance enhancing features of OPB EMAC enabled. Features such as Scatter/Gather DMA, hardware data realignment engine (DRE), and checksum offloading (CSO) are all enabled. This reference system also includes a self-test application that can be used to verify the functionality of the OPB EMAC core. This application includes register accesses, verifying DMA capabilities, and transmitting/receiving packets in loopback mode. This reference system is targeted for the Memec Spartan™-3 Development Board.

Included Systems

Included with this application note is one reference system:

- www.xilinx.com/bvdocs/appnotes/xapp942.zip

Introduction

Using Ethernet Media Access Controllers in embedded microprocessor systems is becoming increasingly prevalent. Xilinx has a variety of different Ethernet solutions available to be used in embedded applications as peripherals to both the Processor Local Bus (PLB) and On-Chip Peripheral Bus (OPB). The OPB EMAC solution is the main solution for any Spartan-based or MicroBlaze-based designs as it attaches to the OPB. Xilinx also provides a lite version of this core; however, the OPB EMAC Lite core does not provide any performance enhancing features.

The OPB EMAC core is fully compliant with the Media Independent Interface (MII) specification to PHYs and allows a link speed of 10 or 100 Mbps. It has variable size FIFOs that can be independently controlled for both the transmit (TX) and receive (RX) sides. Additionally, it supports Jumbo frames, Scatter/Gather Direct Memory Access (SGDMA), has RX and TX hardware Data Realignment Engine (DRE) and Checksum Offloading (CSO) to allow for low processor and bus utilization, and high Ethernet throughput.

The reference system described in this application note is optimized for Ethernet performance and targeted for the Memec Spartan-3 Development board.

Hardware and Software Requirements

The hardware and software requirements are:

- Xilinx Memec S3 Development Board
- Xilinx Platform USB Cable or Parallel IV Cable
- RS232 Cable
- Serial Communications Utility Program (e.g. HyperTerminal)
- Xilinx Platform Studio 8.2.01i
- ISE 8.2.02i

Reference System Specifics

The reference system delivered with this application note, memec_s3_mb_opb_ethernet, contains only the IP cores necessary to provide an example of how to set up OPB EMAC and how to verify the functionality of this core. In addition to the MicroBlaze processor and OPB EMAC, this system includes Multichannel OPB DDR and LMB Block RAM memory controllers, an OPB UART Lite, and an OPB interrupt controller. The OPB EMAC PHY interface signals are connected to the MII PHY on the Memec S3 Development board.

The MicroBlaze processor and the OPB are both running at 66.67 MHz which is sufficient for the OPB EMAC to operate in 100 Mbps mode. If the OPB frequency falls below 65 MHz, OPB EMAC can only support 10 Mbps mode.

See Figure 1 for the block diagram and Table 1 for the address map of this system.

Block Diagram

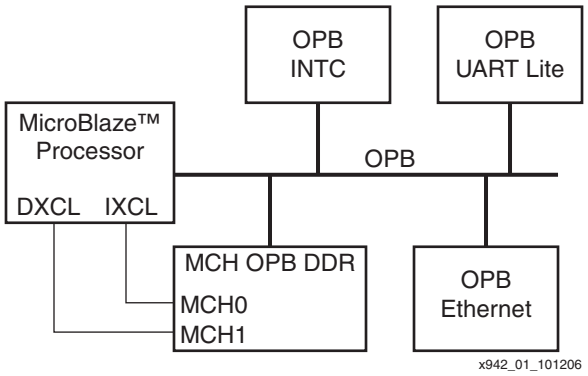

Figure 1: **OPB Ethernet MAC Reference System Block Diagram**

Address Map

Table 1: **Reference System Address Map**

Peripheral	Instance	Base Address	High Address
MCH_OPB_DDR	DDR_SDRAM_16Mx16	0x22000000	0x23FFFFFF
OPB_UARTLite	RS232	0x40600000	0x4060FFFF
OPB_INTC	opb_intc_0	0x41200000	0x4120FFFF
OPB EMAC	Ethernet_MAC	0x40C00000	0x40c0FFFF
LMB_BRAM	lmb_bram_if_cntrl	0x00000000	0x00001FFF

Configuring the OPB EMAC Core

The memec_s3_mb_opb_ethernet reference system has the OPB EMAC configured to use Scatter/Gather DMA by setting `DMA Present` to `Scatter Gather DMA`. DRE is turned on for both TX and RX channels by setting `DRE of Tx Side` and `DRE of RX Side` to `1`. `Support Jumbo Sized Frames` is turned on to allow frame sizes larger than 1500 bytes. Support for hardware checksum calculation is provided on TX and RX channels by setting `Enable CSUM of TX Side` and `Enable CSUM of TX Side`. Also, `Support DMA Interrupt Coalesce` function is enabled so that multiple interrupt events can be queued up in order to reduce processor overhead due to servicing too many interrupts.

Figure 2 shows a complete setting of the OPB EMAC parameters in the memec_s3_mb_opb_ethernet reference system.

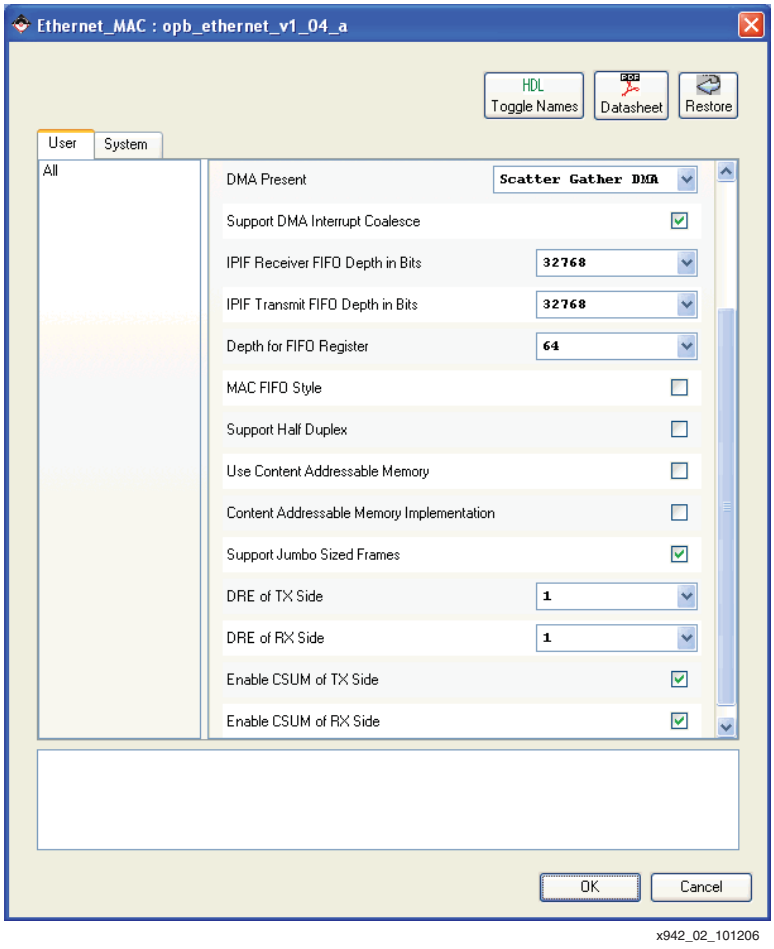

Figure 2: **OPB EMAC Parameters**

Software Application

The software application for this reference system runs the self-test application for the OPB EMAC core. These tests are also available in the software area of the EDK installation directory as standalone tests, however, this reference system has combined all of them and slightly modified them to target the MicroBlaze processor, rather than the PowerPC processor that was originally targeted. Specifically, this combined test exercises the OPB EMAC core in polled, FIFO driven interrupt, and SGDMA driven interrupt modes. This test is run in internal loopback mode that can be turned on or off by writing to the internal loopback enable bit location in the EMAC control register. If the internal loopback is disabled, the test will fail.

Executing the Reference System

To execute this reference system, the Memec S3 Development board must be set up correctly, and the bitstreams must have been updated and be ready for download. Pre-built bitstreams that have been verified to work properly are also available in the `ready_for_download/` directory under the project root directory. This directory contains the hardware bitstream and `executable.elf` for the selftest application. A HyperTerminal (or any other serial communications utility) must be connected to the COM port that is connected to the UART terminal on the Memec S3 Development board. The terminal settings must have the baud rate set to **9600** and data bits to **8**.

See Figure 3 for the HyperTerminal settings. The UART terminal is used to capture the results of the tests.

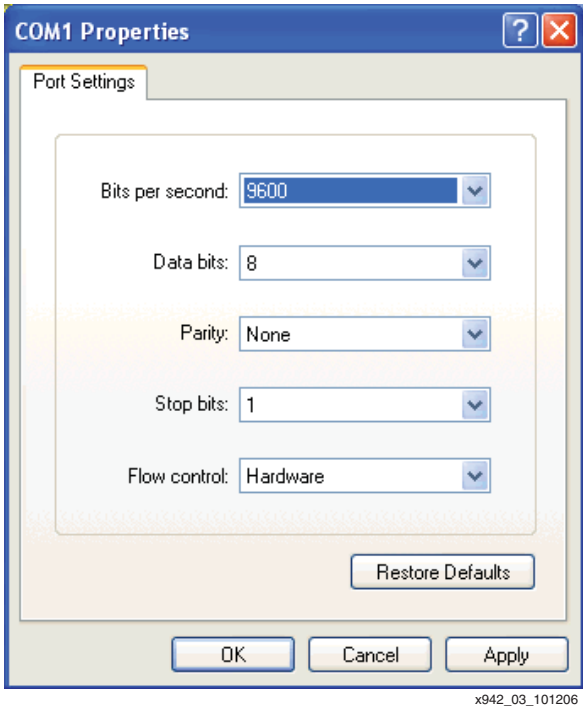

Figure 3: **HyperTerminal Settings**

Executing the Reference System using the Pre-Built Bitstream and the Compiled Software Applications

To execute the system using files inside the `ready_for_download/` in the project root directory, follow these steps:

1. Change directories to the `ready_for_download` directory.
2. Use iMPACT to download the bitstream by using the following:

   ```
   impact -batch xapp942.cmd
   ```

3. Invoke XMD and connect to the MicroBlaze processor by the following command:

   ```
   xmd -opt xapp942.opt
   ```

4. Download the executables by the following command:

   ```
   dow executable.elf
   ```

Executing the Reference System from EDK

To execute the system using EDK, follow these steps:

1. Open `system.xmp` inside EDK.
2. Use **Hardware→Generate Bitstream** to generate a bitstream for the system.
3. Download the bitstream to the board with **Device Configuration→Download Bitstream**.
4. Launch XMD with **Debug→Launch XMD...**
5. Download the executables by the following command:

   ```
   dow executable.elf
   ```

Running the Software Applications

To run the software application, use the ***run*** command inside XMD. The status of the software application is displayed in the HyperTerminal data screen. The expected output for the selftest application is following:

```
-- Entering main() --

Starting XemacFifoIntrExample
Successfully finished XemacFifoIntrExample

Starting XemacPolledExample
Successfully finished XemacPolledExample

Starting XemacSgDmaIntrExample
Successfully finished XemacSgDmaIntrExample

-- Exiting main() --
```

If the tests produce no output, make sure that the UART connection is established properly and that there were no errors while building the project or downloading the hardware and software bitstreams.

References

OPB EMAC Product Specification, Xilinx DS435

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/20/06	1.0	Initial Xilinx release.