Optimizing a system for cost requires analysis of every silicon device on the board, particularly the ‘high value’ components, whether they are ASSPs, ASICs, FPGAs, or SoCs. A versatile silicon technology is always attractive, but to be truly cost optimized, a system architect wants just the right feature set—nothing that's above and beyond what is needed nor anything that falls short of meeting requirements. For example, an I/O expansion device is not likely to need high DSP ratios for heavy signal processing workloads, and it may not need to bear the cost of high-performance transceivers.

Xilinx’s Cost-Optimized Portfolio of All Programmable FPGAs and SoCs offers software and hardware flexibility and scalability unique in the industry. Comprised of recently enhanced Spartan®, Artix®, and Zynq® families, the portfolio is diversified for I/O connectivity, high-bandwidth workloads, and intelligent analytics.

To be used for part or all of the system, the families range in capability and integration, each with a unique feature set, resource mix, and price point—because there can’t be a “catch all” device family for every use model. At the same time, scalability is key because designers want the option to add capability and feature sets—whether for a current or next-generation platform. Specifically, designers may want to:

1. Customize a portfolio of similar end products, e.g., streamlined, mid-range, or high-end variants
2. Future-proof their systems for changing requirements or evolving standards
3. Develop different product lines that share common IP, architectural blocks, or design flows

With Xilinx silicon, software, and methodology, the designer has these options.
Scalability for Industrial IoT and Embedded Vision

The Cost-Optimized Portfolio is well suited for a breadth of markets, but industrial IoT, in particular, shows the versatility of the portfolio as a scalable platform.

Because the industrial automation market is rapidly moving from centralized control to ‘edge compute,’ industrial IoT endpoint systems are often tasked with multi-sensor data acquisition for real-time control and downstream analytics. For end applications ranging from machine vision camera to vision-guided robotics, the portfolio excels in workloads ranging from ‘any-to-any’ connectivity, sensor fusion, precision control, image processing, system-wide safety and security, analytics and cloud connectivity. See Figure 1.

Device Families: From ‘Low-Cost’ FPGAs to ‘Low-Cost’ SoCs

Whether used as an interface bridge on a server line card or placed at the heart of an industrial connected control unit, the portfolio’s diverse resource mix makes it attractive for meeting immediate product requirements and enabling longer term development strategies.
**Spartan-6 FPGAs – Now with Windows 10 OS Support**

The Spartan-6 FPGA family is I/O optimized for connectivity and is the well-established, low-cost market leader. With 25+ design kits and evaluation boards, the entire family is in volume production for immediate implementation, with over 80 million units shipped. Because it is biased towards raw connectivity, the family has best-in-class I/O and form factor related features, including:

- Highest I/O to logic cell ratio
- Most total package offerings
- Smallest form-factor offerings
- Support for 40+ protocols

This makes it an ideal bridging and companion chip solution. Based on Samsung’s 45nm low power (LP) process, it can also be a cost-effective algorithm engine, e.g., for video or motor control, with a competitive performance/watt profile.

Now, new Windows 10 and CentOS Linux OS support is available on Spartan-6 FPGA design tools (ISE® Design Suite) so designers can benefit from modern design environments and OSs for new design starts.

**The New Spartan-7 FPGA Family – 2.5X Performance/Watt**

The new Spartan-7 FPGA family has the best performance/watt profile in an I/O optimized device—2.5X that of Spartan-6 FPGAs. Based on the 28nm production-proven 7 series FPGA fabric, it is the lowest cost entry point into Xilinx’s 7 series FPGAs, offering:

- Spartan-class connectivity features
- Half the power of Spartan-6 FPGAs at 30% greater FMAX
- Industry’s smallest form factor (8x8mm) in a 28nm device
- Vivado® Design Suite support for a vast IP catalog and ASIC-class design flows
Artix-7 FPGAs – Now with Two New Low-Density Devices

The Artix-7 family is transceiver-optimized and is the portfolio’s high bandwidth FPGA. It serves as a cost-effective option for “high-end applications at the low end” that would otherwise need a mid-range solution. Boasting the highest transceiver line rates and DSP-to-logic ratios in any low-cost device, it leads the portfolio and the industry in key measures of performance and bandwidth:

- Up to sixteen 6.6Gb/s transceivers – highest line rate and aggregate bandwidth
- Lowest cost entry to key protocols, e.g., PCIe Gen2, HDMI, USB 3.0, SATA 3.0, DisplayPort
- 1,066Mb/s DDR3 – highest memory interface performance
- Up to 929 GMACs – highest signal processing bandwidth

Two new low-density Artix-7 devices have recently been added to the family, at 12,000 and 25,000 logic cells, giving an even lower cost access point to high performance transceiver.

<table>
<thead>
<tr>
<th>Logic Cells (LC)</th>
<th>12,800</th>
<th>16,640</th>
<th>23,360</th>
<th>33,280</th>
<th>52,160</th>
<th>75,520</th>
<th>101,440</th>
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<td>90</td>
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<td>180</td>
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<tr>
<td>Number of 6.6Gb/s Transceivers1</td>
<td>2</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>8</td>
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<td>16</td>
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<td>DDR3 Performance (Mb/s)</td>
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<td>1,066</td>
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<td>Key Protocols</td>
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Table 1: Two New Low Density Artix-7 Devices for Lower Cost Entry Points

Vivado Design Suite support is one of the Spartan-7 FPGA’s biggest advantages. The design suite has a vast library of proven IP cores along with its drag-and-drop IP integration methodology.

Meanwhile, its analytical place-and-route engine ensures up to 20% better utilization than preceding tools and the highest quality of results to fit into the smallest and most cost-effective device.
Zynq-7000 All Programmable SoCs – Now in Single-Core Configurations

The Zynq-7000 All Programmable SoC is perhaps the most diversely capable family in the portfolio for a breed of applications needing analytics and intelligence, and often running robust application software and operating systems. The long-established, cost-optimized Zynq-7000 devices are based on a dual-core ARM® Cortex™-A9 processing subsystem (PS) fused with Artix-7 FPGA programmable logic (PL). ARM® AMBA® AXI interfaces enables over 3000 interconnects between PL and PS—in other words more connectivity than is possible from a ‘processor-plus-FPGA’ implementation. This gives you ASSP, FPGA, DSP, and AMS functionality in a single chip, making it easier to offload algorithms to hardware for more performance than is possible by a stand-alone processor.

A Complete Platform with Tools and Ecosystem

But the best silicon, even with a scalable density range and resource mix, doesn't mean much without the right tools, methodologies, and 3rd party ecosystem. Because cost-sensitive markets tend to have exceptional time-to-market pressure—rapid design and bring-up in the least expensive part is especially critical.

With logic densities ranging from 4K to 200K logic cells, designers can target Spartan-7, Artix-7, and Zynq-7000 devices with the same hardware IP subsystems for derivative end products. This avoids time unnecessarily spent on porting the same design blocks for different architectures, or having to come up to speed on different design or debug tools.

Empowering hardware designers, the well-established Vivado Design Suite simplifies IP-reuse across the portfolio with the industry's first plug-and-play IP integration environment. With IP Integrator, designers can intuitively build a system or subsystem from a vast IP catalog, or create their own reusable IP. For implementation, Vivado offers the industry's first analytical place-and-route engine for 20% greater utilization than its predecessor, so you can use the smallest, lowest cost device possible.

Empowering embedded designers, Xilinx provides both High Level Synthesis (HLS) and SDx™ Development Environments for an application software development and runtime experience familiar to software engineers, all without the need for RTL expertise. Designers can accelerate the C, C++, or OpenCL function of their choosing into hardware by the click of a button, and let the tool compile the entire SoC.

Of equal importance is the ecosystem. To bring a design to closure, developers need a breadth of options at their disposal—often beyond the scope of a single vendor. Plugging into over 400 ecosystem partners, Xilinx customers can select from a range of IP, tools, OS's, development kits, and design services.
Choosing Your Device Family

Diverse and scalable—the Cost-Optimized Portfolio gives a range of low cost options depending on desired use models. Spartan devices offer best-in-class connectivity, with the Spartan-7 family being the industry's highest performance-per-watt FPGA in the smallest form factor. Artix-7 FPGAs are a great low-cost alternative for bandwidth-hungry applications, while Zynq-7000 SoCs offer a scalable processing platform ideal for heavier analytics and secured cloud connectivity.

Table 2 represents the portfolio at a glance in terms of resource mix. For more information, please visit: www.xilinx.com/cost-optimized-portfolio.

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<thead>
<tr>
<th></th>
<th>FPGA</th>
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<td>Spartan-6</td>
<td>Spartan-7</td>
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<td>Transceiver Performance</td>
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Table 2: Portfolio at a Glance