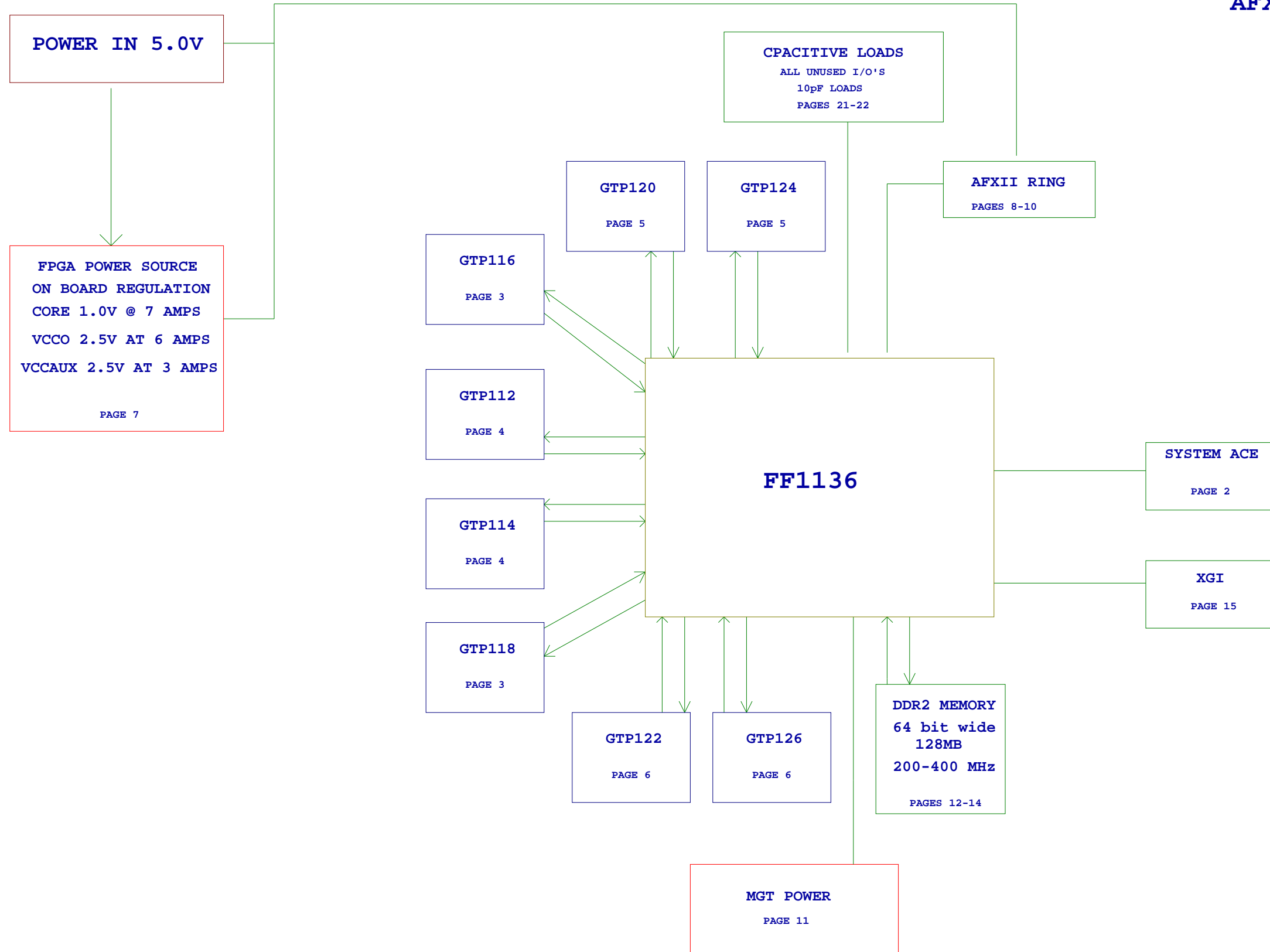

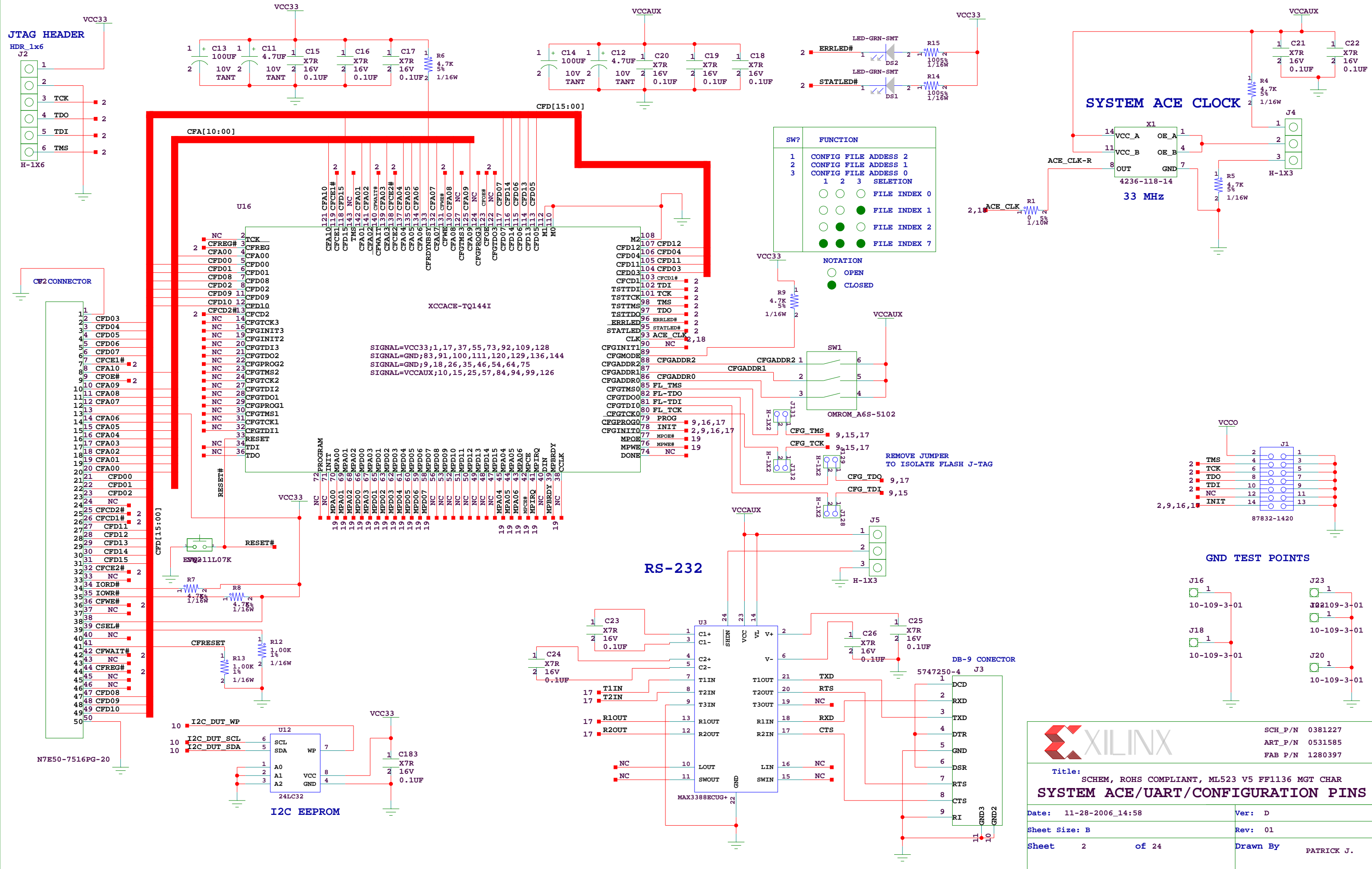


MGT CHARACTERIZATION BOARD FOR V5
AFXII COMPATIBLE



| | | | |
|---|-------|---------------------|--|
|  | | SCH_P/N 0381227 | |
| | | ART_P/N 0531585 | |
| | | FAB P/N 1280397 | |
| Title: SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR BLOCK DIAGRAM | | | |
| Date: 11-28-2006_14:58 | | Ver: D | |
| Sheet Size: B | | Rev: 01 | |
| Sheet 1 | of 24 | Drawn By PATRICK J. | |



| SW? | FUNCTION | | |
|----------------------------------|----------------------------------|----------------------------------|--------------|
| 1 | CONFIG FILE ADDRESS 2 | | |
| 2 | CONFIG FILE ADDRESS 1 | | |
| 3 | CONFIG FILE ADDRESS 0 | | |
| 1 | 2 | 3 | SELECTION |
| <input type="radio"/> | <input type="radio"/> | <input type="radio"/> | FILE INDEX 0 |
| <input type="radio"/> | <input type="radio"/> | <input checked="" type="radio"/> | FILE INDEX 1 |
| <input type="radio"/> | <input checked="" type="radio"/> | <input type="radio"/> | FILE INDEX 2 |
| <input checked="" type="radio"/> | <input checked="" type="radio"/> | <input checked="" type="radio"/> | FILE INDEX 7 |

NOTATION
 OPEN
 CLOSED

SIGNAL=VCC33;1,17,37,55,73,92,109,128
 SIGNAL=GND;83,91,100,111,120,129,136,144
 SIGNAL=GND;9,18,26,35,46,54,64,75
 SIGNAL=VCCAUX;10,15,25,57,84,94,99,126

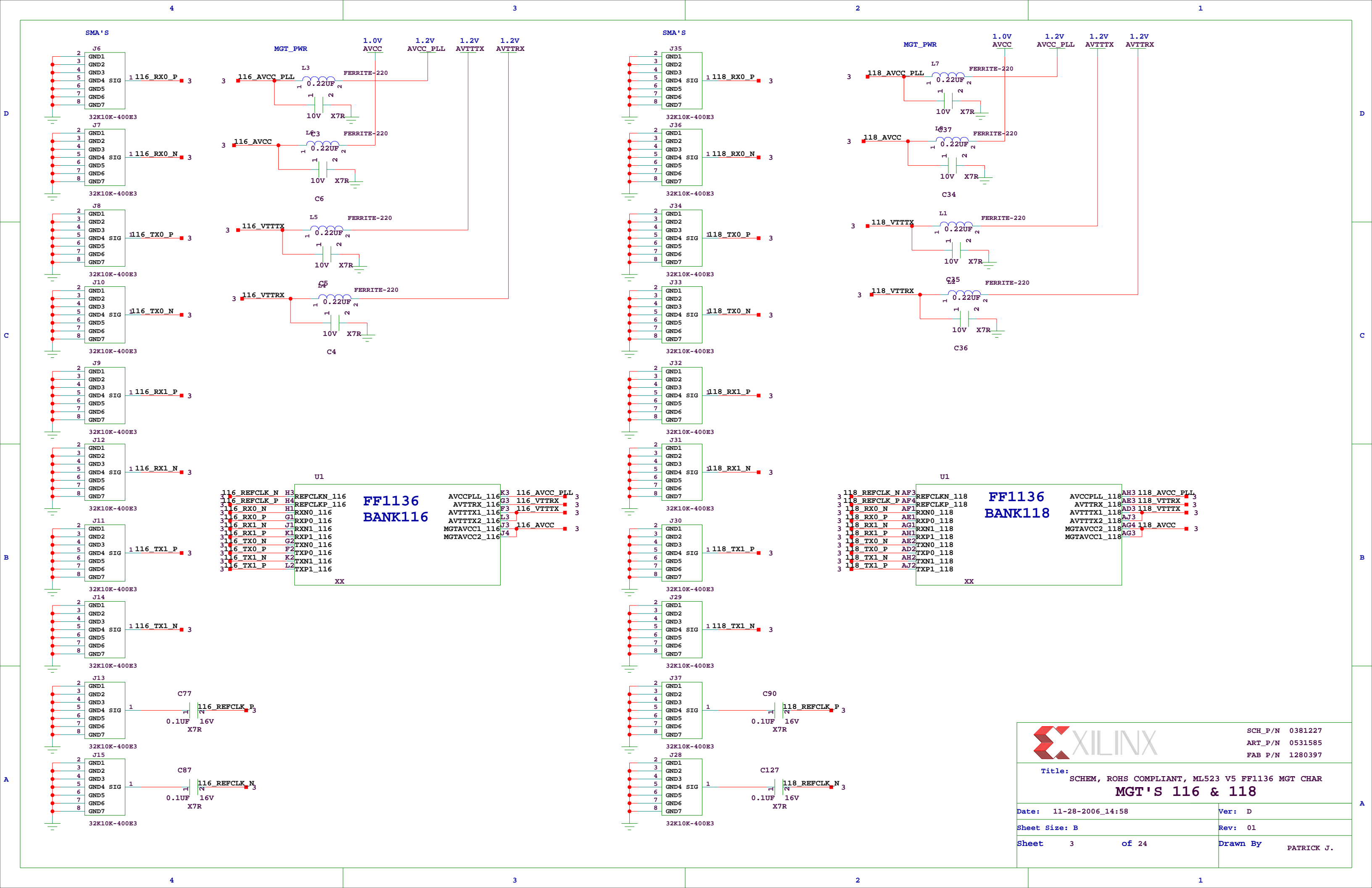
REMOVE JUMPER TO ISOLATE FLASH J-TAG

XILINX

SCH_P/N 0381227
 ART_P/N 0531585
 FAB_P/N 1280397

Title: SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR
SYSTEM ACE/UART/CONFIGURATION PINS

| | |
|------------------------|---------------------|
| Date: 11-28-2006_14:58 | Ver: D |
| Sheet Size: B | Rev: 01 |
| Sheet 2 of 24 | Drawn By PATRICK J. |

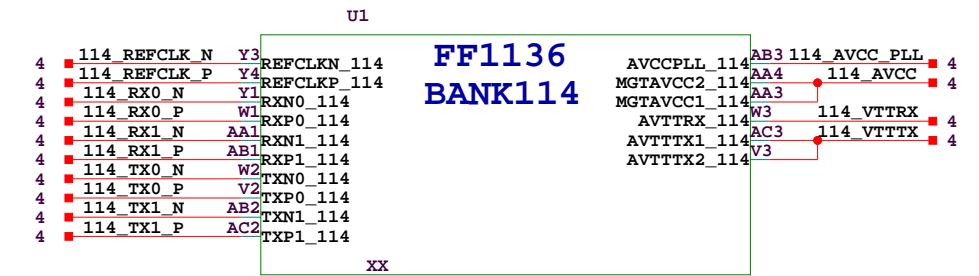
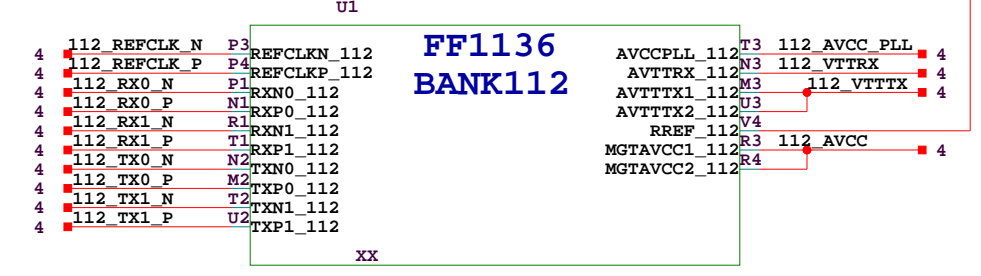
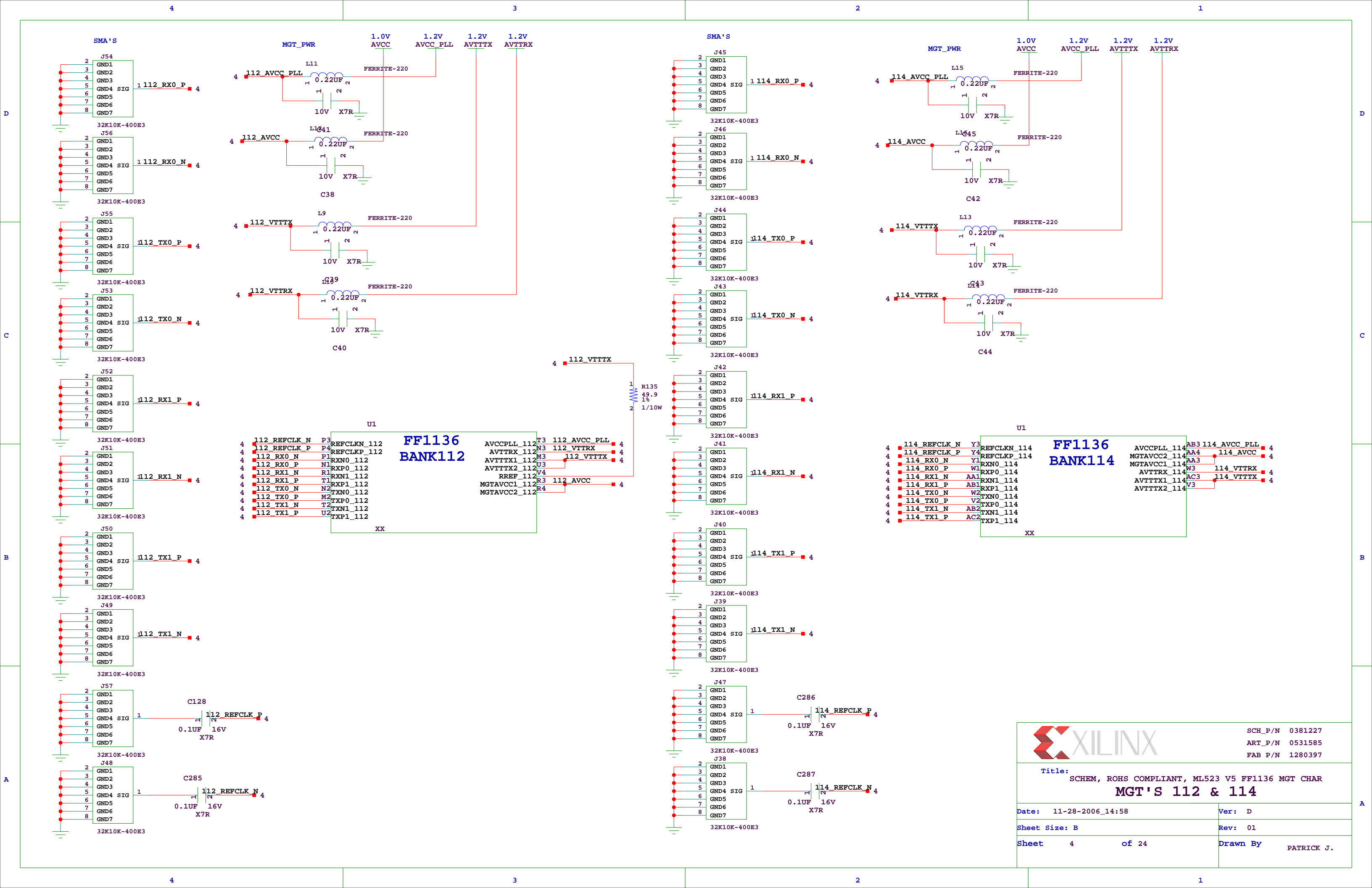


XILINX

SCH_P/N 0381227
 ART_P/N 0531585
 FAB_P/N 1280397

Title: SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR
MGT'S 116 & 118

Date: 11-28-2006_14:58 Ver: D
 Sheet Size: B Rev: 01
 Sheet 3 of 24 Drawn By PATRICK J.

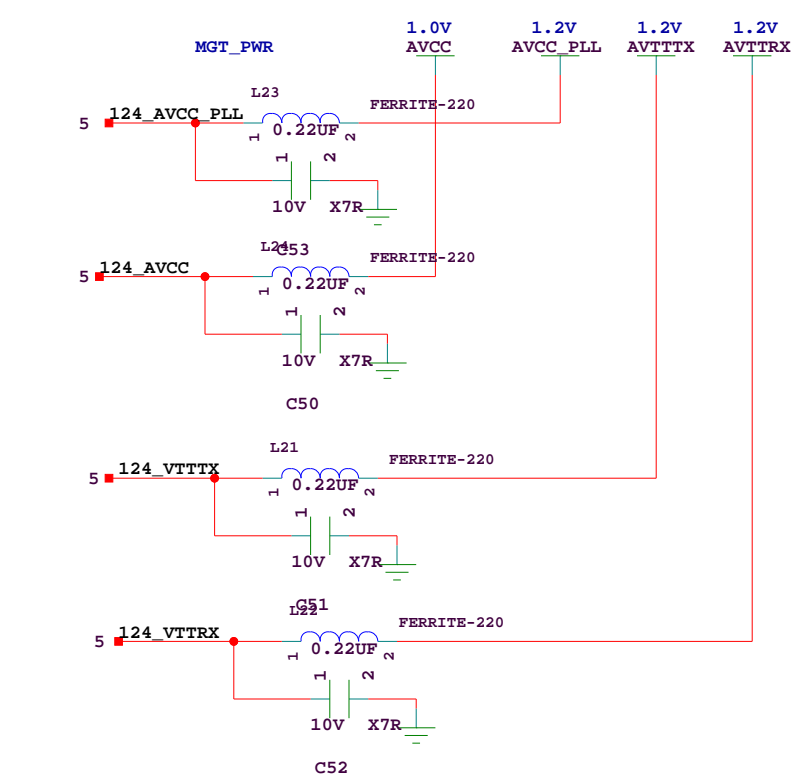
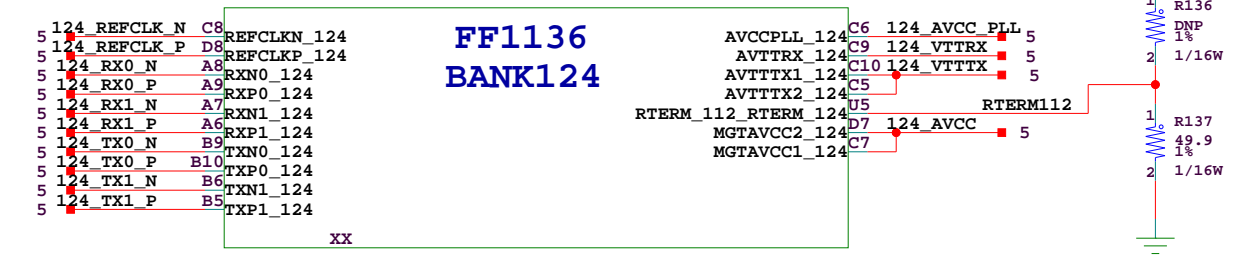
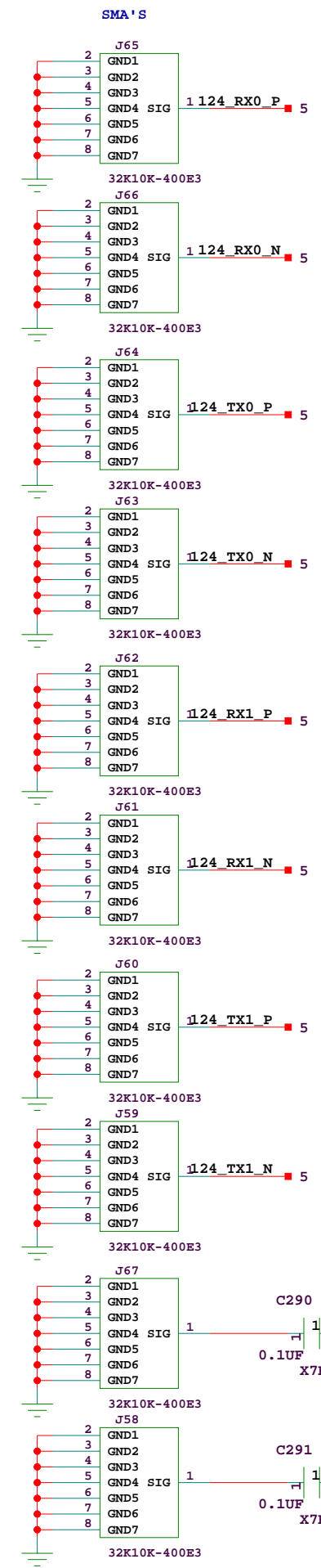
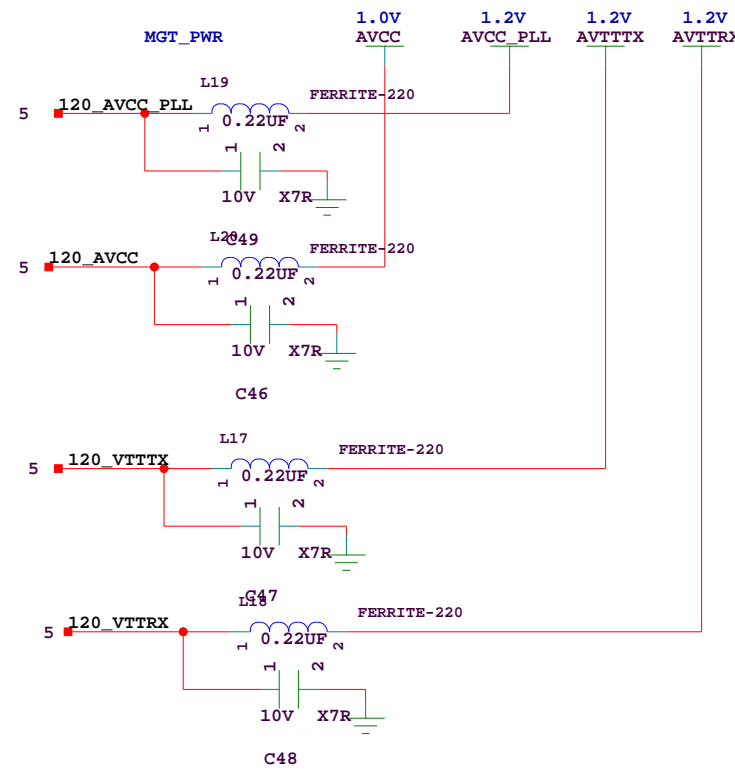
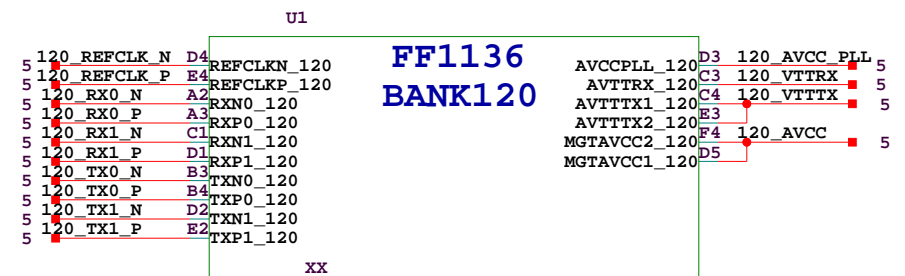
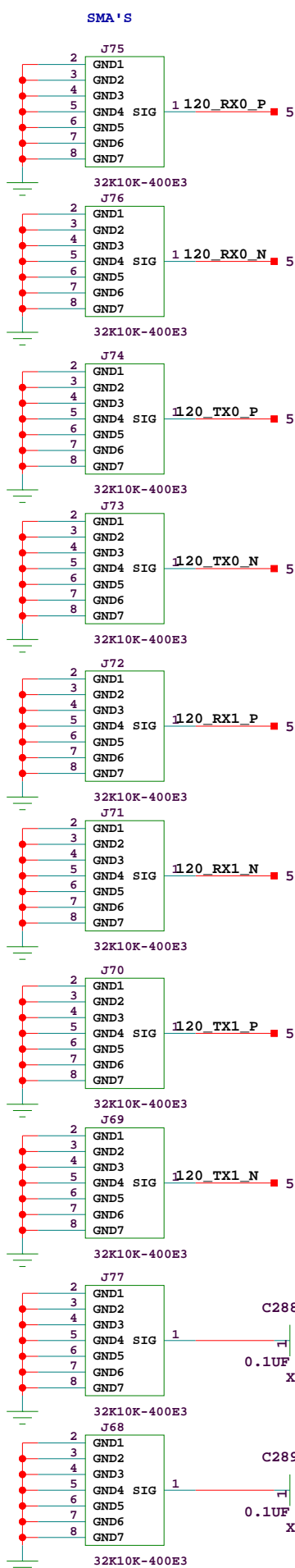


XILINX

SCH_P/N 0381227
 ART_P/N 0531585
 FAB_P/N 1280397

Title: SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR
MGT'S 112 & 114

| | |
|------------------------|---------------------|
| Date: 11-28-2006_14:58 | Ver: D |
| Sheet Size: B | Rev: 01 |
| Sheet 4 of 24 | Drawn By PATRICK J. |

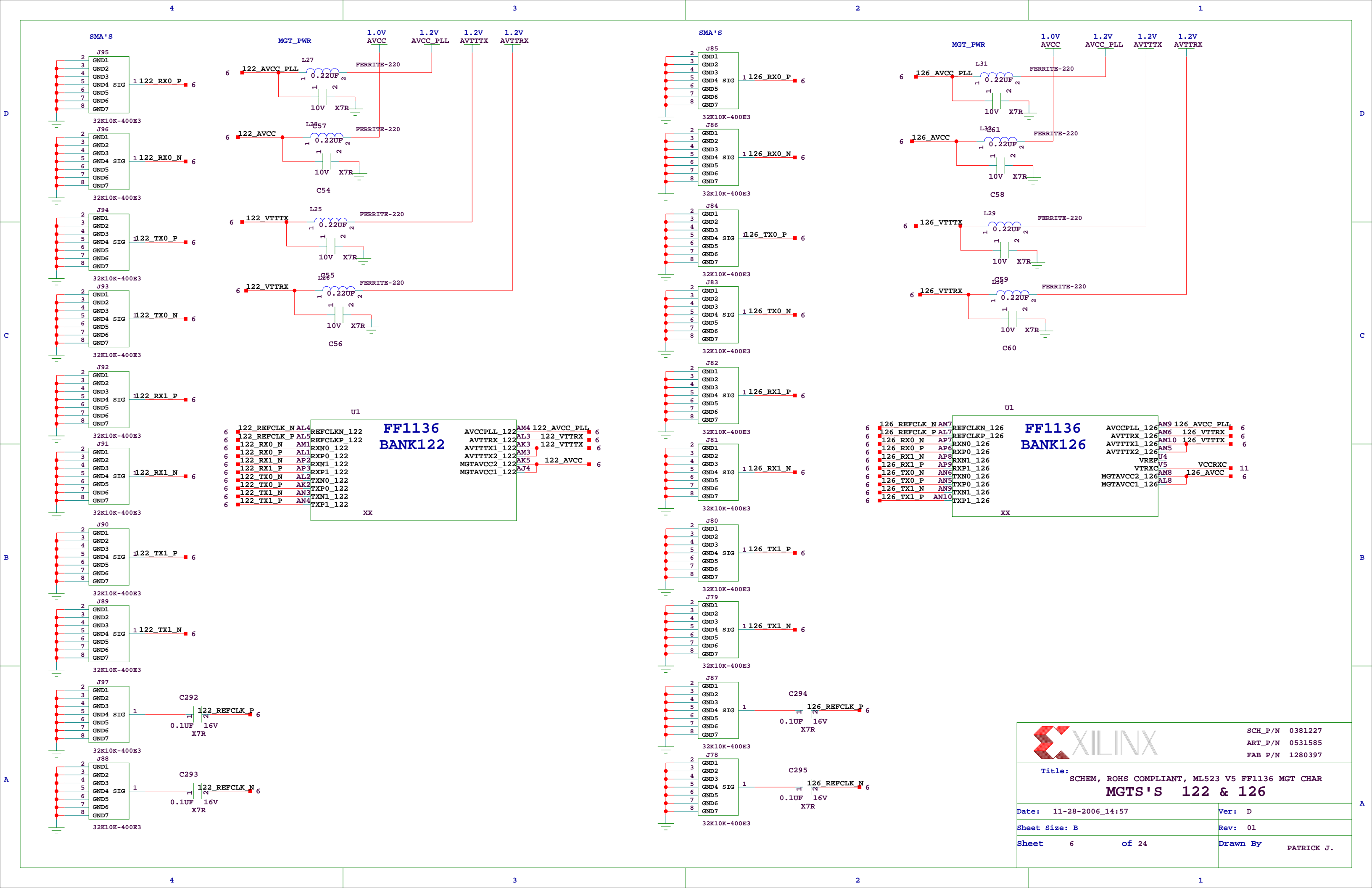


FEATURE AVAILABLE ON FX DEVICE

SCH_P/N 0381227
 ART_P/N 0531585
 FAB_P/N 1280397

Title: SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR
MGTS'S 120 & 124

| | |
|------------------------|---------------------|
| Date: 11-28-2006_14:57 | Ver: D |
| Sheet Size: B | Rev: 01 |
| Sheet 5 of 24 | Drawn By PATRICK J. |

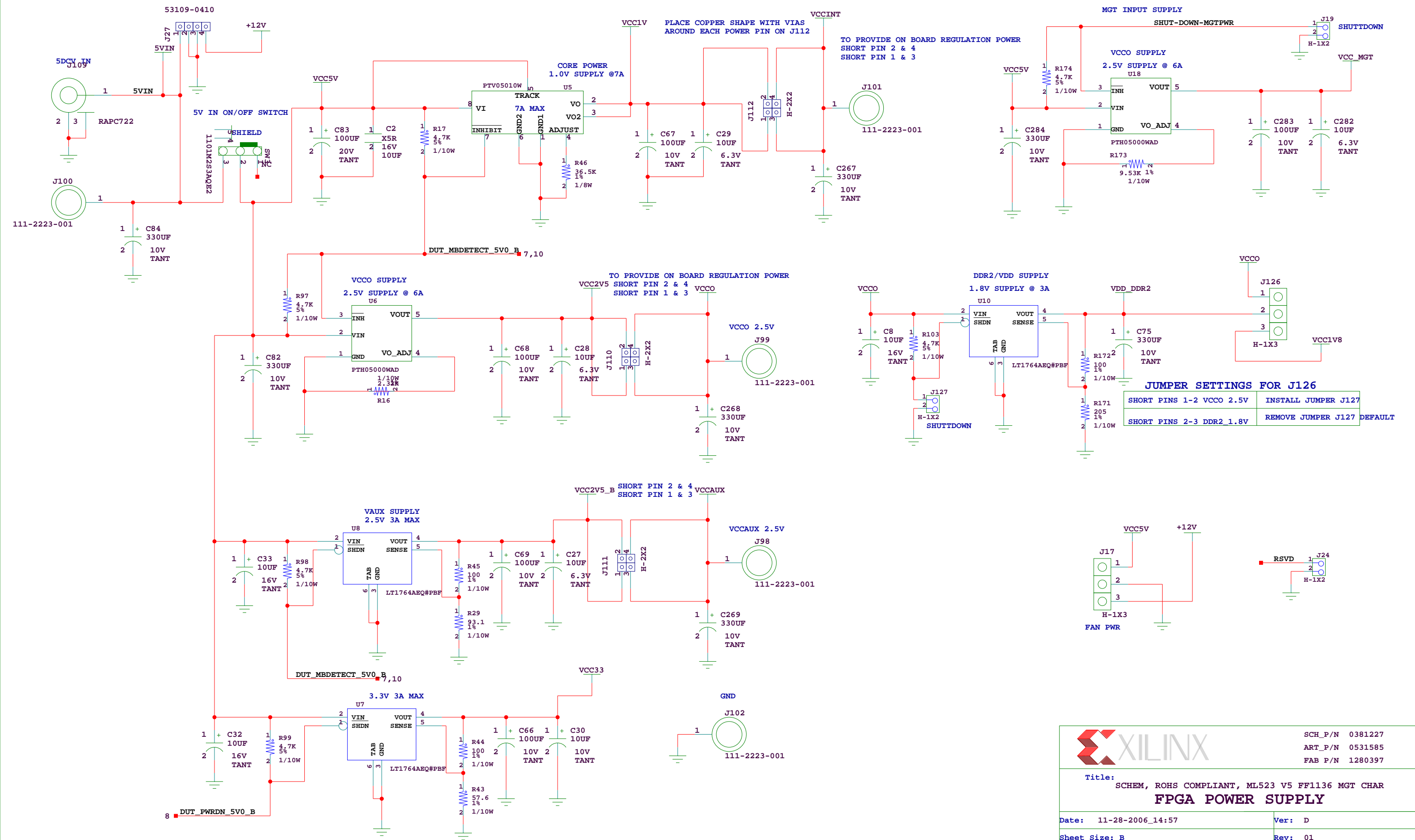


XILINX

SCH_P/N 0381227
 ART_P/N 0531585
 FAB_P/N 1280397

Title: SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR
MGTS'S 122 & 126

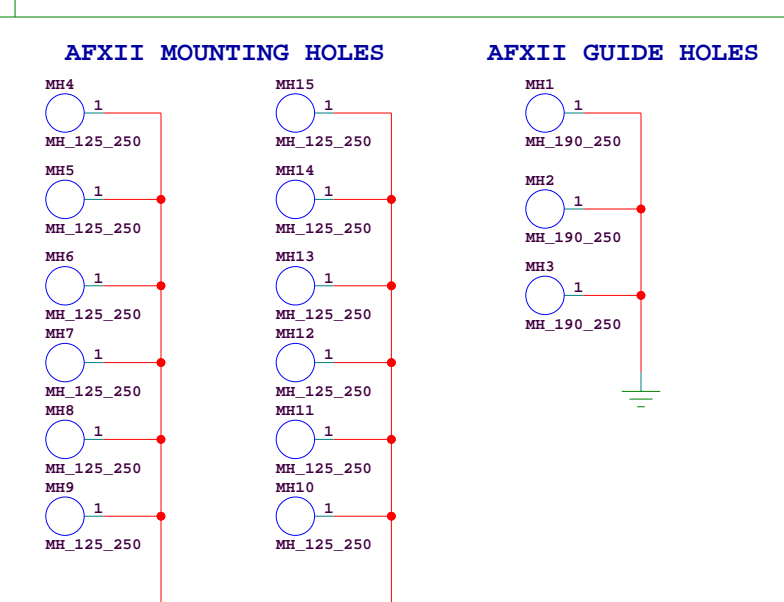
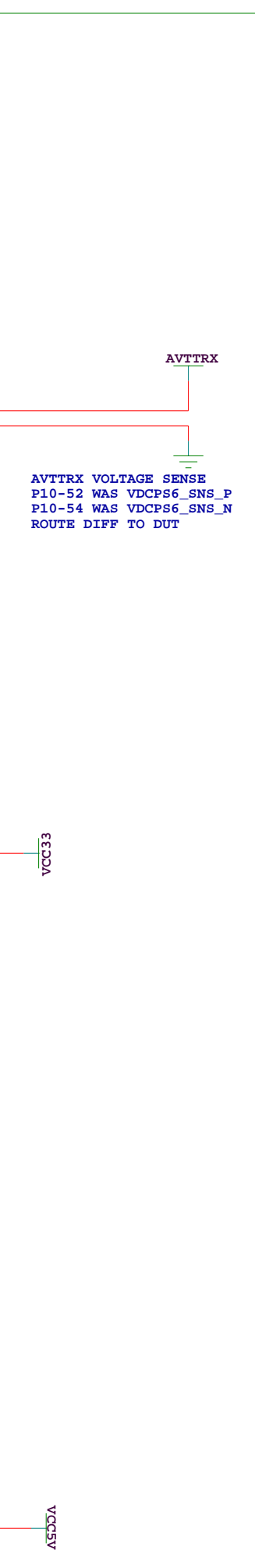
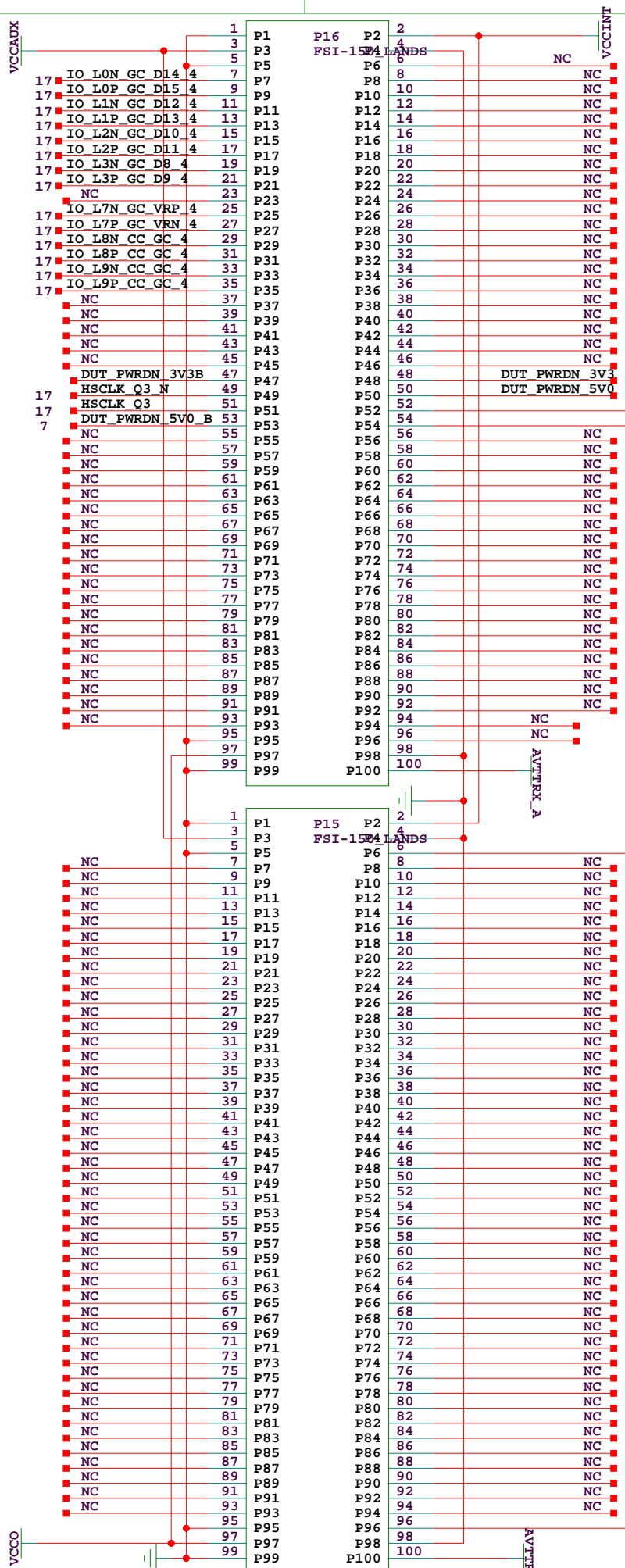
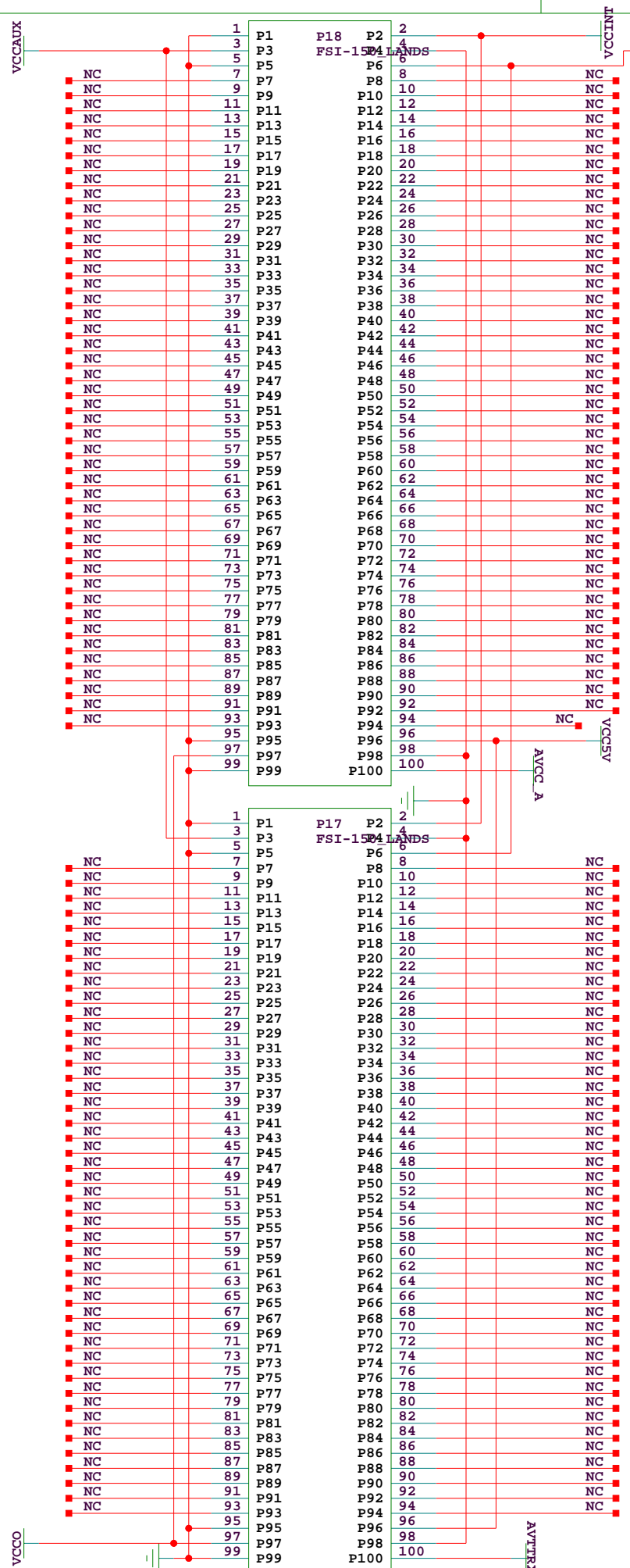
Date: 11-28-2006_14:57 Ver: D
 Sheet Size: B Rev: 01
 Sheet 6 of 24 Drawn By PATRICK J.



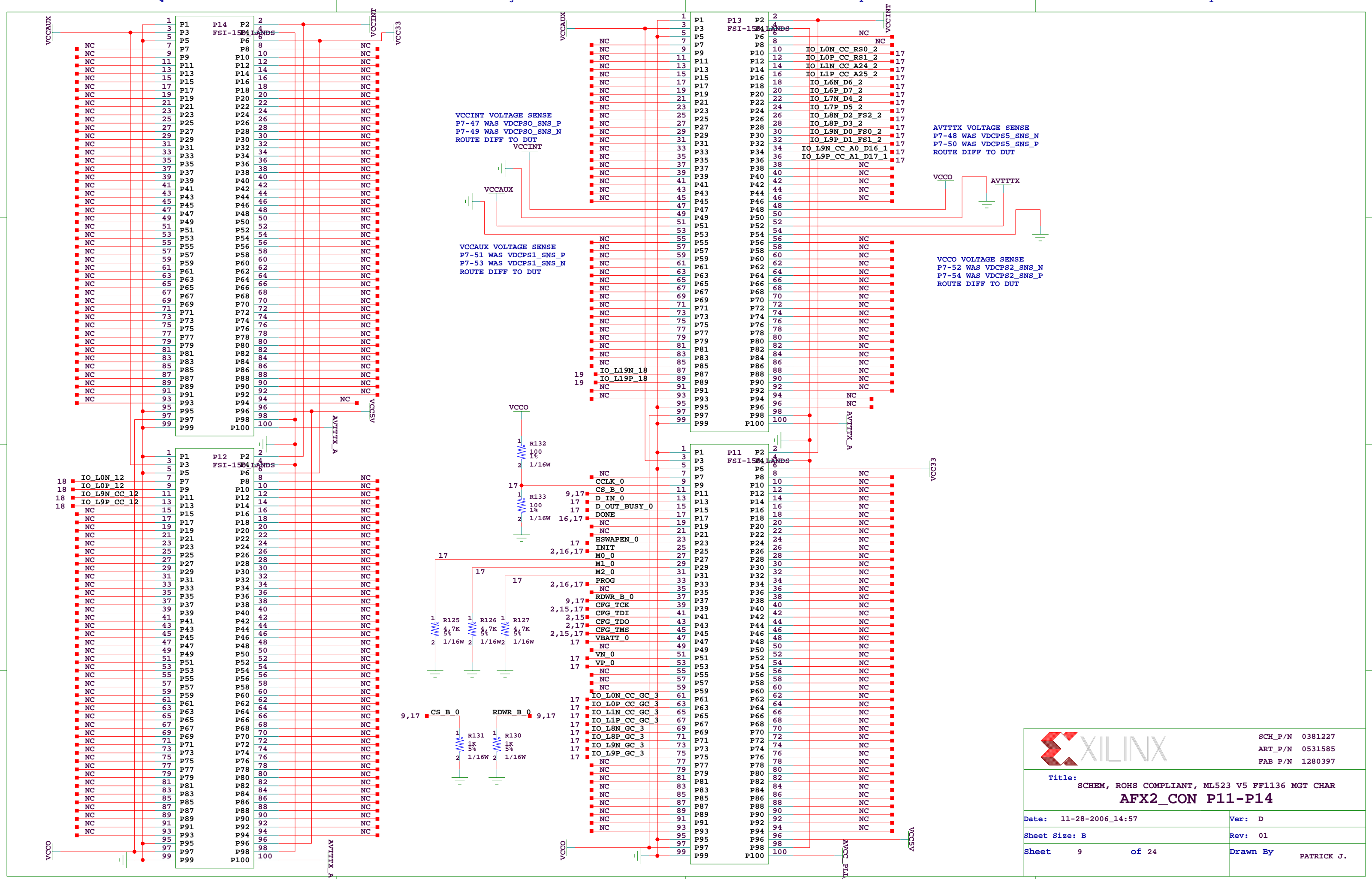
SCH P/N 0381227
 ART P/N 0531585
 FAB P/N 1280397

Title:
 SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR
FPGA POWER SUPPLY

Date: 11-28-2006_14:57 Ver: D
 Sheet Size: B Rev: 01
 Sheet 7 of 24 Drawn By PATRICK J.



| | | | |
|---|-------|---------------------|---------|
| | | SCH_P/N | 0381227 |
| | | ART_P/N | 0531585 |
| | | FAB_P/N | 1280397 |
| Title: SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR AFX2_CON P15-P18 | | | |
| Date: 11-28-2006_14:57 | | Ver: D | |
| Sheet Size: B | | Rev: 01 | |
| Sheet 8 | of 24 | Drawn By PATRICK J. | |

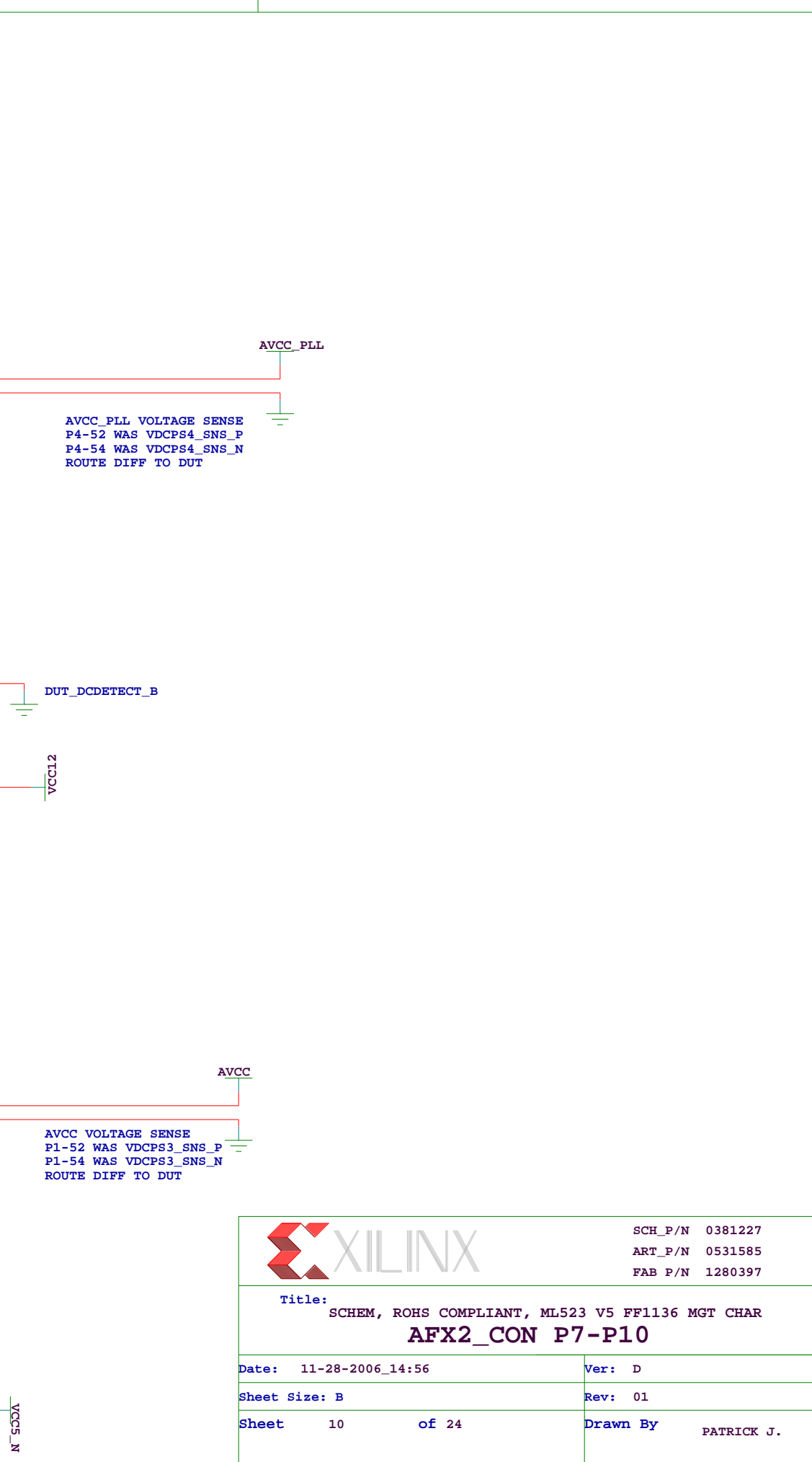
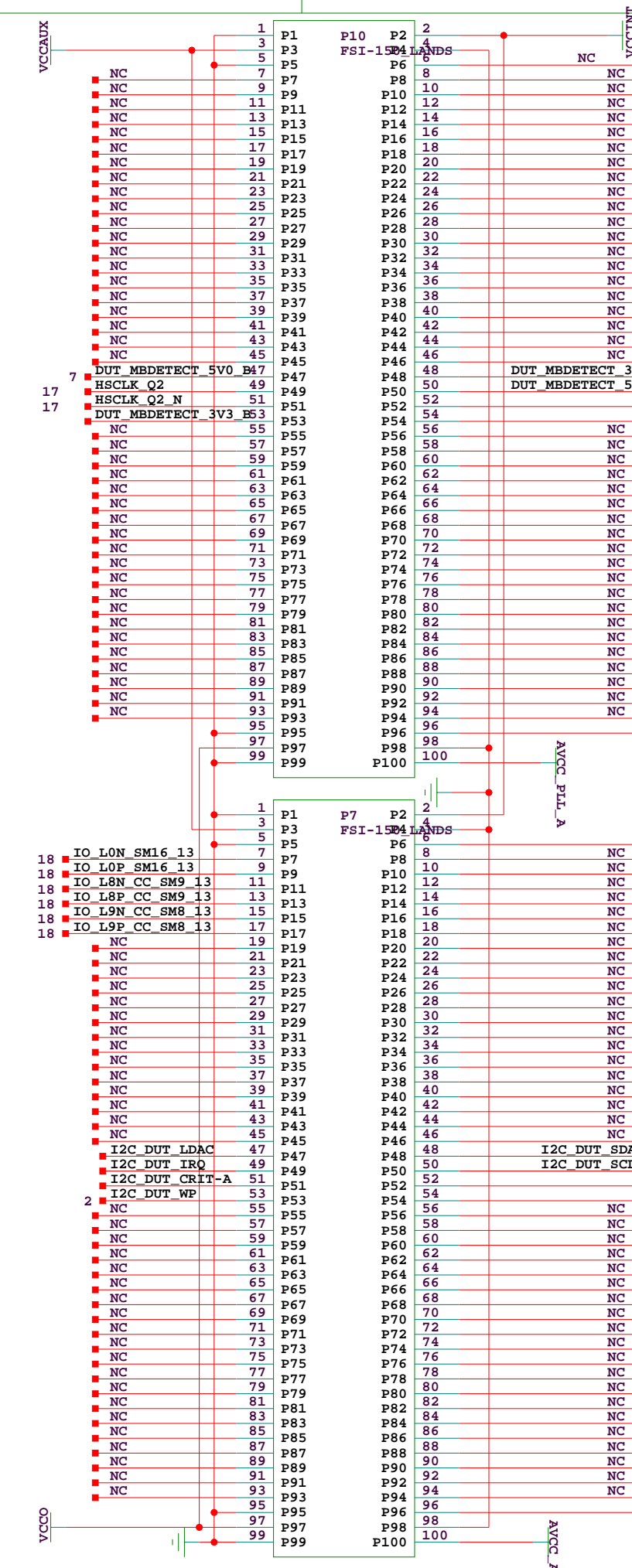
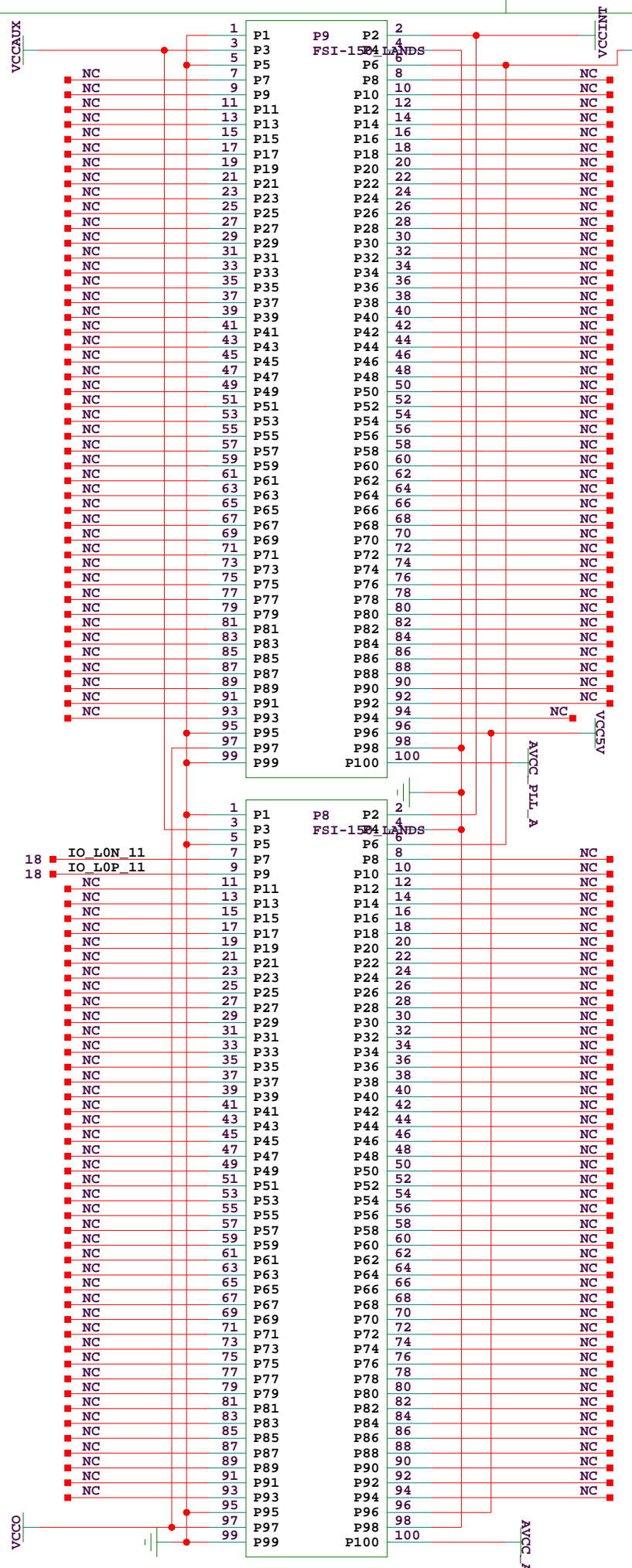


XILINX

SCH_P/N 0381227
ART_P/N 0531585
FAB_P/N 1280397

Title: SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR
AFX2_CON P11-P14

Date: 11-28-2006_14:57 Ver: D
Sheet Size: B Rev: 01
Sheet 9 of 24 Drawn By PATRICK J.



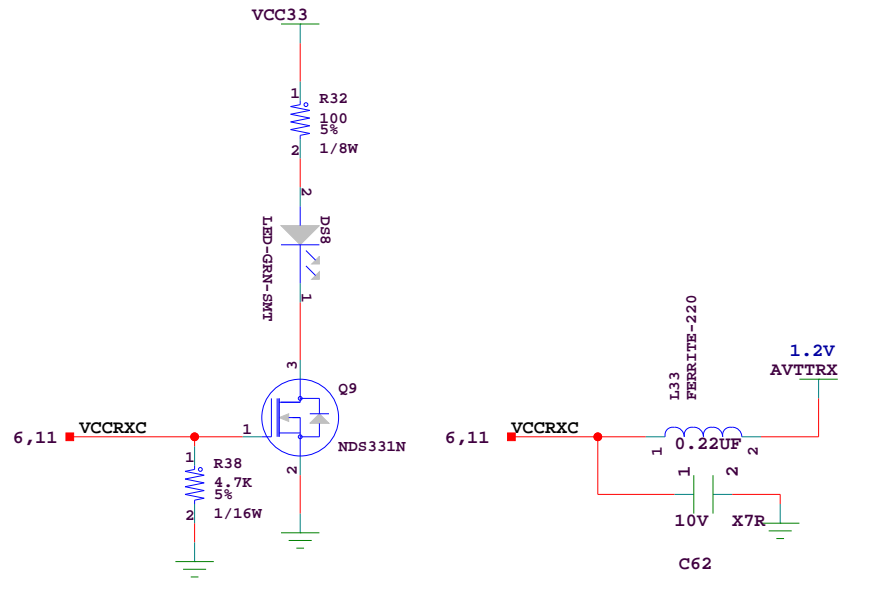
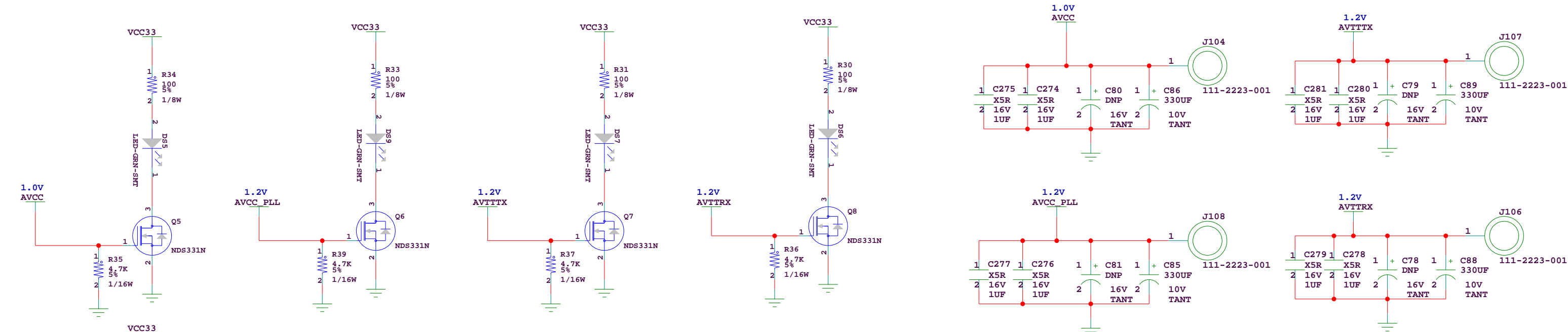
XILINX

SCH_P/N 0381227
ART_P/N 0531585
FAB_P/N 1280397

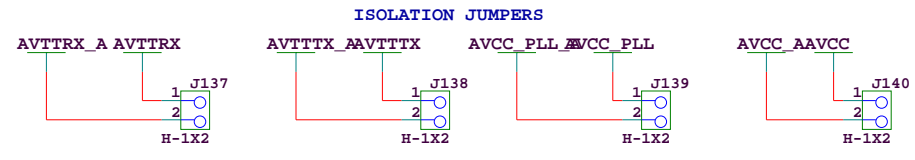
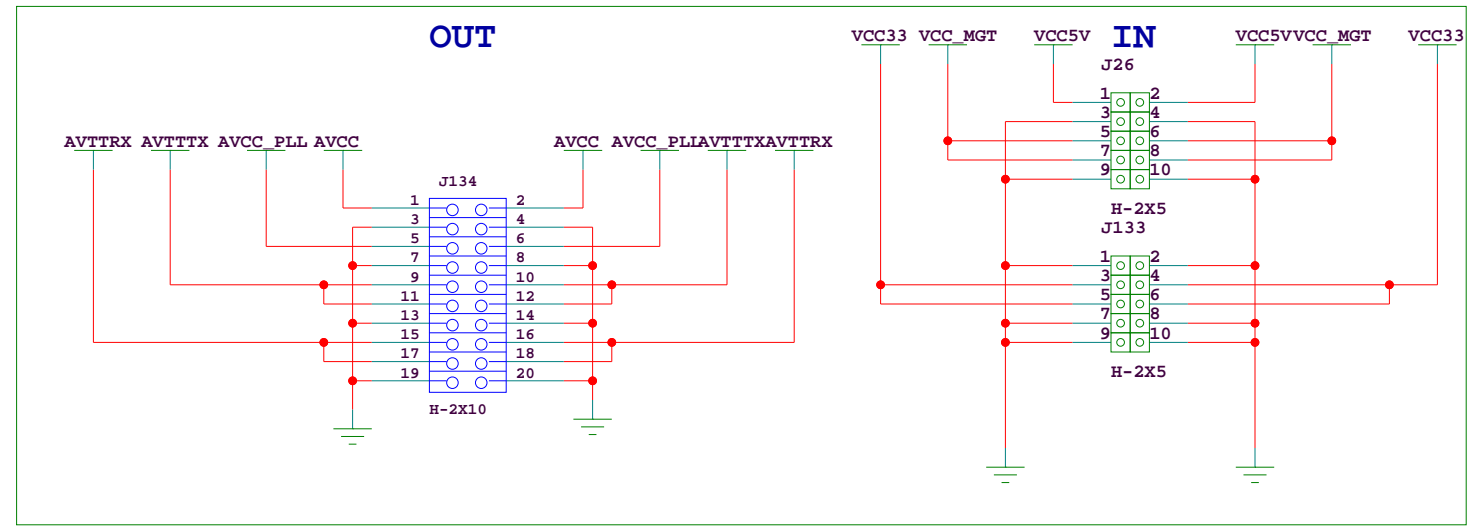
Title:
SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR

AFX2_CON P7-P10

| | |
|------------------------|---------------------|
| Date: 11-28-2006_14:56 | Ver: D |
| Sheet Size: B | Rev: 01 |
| Sheet 10 of 24 | Drawn By PATRICK J. |

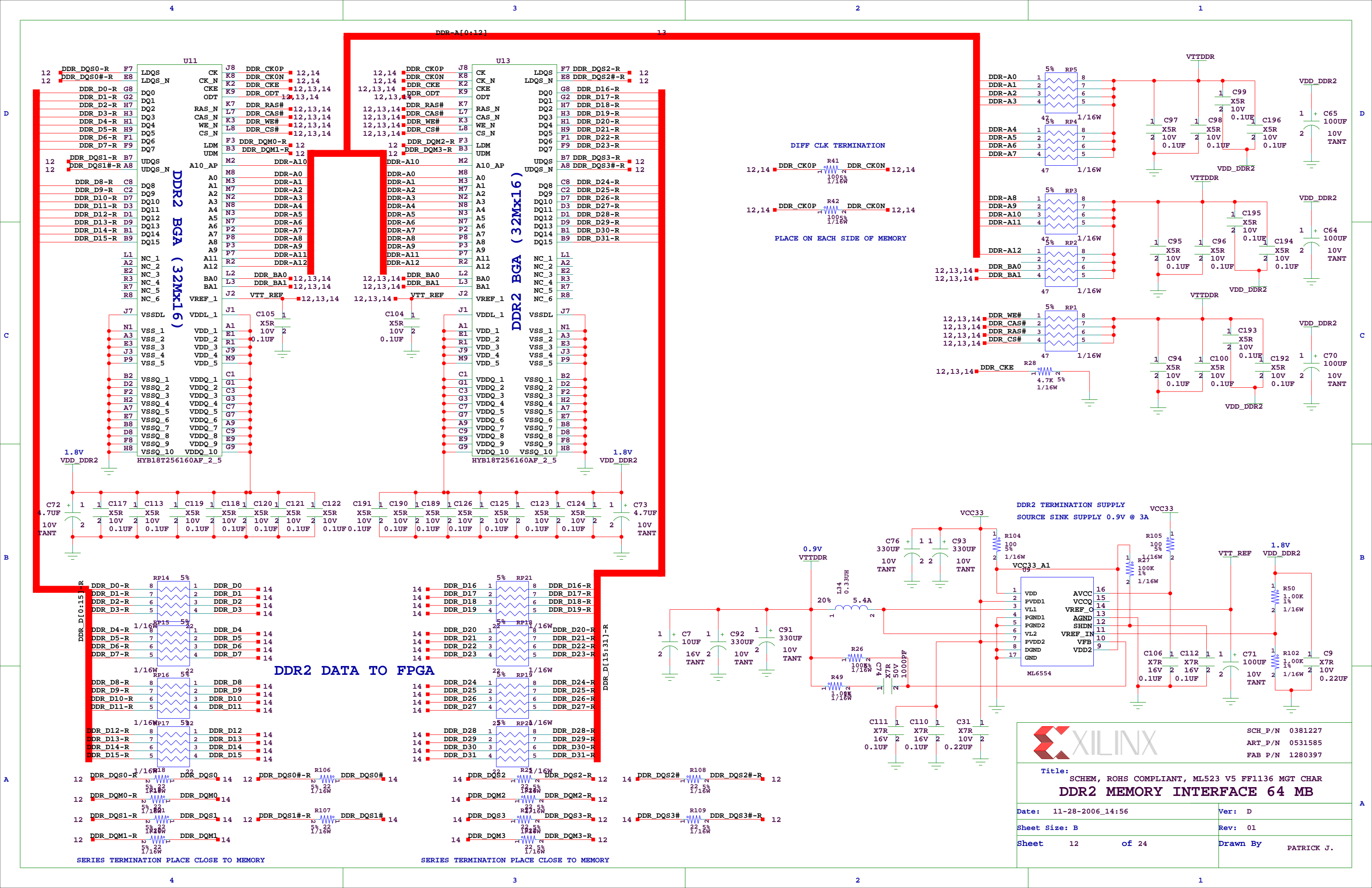


POWER SUPPLY MODULE



JUMPER ON FOR AFXII DCPS POWER FOR MGT'S
 JUMPER OFF FOR ON BOARD REGULATION

| | | | |
|---|--|---------------------|--|
| | | SCH_P/N 0381227 | |
| | | ART_P/N 0531585 | |
| | | FAB P/N 1280397 | |
| Title: SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR MGT'S POWER SUPPLY | | | |
| Date: 11-28-2006_14:56 | | Ver: D | |
| Sheet Size: B | | Rev: 01 | |
| Sheet 11 of 24 | | Drawn By PATRICK J. | |



DDR2 BGA (32Mx16)

DDR2 BGA (32Mx16)

DDR2 DATA TO FPGA

DDR2 TERMINATION SUPPLY
SOURCE SINK SUPPLY 0.9V @ 3A



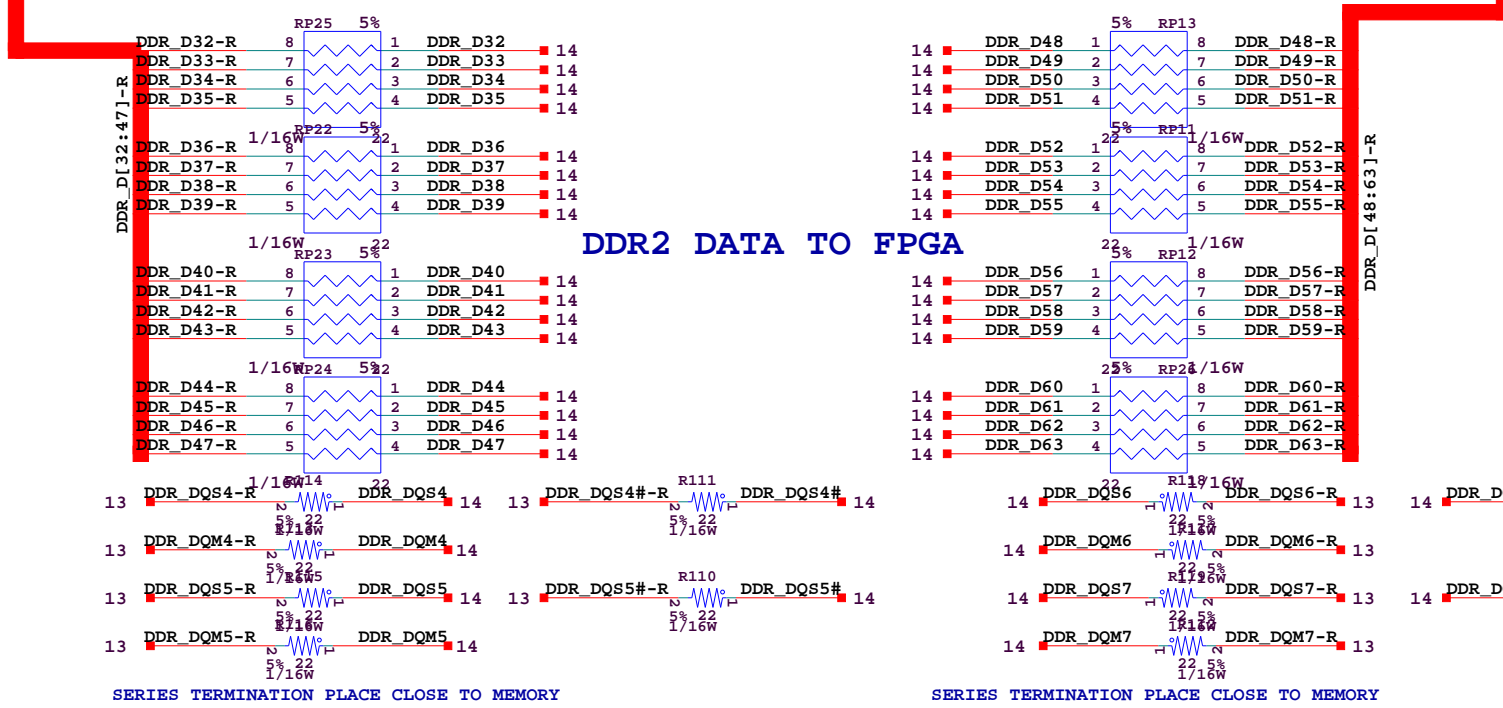
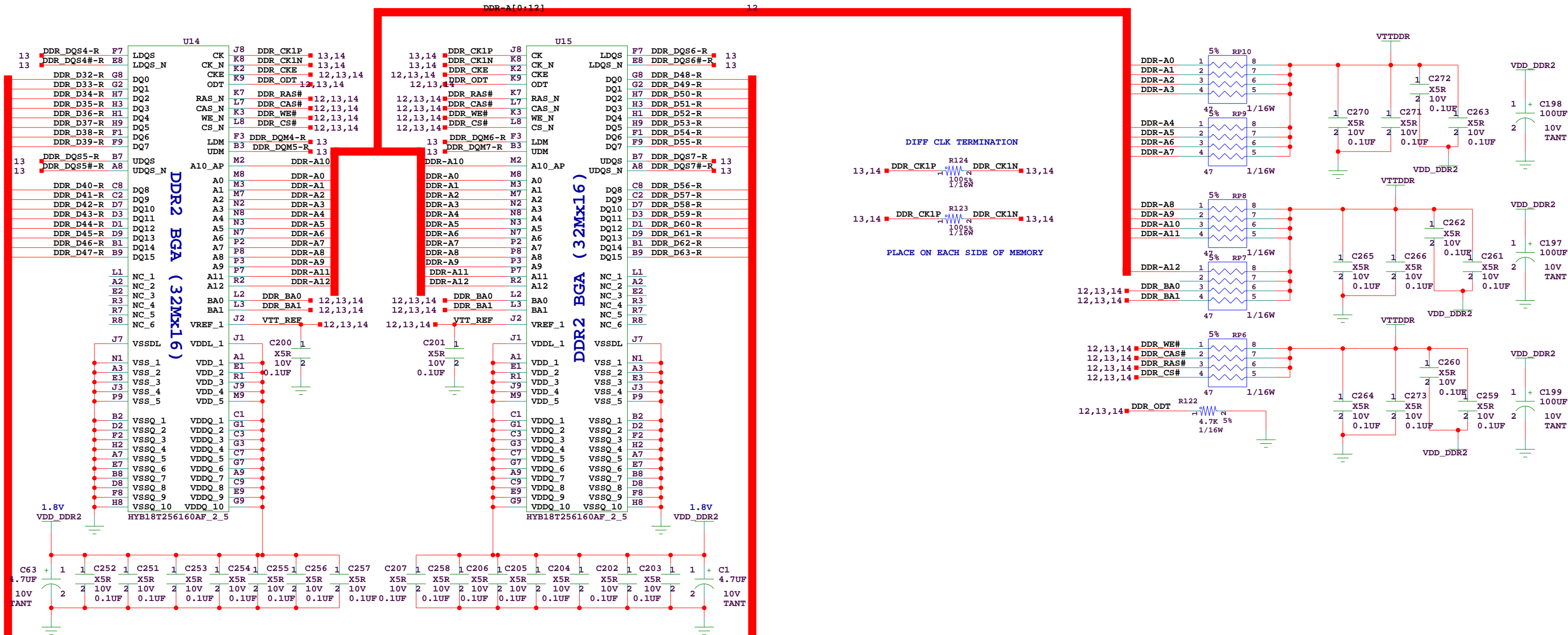
Title: SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR
DDR2 MEMORY INTERFACE 64 MB

| | |
|------------------------|---------------------|
| Date: 11-28-2006_14:56 | Ver: D |
| Sheet Size: B | Rev: 01 |
| Sheet 12 of 24 | Drawn By PATRICK J. |

SCH_P/N 0381227
ART_P/N 0531585
FAB_P/N 1280397

SERIES TERMINATION PLACE CLOSE TO MEMORY

SERIES TERMINATION PLACE CLOSE TO MEMORY



XILINX

SCH_P/N 0381227
 ART_P/N 0531585
 FAB_P/N 1280397

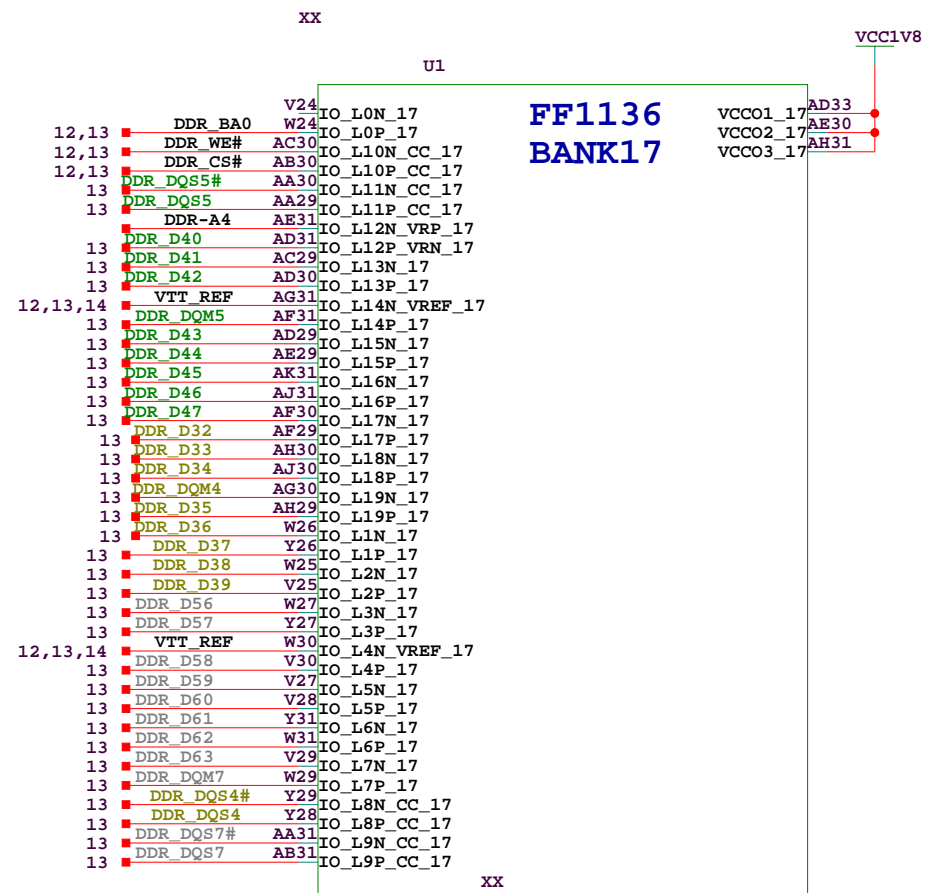
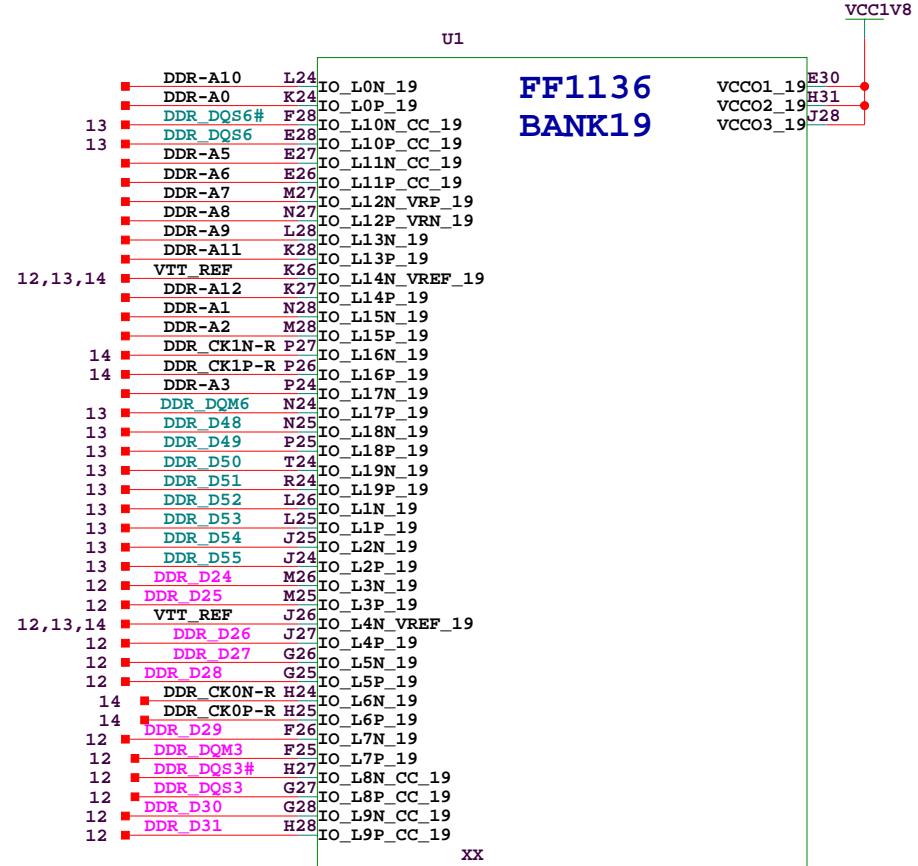
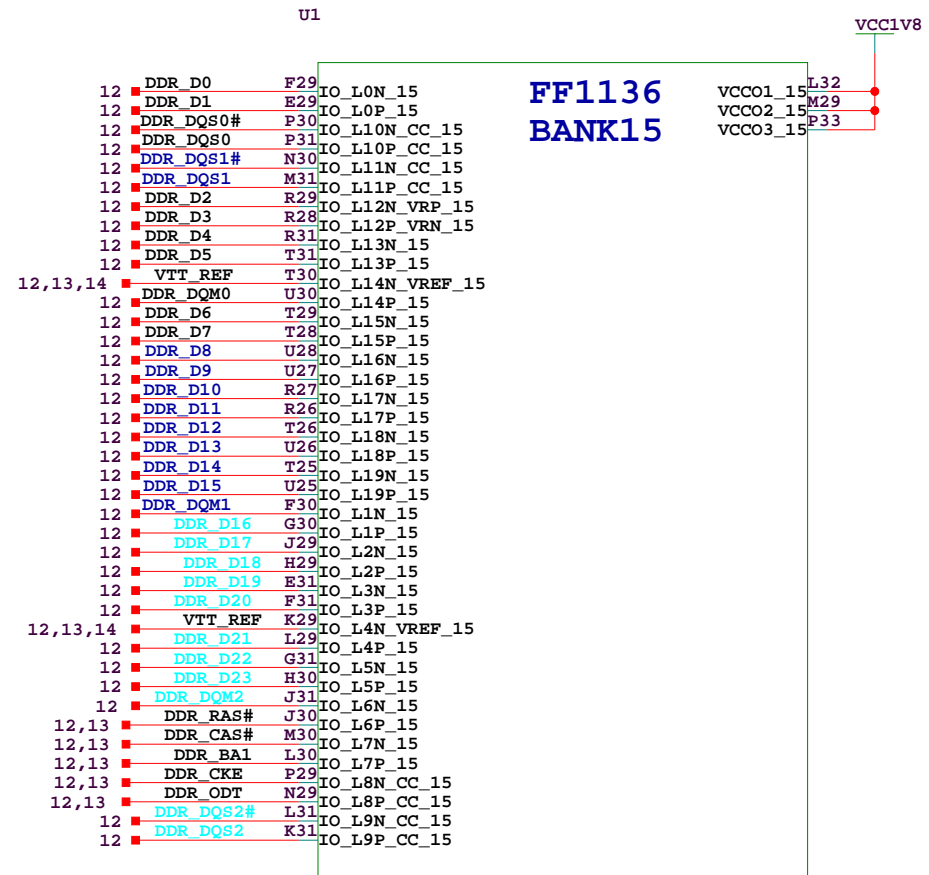
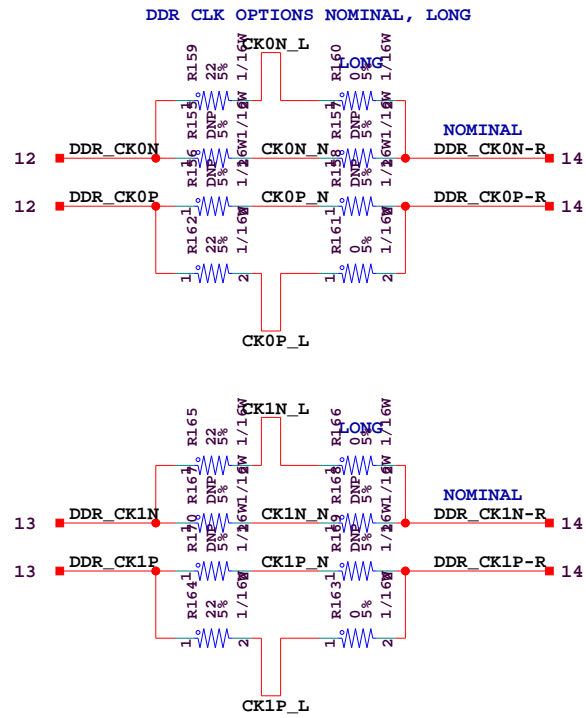
Title: SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR
DDR2 MEMORY INTERFACE 64 MB

Date: 11-28-2006_14:56 Ver: D
 Sheet Size: B Rev: 01
 Sheet 13 of 24 Drawn By PATRICK J.

NOTE:

DCI IS NOT REQUIRED
 WILL USE EXTERNAL SERIES TERMINATION
 VREF PINS ARE TIED TO VREF TERMINATION

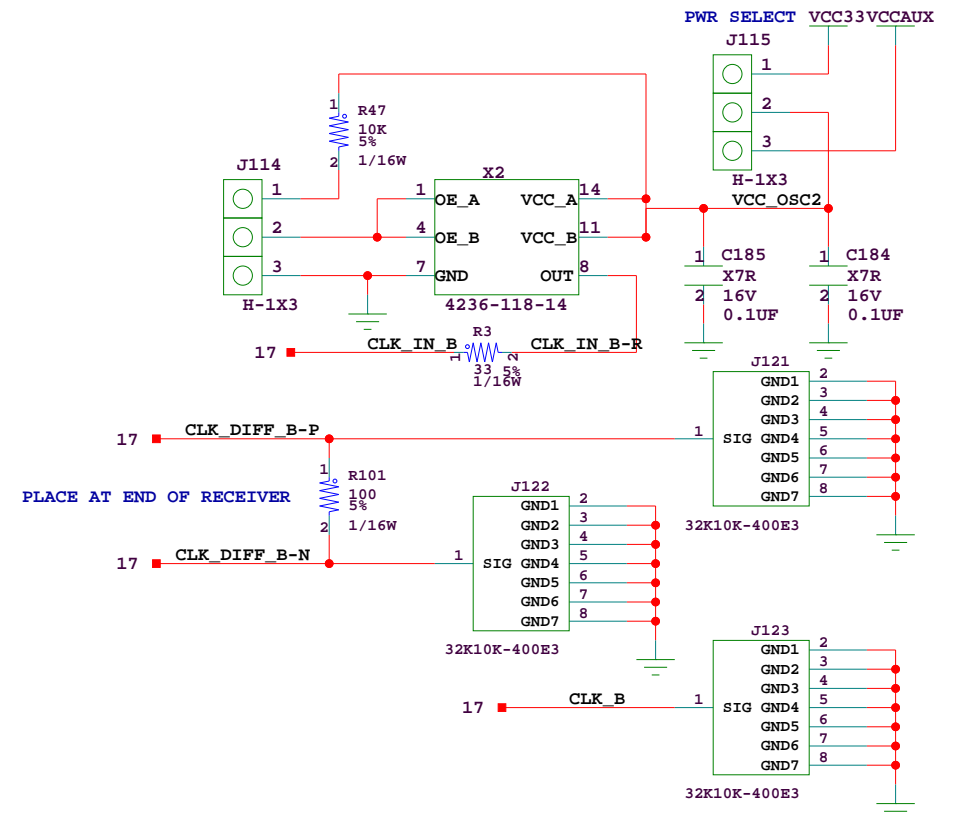
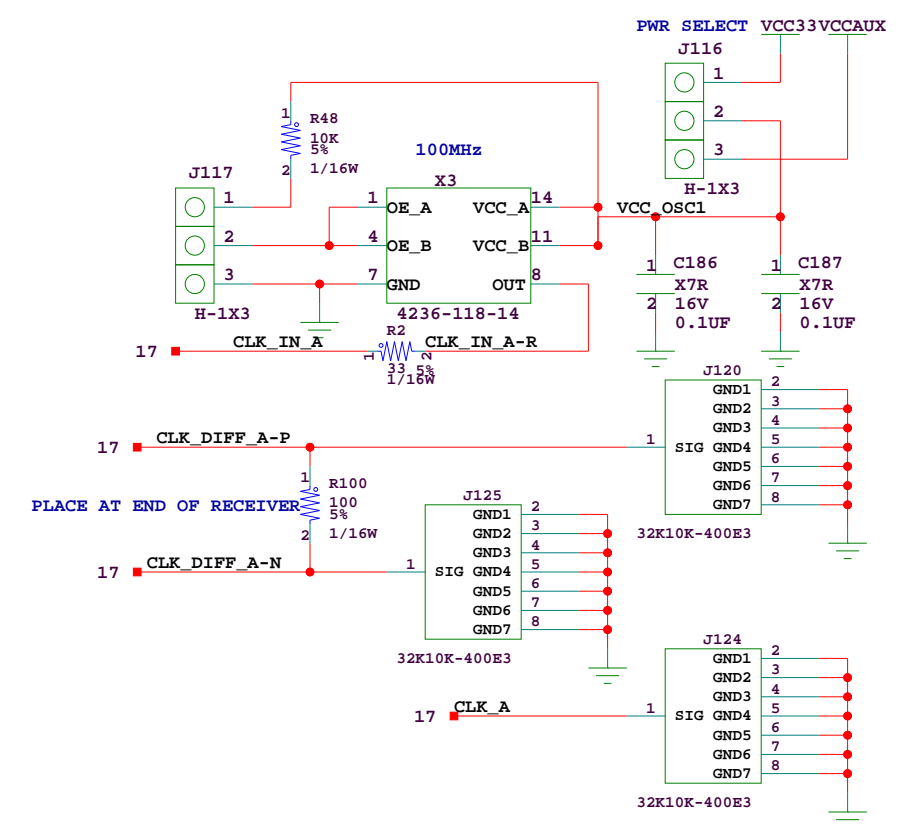
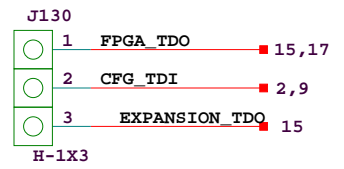
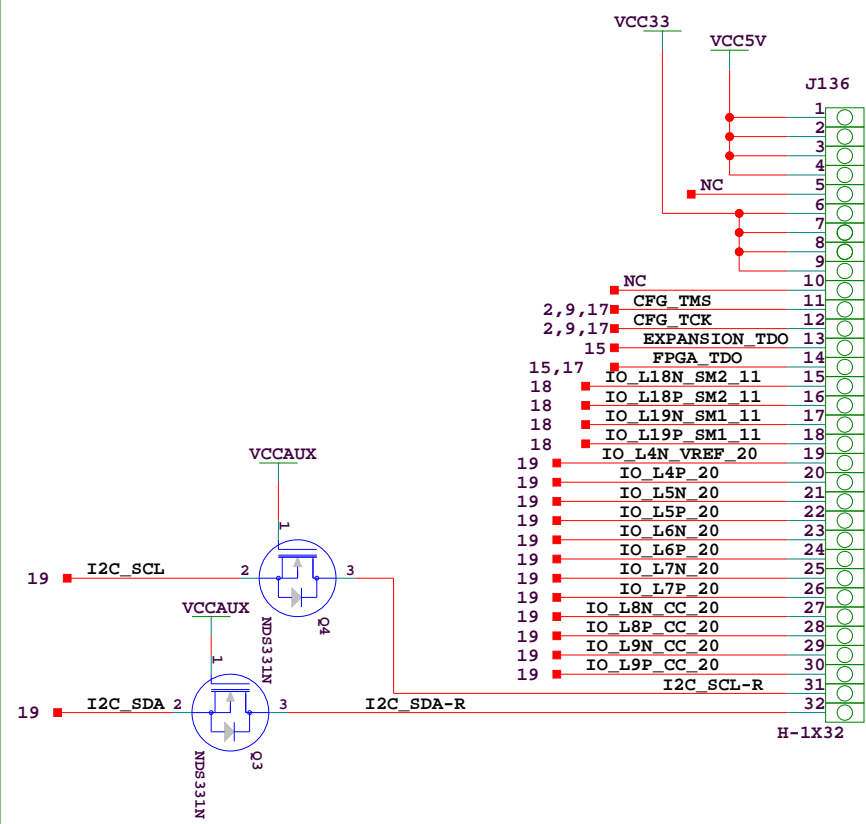
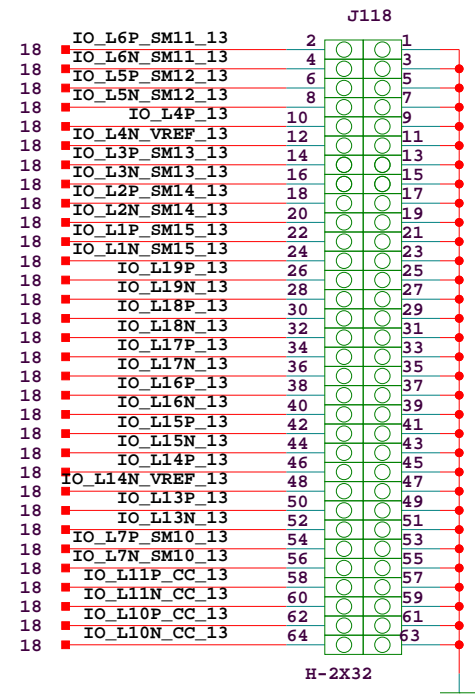
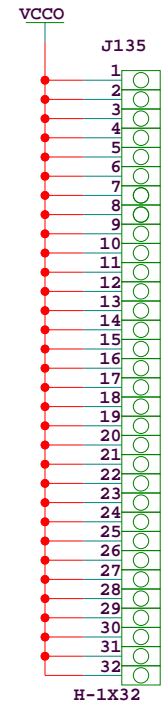
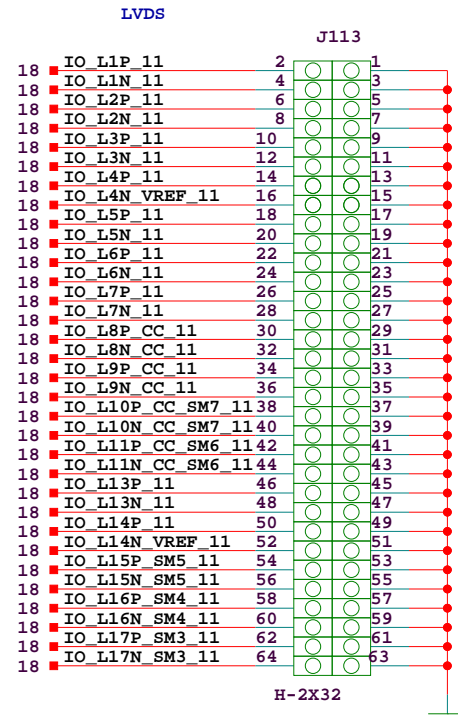
CHECK TO SEE IF CC PINS ARE CAPABLE
 OF DRIVING DIFFERENTIAL CLOCKS




SCH_P/N 0381227
 ART_P/N 0531585
 FAB_P/N 1280397

Title: SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR
DDR2 MEMORY INTERFACE FPGA SIDE

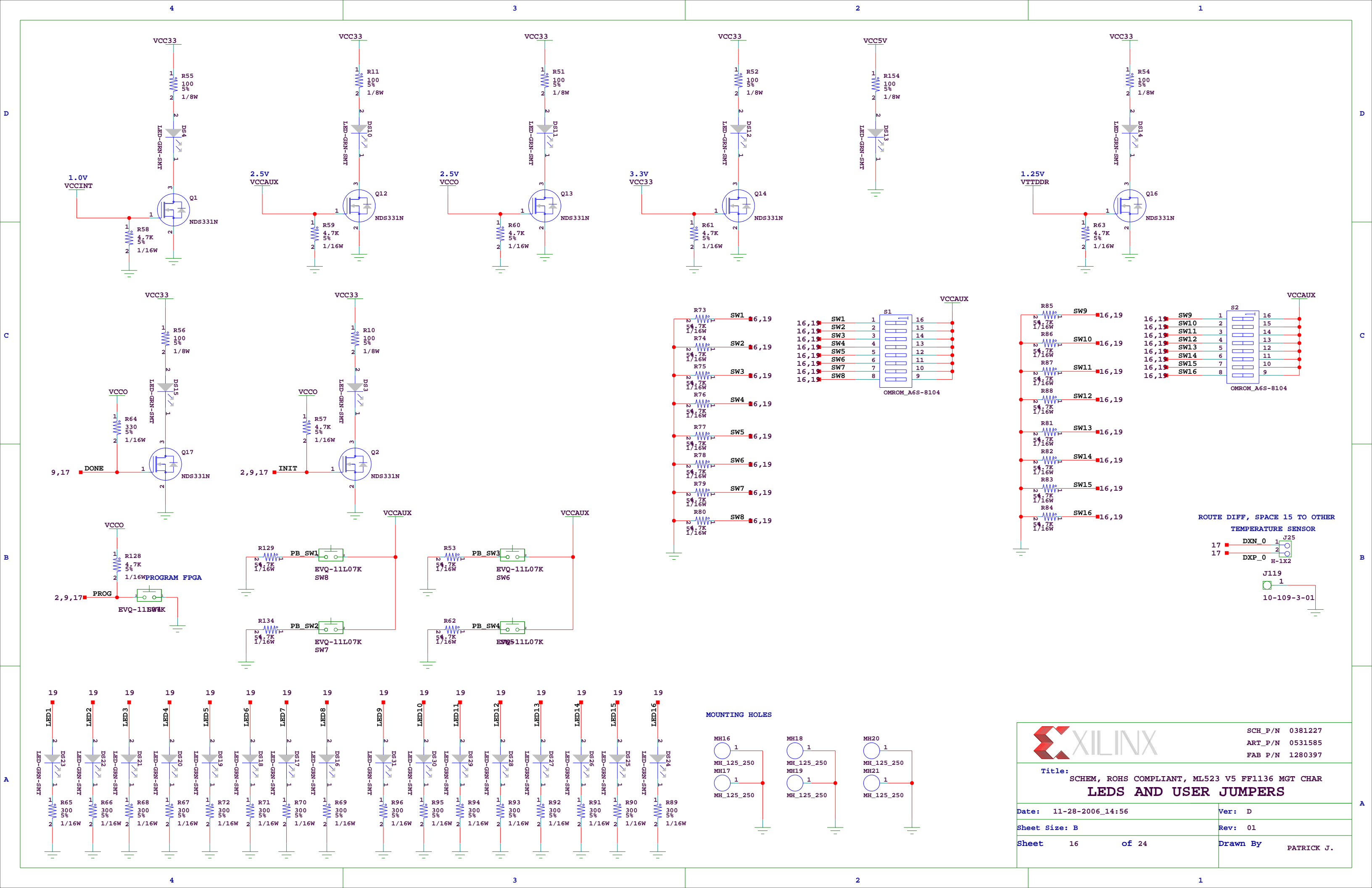
| | |
|------------------------|---------------------|
| Date: 11-28-2006_14:56 | Ver: D |
| Sheet Size: B | Rev: 01 |
| Sheet 14 of 24 | Drawn By PATRICK J. |




 SCH_P/N 0381227
 ART_P/N 0531585
 FAB_P/N 1280397

Title:
 SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR
XGI INTERFACE & GLOBAL CLOCKS

| | |
|-------------------------------|----------------------------|
| Date: 12-22-2006_11:40 | Ver: D |
| Sheet Size: B | Rev: 01 |
| Sheet 15 of 24 | Drawn By PATRICK J. |

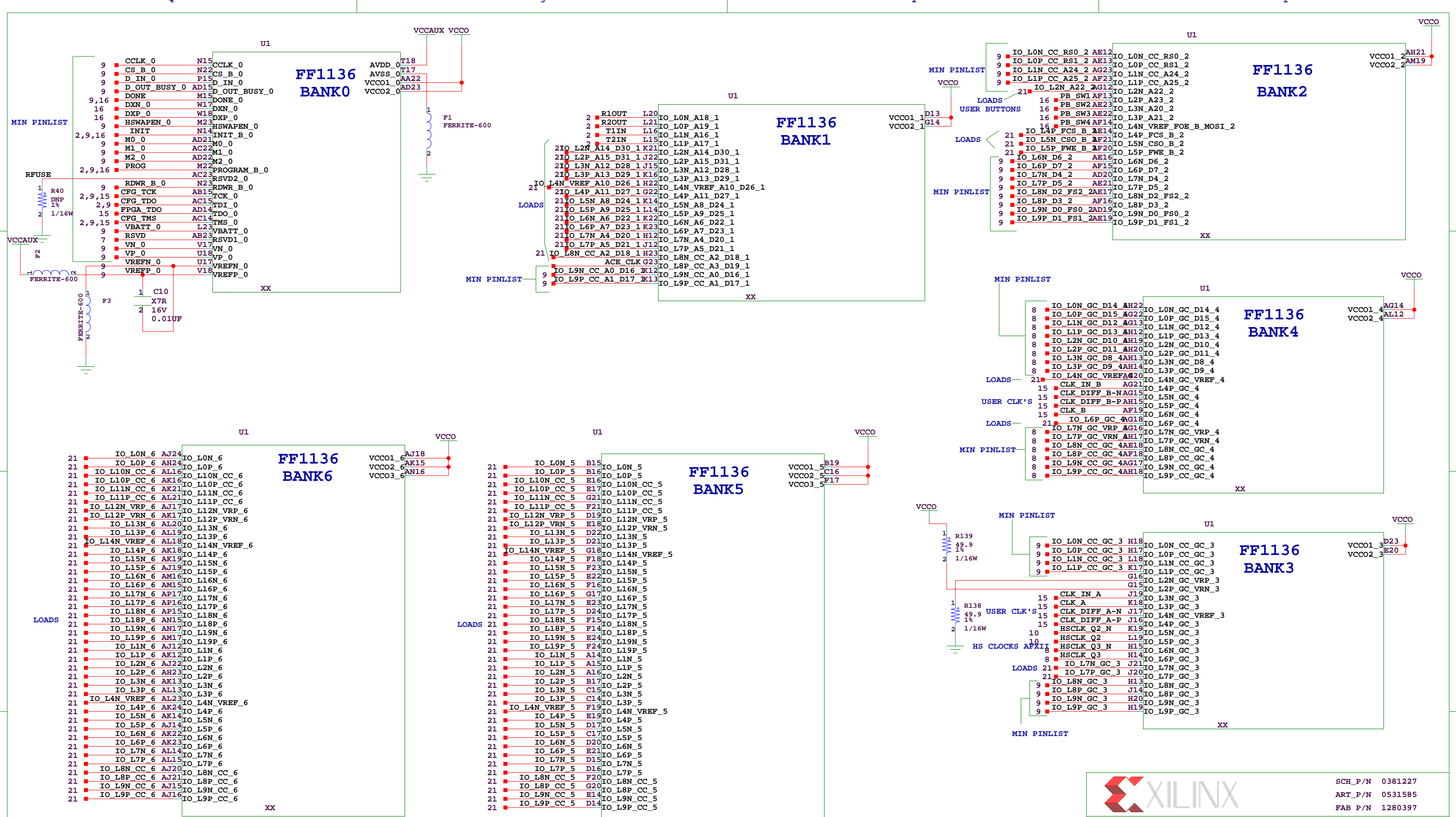



XILINX

SCH_P/N 0381227
 ART_P/N 0531585
 FAB_P/N 1280397

Title: SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR
LEDS AND USER JUMPERS

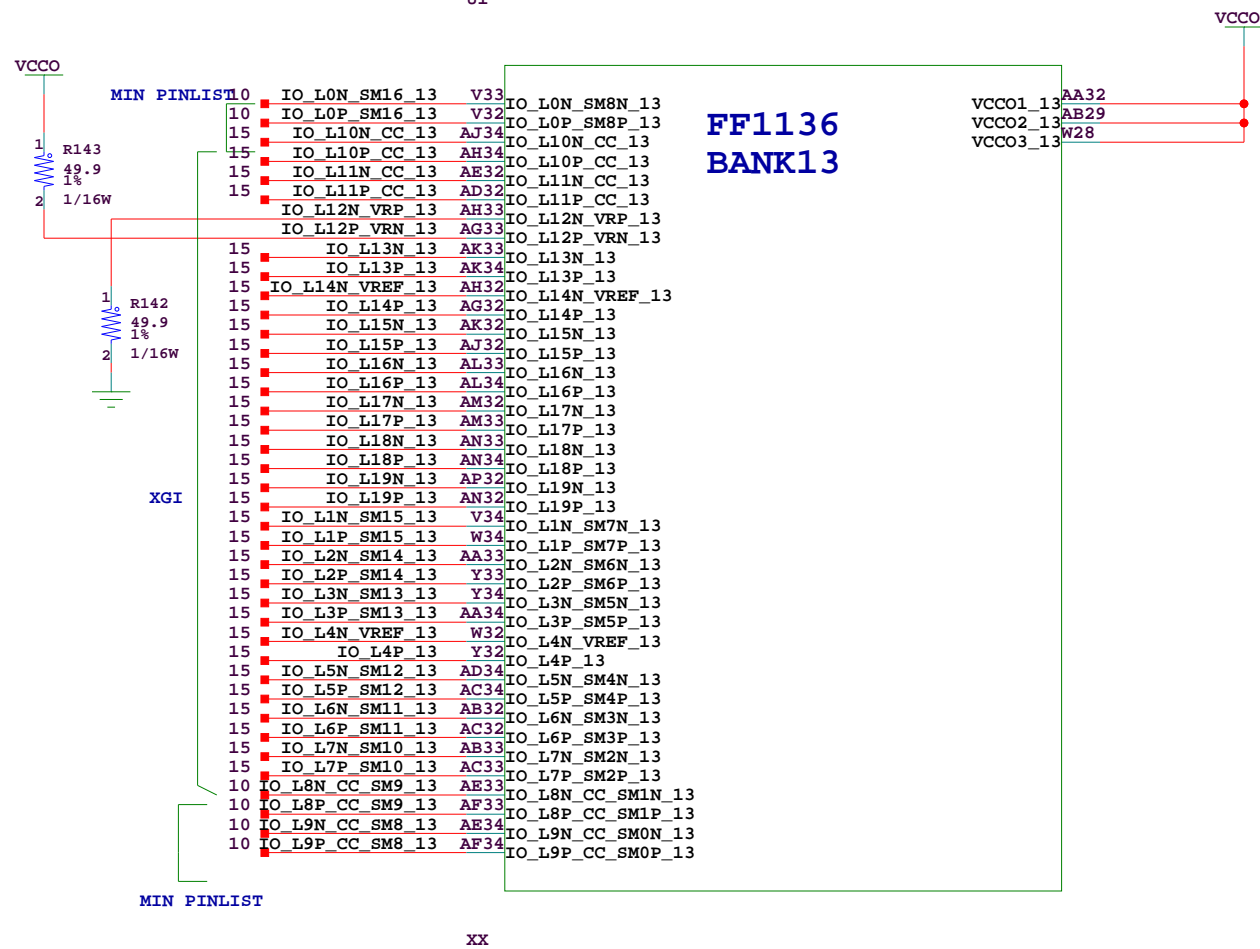
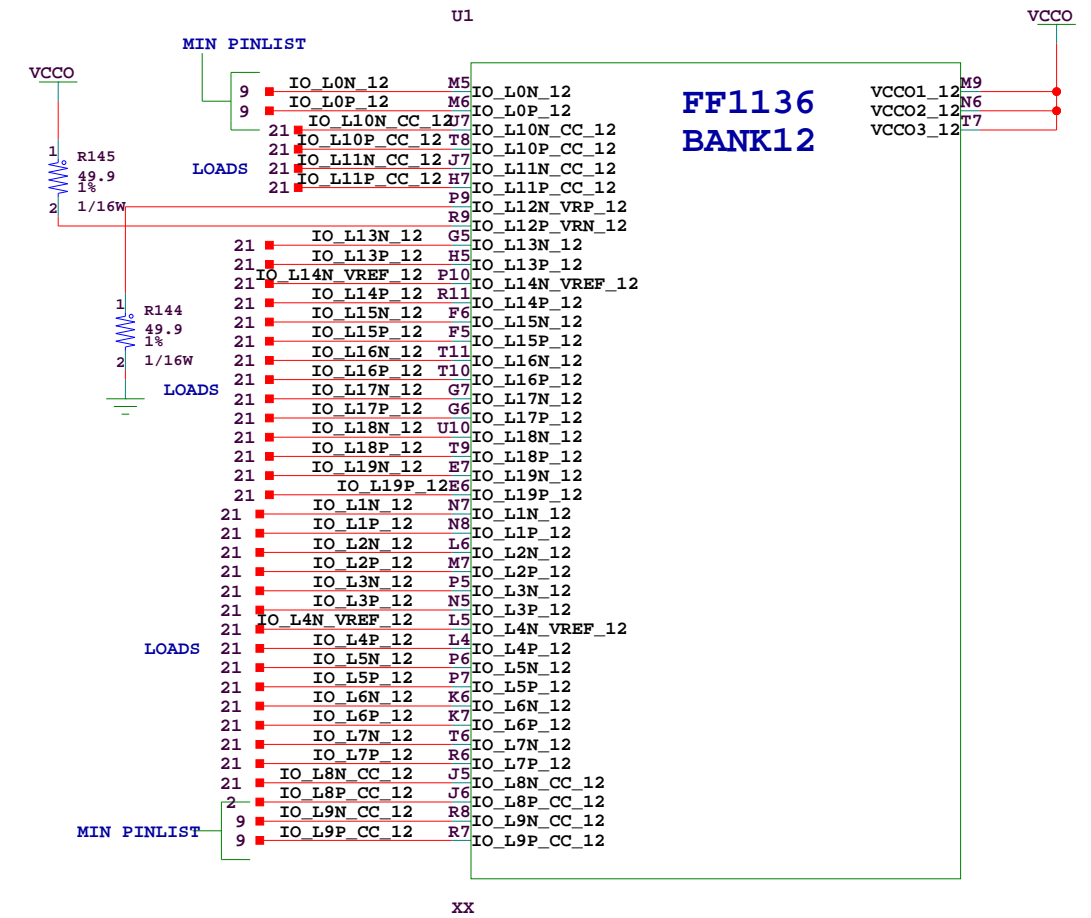
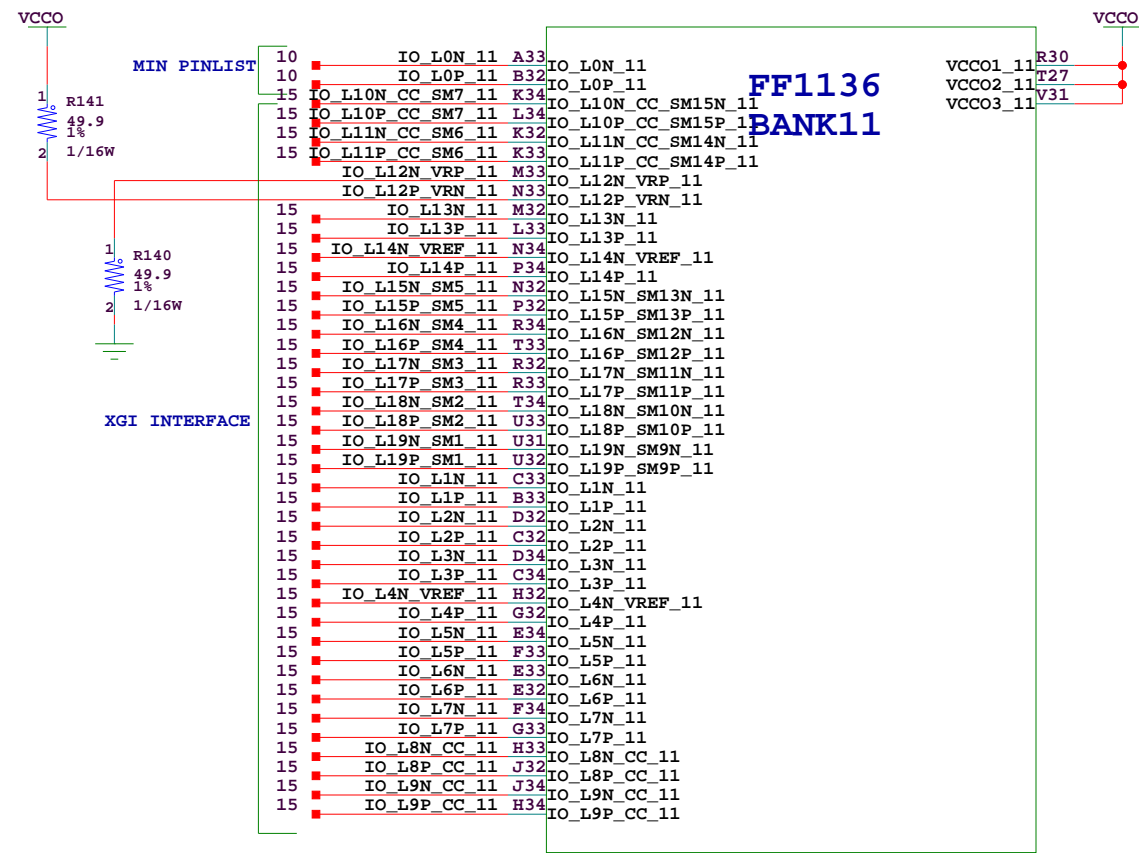
Date: 11-28-2006_14:56 Ver: D
 Sheet Size: B Rev: 01
 Sheet 16 of 24 Drawn By PATRICK J.




 SCH_P/N 0381227
 ART_P/N 0531585
 FAB_P/N 1280397

Title:
 SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR
FPGA_BANKS [0-6]

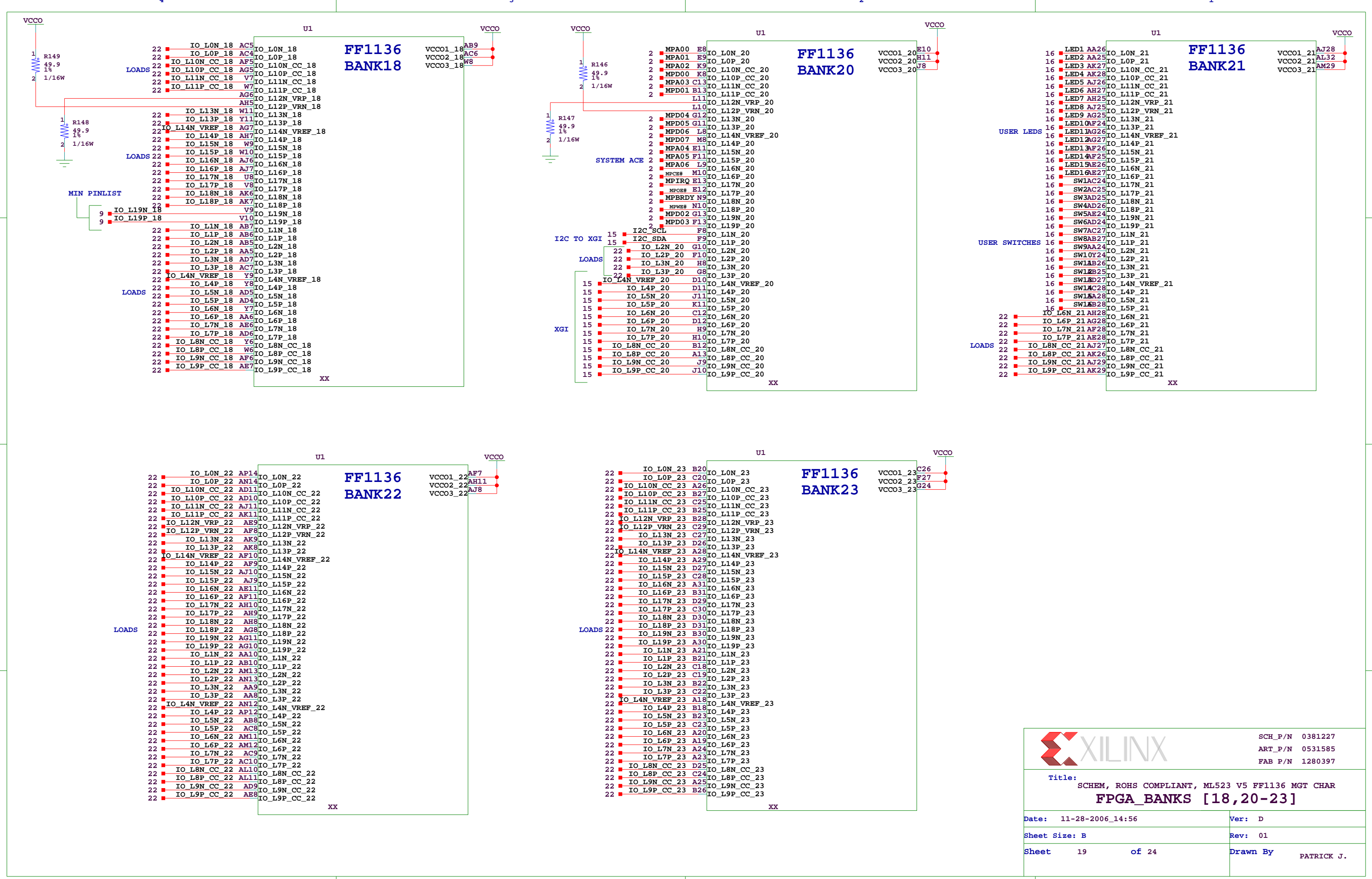
| | |
|-------------------------------|----------------------------|
| Date: 11-28-2006_14:56 | Ver: D |
| Sheet Size: B | Rev: 01 |
| Sheet 17 of 24 | Drawn By PATRICK J. |



SCH_P/N 0381227
 ART_P/N 0531585
 FAB_P/N 1280397

Title: SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR
FPGA_BANKS [11-13]

Date: 11-28-2006_14:56 Ver: D
 Sheet Size: B Rev: 01
 Sheet 18 of 24 Drawn By PATRICK J.

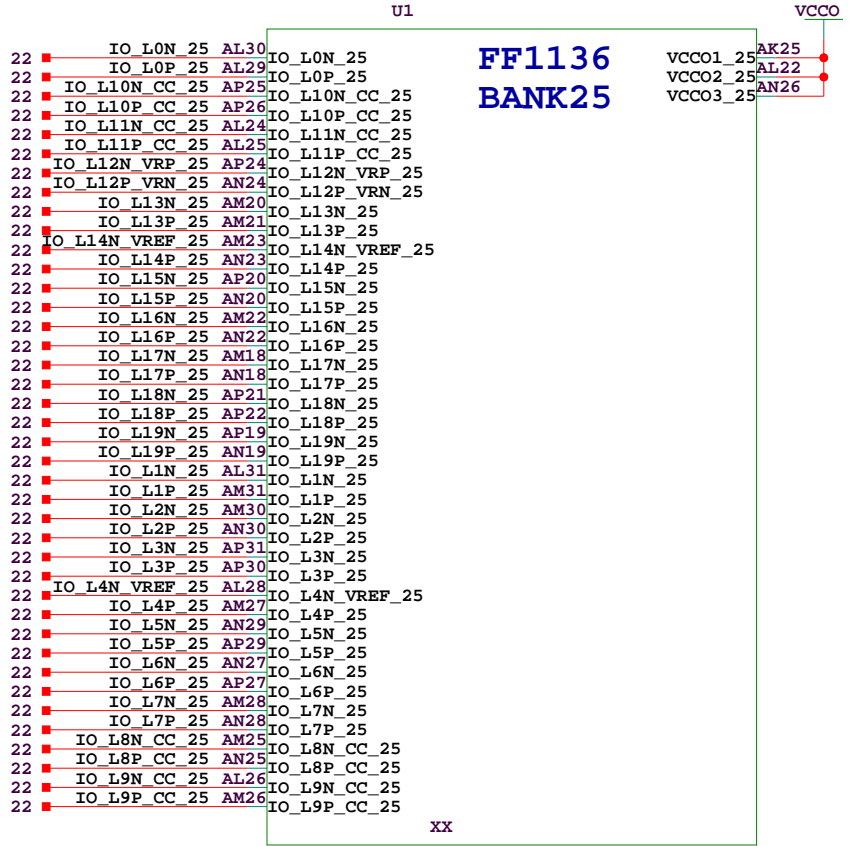


XILINX

SCH_P/N 0381227
 ART_P/N 0531585
 FAB_P/N 1280397

Title: SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR
FPGA_BANKS [18,20-23]

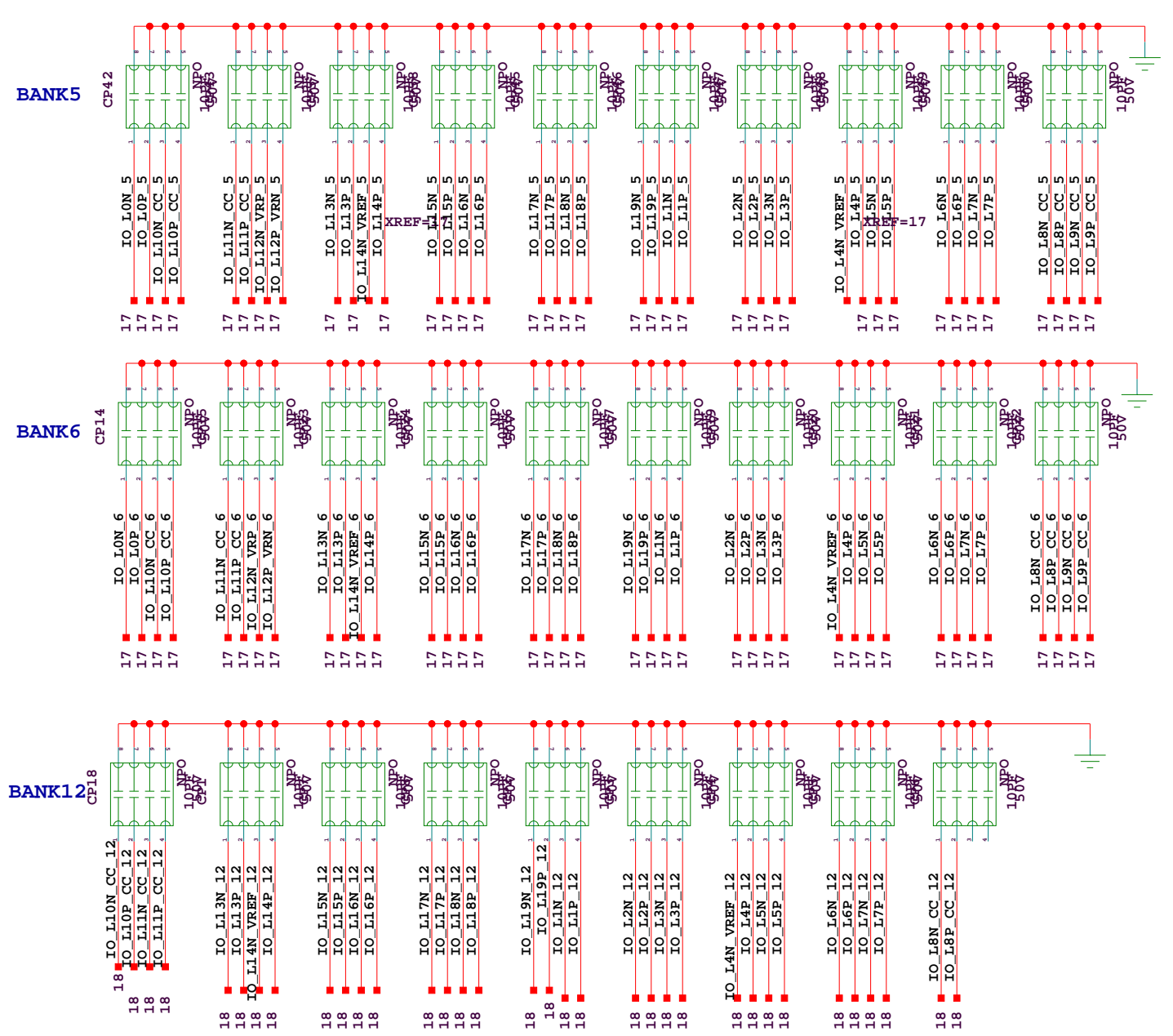
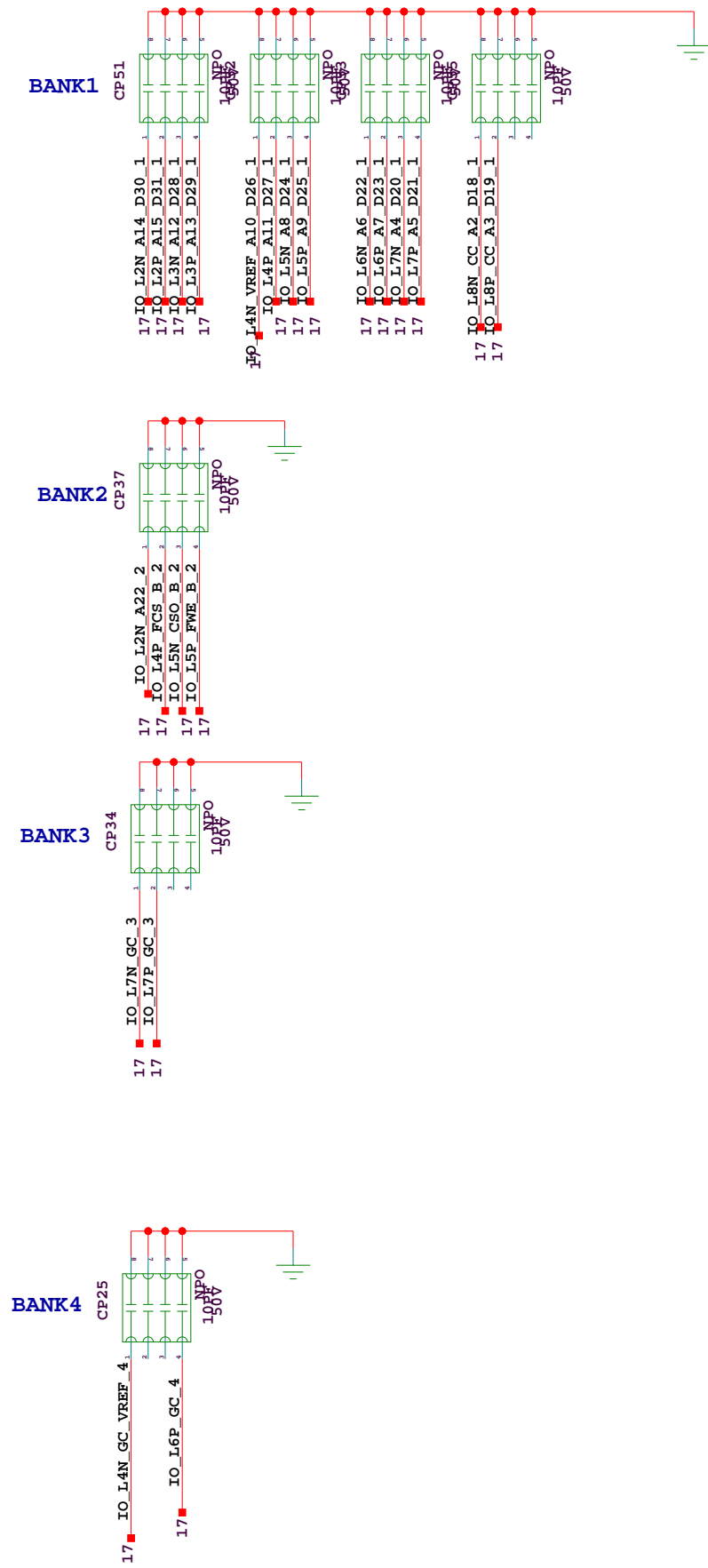
Date: 11-28-2006_14:56 Ver: D
 Sheet Size: B Rev: 01
 Sheet 19 of 24 Drawn By PATRICK J.



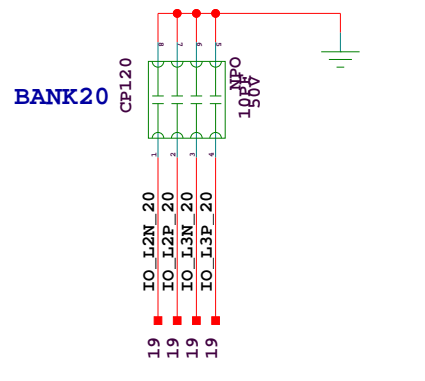
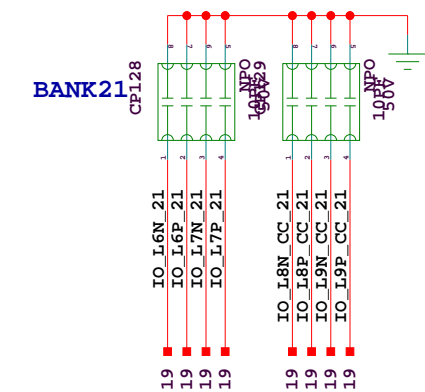
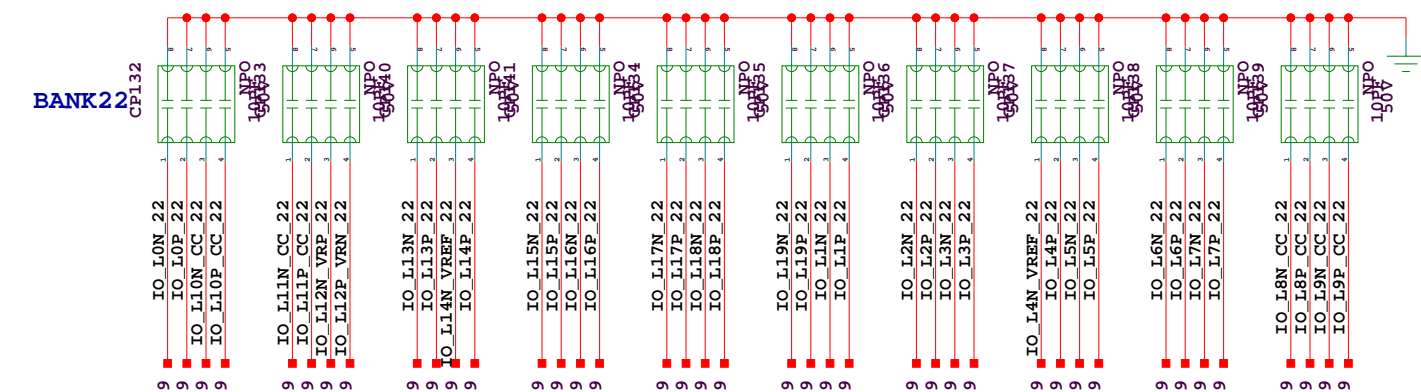
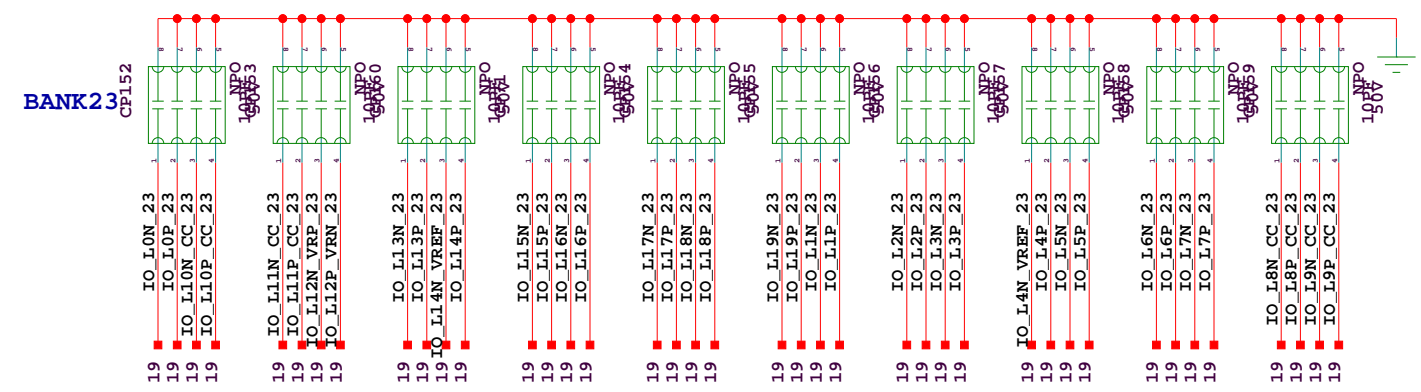
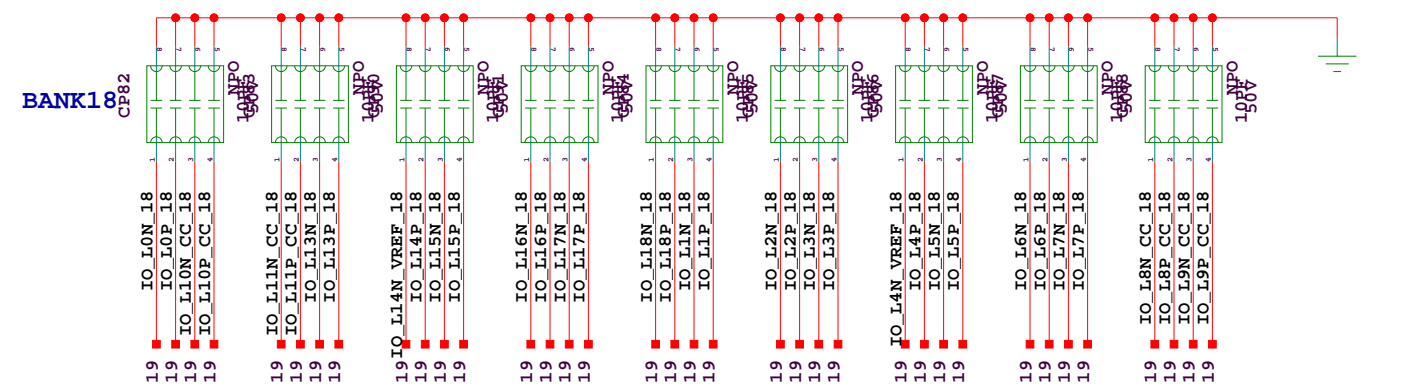
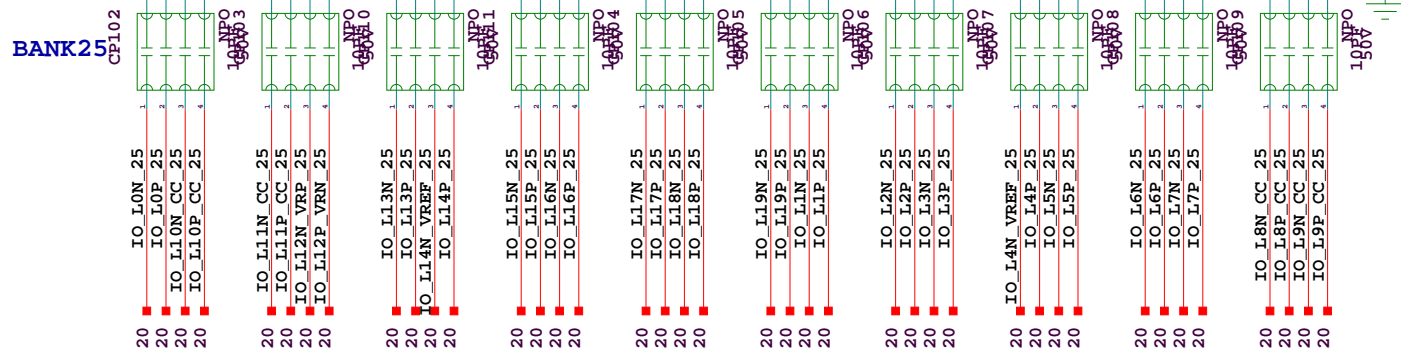
SCH_P/N 0381227
ART_P/N 0531585
FAB P/N 1280397

Title: SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR
FPGA_BANK [25]

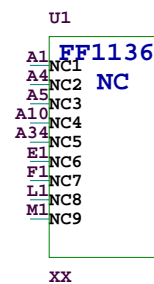
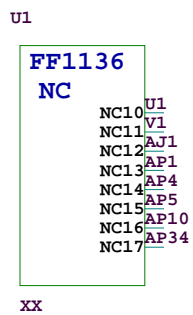
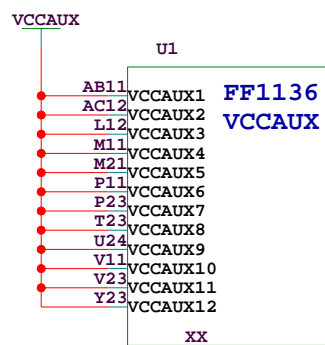
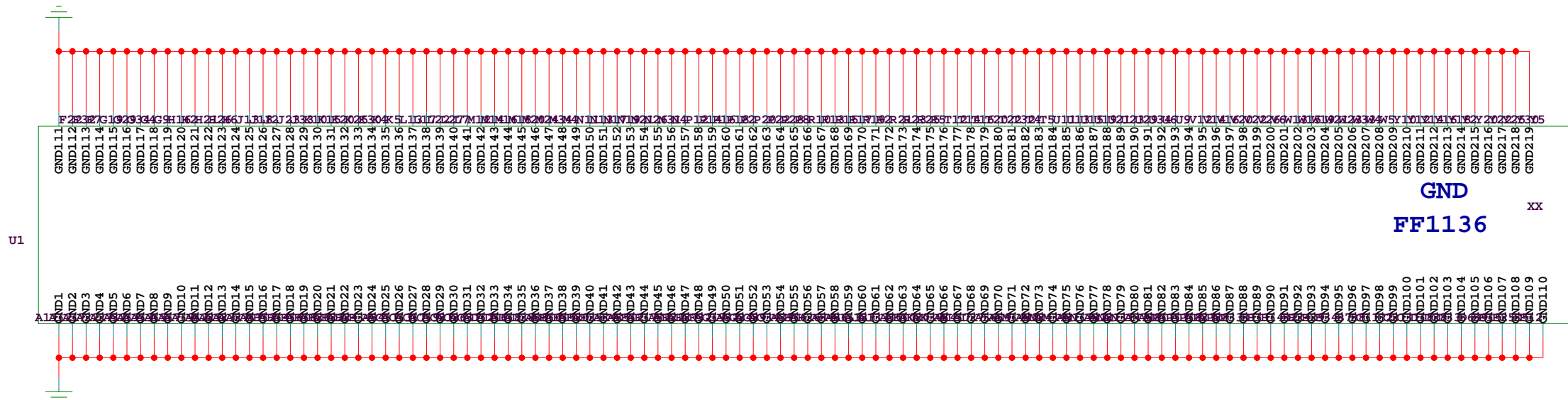
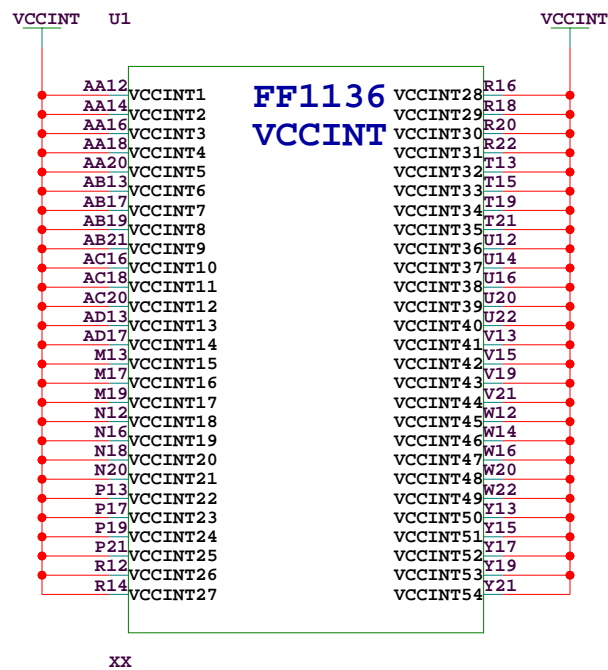
| | |
|------------------------|---------------------|
| Date: 11-28-2006_14:56 | Ver: D |
| Sheet Size: B | Rev: 01 |
| Sheet 20 of 24 | Drawn By PATRICK J. |



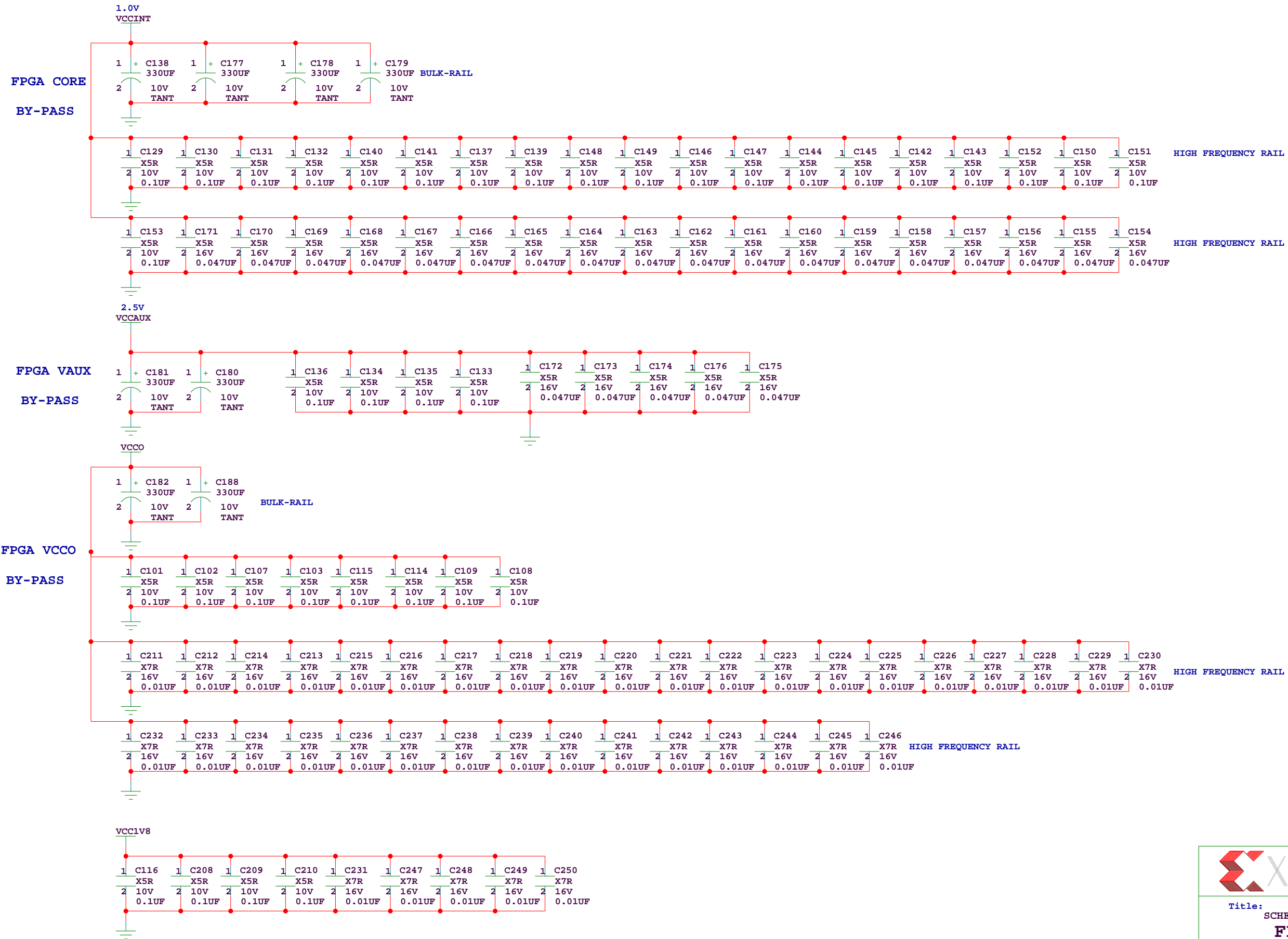
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| | | SCH_P/N 0381227 | |
| | | ART_P/N 0531585 | |
| | | FAB_P/N 1280397 | |
| Title: SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR CAPACITIVE LOADS | | | |
| Date: | 11-28-2006_14:56 | Ver: | D |
| Sheet Size: | B | Rev: | 01 |
| Sheet | 21 of 24 | Drawn By | PATRICK J. |



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| | | SCH_P/N 0381227 |
| | | ART_P/N 0531585 |
| | | FAB_P/N 1280397 |
| Title: SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR | | |
| CAPACITIVE LOADS | | |
| Date: 11-28-2006_14:56 | Ver: D | |
| Sheet Size: B | Rev: 01 | |
| Sheet 22 of 24 | Drawn By | PATRICK J. |



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| | | SCH_P/N 0381227 | |
| | | ART_P/N 0531585 | |
| | | FAB P/N 1280397 | |
| Title: SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR FPGA PWR/GND | | | |
| Date: 11-28-2006_14:56 | | Ver: D | |
| Sheet Size: B | | Rev: 01 | |
| Sheet 23 | of 24 | Drawn By | PATRICK J. |



SCH_P/N 0381227
 ART_P/N 0531585
 FAB_P/N 1280397

Title: SCHEM, ROHS COMPLIANT, ML523 V5 FF1136 MGT CHAR
FPGA_DECOUPLING NETWORK

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| Date: 11-28-2006_14:56 | Ver: D |
| Sheet Size: B | Rev: 01 |
| Sheet 24 of 24 | Drawn By PATRICK J. |