

Spartan-3A DSP Starter Board

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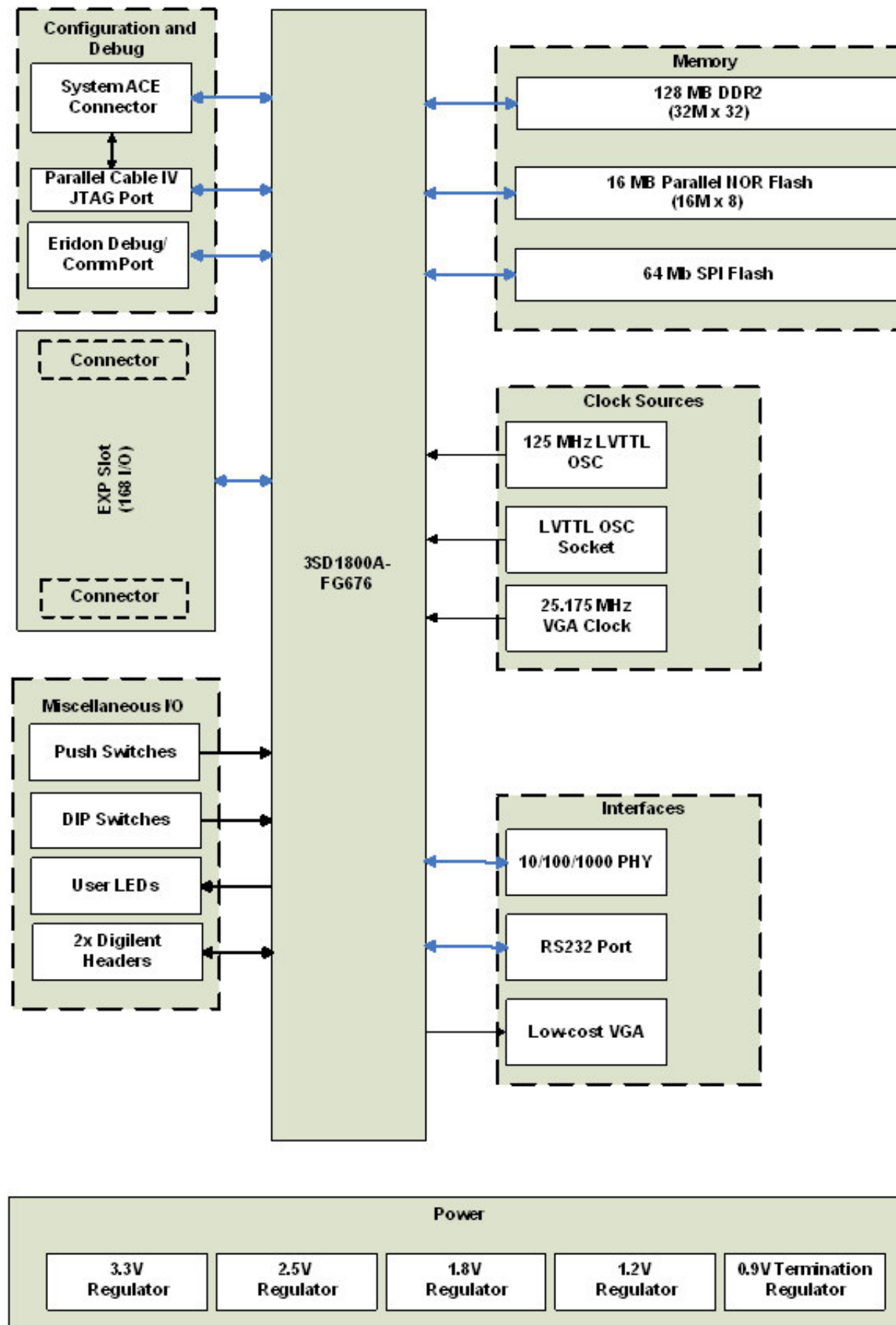
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07/11/08

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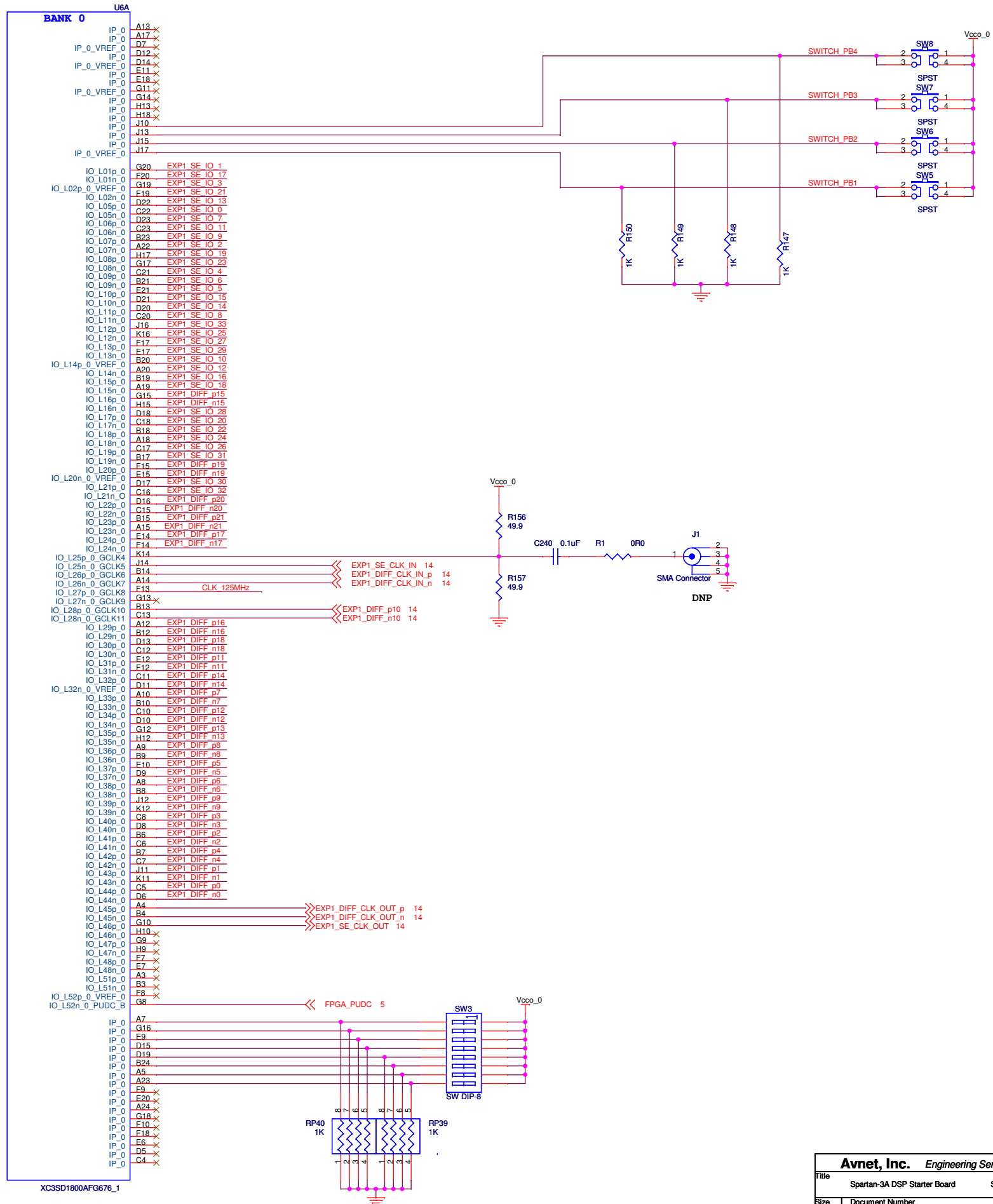
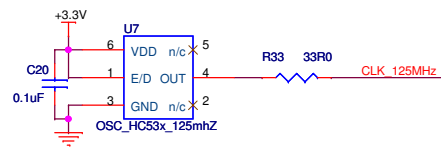


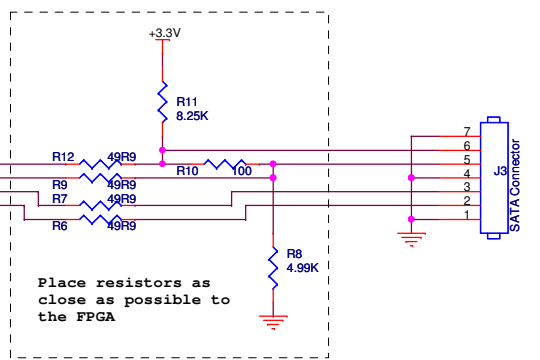
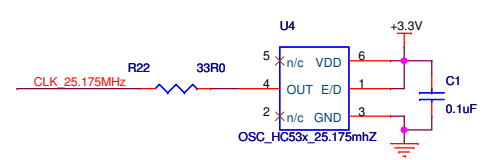
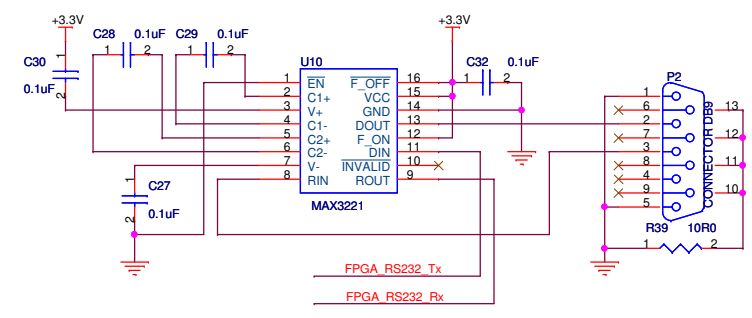
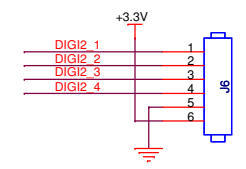
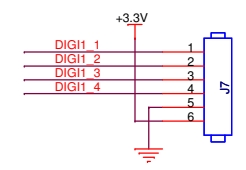
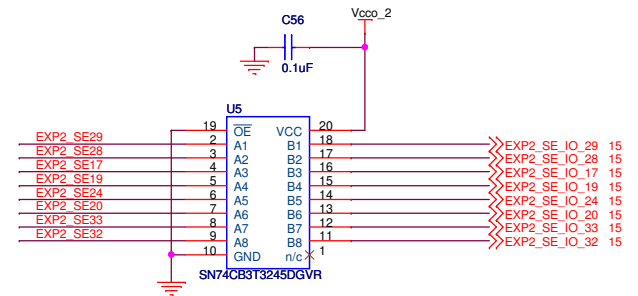
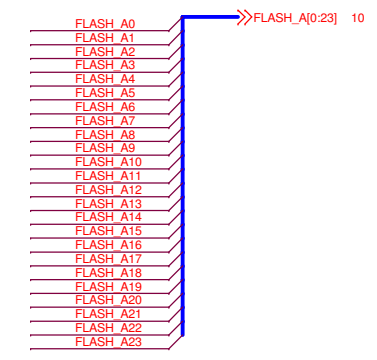
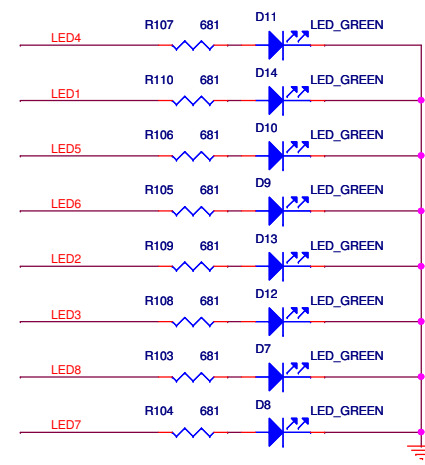
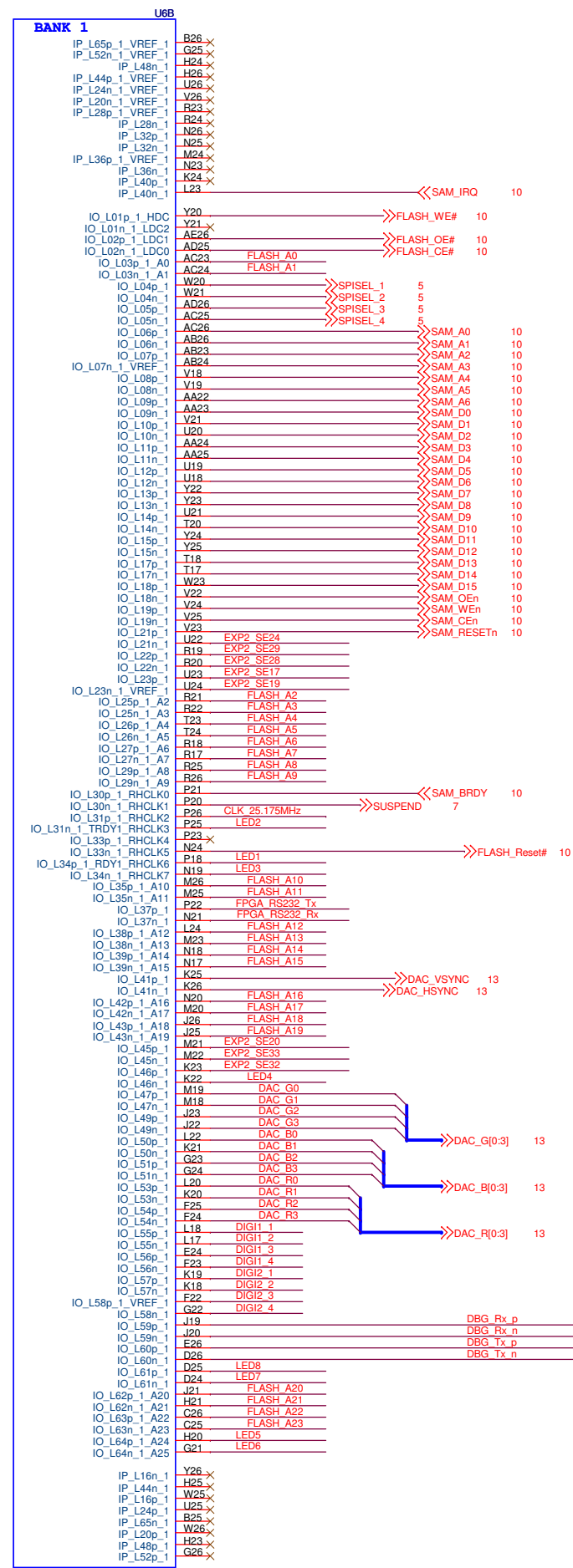
4,5,15 EXP2_SE_IO_[0:33] << EXP2_SE_IO_33

14 EXP1_SE_IO_[0:33] << EXP1_SE_IO_0
EXP1_SE_IO_1
EXP1_SE_IO_2
EXP1_SE_IO_3
EXP1_SE_IO_4
EXP1_SE_IO_5
EXP1_SE_IO_6
EXP1_SE_IO_7
EXP1_SE_IO_8
EXP1_SE_IO_9
EXP1_SE_IO_10
EXP1_SE_IO_11
EXP1_SE_IO_12
EXP1_SE_IO_13
EXP1_SE_IO_14
EXP1_SE_IO_15
EXP1_SE_IO_16
EXP1_SE_IO_17
EXP1_SE_IO_18
EXP1_SE_IO_19
EXP1_SE_IO_20
EXP1_SE_IO_21
EXP1_SE_IO_22
EXP1_SE_IO_23
EXP1_SE_IO_24
EXP1_SE_IO_25
EXP1_SE_IO_26
EXP1_SE_IO_27
EXP1_SE_IO_28
EXP1_SE_IO_29
EXP1_SE_IO_30
EXP1_SE_IO_31
EXP1_SE_IO_32
EXP1_SE_IO_33

14 EXP1_DIFF_p[0:21] << EXP1_DIFF_p0
EXP1_DIFF_p1
EXP1_DIFF_p2
EXP1_DIFF_p3
EXP1_DIFF_p4
EXP1_DIFF_p5
EXP1_DIFF_p6
EXP1_DIFF_p7
EXP1_DIFF_p8
EXP1_DIFF_p9
EXP1_DIFF_p11
EXP1_DIFF_p12
EXP1_DIFF_p13
EXP1_DIFF_p14
EXP1_DIFF_p15
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EXP1_DIFF_p19
EXP1_DIFF_p20
EXP1_DIFF_p21

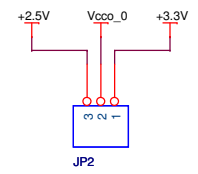
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EXP1_DIFF_n1
EXP1_DIFF_n2
EXP1_DIFF_n3
EXP1_DIFF_n4
EXP1_DIFF_n5
EXP1_DIFF_n6
EXP1_DIFF_n7
EXP1_DIFF_n8
EXP1_DIFF_n9
EXP1_DIFF_n11
EXP1_DIFF_n12
EXP1_DIFF_n13
EXP1_DIFF_n14
EXP1_DIFF_n15
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EXP1_DIFF_n20
EXP1_DIFF_n21





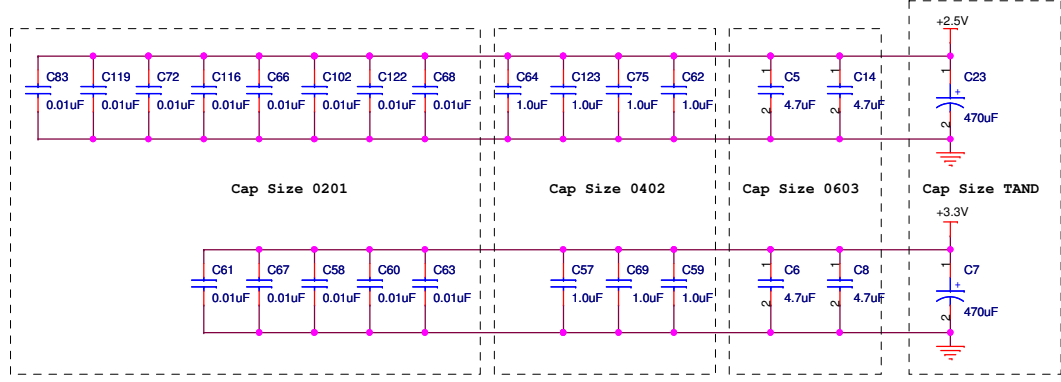
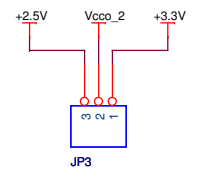
XC3SD1800AFG676_1

EXP1 VOLTAGE SELECT

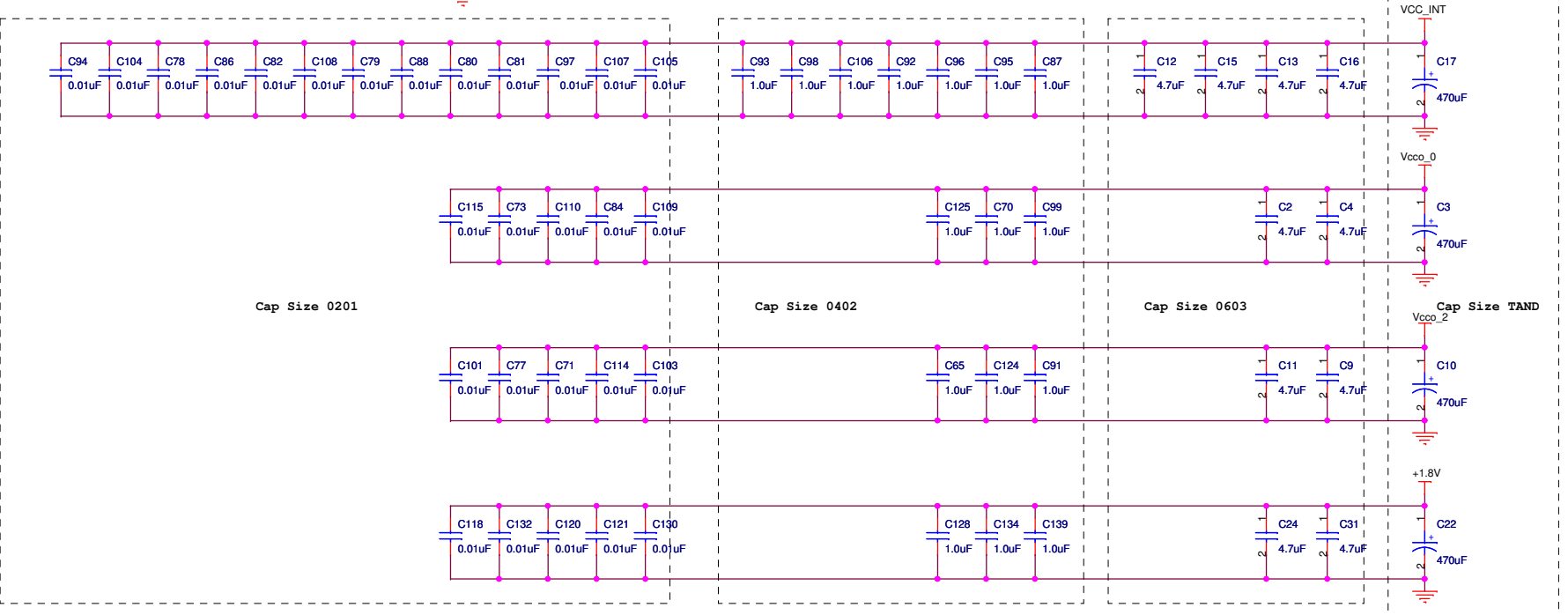
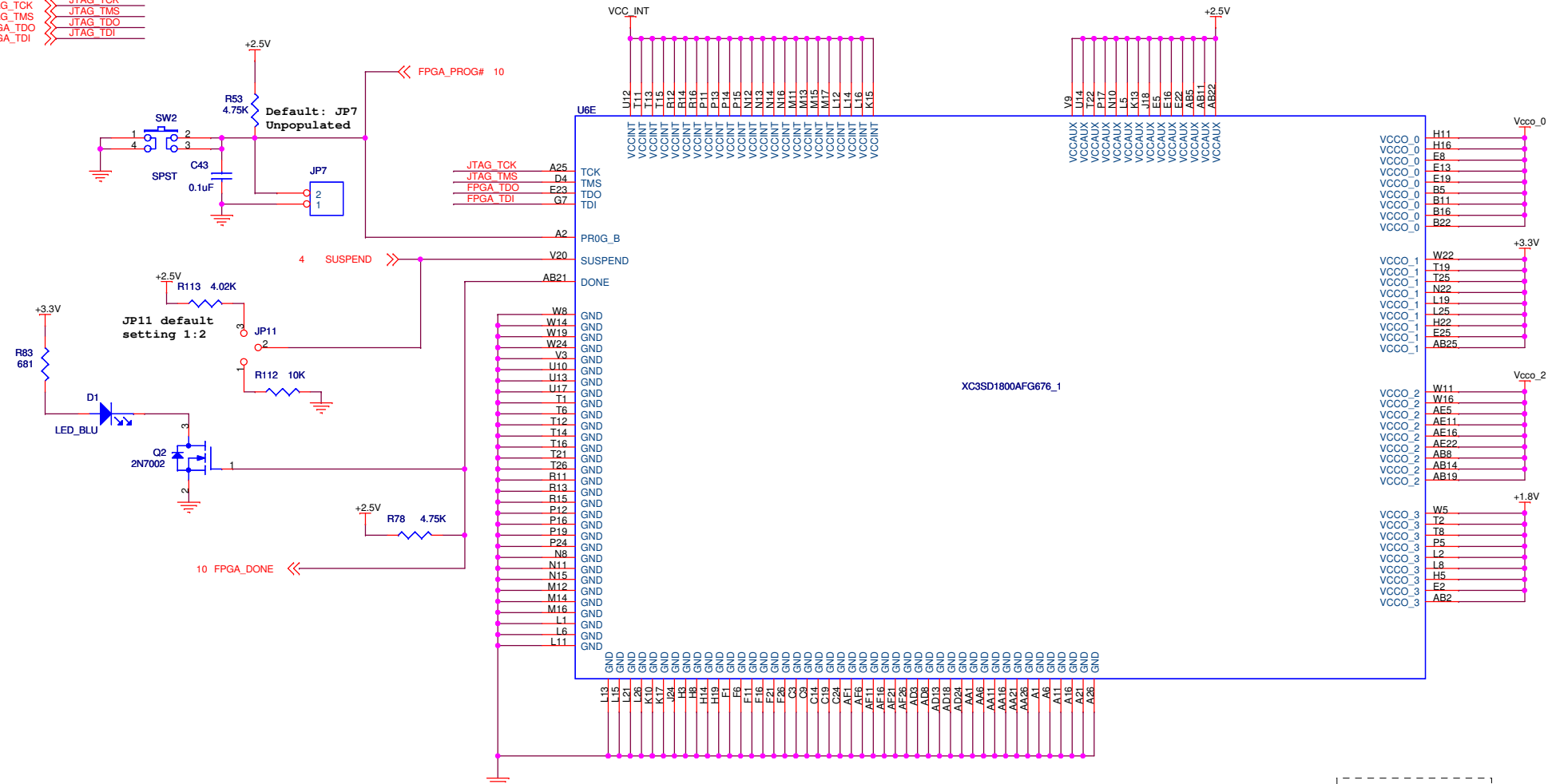


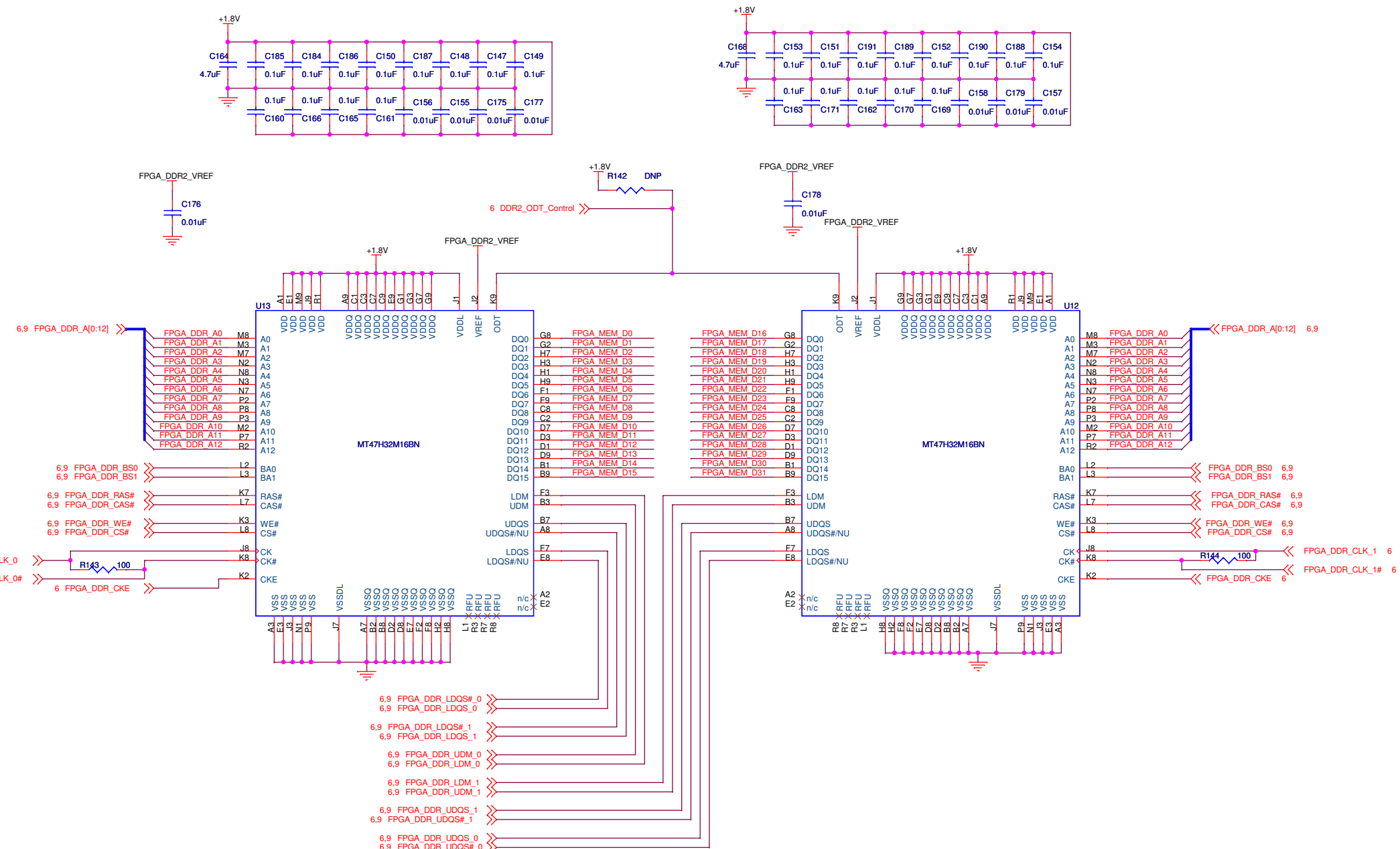
Default: JP2 1:2 (VCCO_0 = +3.3V)
 Default: JP3 1:2 (VCCO_2 = +3.3V)

EXP2 VOLTAGE SELECT

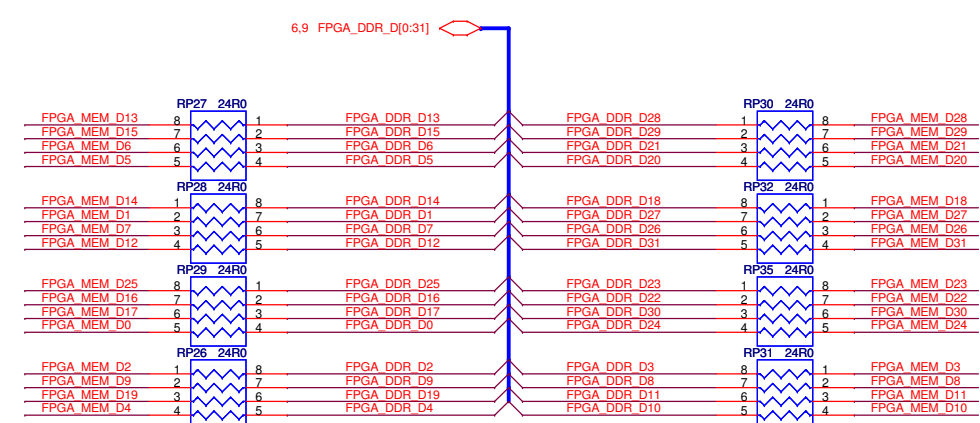


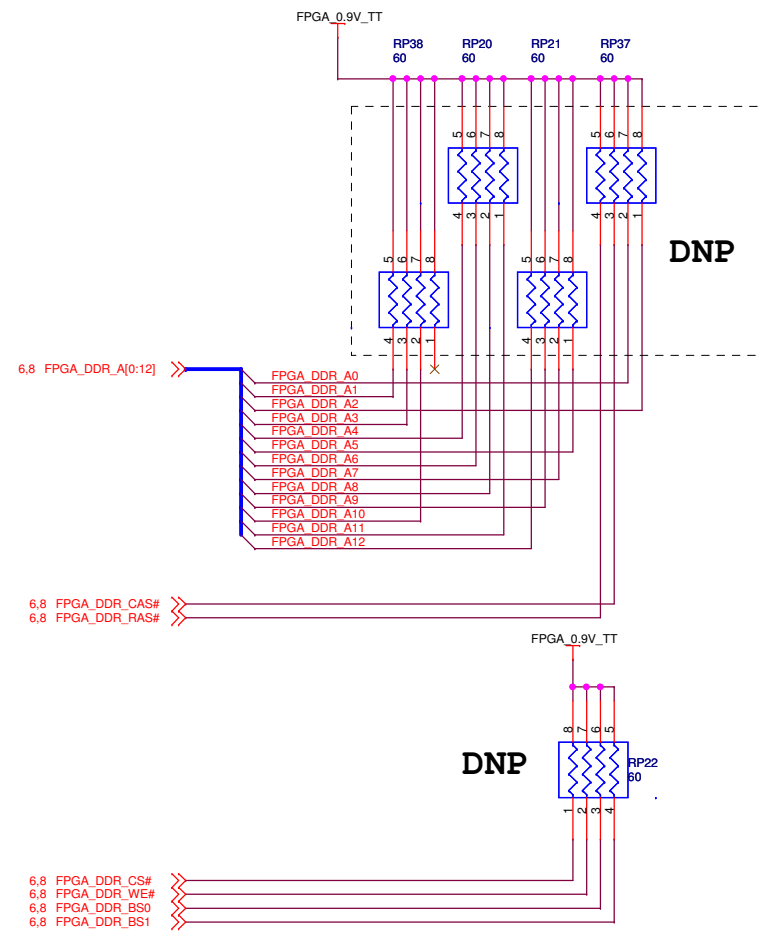
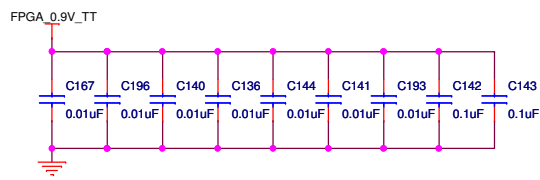
- 10 JTAG_TCK
- 10 JTAG_TMS
- 10 JTAG_TDO
- 10 JTAG_TDI



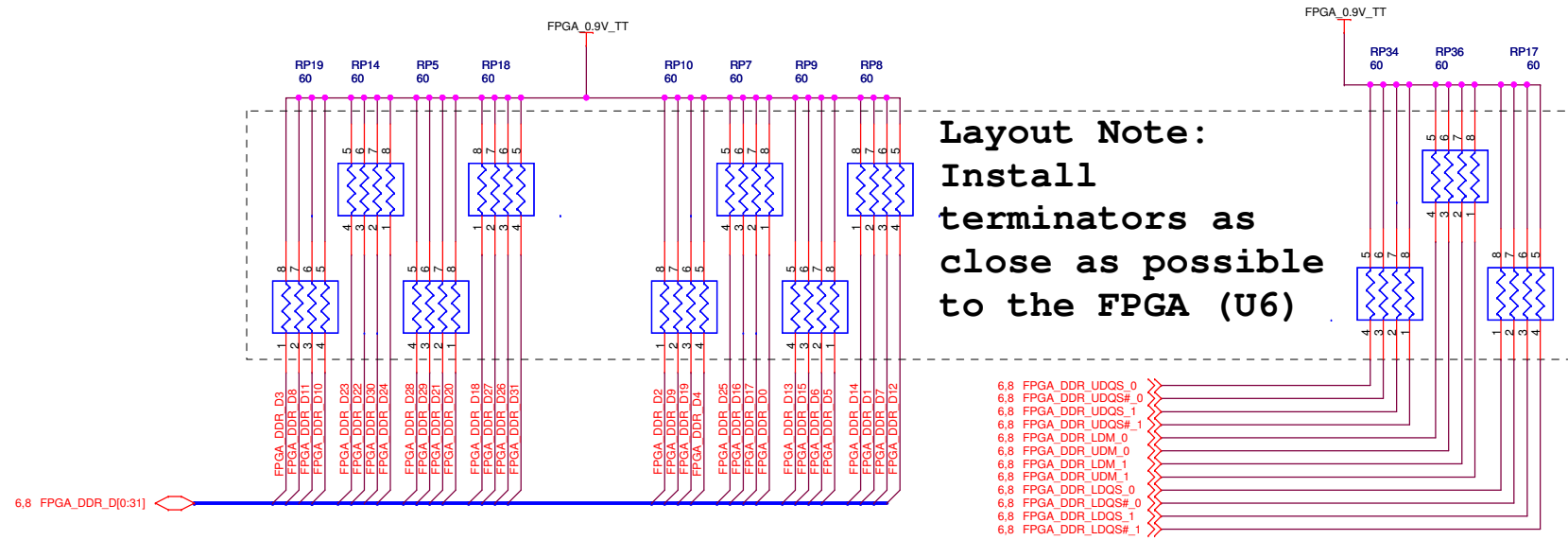
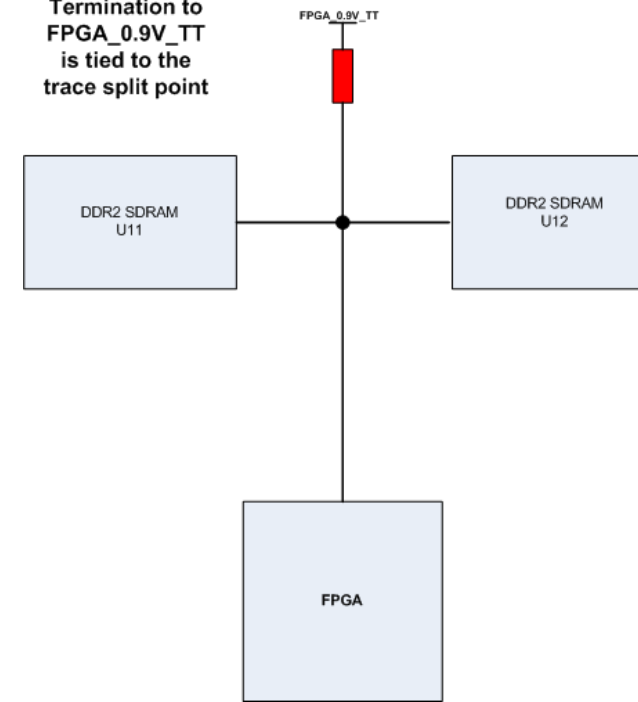


Place series terminations close to FPGA

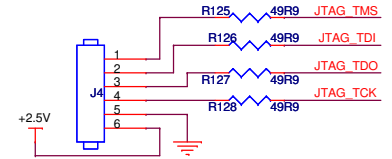
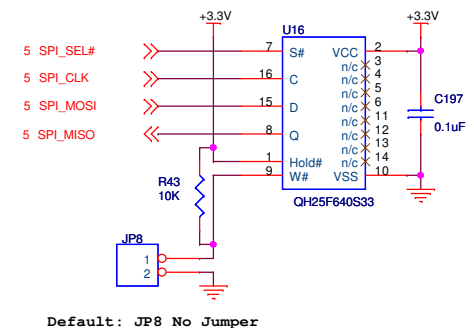
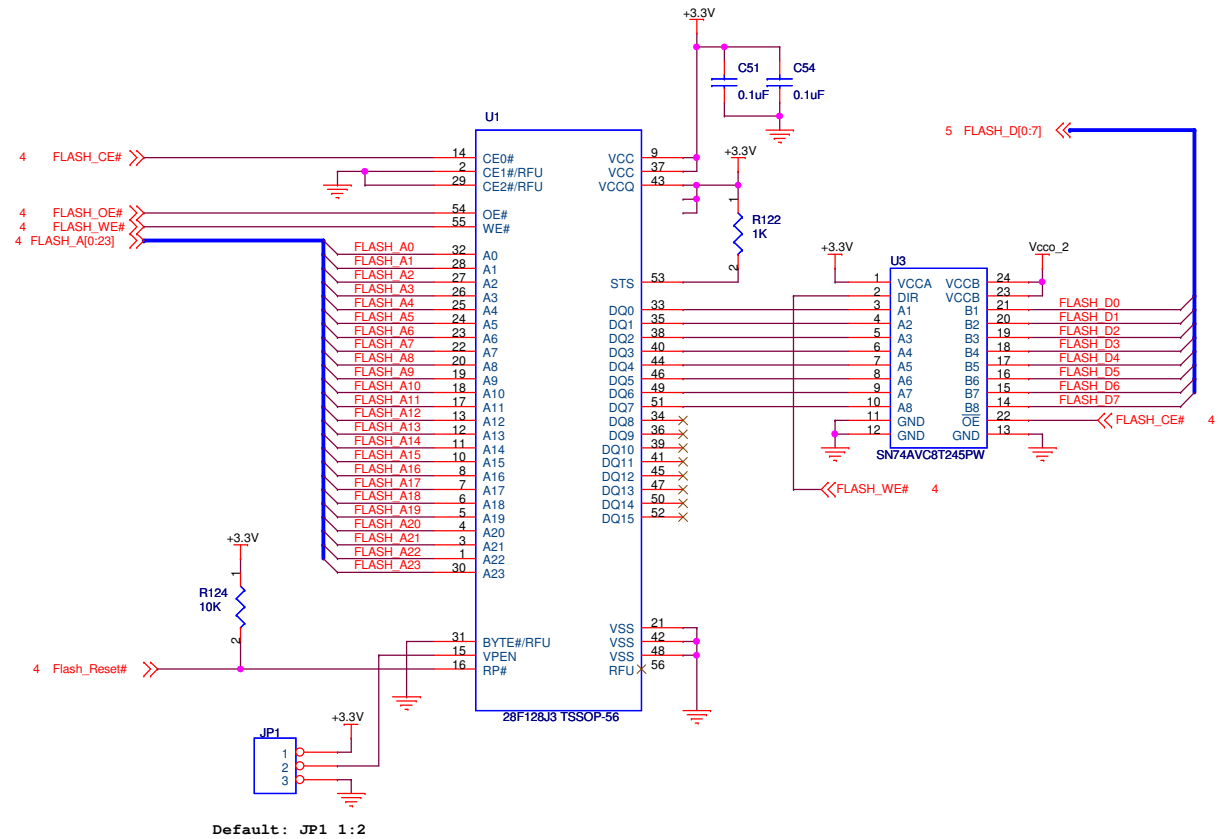




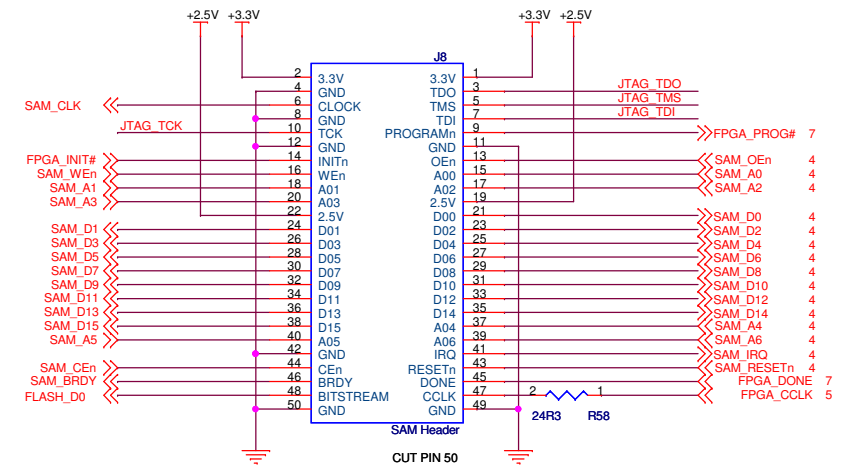
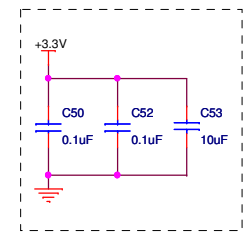
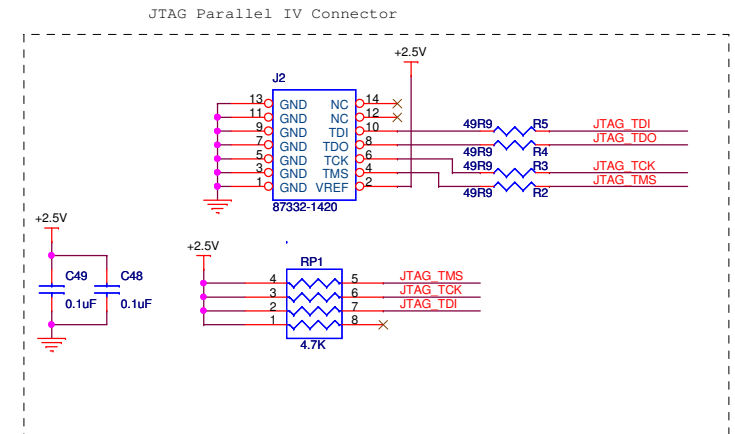
NOTE:
Termination to
FPGA_0.9V_TT
is tied to the
trace split point

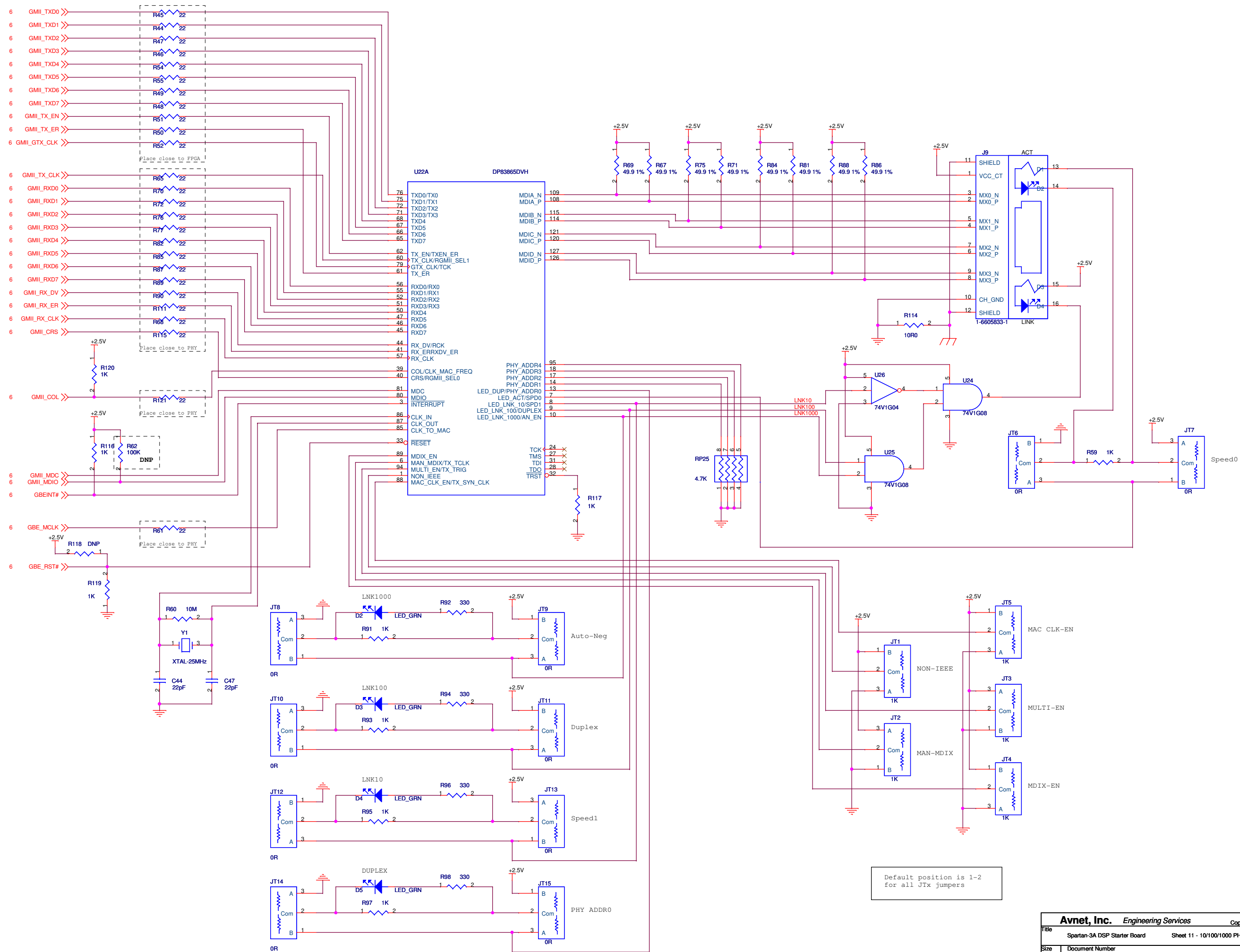


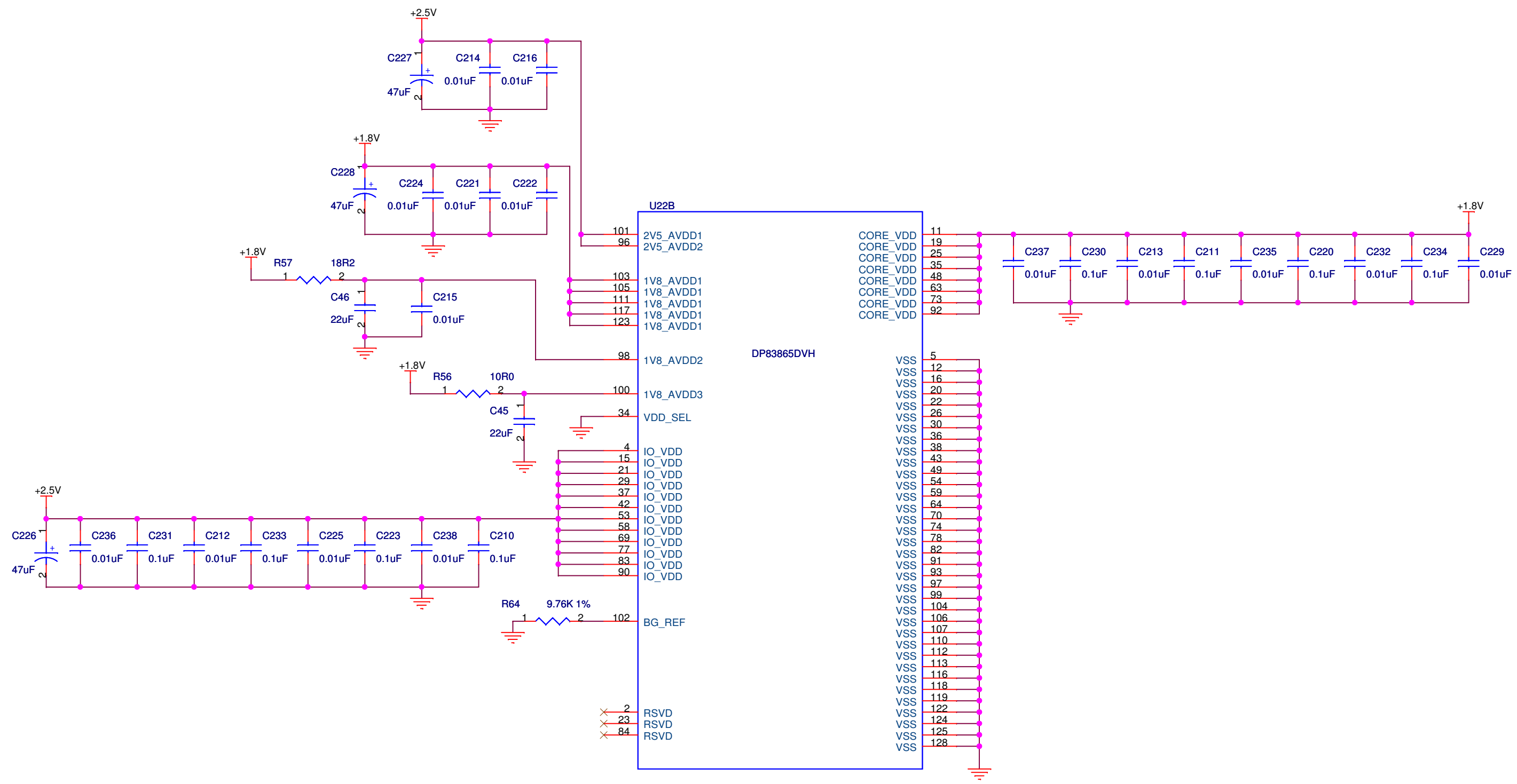
Layout Note:
Install
terminators as
close as possible
to the FPGA (U6)

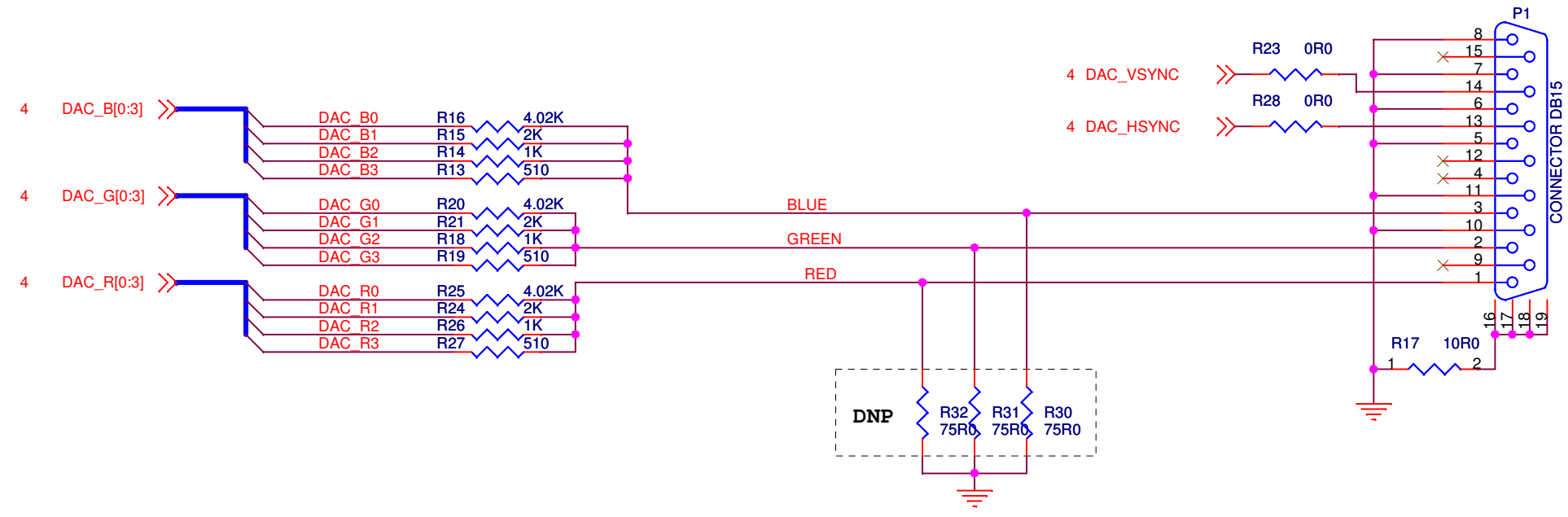


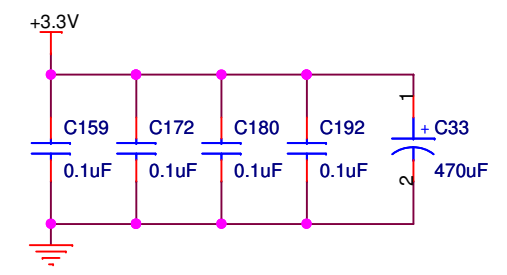
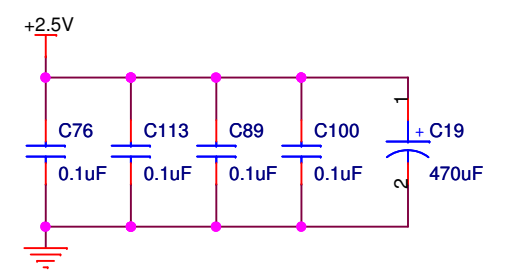
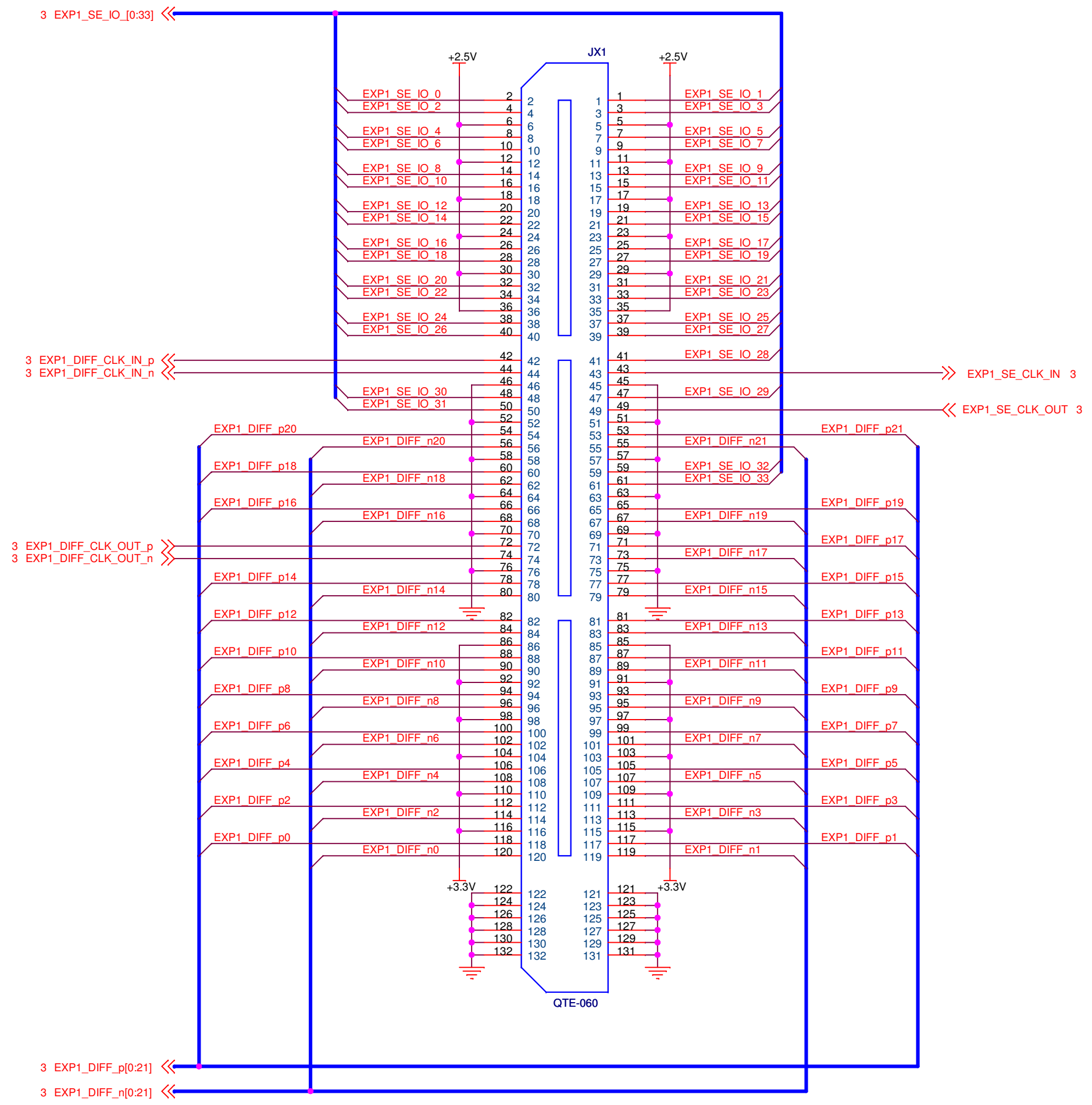
Layout Note: Place J4 and J2 close together











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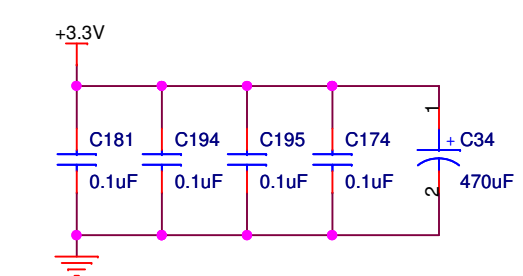
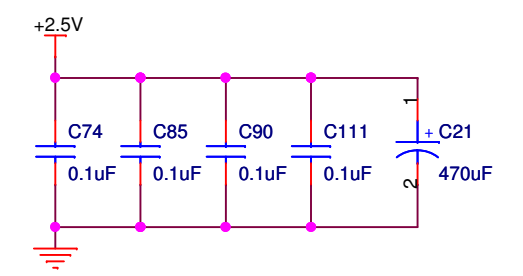
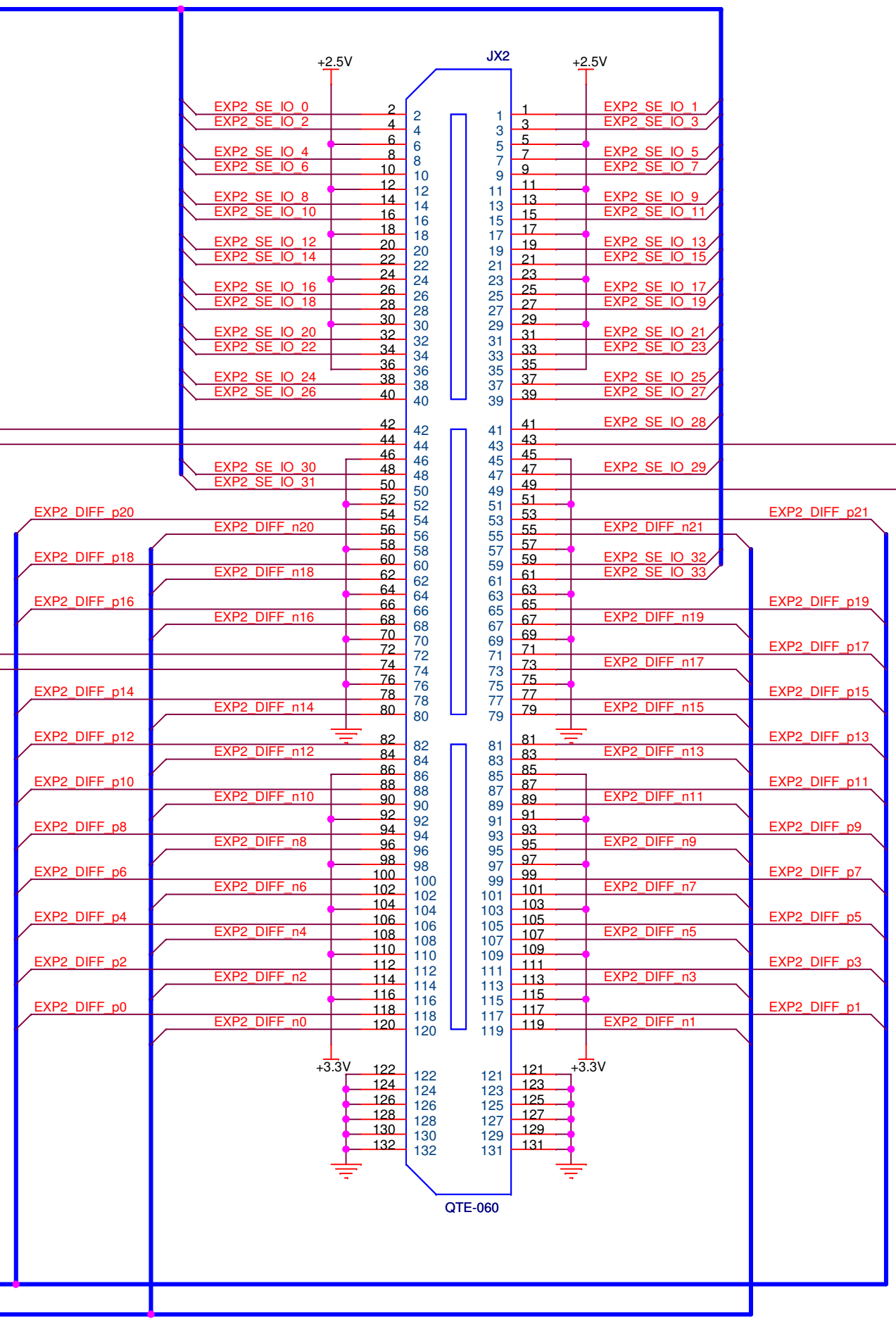
4,5 EXP2_SE_IO_[0:33] <<<

5 EXP2_DIFF_CLK_IN_p <<<
5 EXP2_DIFF_CLK_IN_n <<<

5 EXP2_DIFF_CLK_OUT_p >>>
5 EXP2_DIFF_CLK_OUT_n >>>

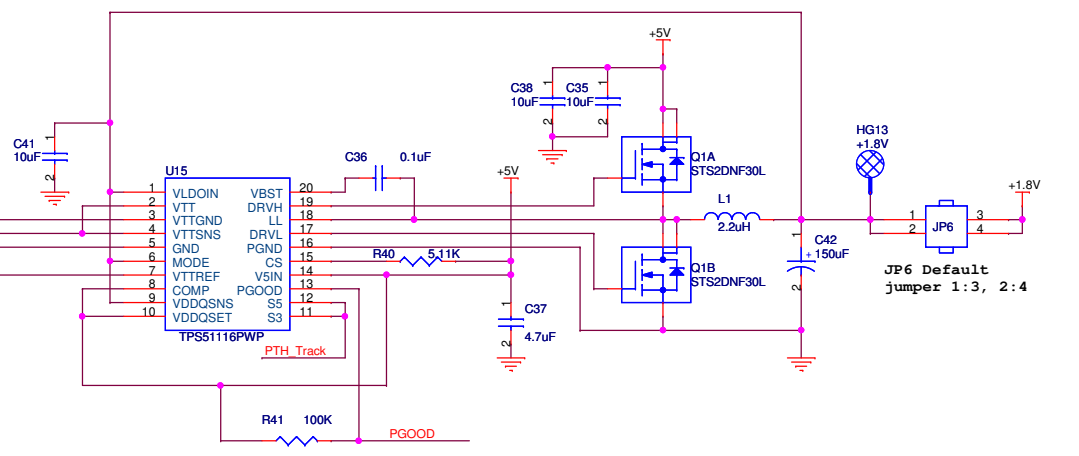
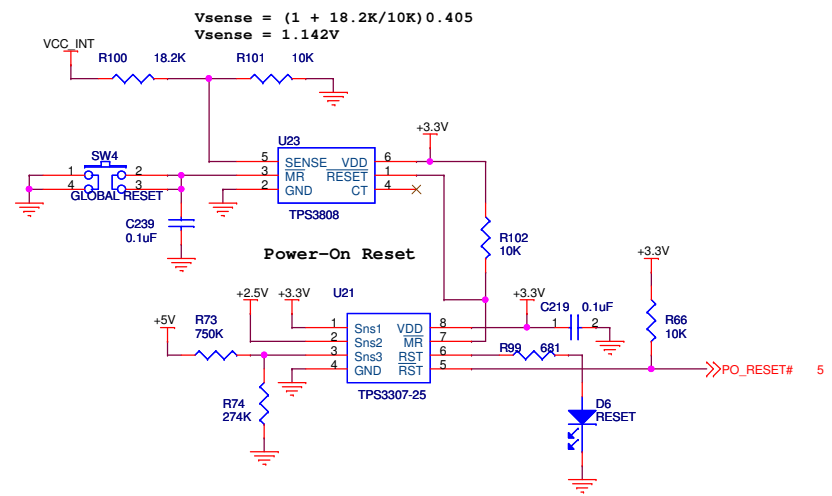
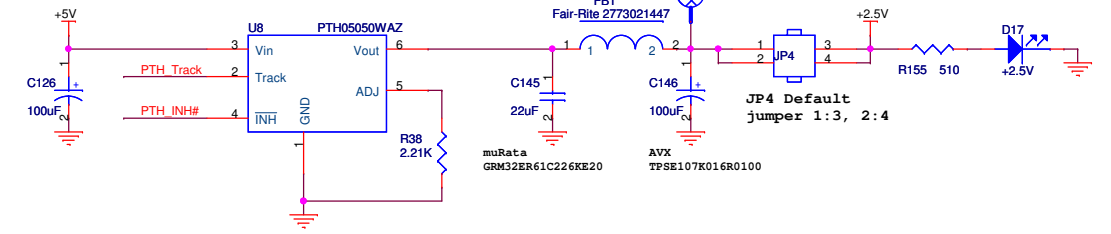
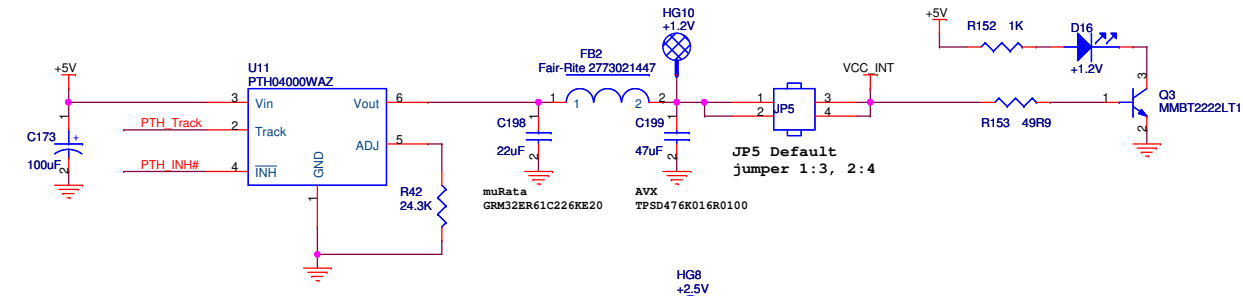
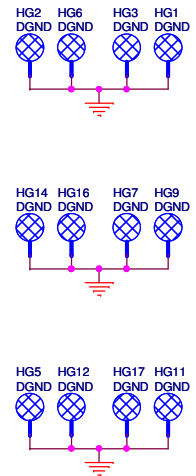
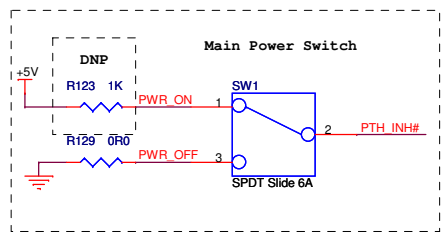
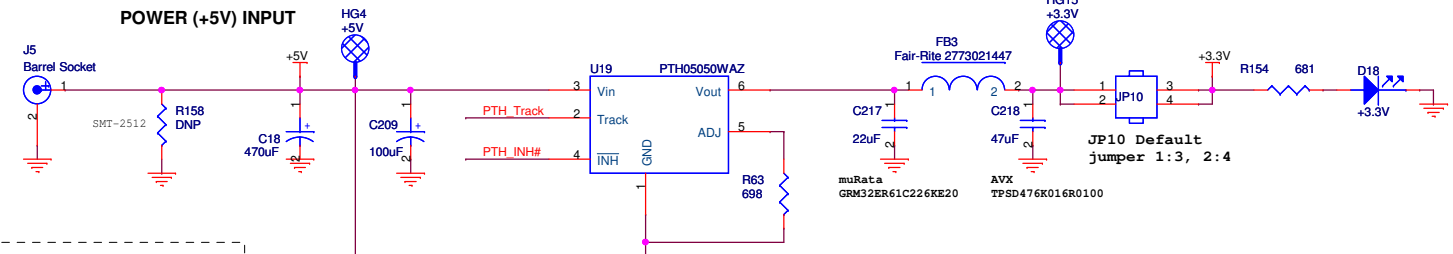
5 EXP2_DIFF_p[0:21] <<<

5 EXP2_DIFF_n[0:21] <<<



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POWER (+5V) INPUT



REV A

REV 1

ADDED POWER LEDS TO VCC_INT, +2.5V AND +3.3V RAILS
CONNECTED U20.3 TO PTH_INH# NET
ADDED A 2512 PKG LOAD RESISTOR TO +5V RAIL AT PWR JACK
ADDED PARALLEL TERMINATION TO SMA CLOCK INPUT
REMOVED LEVEL SHIFTER U14 & DIRECTLY CONNECTED SPI NETS TO U16
GROUNDING UNUSED I/O PINS ON TRANSCEIVERS U9, U17 & U18
CHANGED NAME OF PIN "V24" ON FPGA SYMBOL FROM "IP" TO "IO"

09/21/07: Updated Bank 2 of FPGA package by adding pin AA8 (IP_2) and changing pin AC22 from IP_2 (input only) to IO_2 (bidirectional)

11/26/07: Changed U1 device type from 28F128J3/P30 EBGA to 28F128J3 TSSOP-56

07/11/08: Corrected typo on pin U23 of FPGA (U6)

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