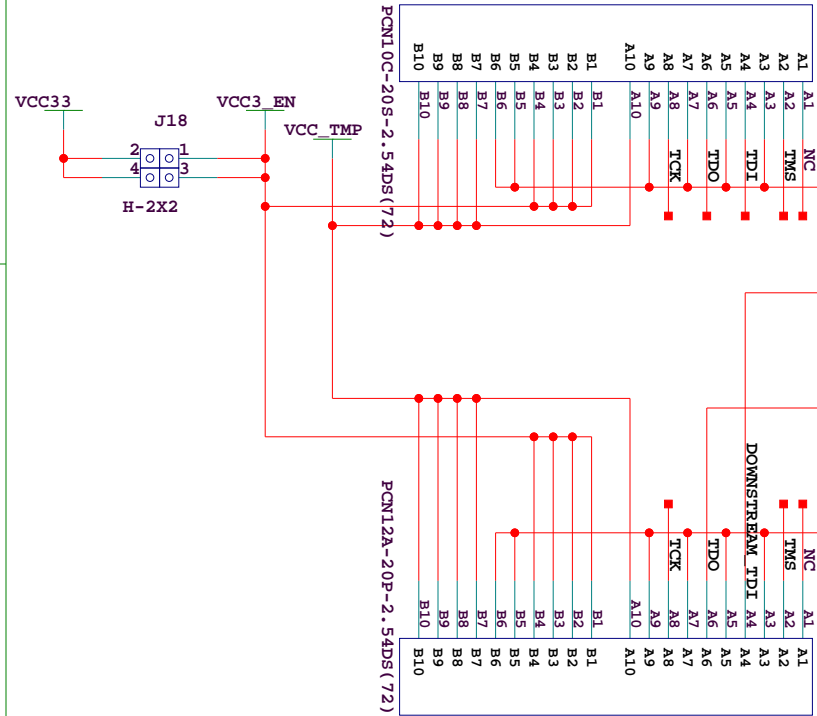
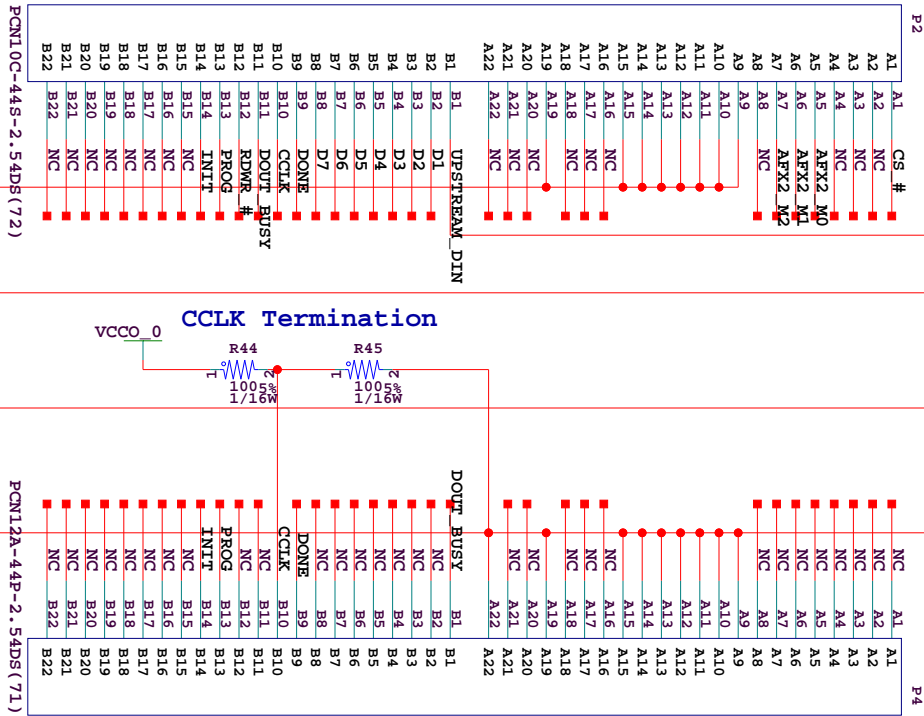


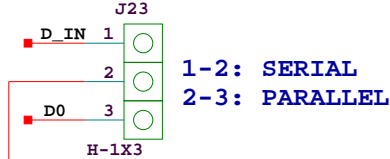
SYSTEM ACE UPSTREAM



UPSTREAM CONNECTORS

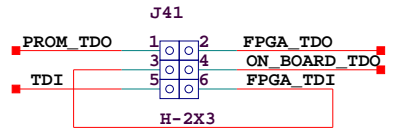


DOWNSTREAM CONFIG



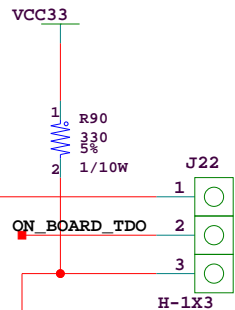
ON BOARD JTAG CHAIN SELECTION

PROM JTAG FPGA JTAG
1-3: Enable 2-4: Enable
3-5: Disable 4-6: Disable

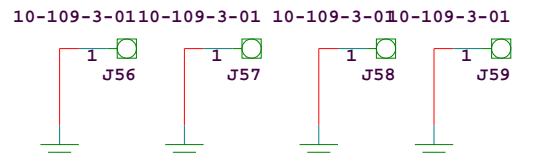


1-2: SERIAL CHAINING TO NEXT BOARD
2-3: TERMINATION OF LAST BOARD IN THE CHAIN

JTAG JUMPER



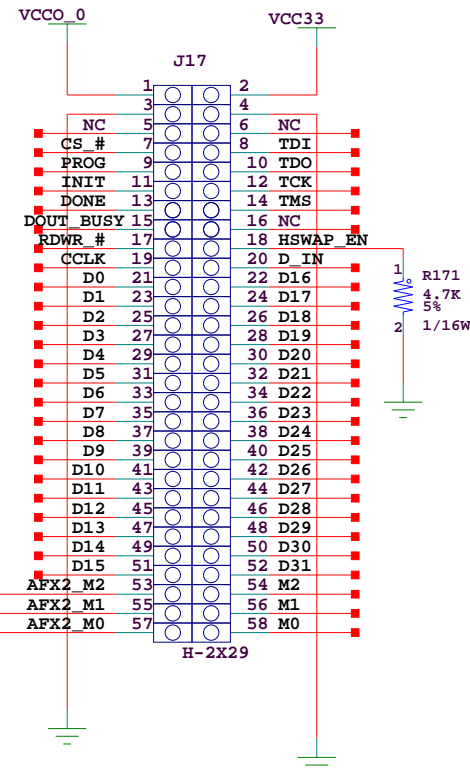
TEST POINTS



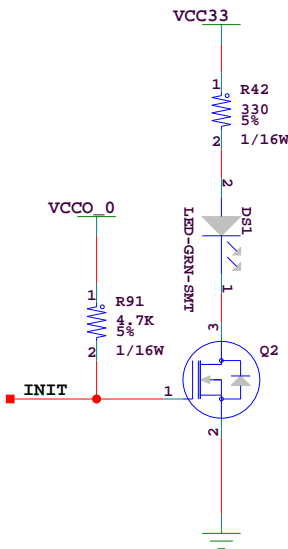
SYSTEM ACE DOWNSTREAM

DOWNSTREAM CONNECTORS

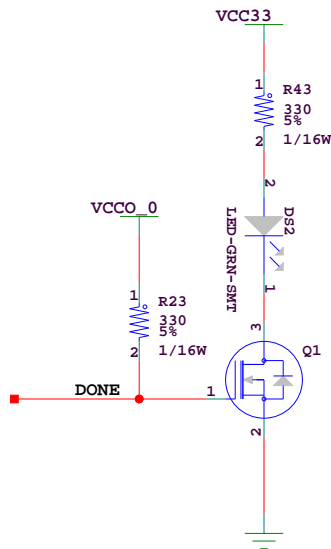
FLYING WIRE CONFIGURATION PORT



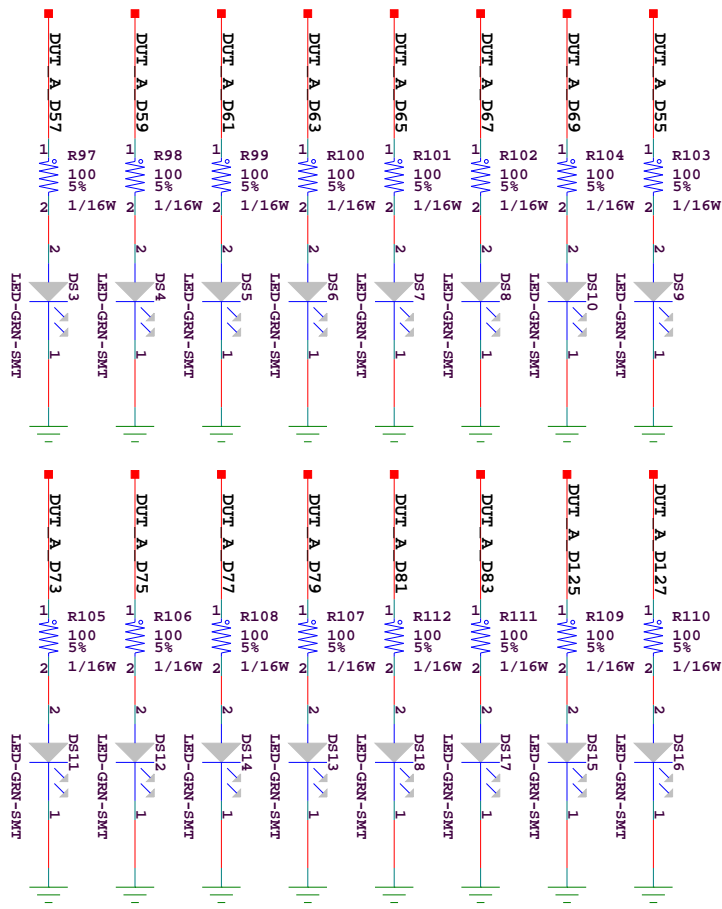
INIT LED



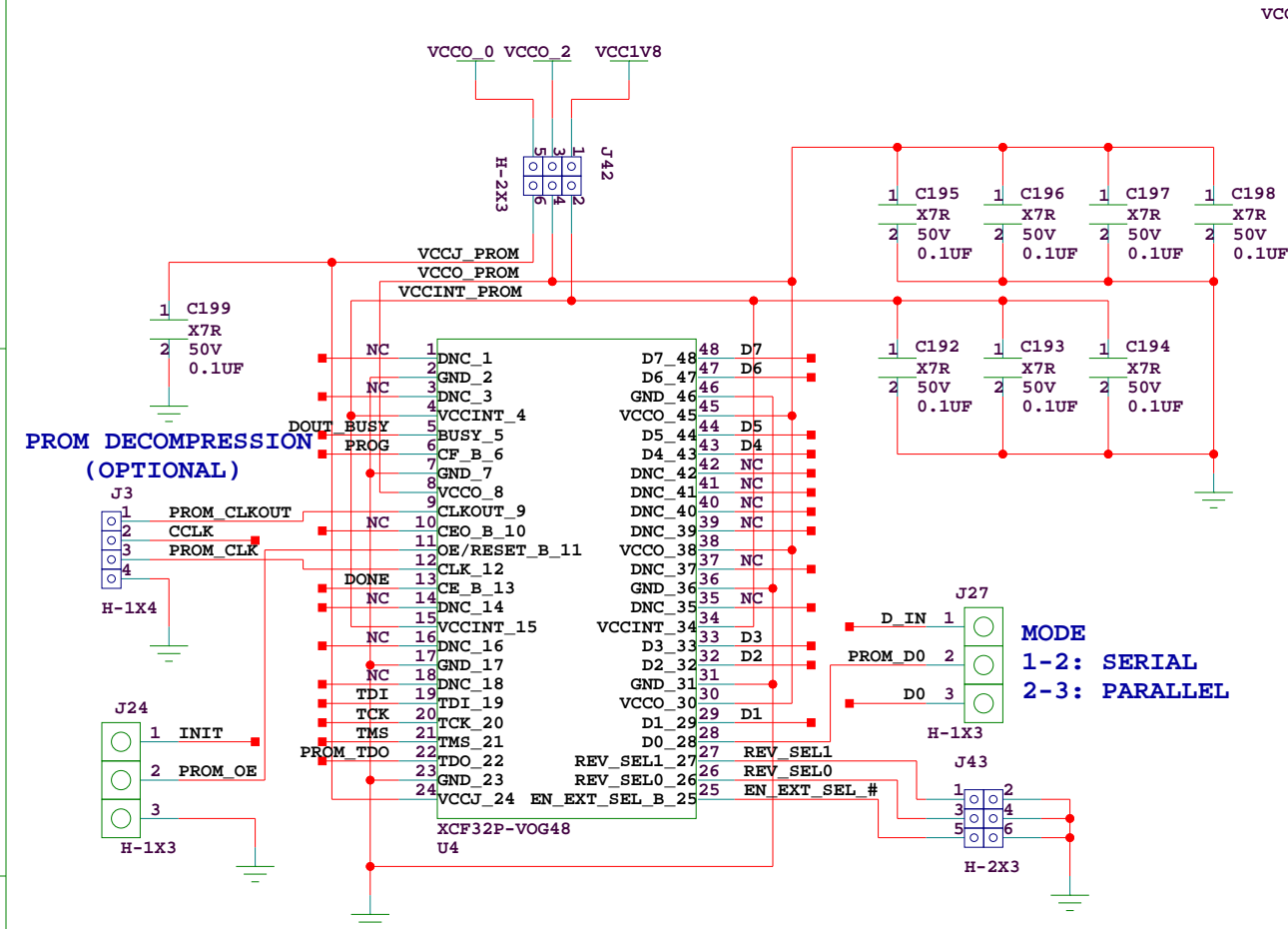
DONE LED



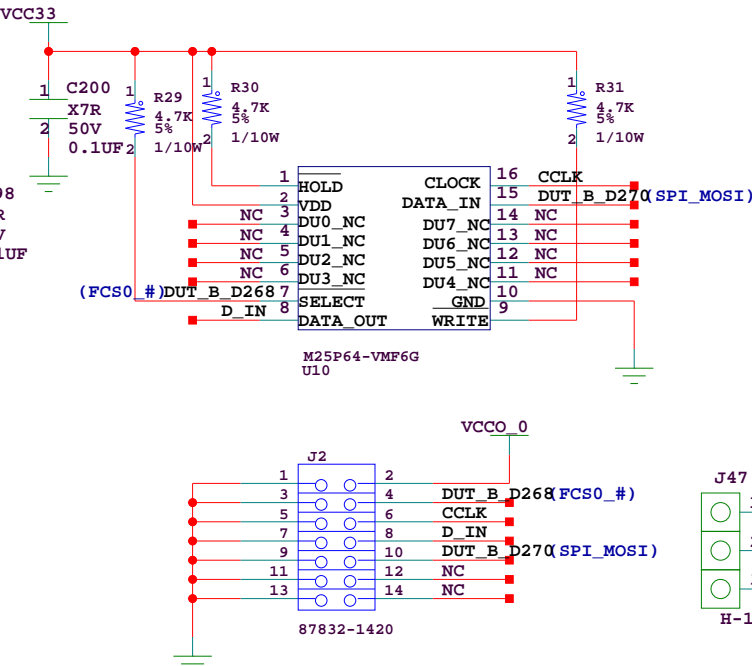
USER LED'S



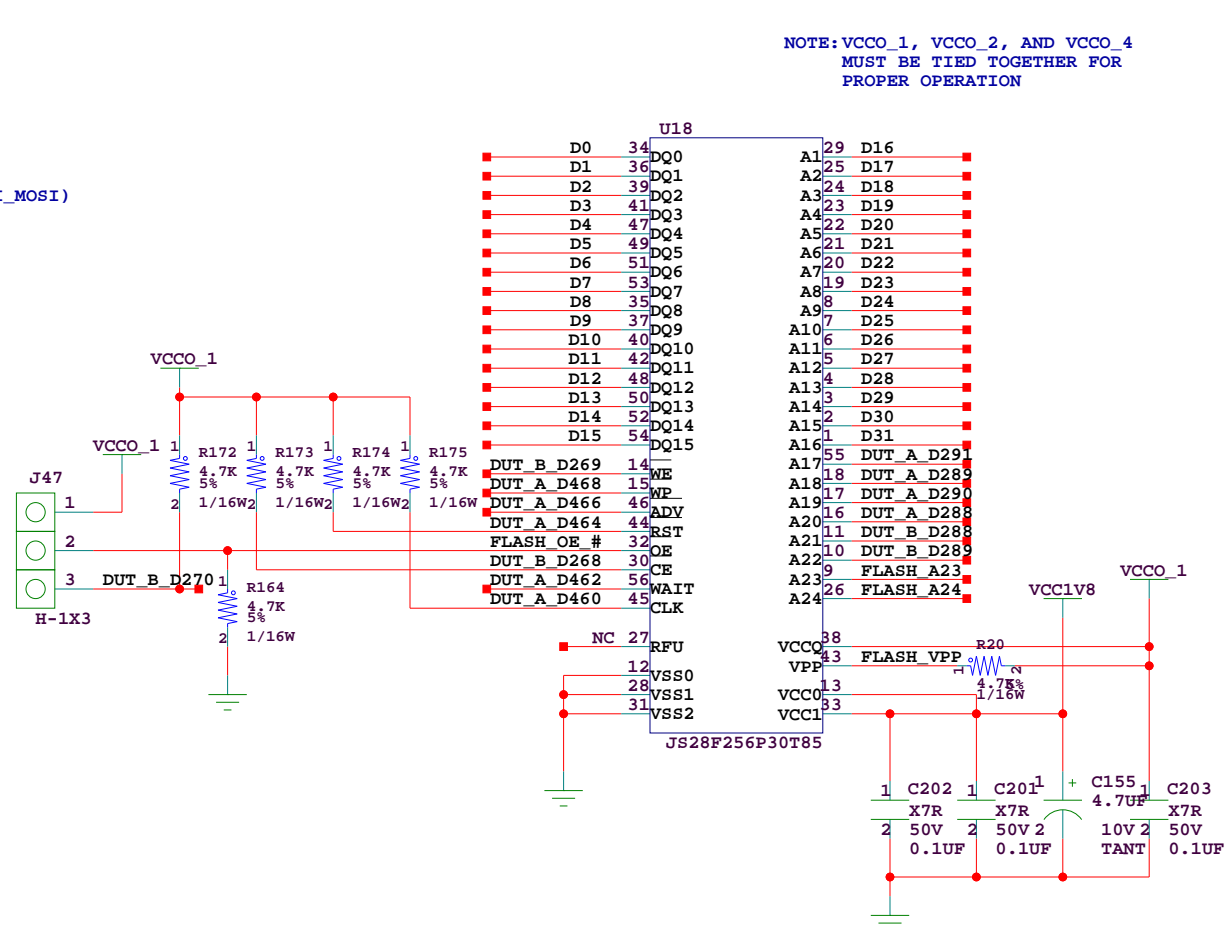
CONFIGURATION PROM



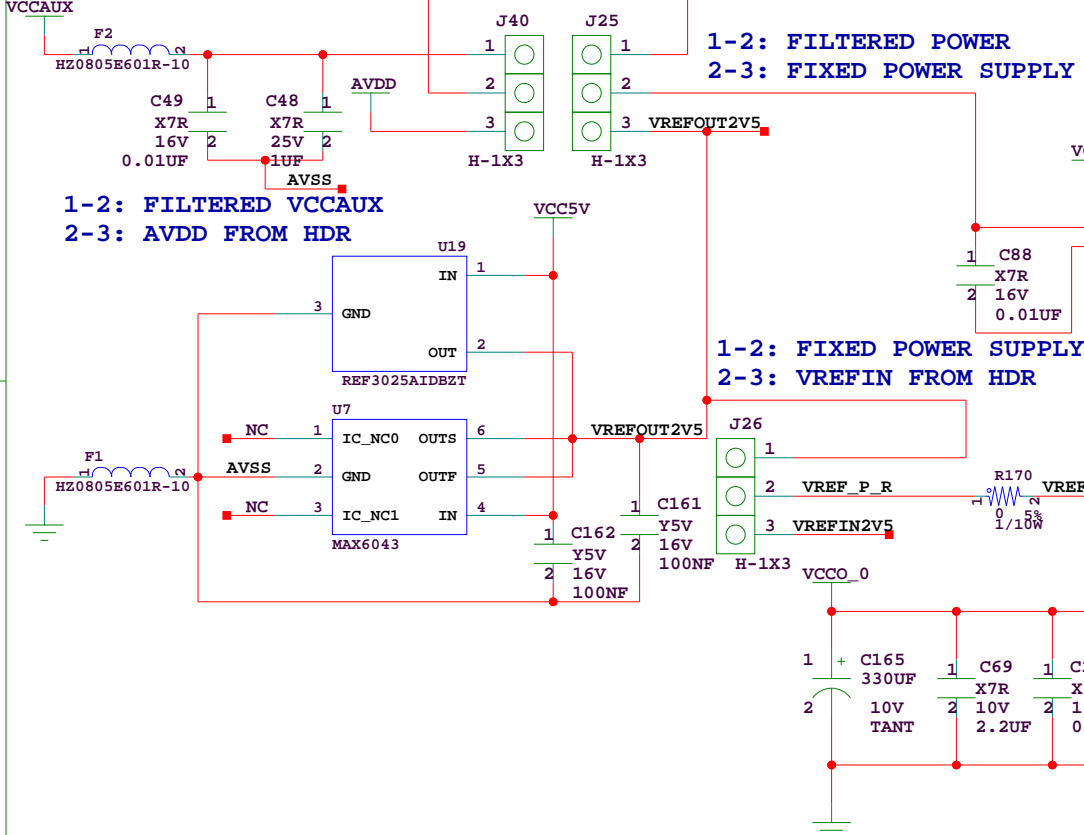
SPI INTERFACE



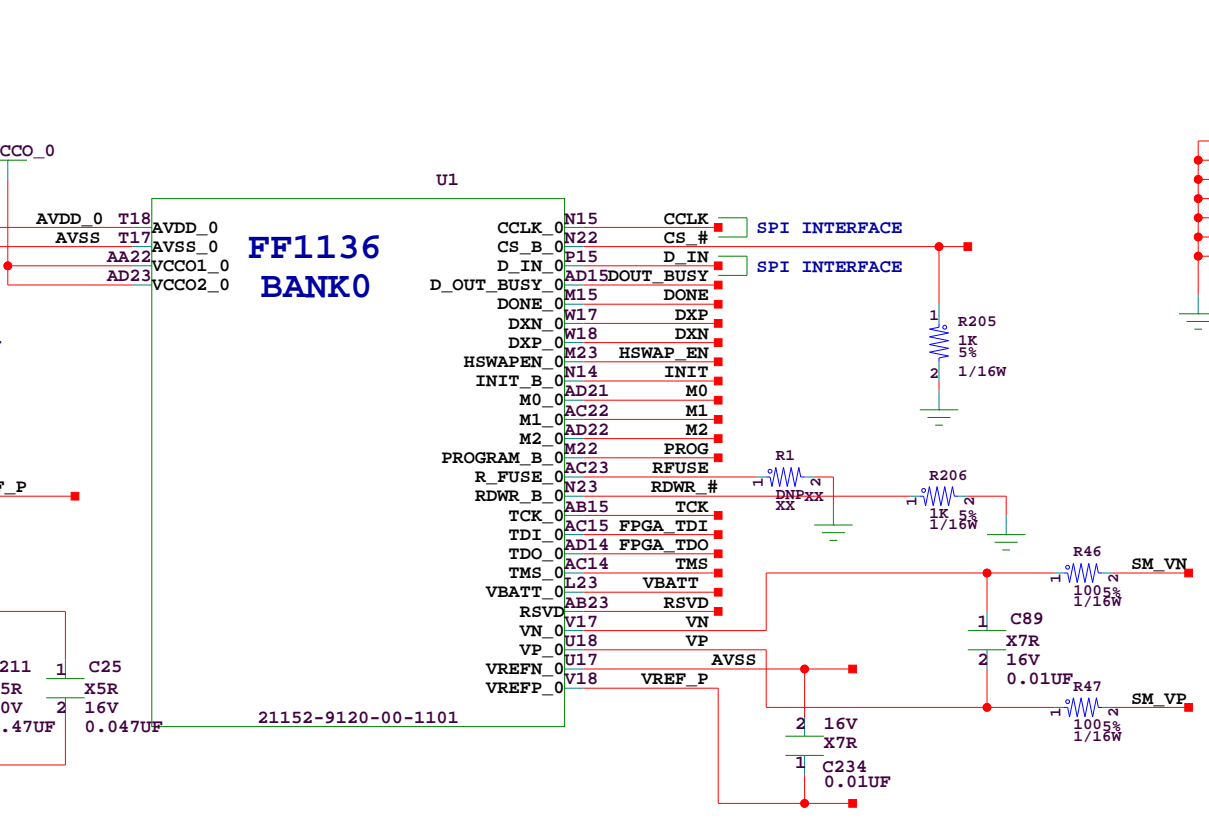
BPI INTERFACE



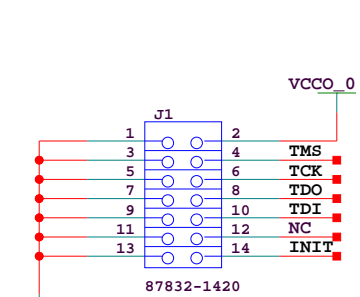
SYSTEM MONITOR SUPPLY



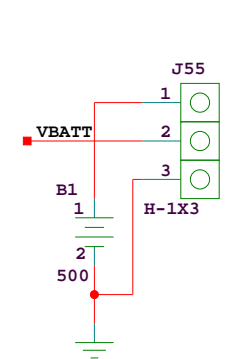
FPGA BANK0 CONFIGURATION



PARALLEL 4 CABLE CONNECTOR



VBATT Supply

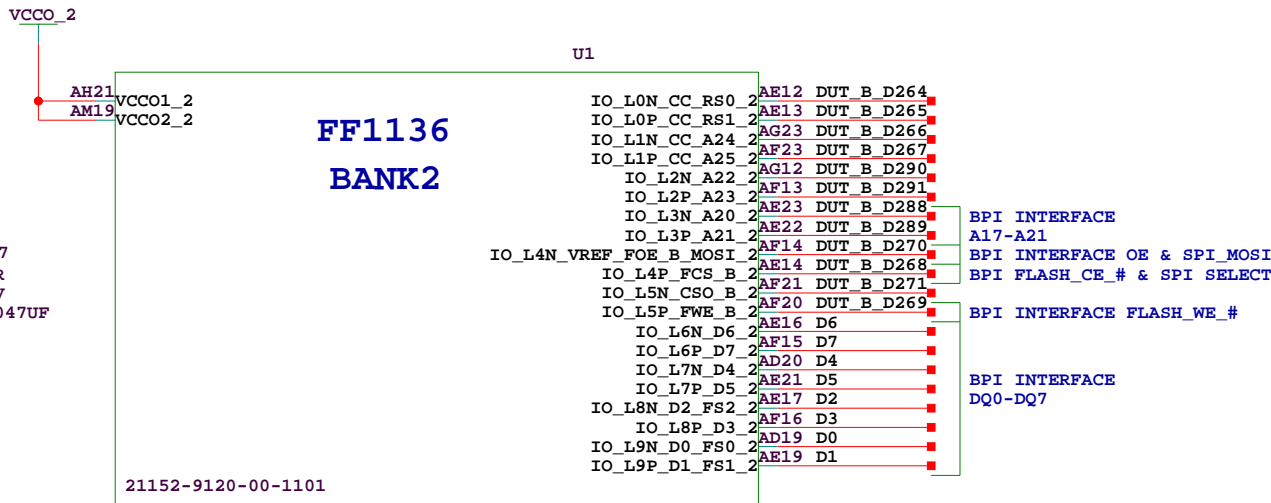
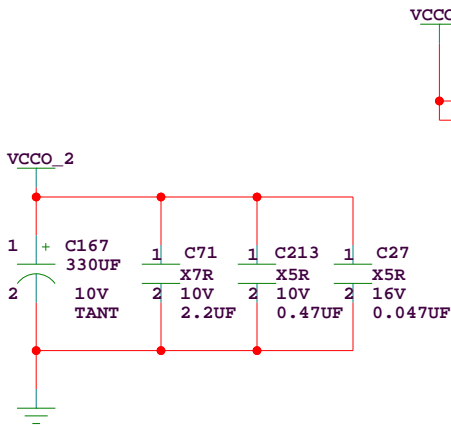
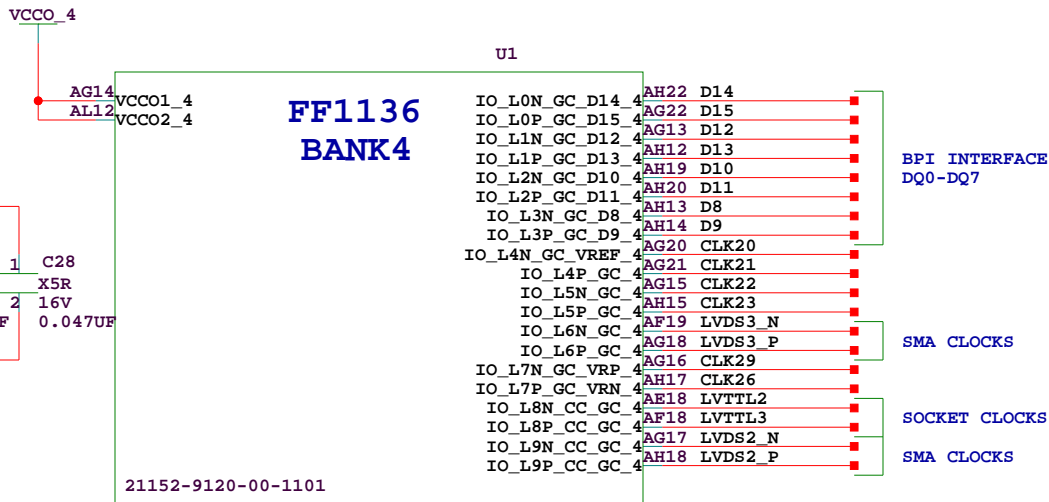
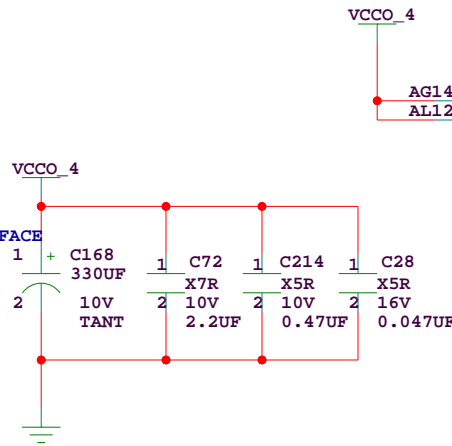
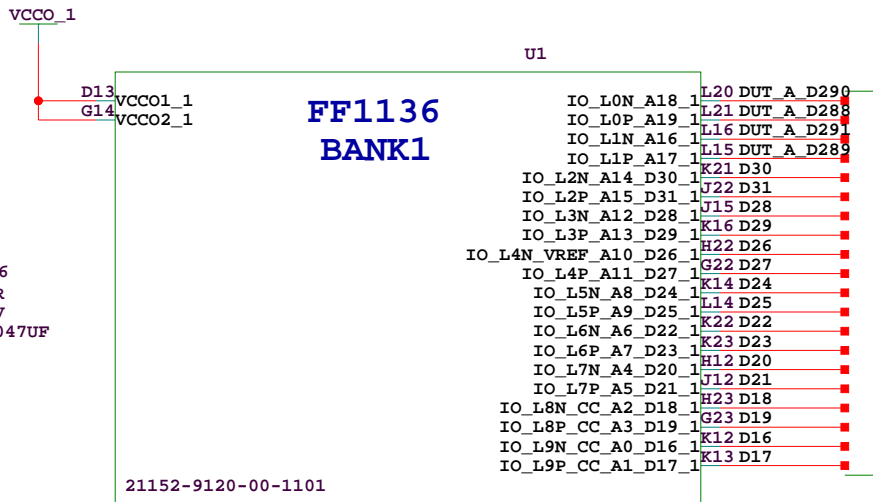
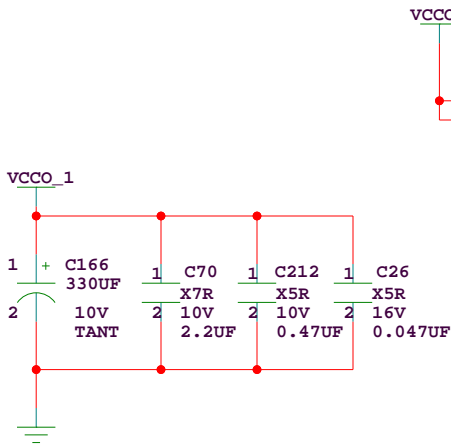


SCH P/N 0381247
ART P/N 0531583
FAB P/N 1280395

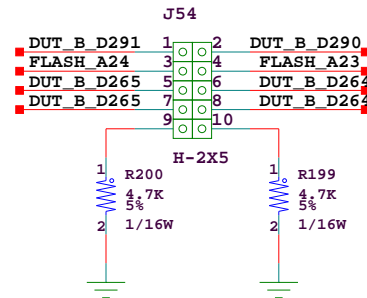
Title:
SCHEM, ROHS COMPLIANT, VIRTEX 5 FF1136 DAUGHTER, 1280395

CONFIGURATION

Date:	2-14-2008_11:35	Ver:	D
Sheet Size:	B	Rev:	02
Sheet	3 of 26	Drawn By	S.S.



BPI REVISION SELECT PINS



- 1-3: Selects ADDR23 from FPGA to FLASH ADDR24
3-5: Selects RS1 from FPGA to FLASH ADDR24
7-9: Pulldown for RS applications
2-4: Selects ADDR22 from FPGA to FLASH ADDR23
3-5: Selects RS0 from FPGA to FLASH ADDR23
8-10: Pulldown for RS applications



SCH P/N 0381247
ART P/N 0531583
FAB P/N 1280395

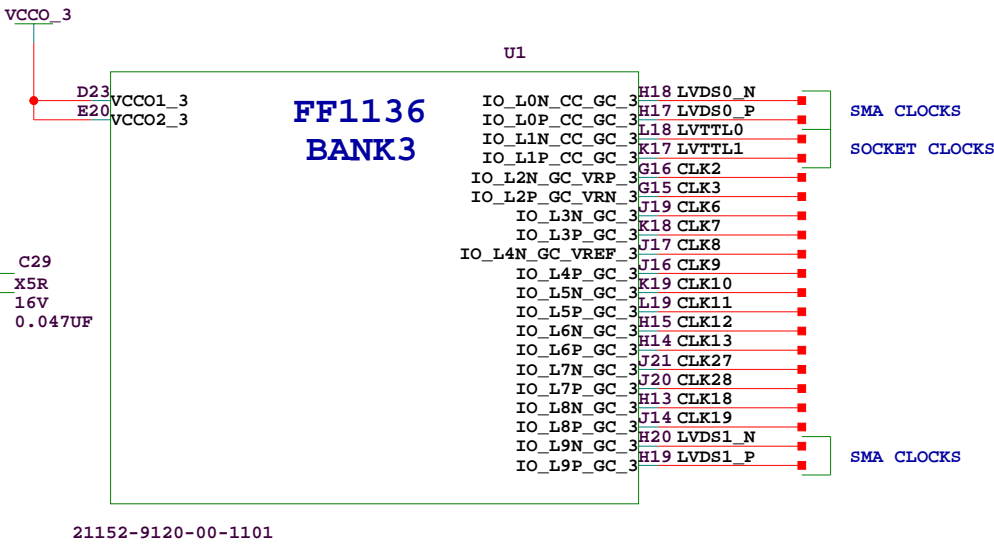
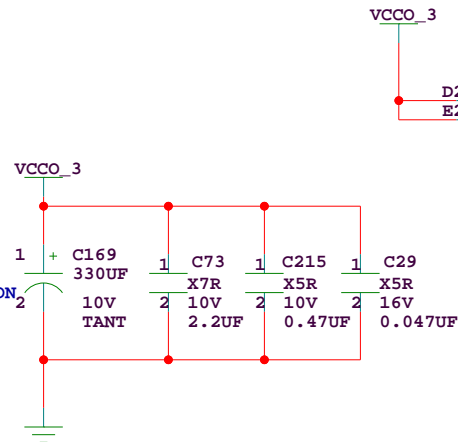
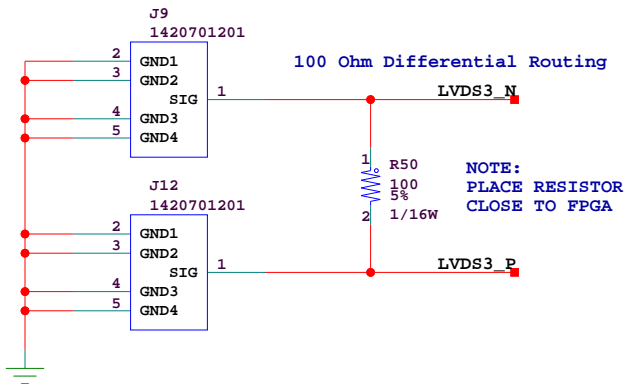
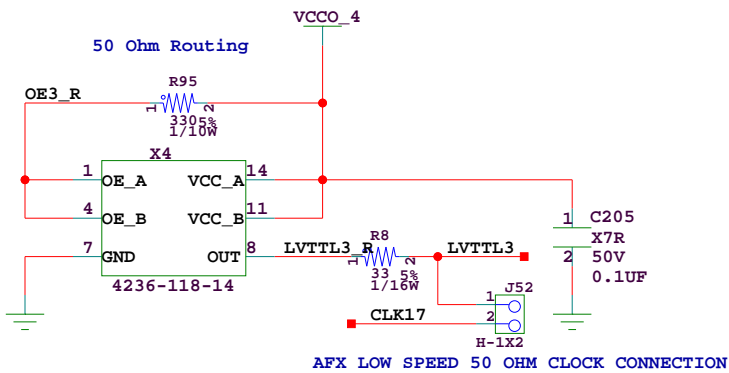
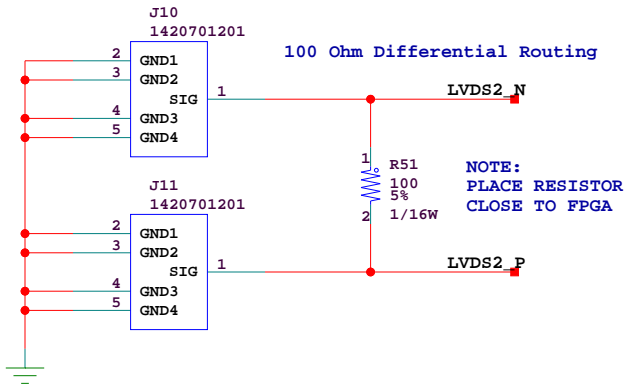
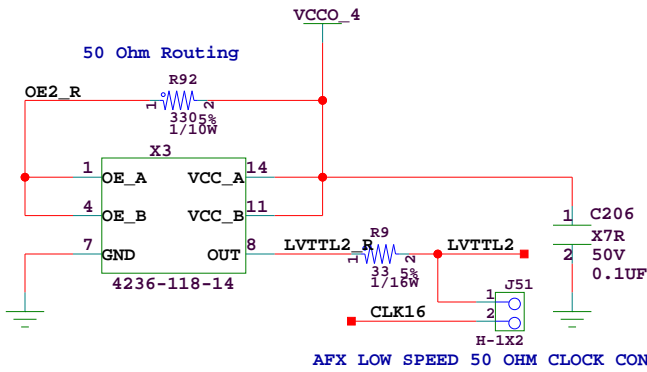
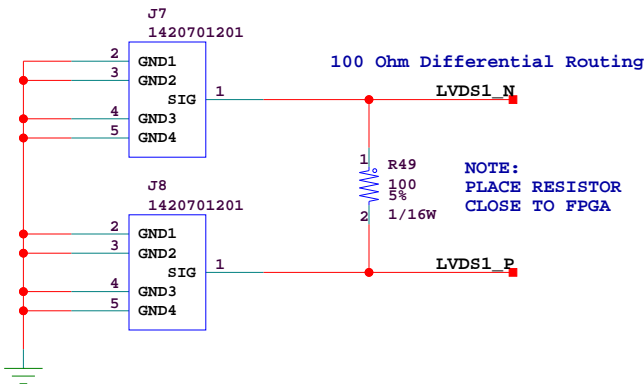
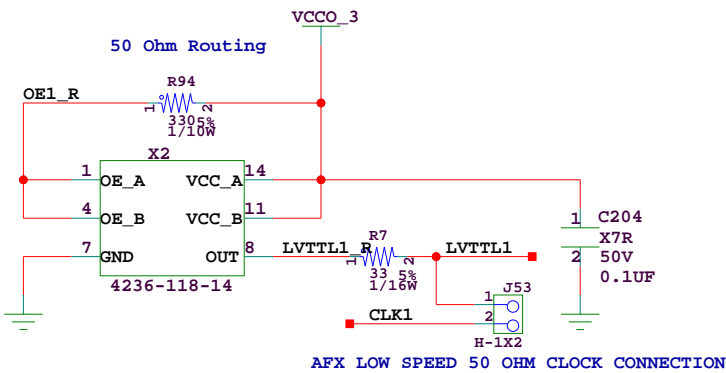
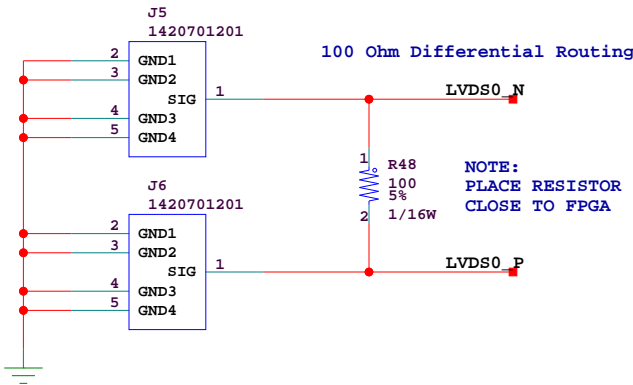
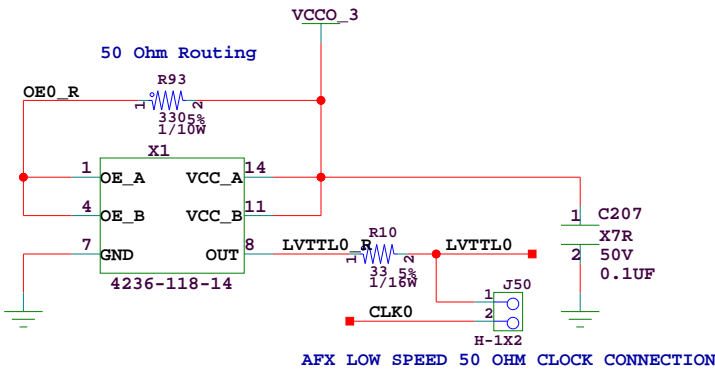
Title:
SCHEM, ROHS COMPLIANT, VIRTEX 5 FF1136 DAUGHTER, 1280395

CONFIGURATION

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Sheet Size: B	Rev: 02
Sheet 4 of 26	Drawn By S.S.

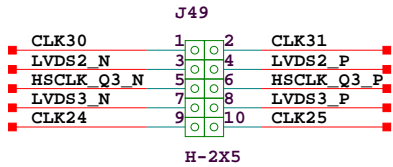
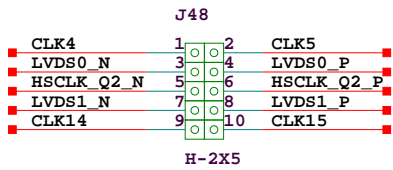
UPPER CLOCKS

BOTTOM CLOCKS



AFX CLOCK CONFIGURATION

1-3, 2-4: LOW SPEED 50 OHM CLOCK CONNECTION
3-5, 4-6: HIGH SPEED 100 OHM DIFFERENTIAL CLOCK CONNECTION TO DIFFERENTIAL PAIR
5-7, 6-8: HIGH SPEED 100 OHM DIFFERENTIAL CLOCK CONNECTION TO DIFFERENTIAL PAIR
7-9, 8-10: LOW SPEED 50 OHM CLOCK CONNECTION



SCH P/N 0381247
ART P/N 0531583
FAB P/N 1280395

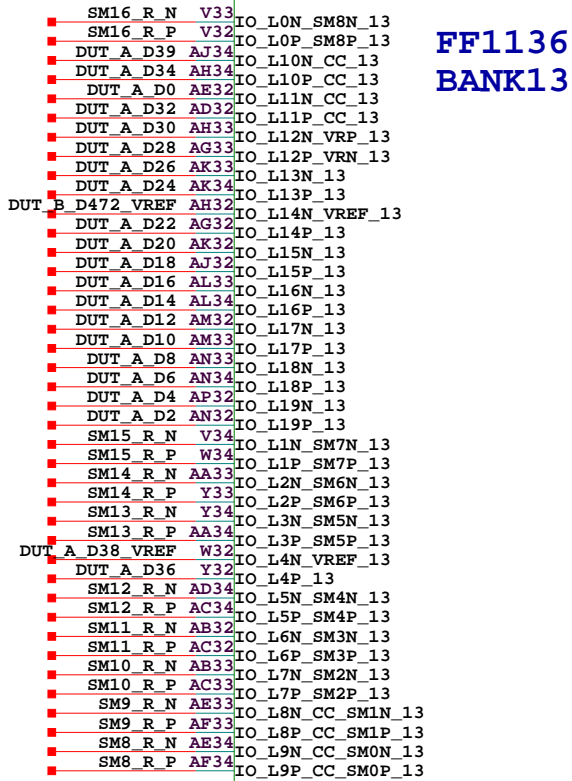
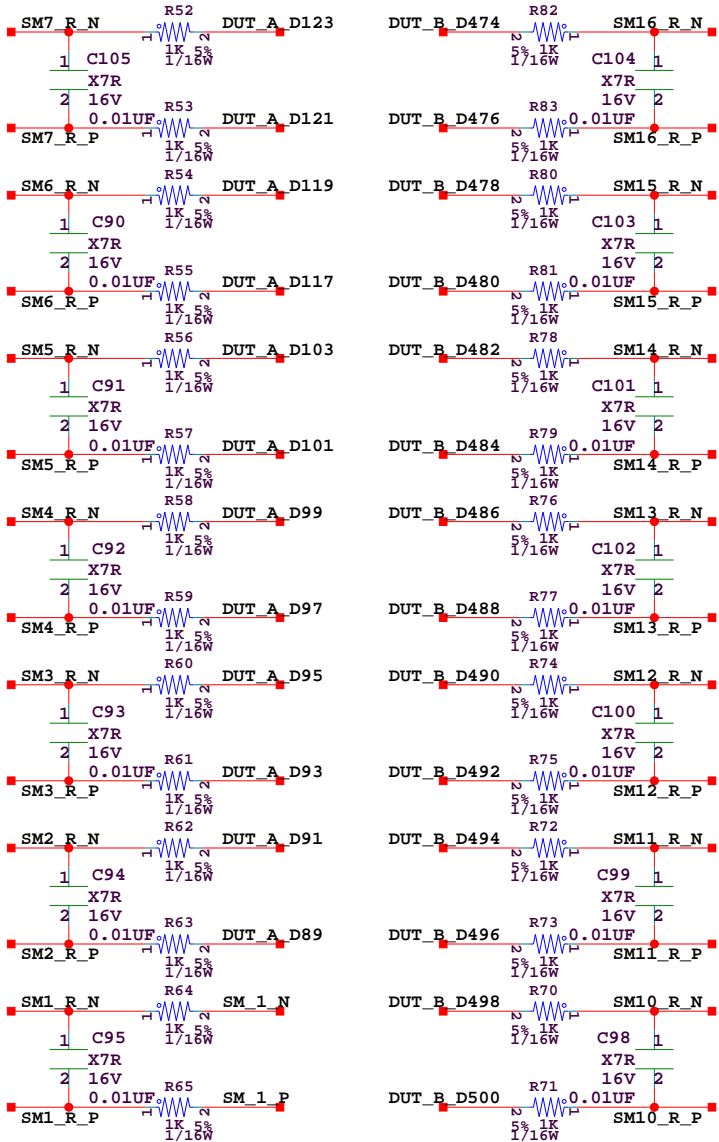
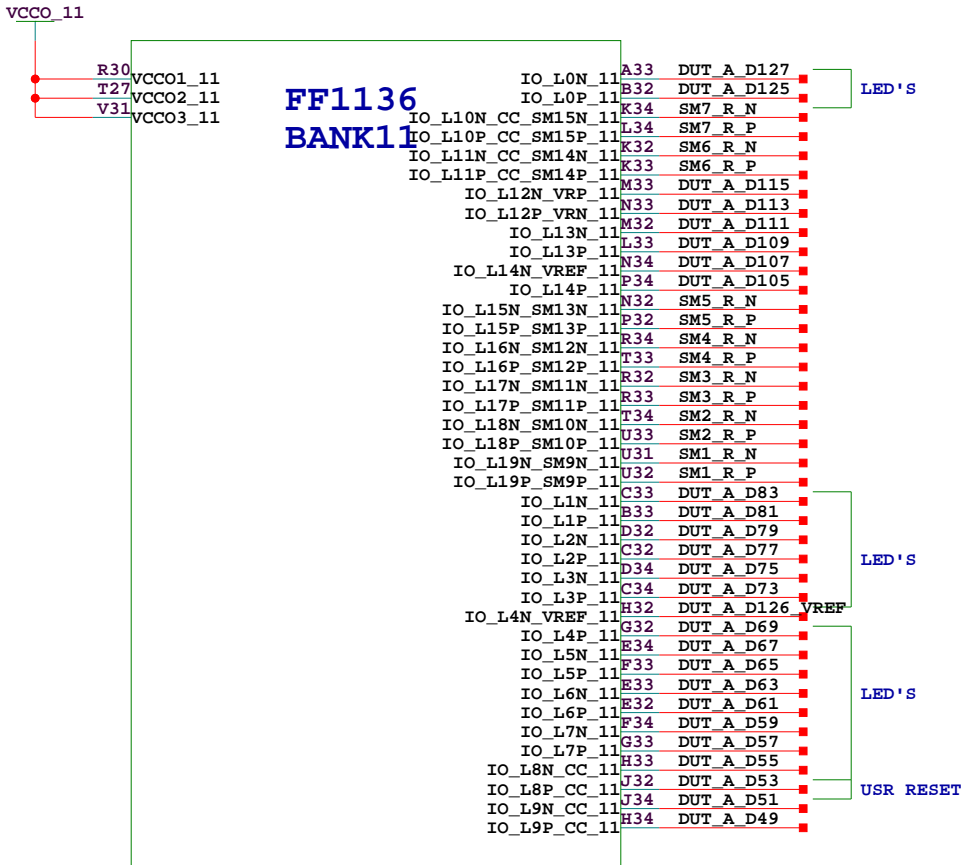
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF1136 DAUGHTER, 1280395
SOCKET CLOCKS, SMA DIFF CLOCKS

Date: 2-14-2008_11:35	Ver: D
Sheet Size: B	Rev: 02
Sheet 5 of 26	Drawn By S.S.

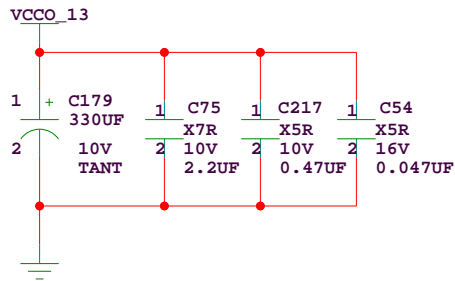
U1

SYSTEM MONITOR FILTERS

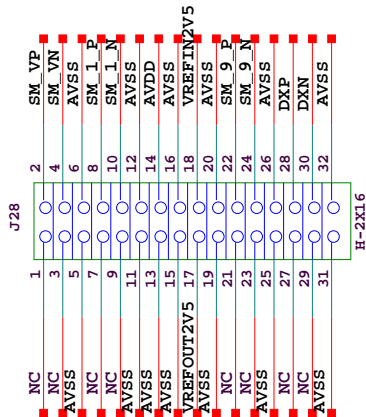
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21152-9120-00-1101



SYSTEM MONITOR MALE CONNECTOR

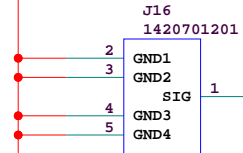
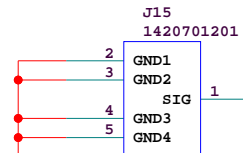
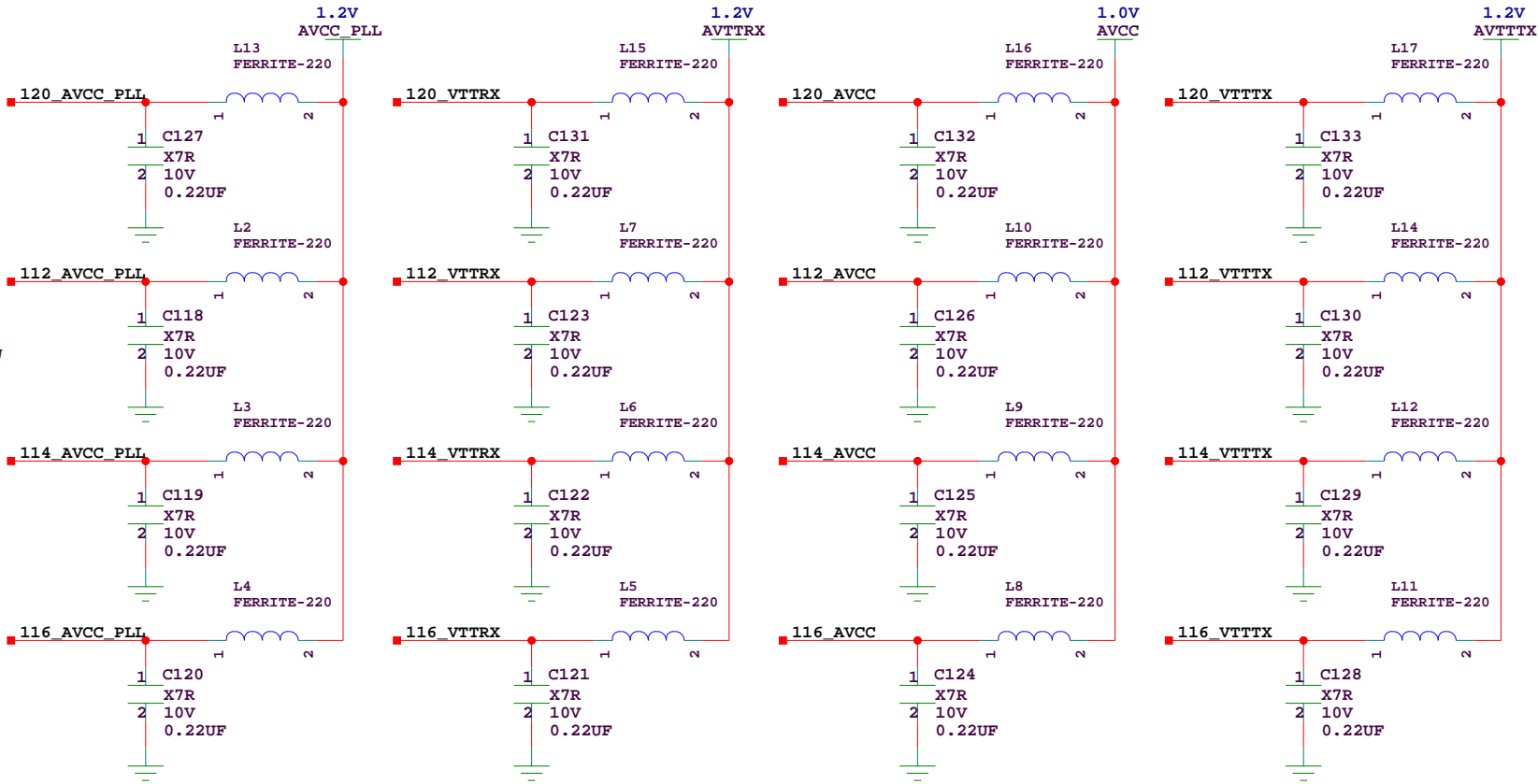
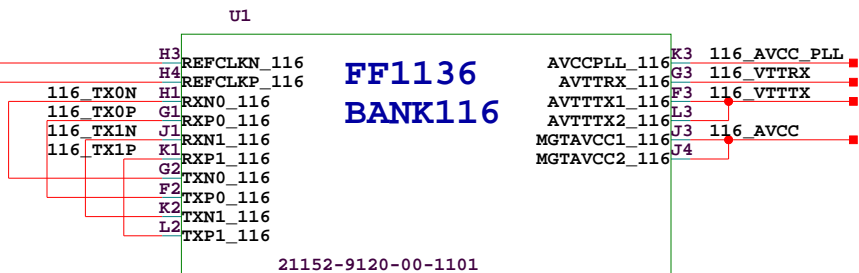
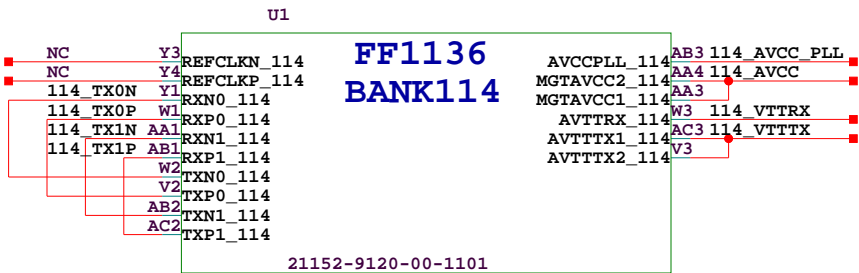
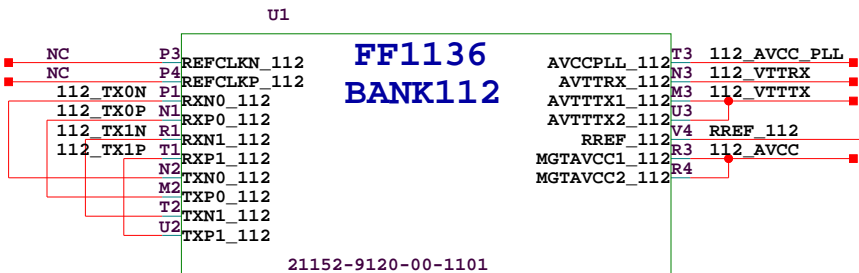
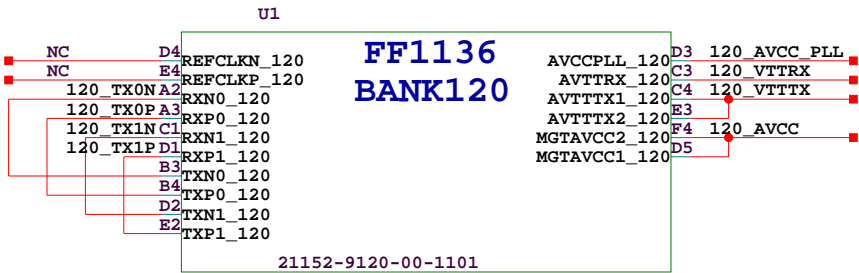


SCH P/N 0381247
ART P/N 0531583
FAB P/N 1280395

Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF1136 DAUGHTER, 1280395

SYSTEM MONITOR

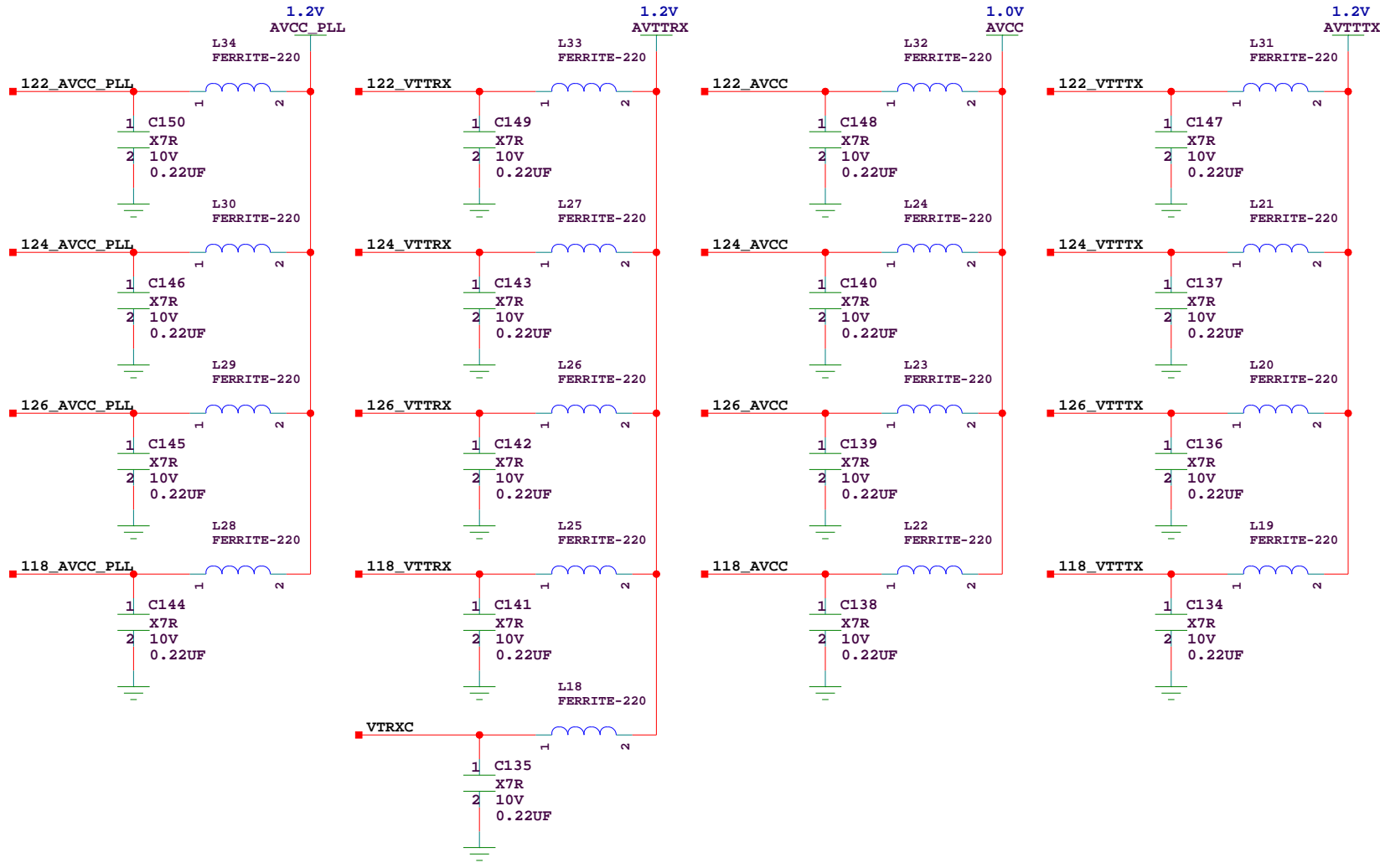
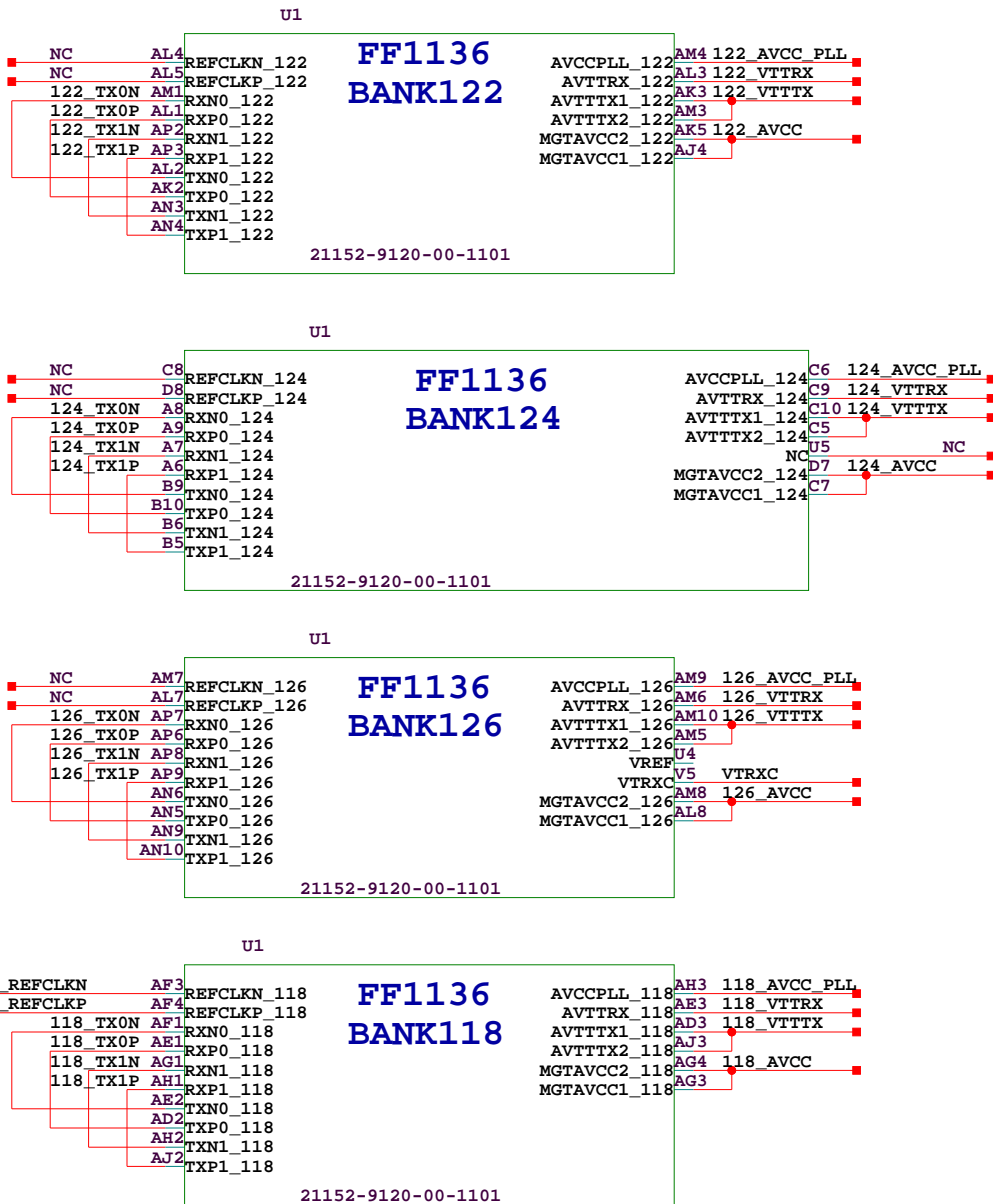
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Sheet Size: B	Rev: 02
Sheet 6 of 26	Drawn By s.s




SCH P/N 0381247
ART P/N 0531583
FAB P/N 1280395

Title:
SCHEM, ROHS COMPLIANT, VIRTEX 5 FF1136 DAUGHTER, 1280395
MGT LOOPBACK 112,114,116,120

Date: 2-14-2008_11:35	Ver: D
Sheet Size: B	Rev: 02
Sheet 7 of 26	Drawn By S.S.





SCH P/N0381247

ART P/N0531583

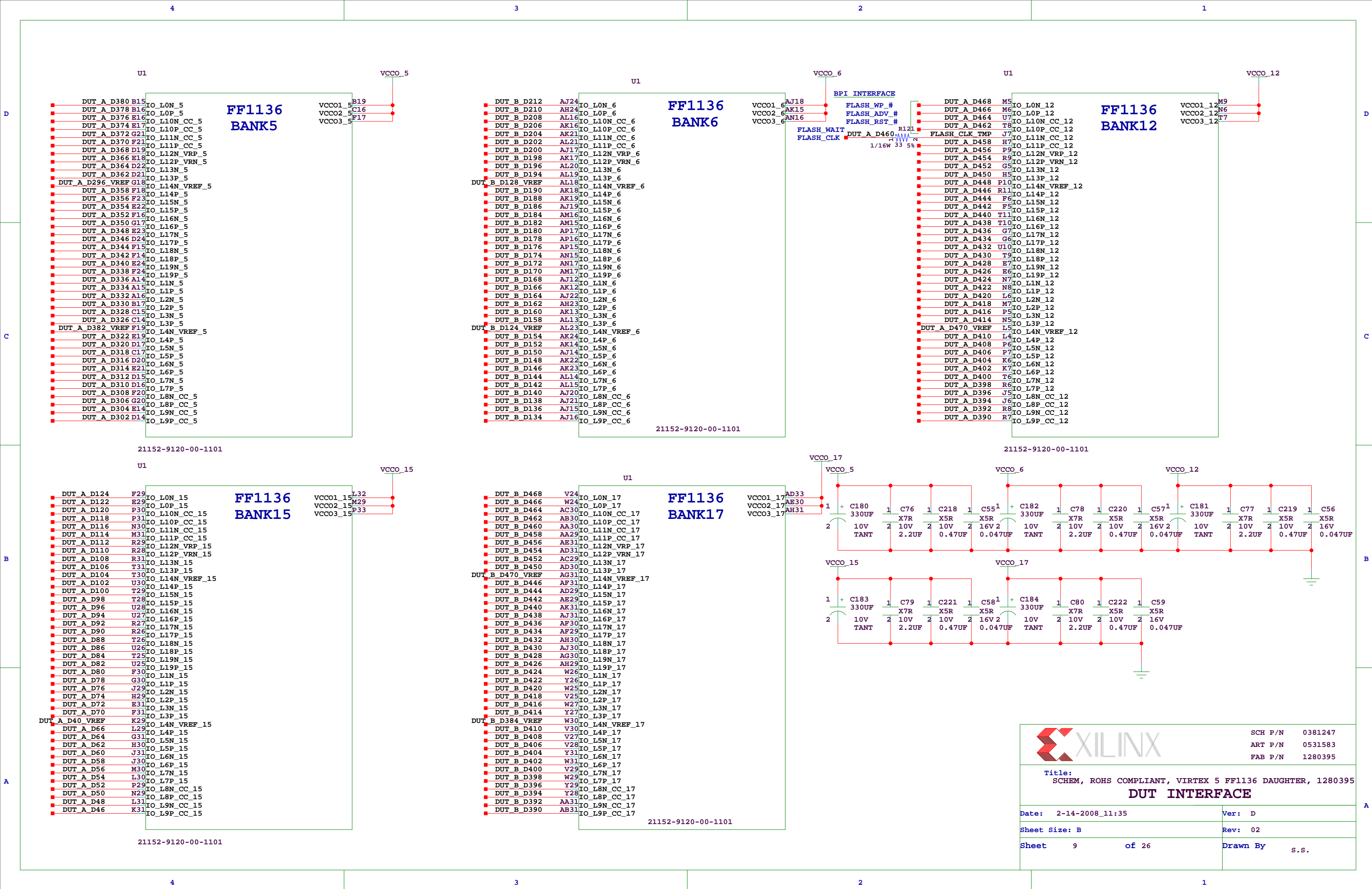
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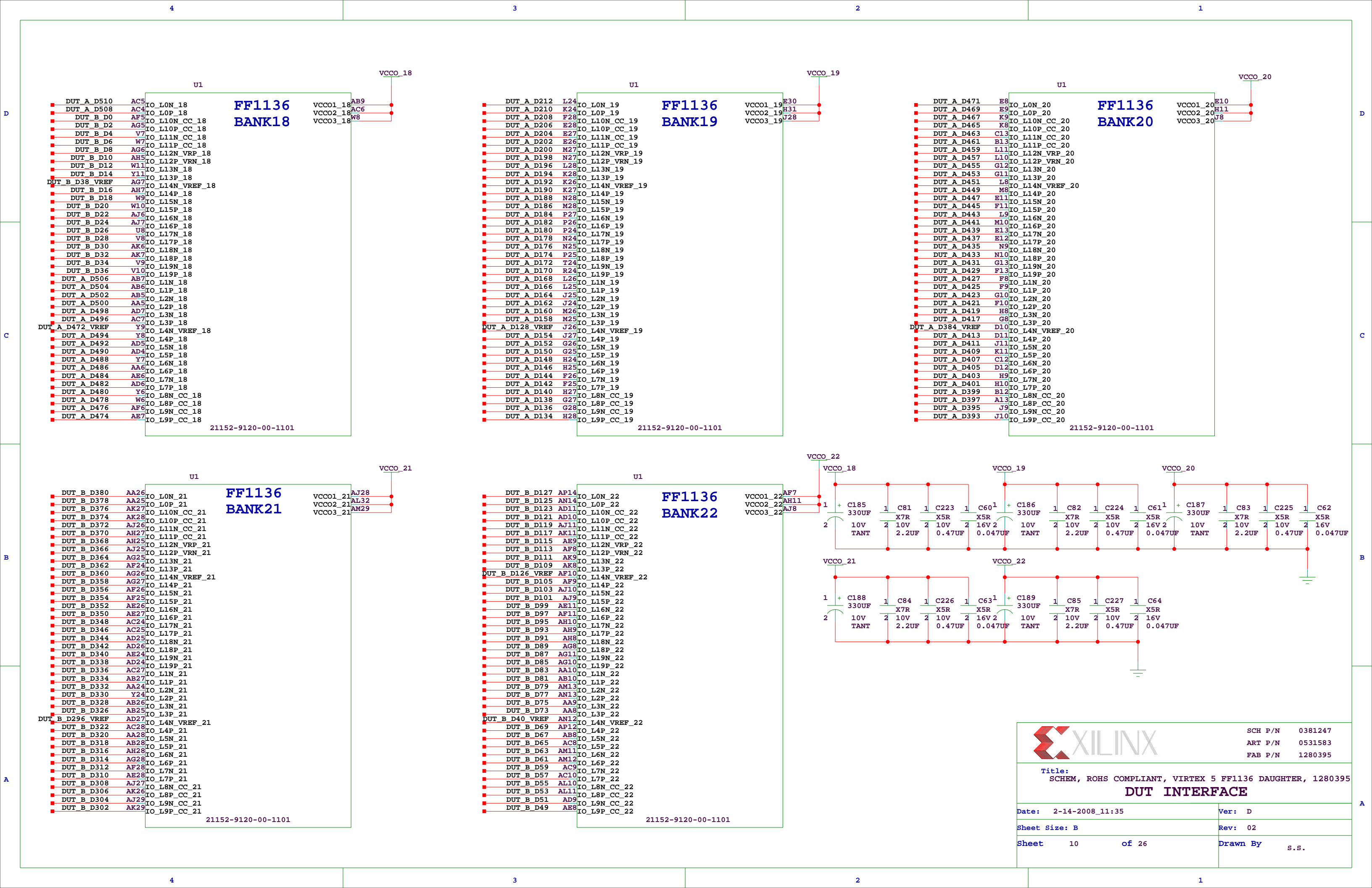
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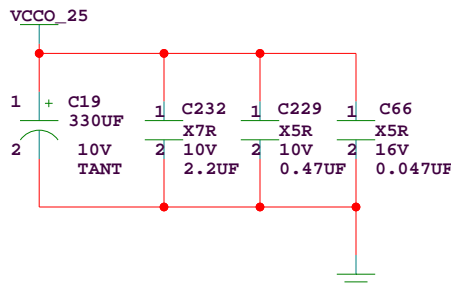
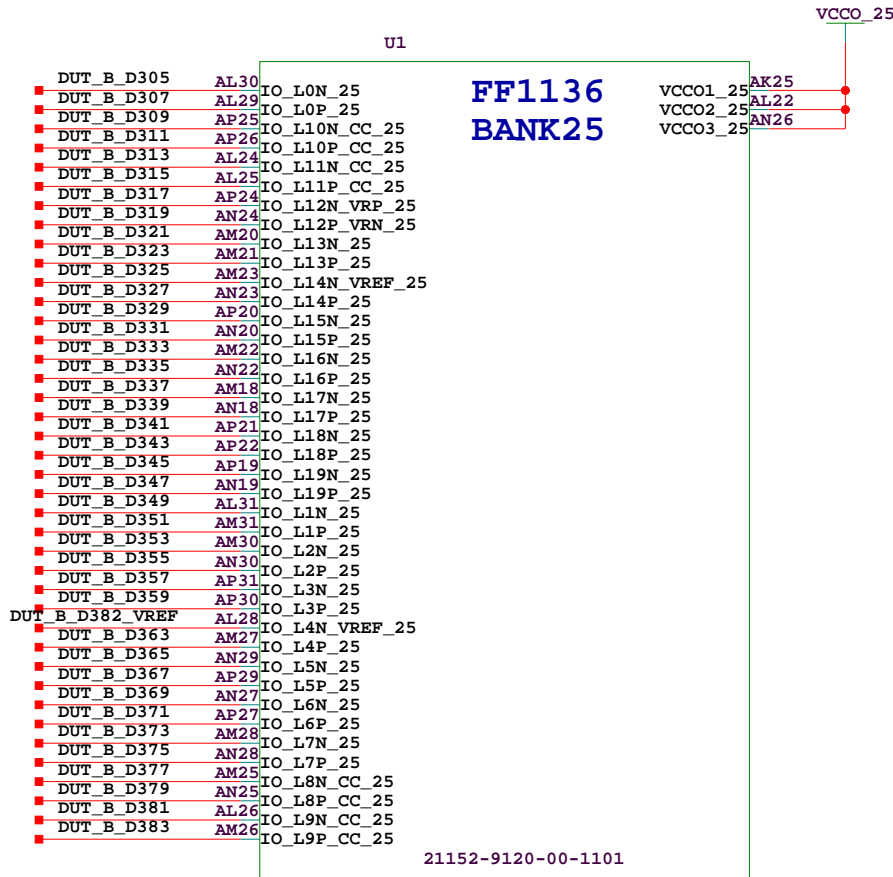
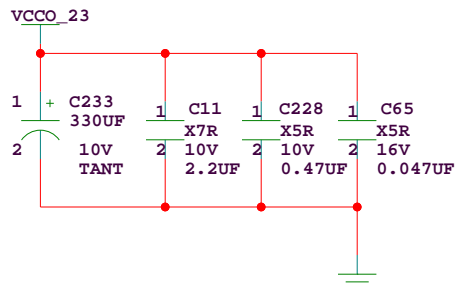
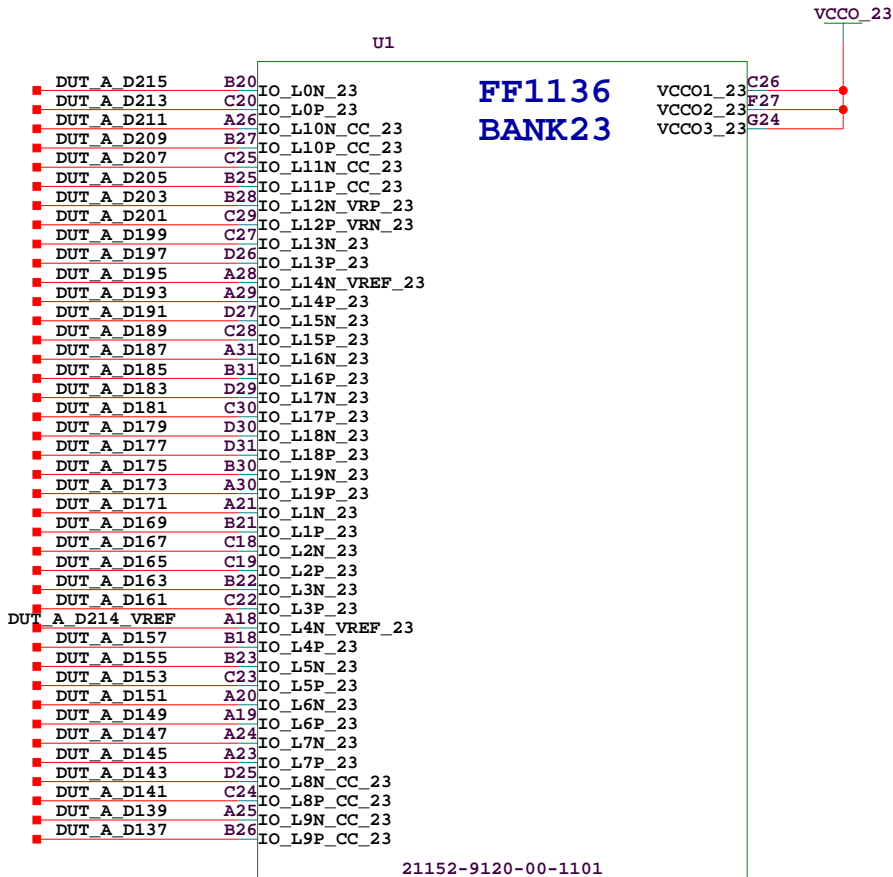
SCHEM, ROHS COMPLIANT, VIRTEX 5 FF1136 DAUGHTER, 1280395


MGT LOOPBACK 118,122,124,126

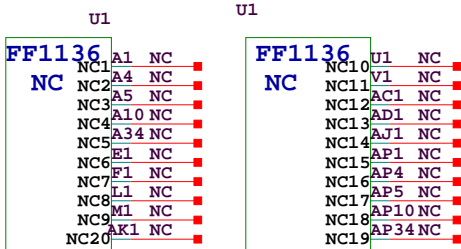
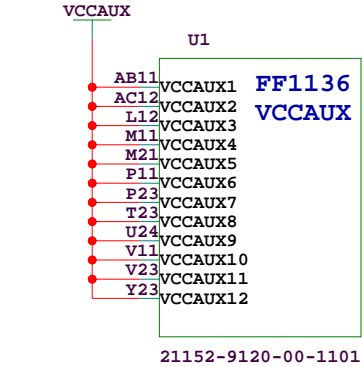
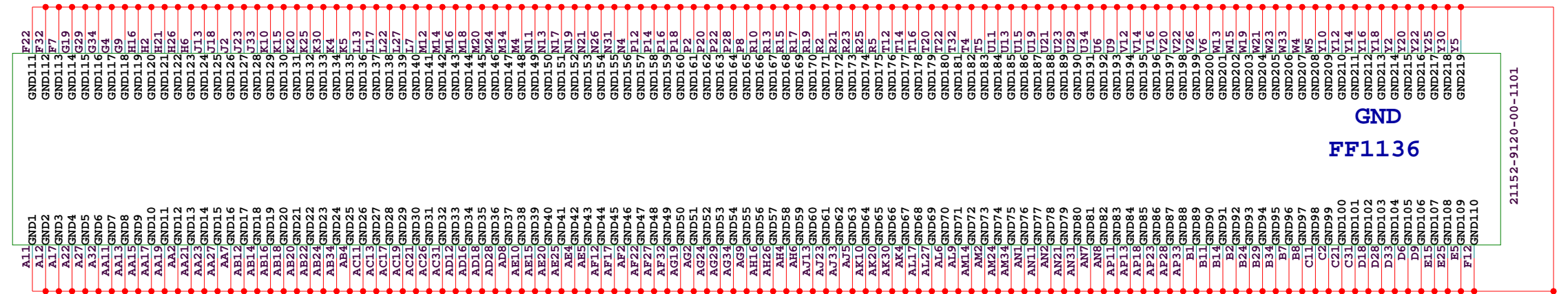
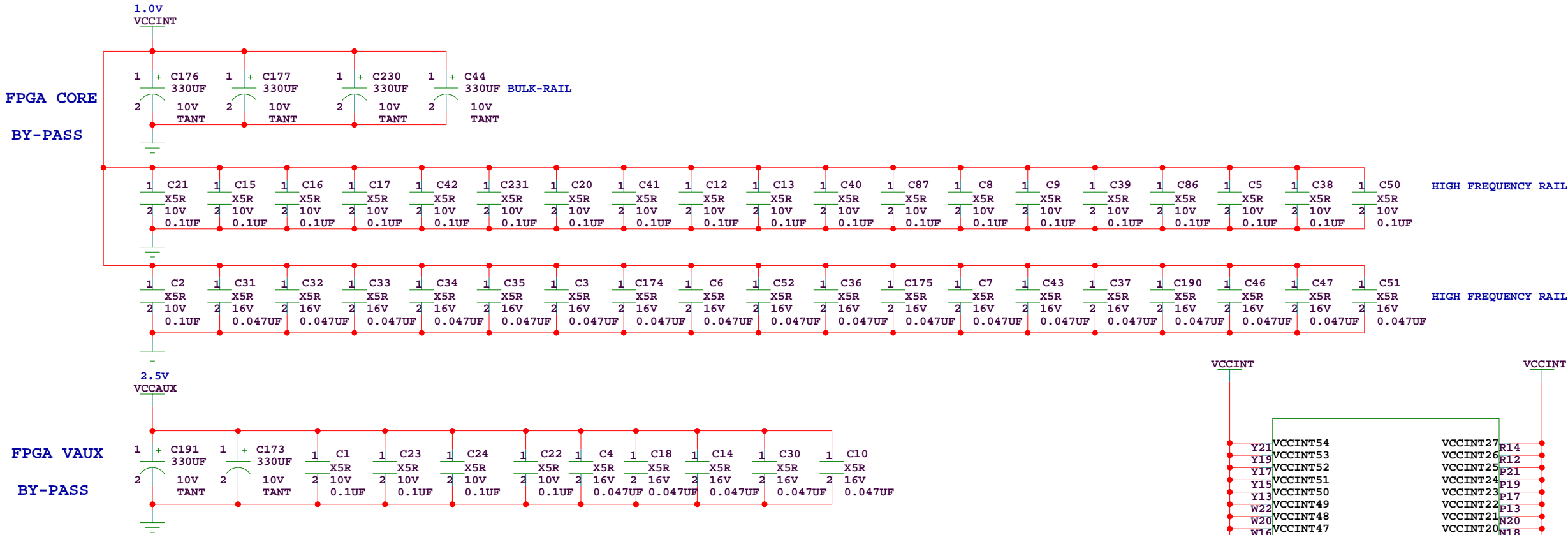
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Sheet Size: B	Rev: 02
Sheet 8 of 26	Drawn By S.S.




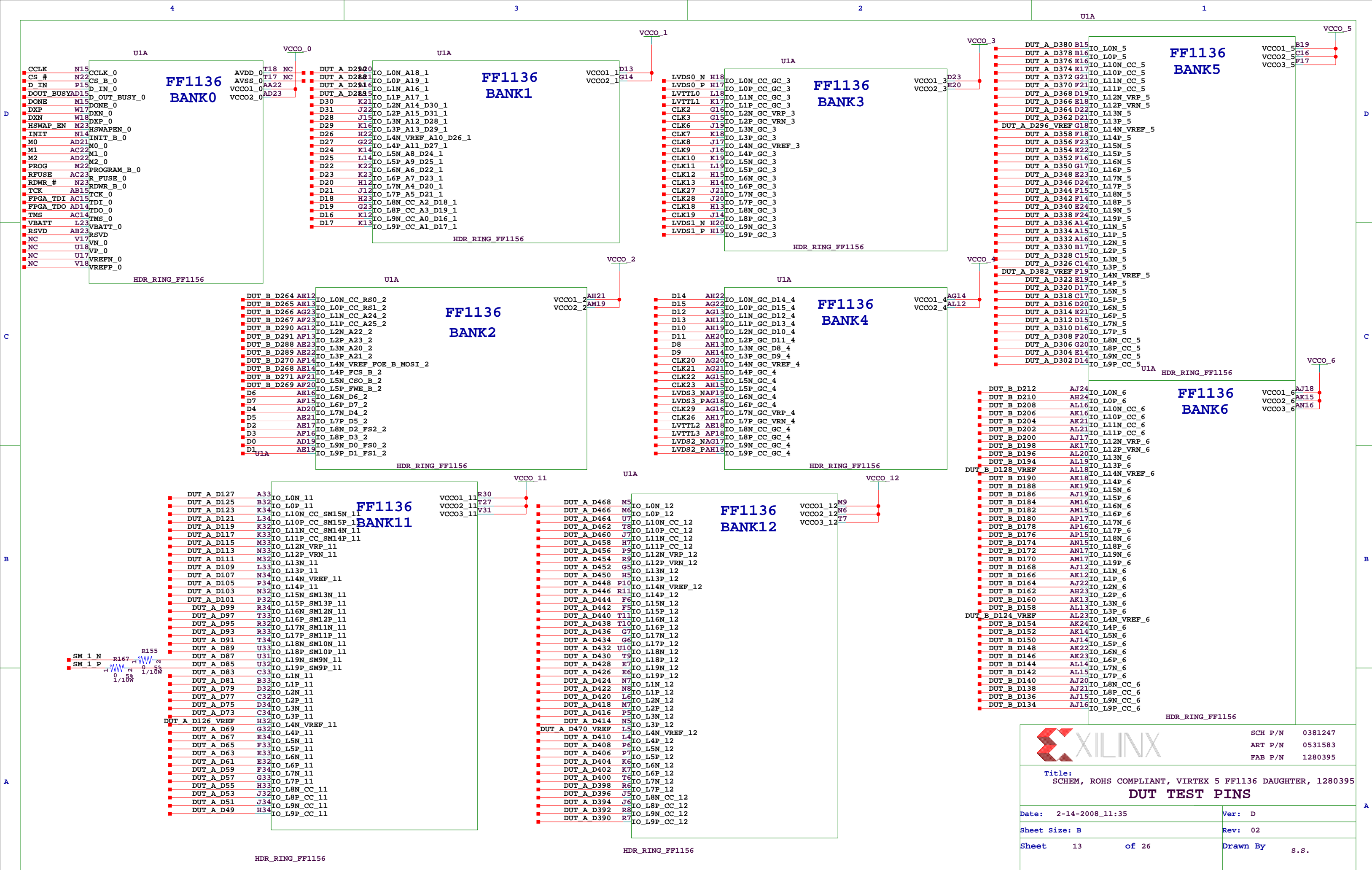


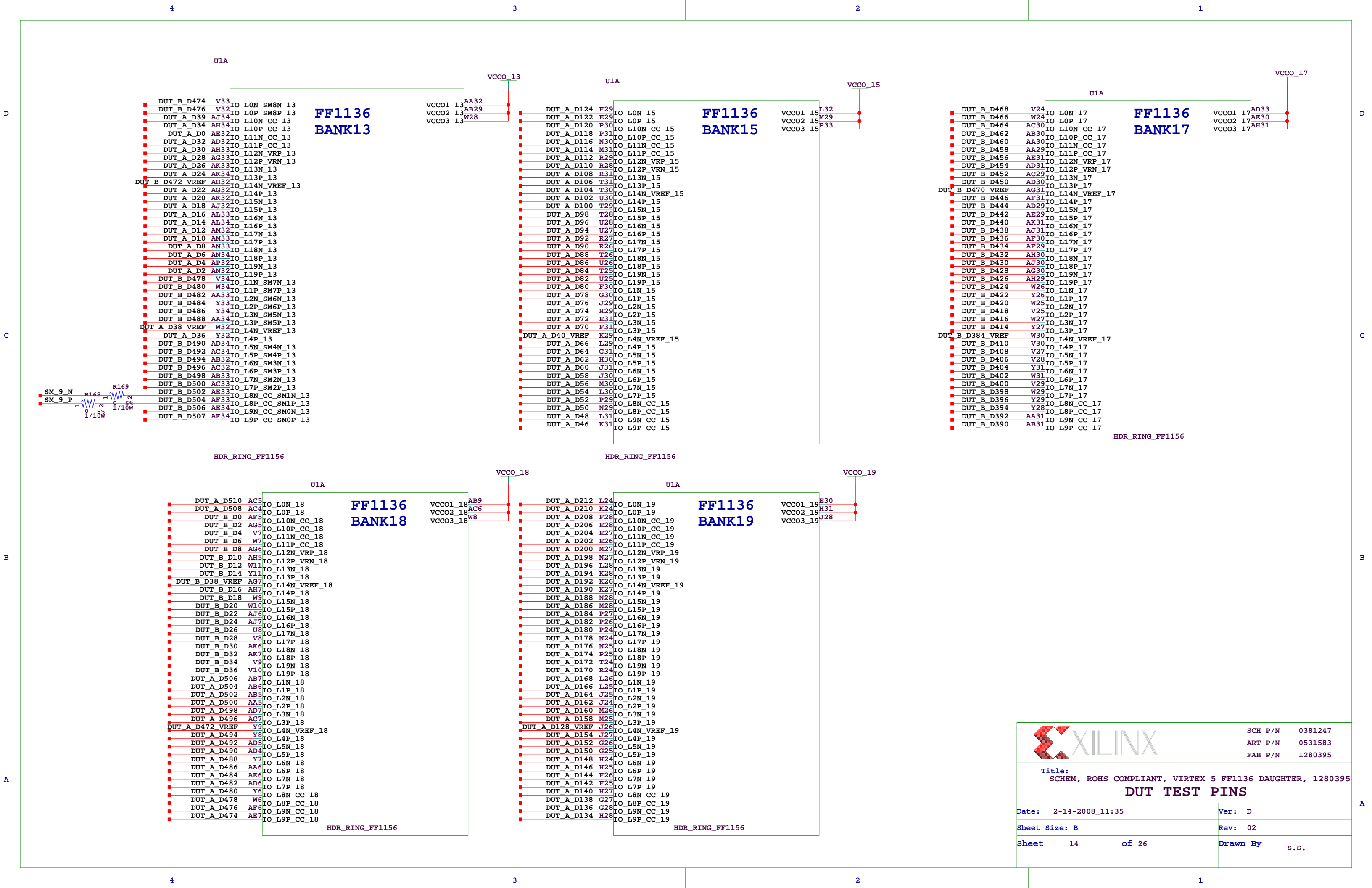


		SCH P/N	0381247
		ART P/N	0531583
		FAB P/N	1280395
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF1136 DAUGHTER, 1280395			
DUT INTERFACE			
Date: 2-14-2008_11:35		Ver: D	
Sheet Size: B		Rev: 02	
Sheet 11 of 26		Drawn By S.S.	




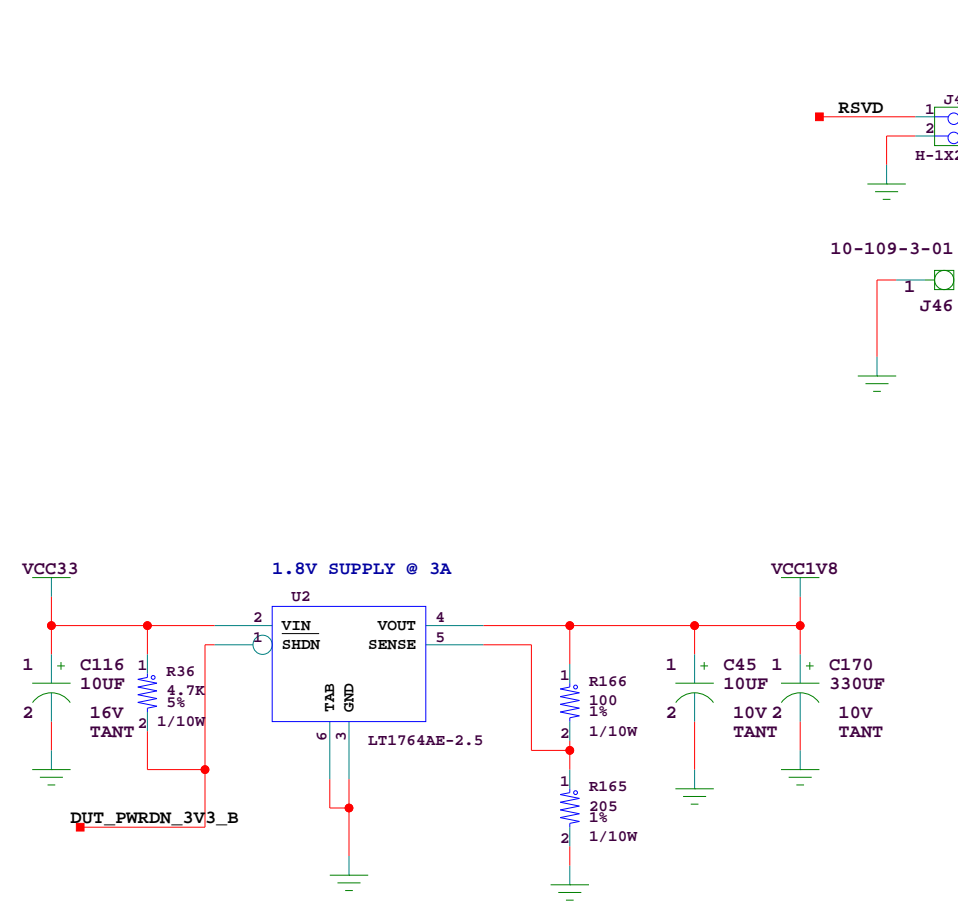
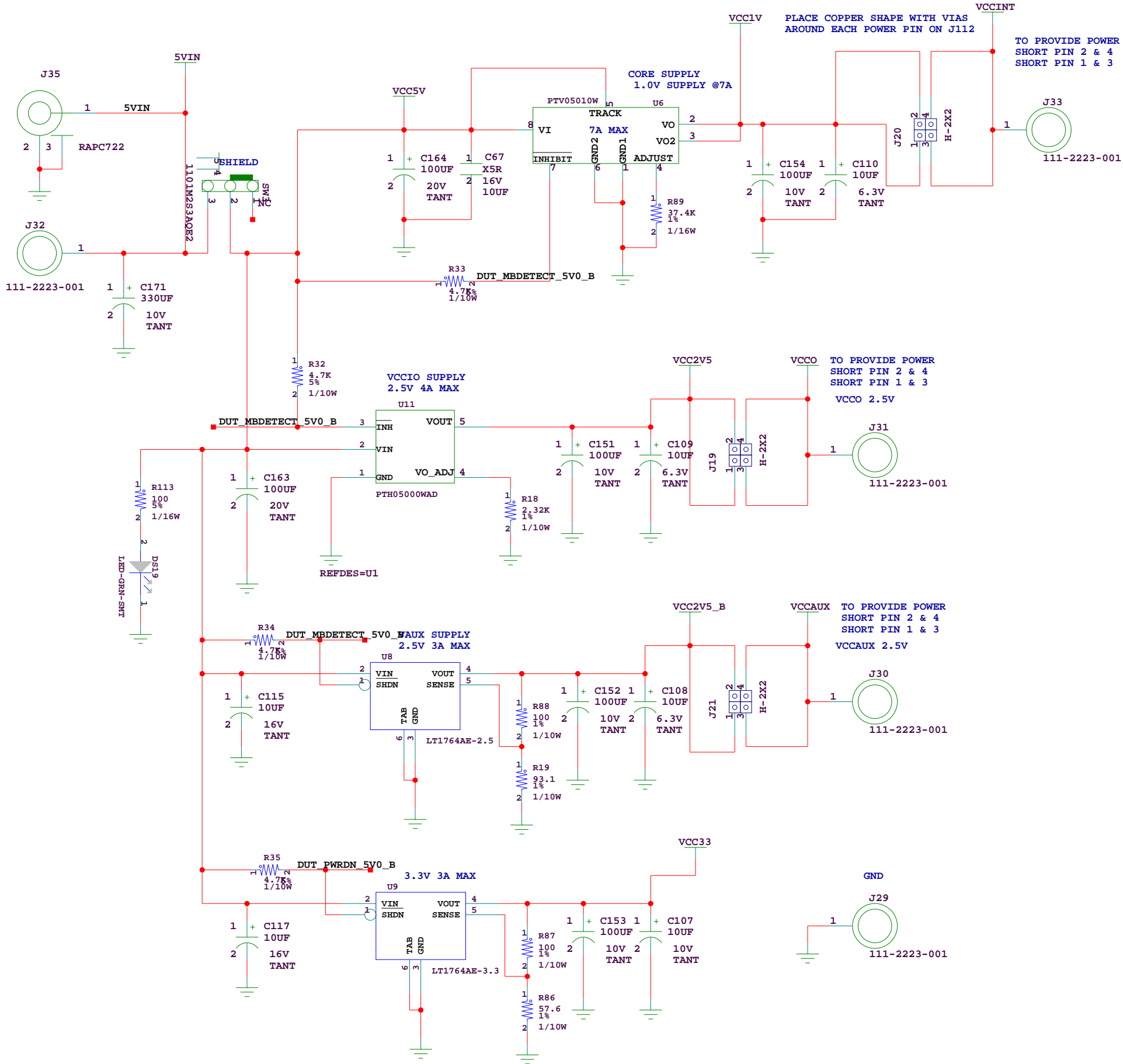
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		ART P/N	0531583
		FAB P/N	1280395
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF1136 DAUGHTER, 1280395			
FPGA DECOUPLING CAPACITORS			
Date:	2-14-2008_11:35	Ver:	D
Sheet Size:	B	Rev:	02
Sheet	12 of 26	Drawn By	s.s.







		SCH P/N	0381247
		ART P/N	0531583
		FAB P/N	1280395
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF1136 DAUGHTER, 1280395			
DUT TEST PINS			
Date: 2-14-2008_11:35		Ver: D	
Sheet Size: B		Rev: 02	
Sheet 15 of 26		Drawn By s.s.	



VCC I/O SELECTION

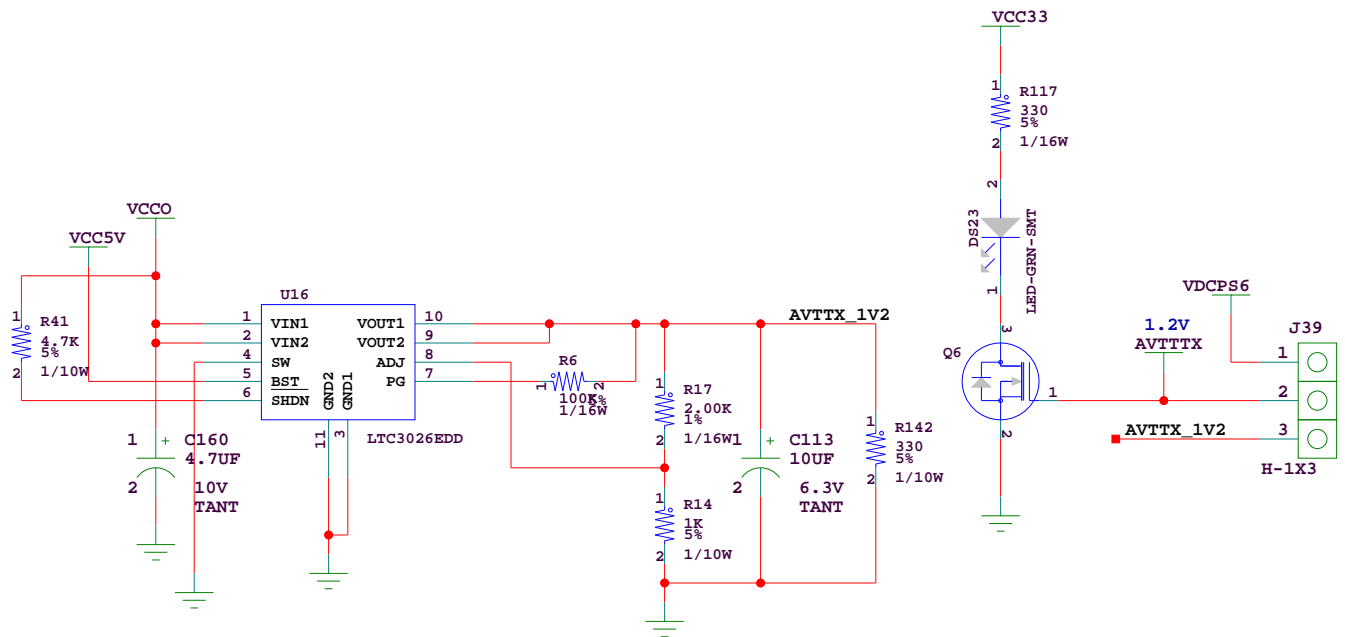
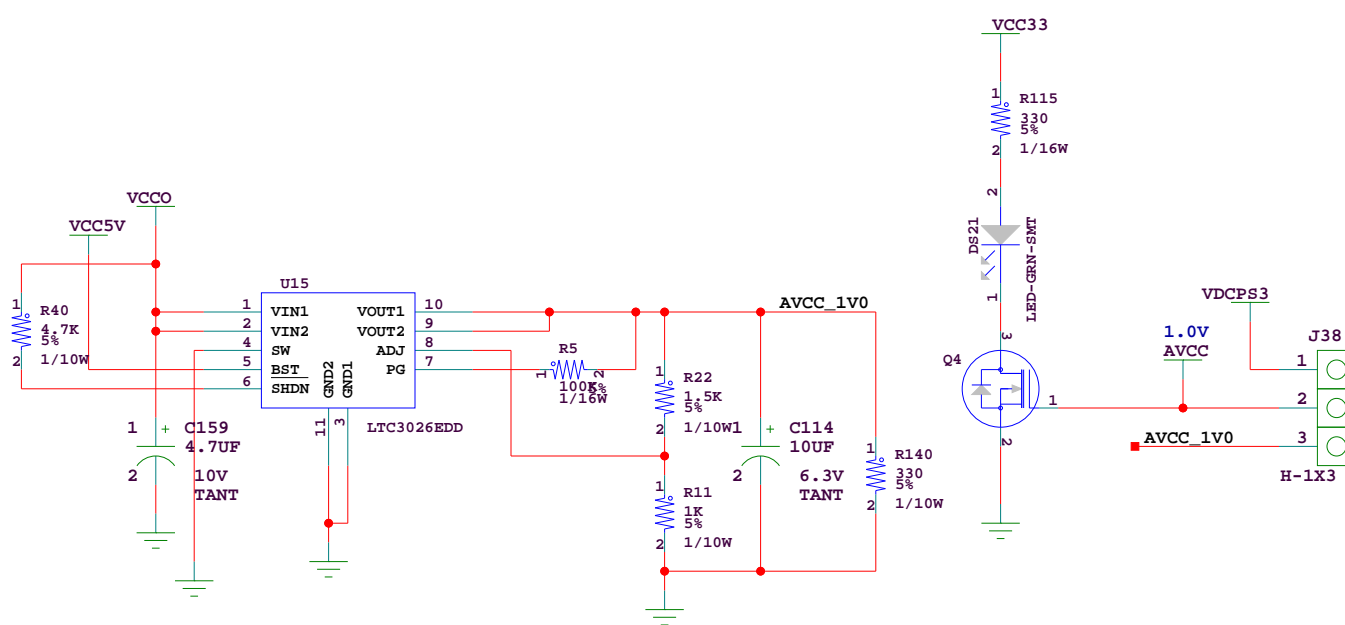
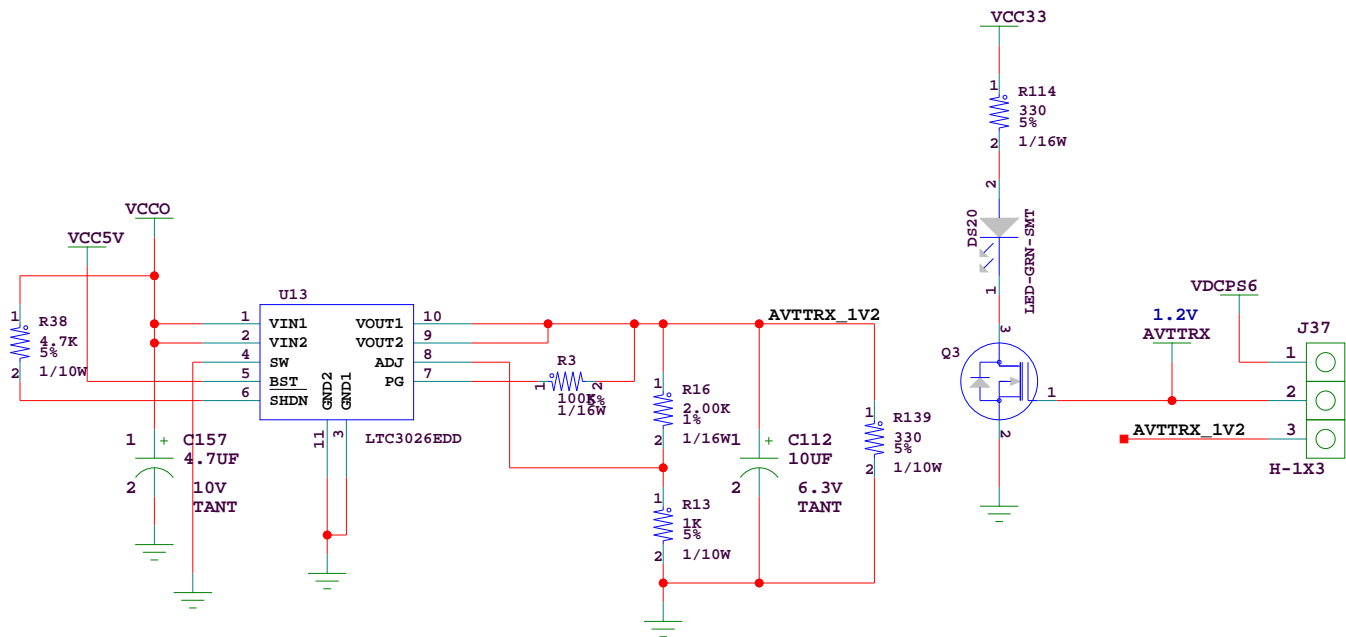
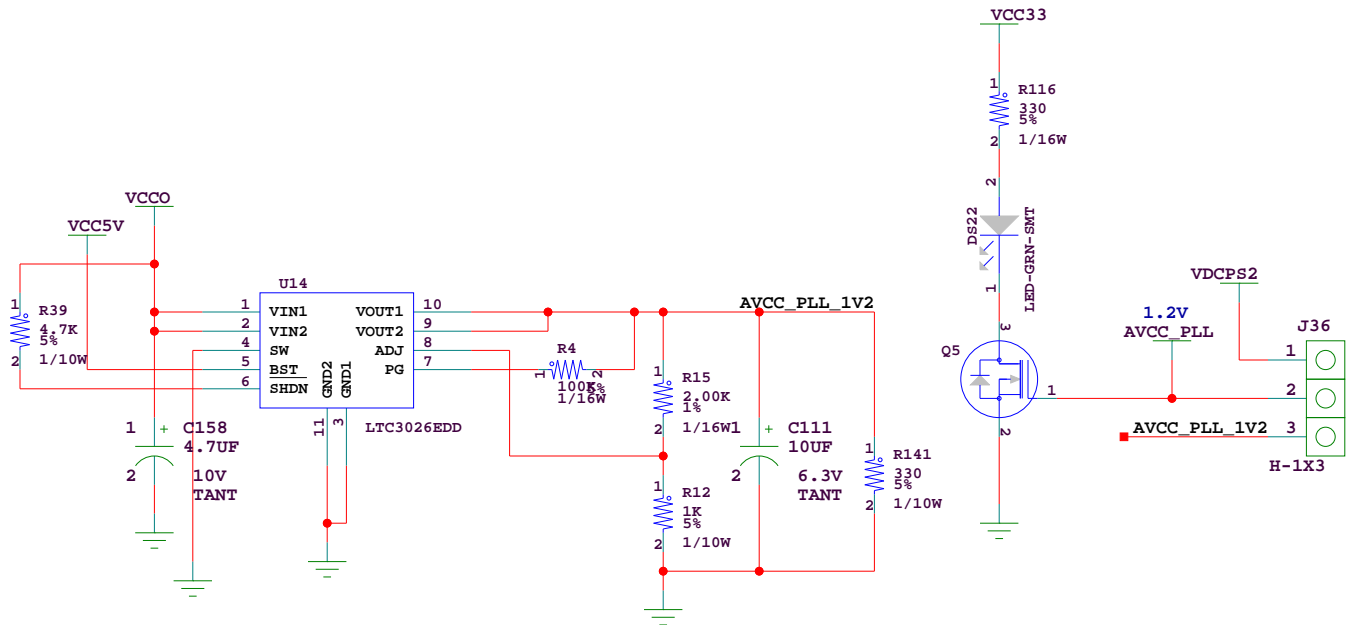
J44				J45				J34			
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VCCO_1	3	4		VCCO_1	3	4		VDCPS2	2		
VCCO_2	5	6		VCCO_2	5	6		VDCPS2	3		
VCCO_3	7	8		VCCO_3	7	8		VDCPS2	4		
VCCO_4	9	10		VCCO_4	9	10		VDCPS2	5		
VCCO_5	11	12		VCCO_5	11	12		VDCPS2	6		
VCCO_6	13	14		VCCO_6	13	14		VDCPS2	7		
VCCO_11	15	16		VCCO_11	15	16		VDCPS3	8		
VCCO_12	17	18		VCCO_12	17	18		VDCPS3	9		
VCCO_13	19	20		VCCO_13	19	20		VDCPS3	10		
VCCO_15	21	22		VCCO_15	21	22		VDCPS4	11		
VCCO_17	23	24		VCCO_17	23	24		VDCPS4	12		
VCCO_18	25	26		VCCO_18	25	26		VDCPS4	13		
VCCO_19	27	28		VCCO_19	27	28		VDCPS5	14		
VCCO_20	29	30		VCCO_20	29	30		VDCPS5	15		
VCCO_21	31	32		VCCO_21	31	32		VDCPS5	16		
VCCO_22	33	34		VCCO_22	33	34		VDCPS6	17		
VCCO_23	35	36		VCCO_23	35	36		VDCPS6	18		
VCCO_25	37	38		VCCO_25	37	38		VDCPS6	19		

SCH P/N0381247ART P/N0531583FAB P/N1280395

Title:
SCHEM, ROHS COMPLIANT, VIRTEX 5 FF1136 DAUGHTER, 1280395

FPGA POWER SUPPLY

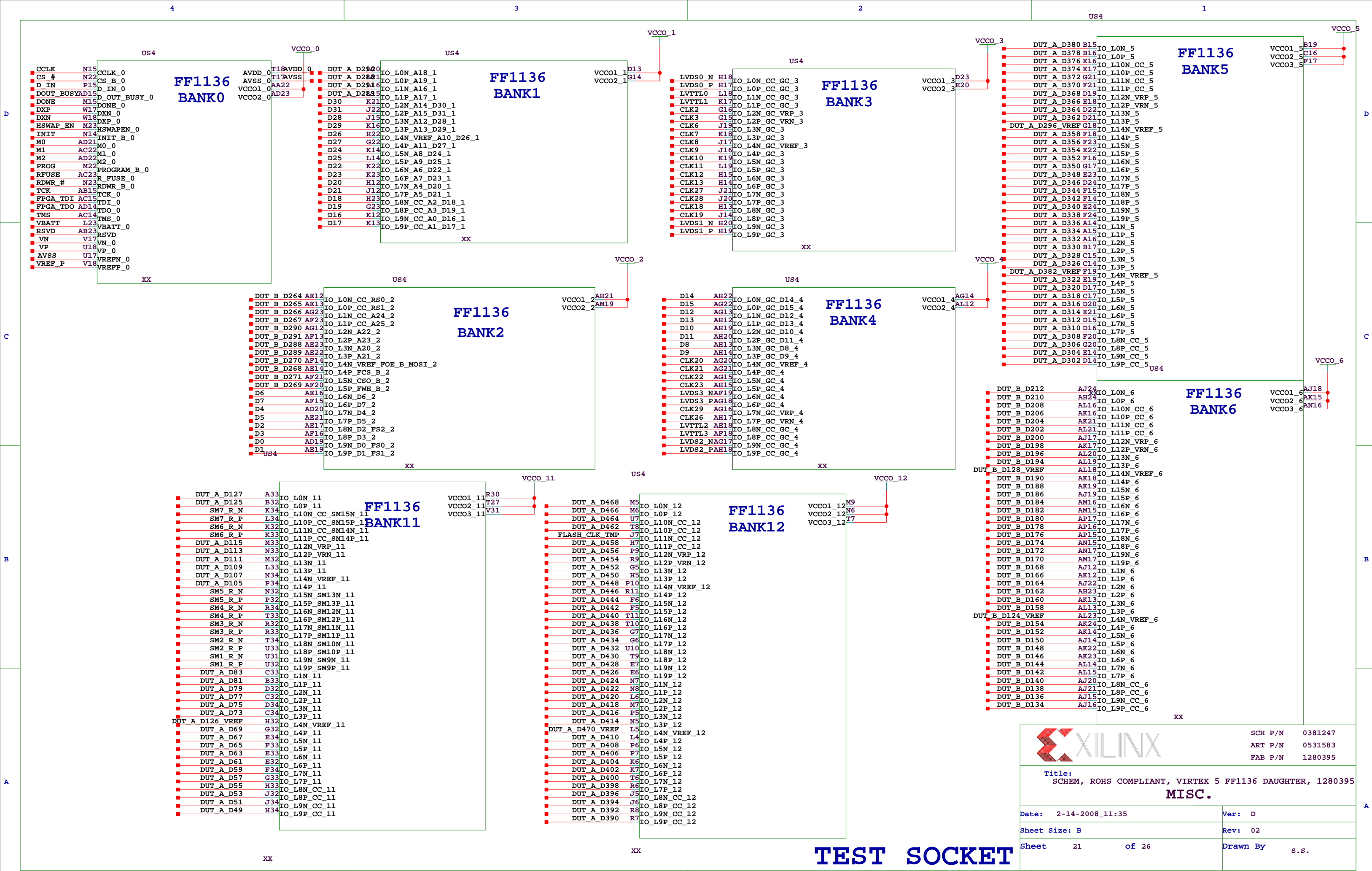
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Sheet Size:B	Rev:02
Sheet16of26	Drawn ByS.S.

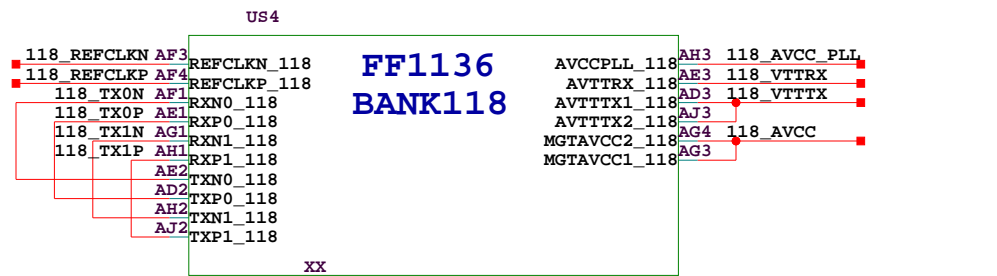
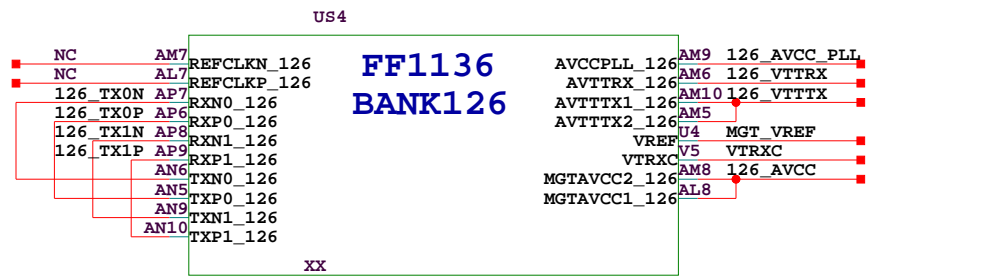
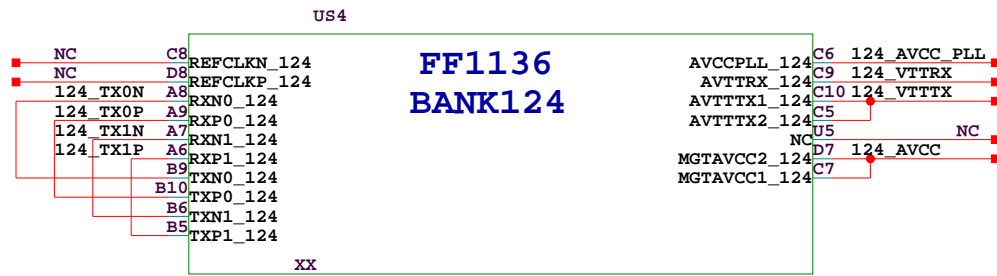
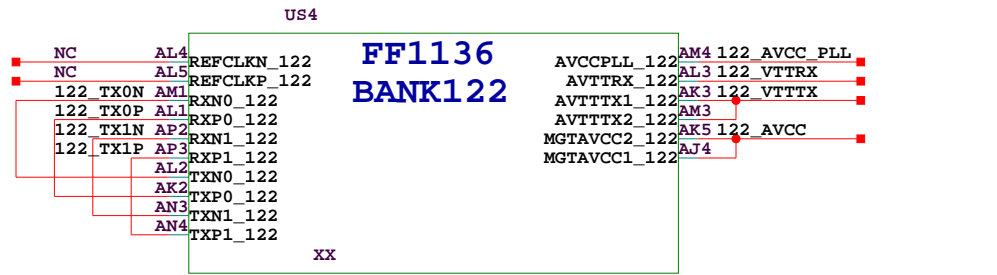
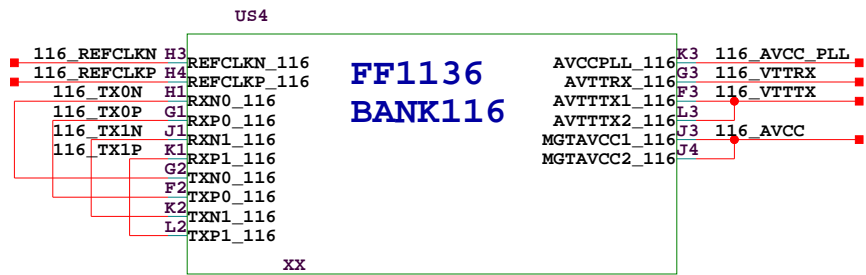
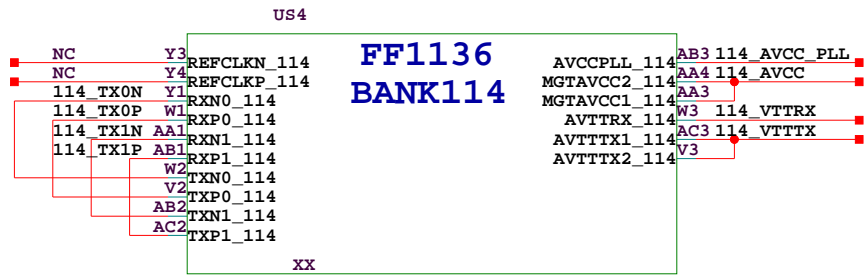
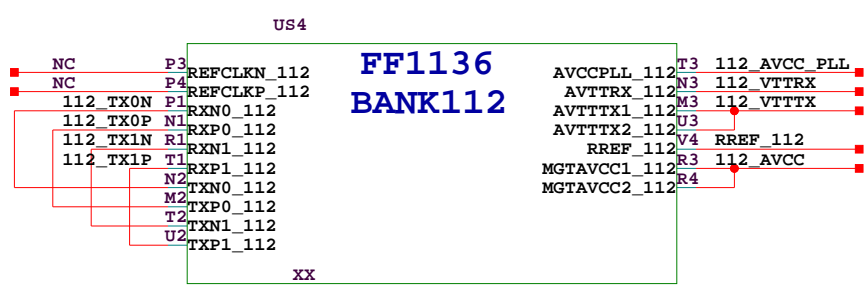
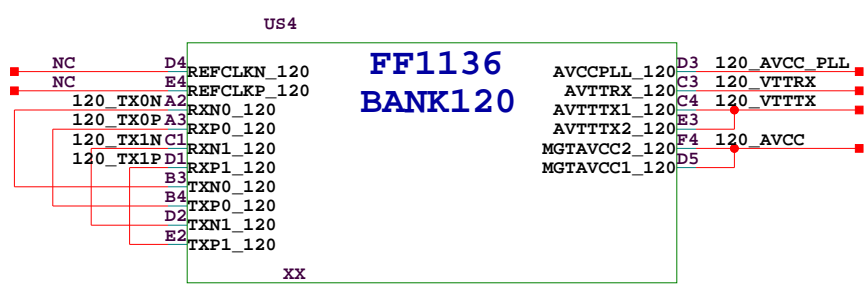


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ART P/N 0531583
FAB P/N 1280395


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SCHEM, ROHS COMPLIANT, VIRTEX 5 FF1136 DAUGHTER, 1280395
MGT POWER SUPPLY

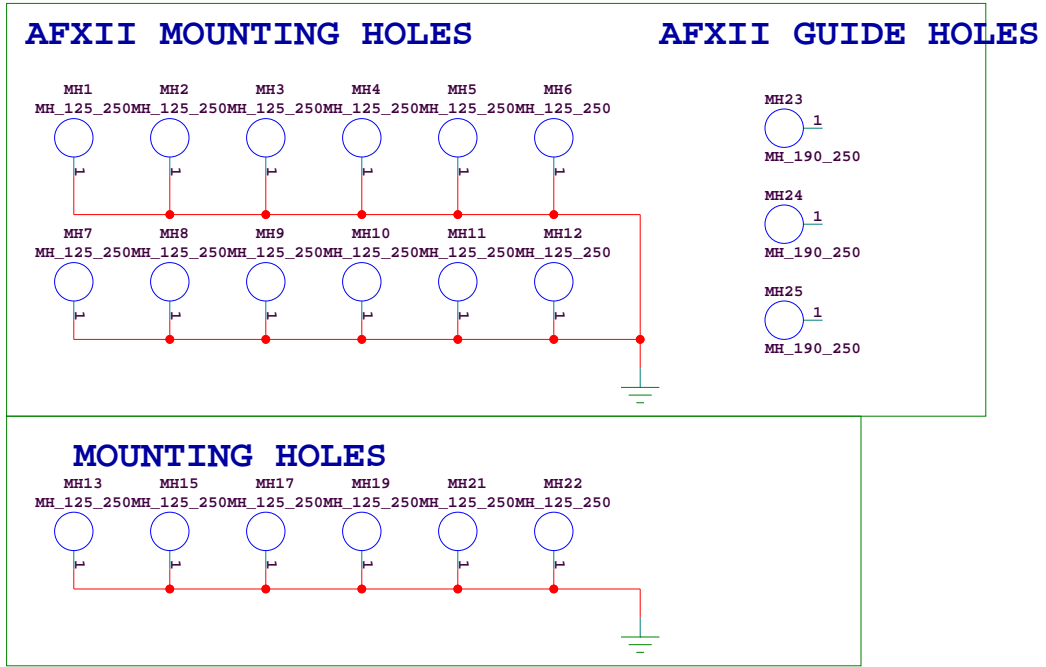
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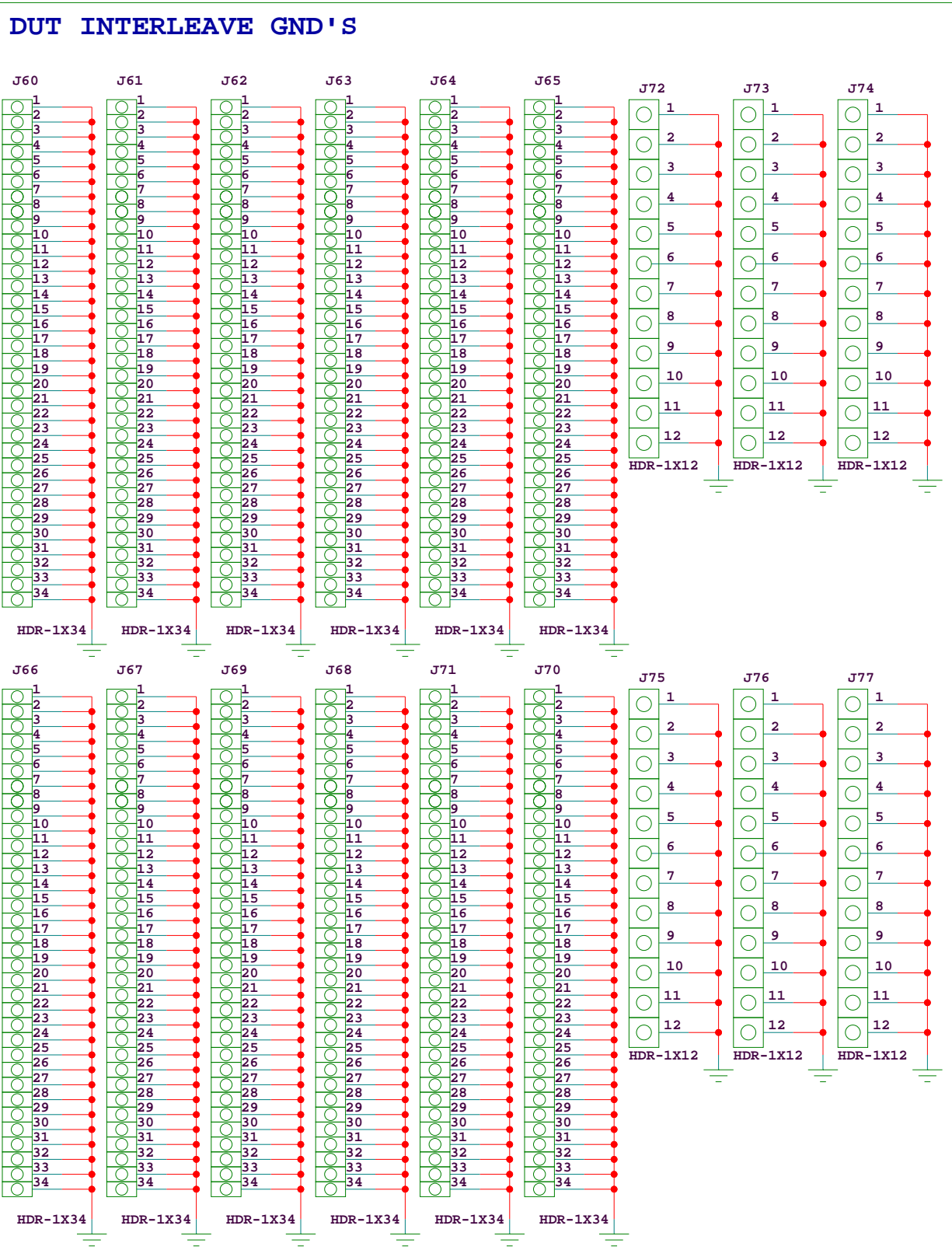
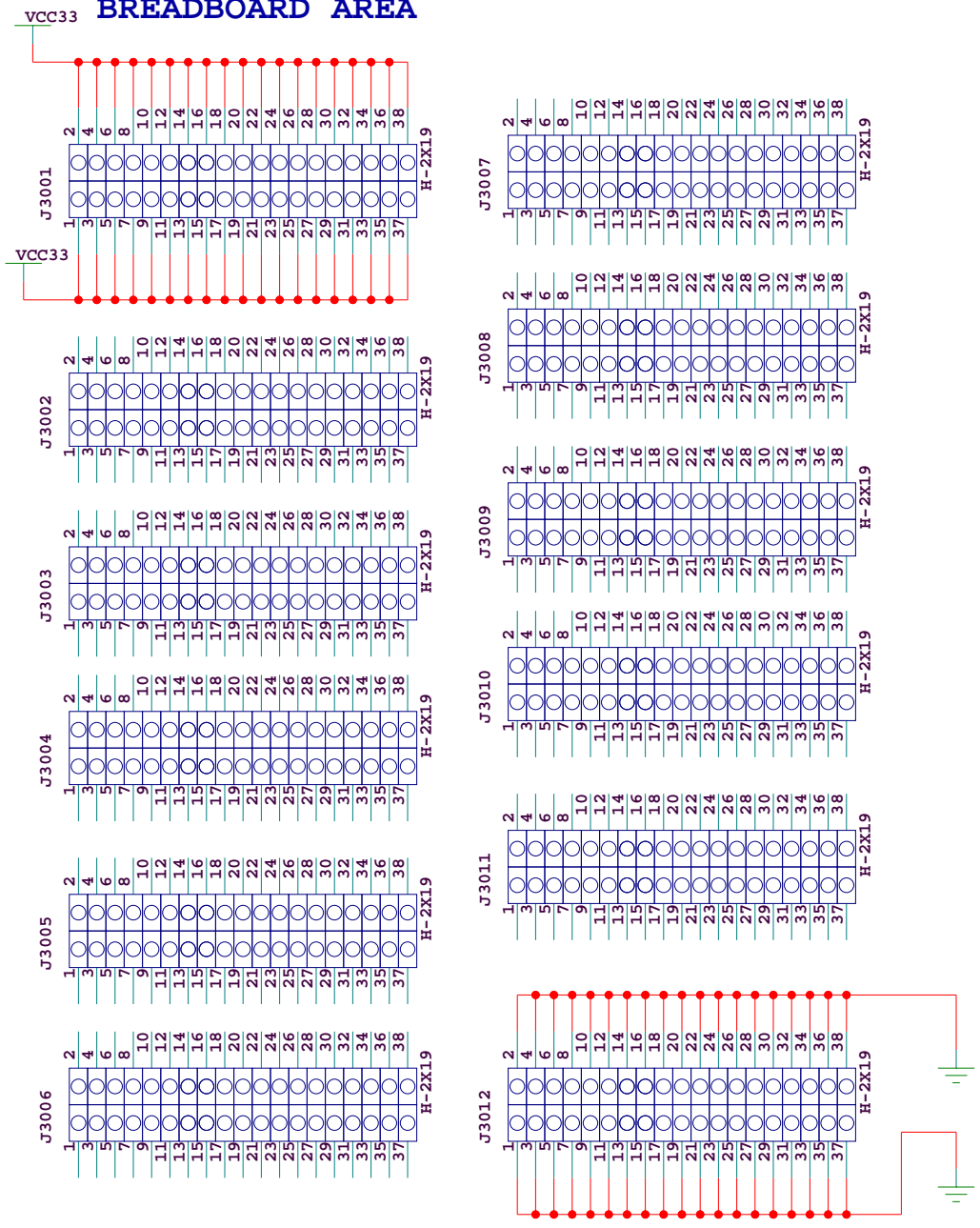



TEST SOCKET

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Sheet	24	of 26	Drawn By s.s.



BREADBOARD AREA





SCH P/N0381247

ART P/N0531583

FAB P/N1280395

Title:
SCHEM, ROHS COMPLIANT, VIRTEX 5 FF1136 DAUGHTER, 1280395

HARDWARE AND BREADBOARD AREA

Date:2-14-2008_11:35

Sheet Size: B

Sheet26of 26

Ver: D

Rev: 02

Drawn By s.s.