

PAGE 6  
System Monitor Aux

PAGE 3  
System Monitor

PAGE 2  
System Ace  
Upstream

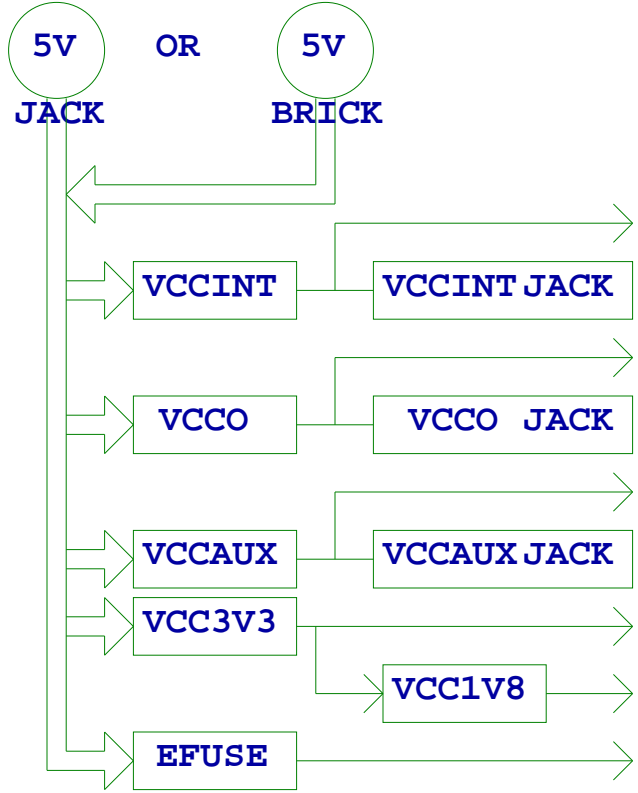
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Upstream Connector

PAGE 5  
Single Ended  
Socket Clocks  
2X

PAGE 5  
Differential  
SMA Clocks  
2X

PAGE 11

Power Bus and Switches



**Virtex 5**  
FF324  
DUT

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PAGE 2  
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ALL DUT I/O TEST POINTS

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System Ace  
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PAGE 2

Downstream Connector

PAGE 2

Single Ended  
Socket Clocks  
2X

PAGE 5

Differential  
SMA Clocks  
2X

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PAGES 9-10



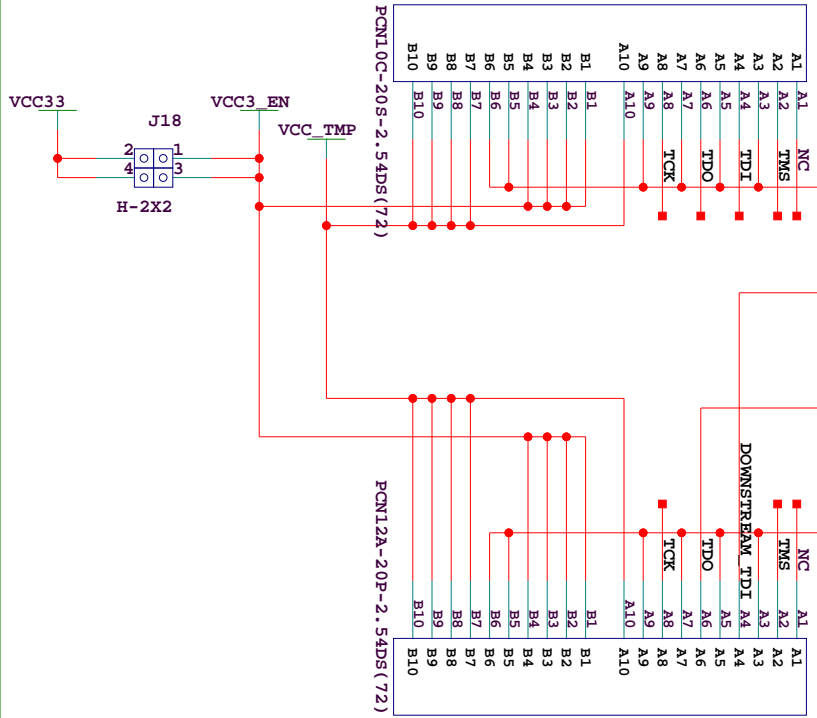
SCH P/N 0381320-01  
ART P/N 0531589-01  
FAB P/N 1280401-01

Title:  
SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401

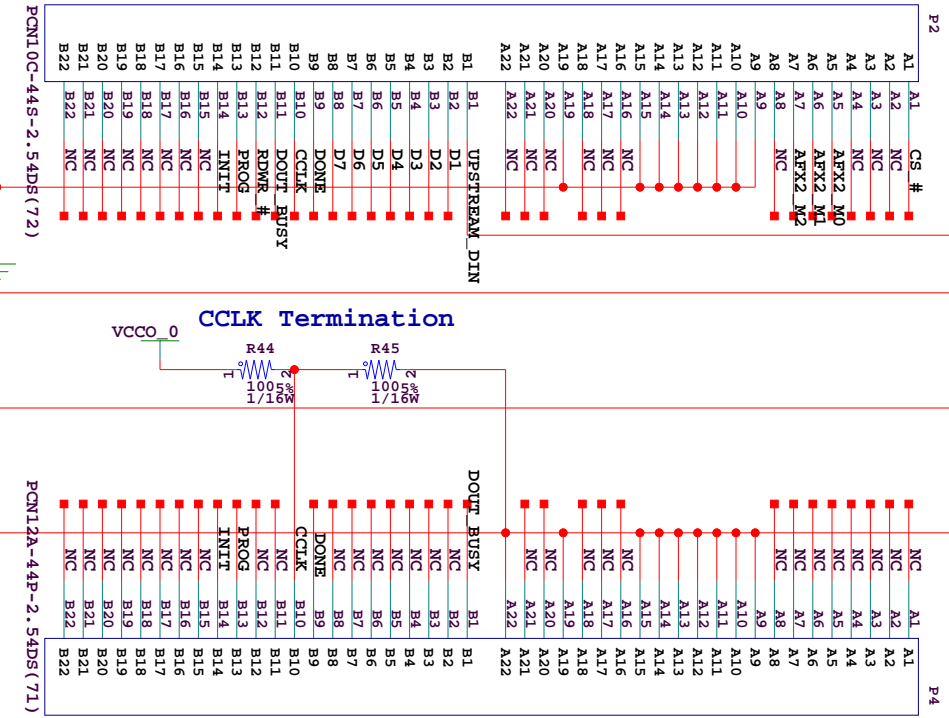
**BLOCK DIAGRAM**

Date: 1-11-2006_11:25	Ver: B
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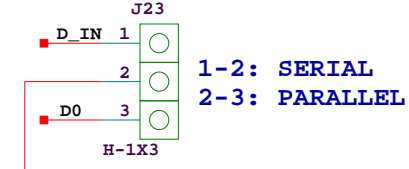
**SYSTEM ACE UPSTREAM**



**UPSTREAM CONNECTORS**

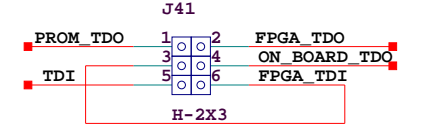


**DOWNSTREAM CONFIG**



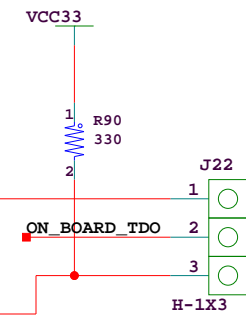
**ON BOARD JTAG CHAIN SELECTION**

PROM JTAG    FPGA JTAG  
 1-3: Enable    2-4: Enable  
 3-5: Disable    4-6: Disable

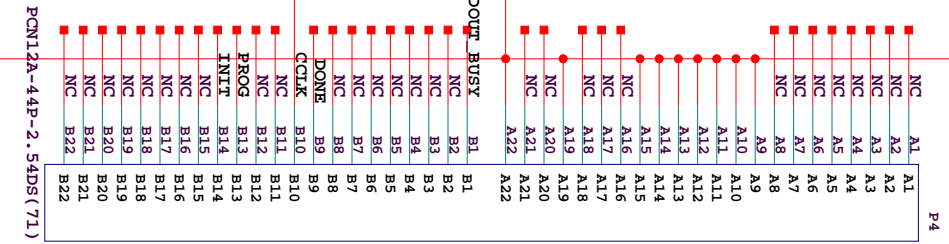
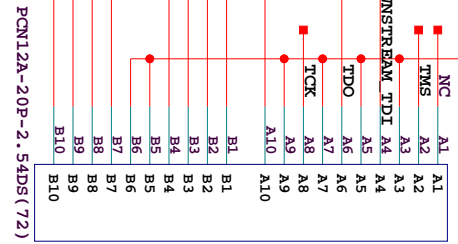


1-2: SERIAL CHAINING TO NEXT BOARD  
 2-3: TERMINATION OF LAST BOARD IN THE CHAIN

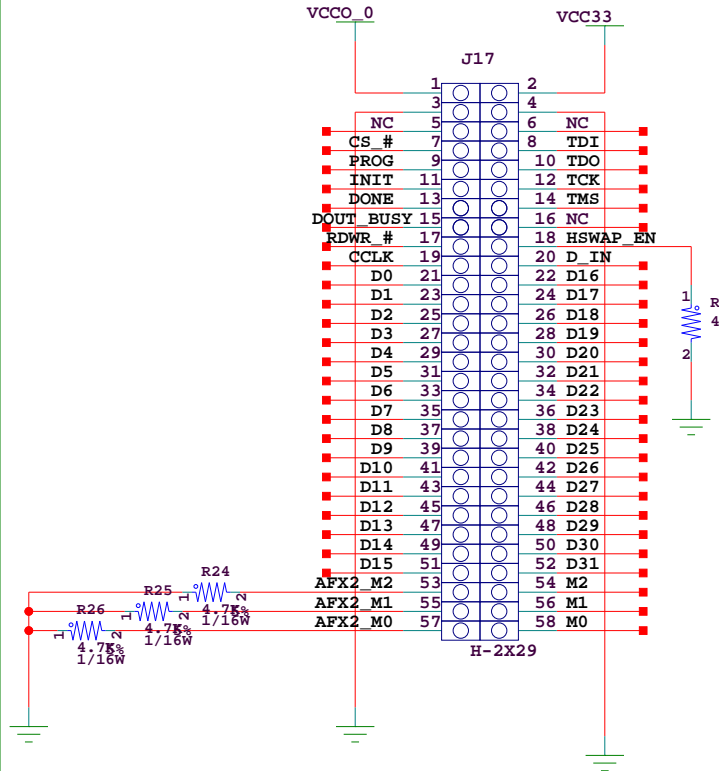
**JTAG JUMPER**



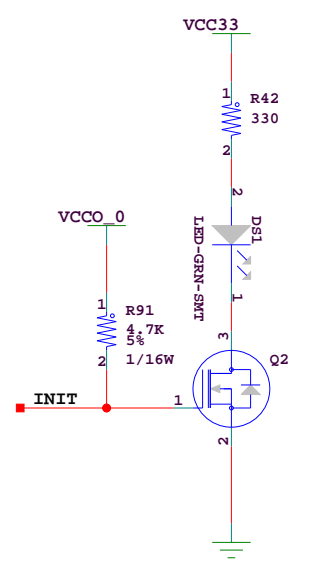
**SYSTEM ACE DOWNSTREAM DOWNSTREAM CONNECTORS**



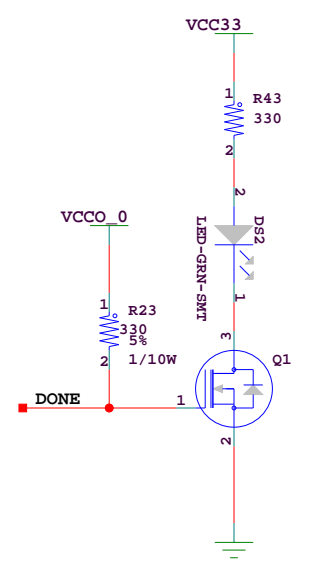
**FLYING WIRE CONFIGURATION PORT**



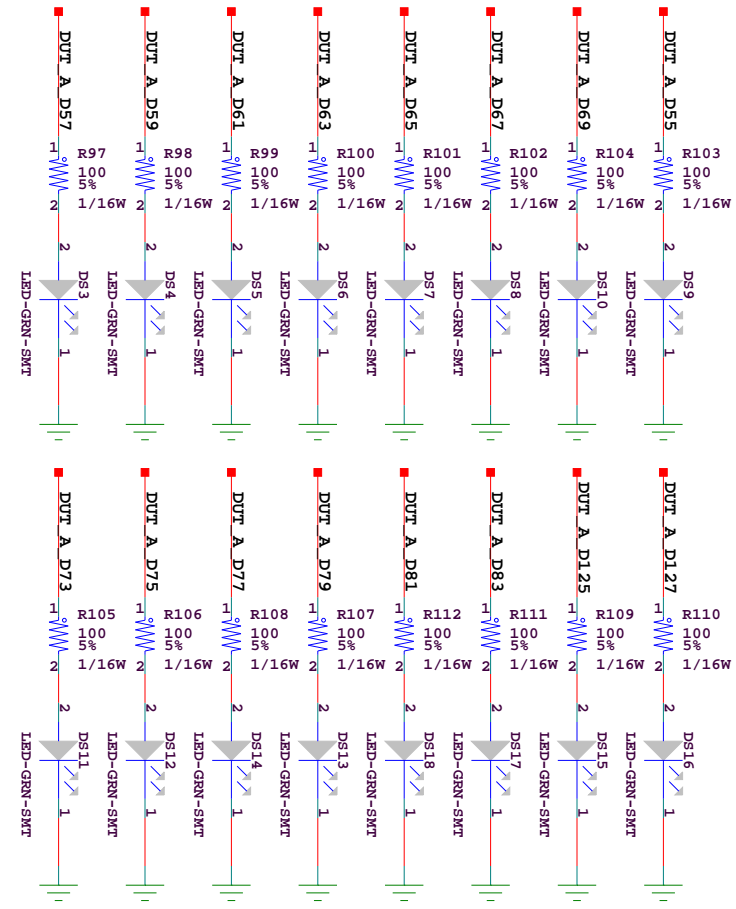
**INIT LED**



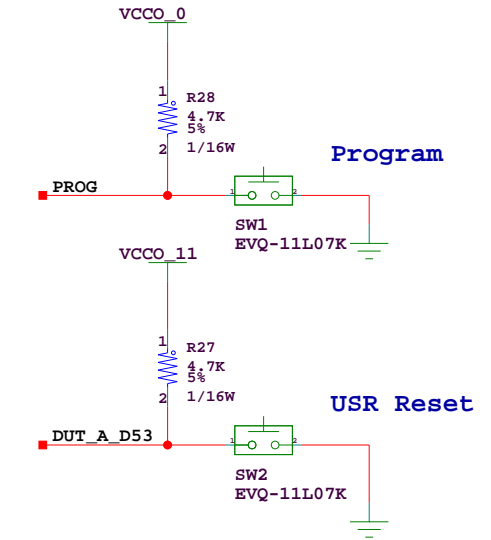
**DONE LED**



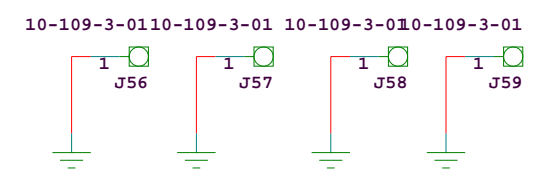
**USER LED'S**



**SWITCHES**



**TEST POINTS**



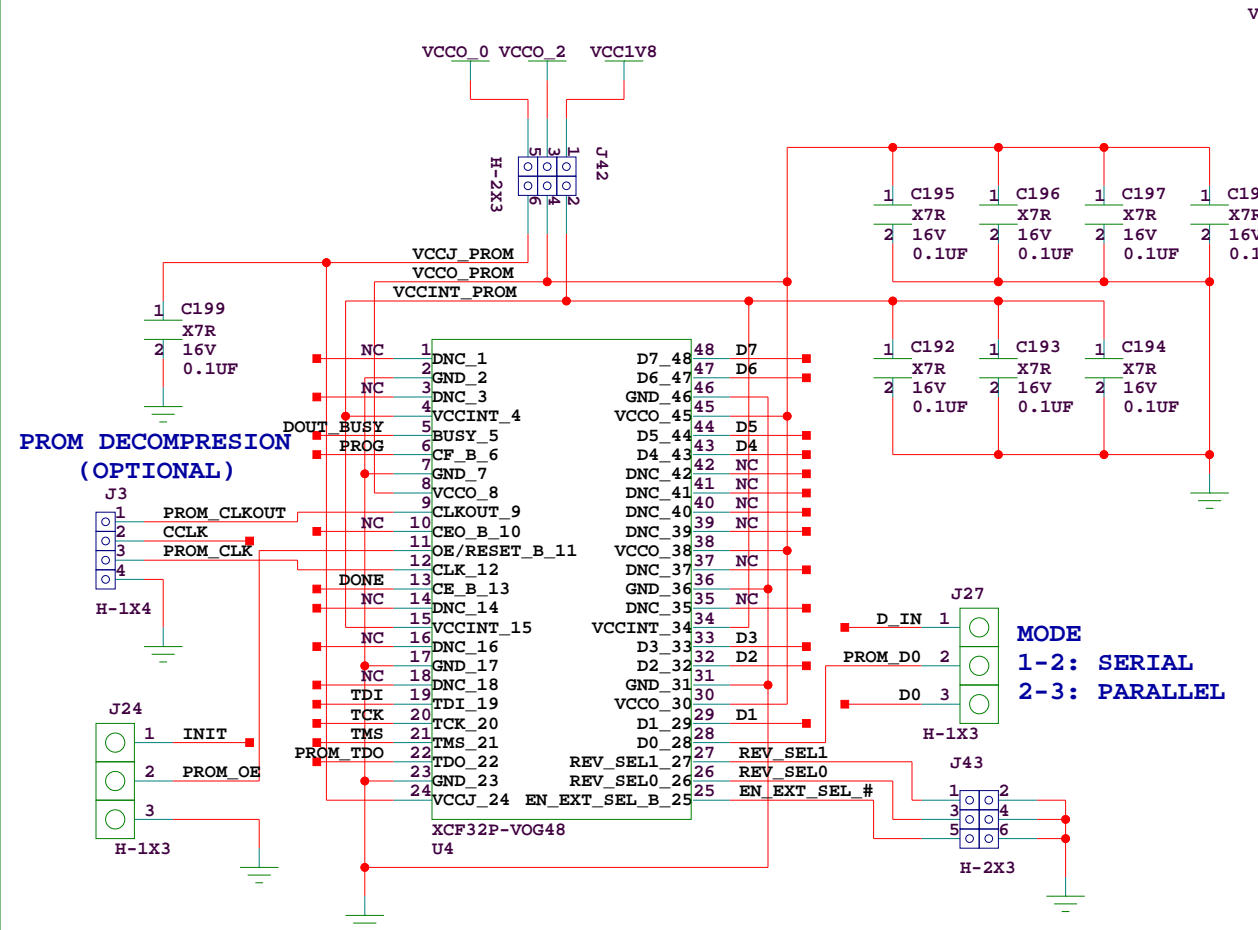
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SCH P/N 0381320-01  
 ART P/N 0531589-01  
 FAB P/N 1280401-01

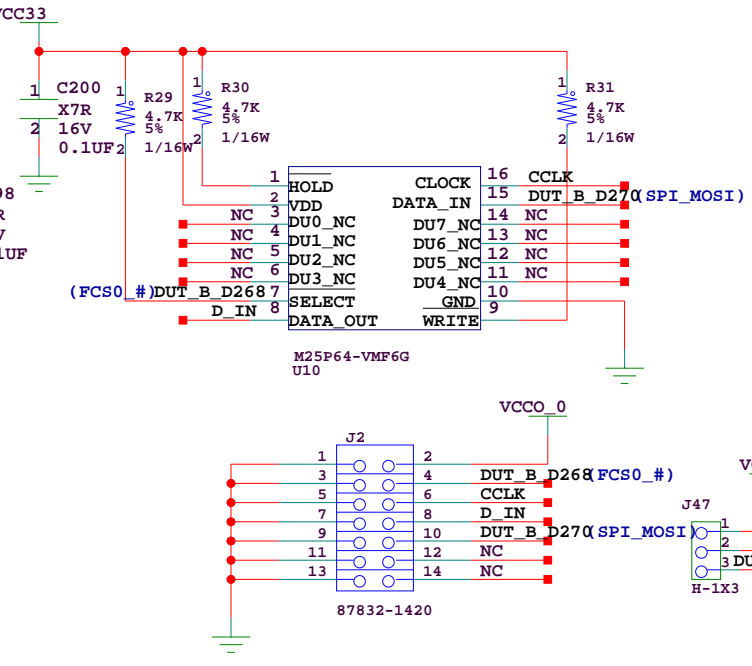
Title: SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401  
**DIN CONN, PORTS, STATUS LEDS, SWITCHES**

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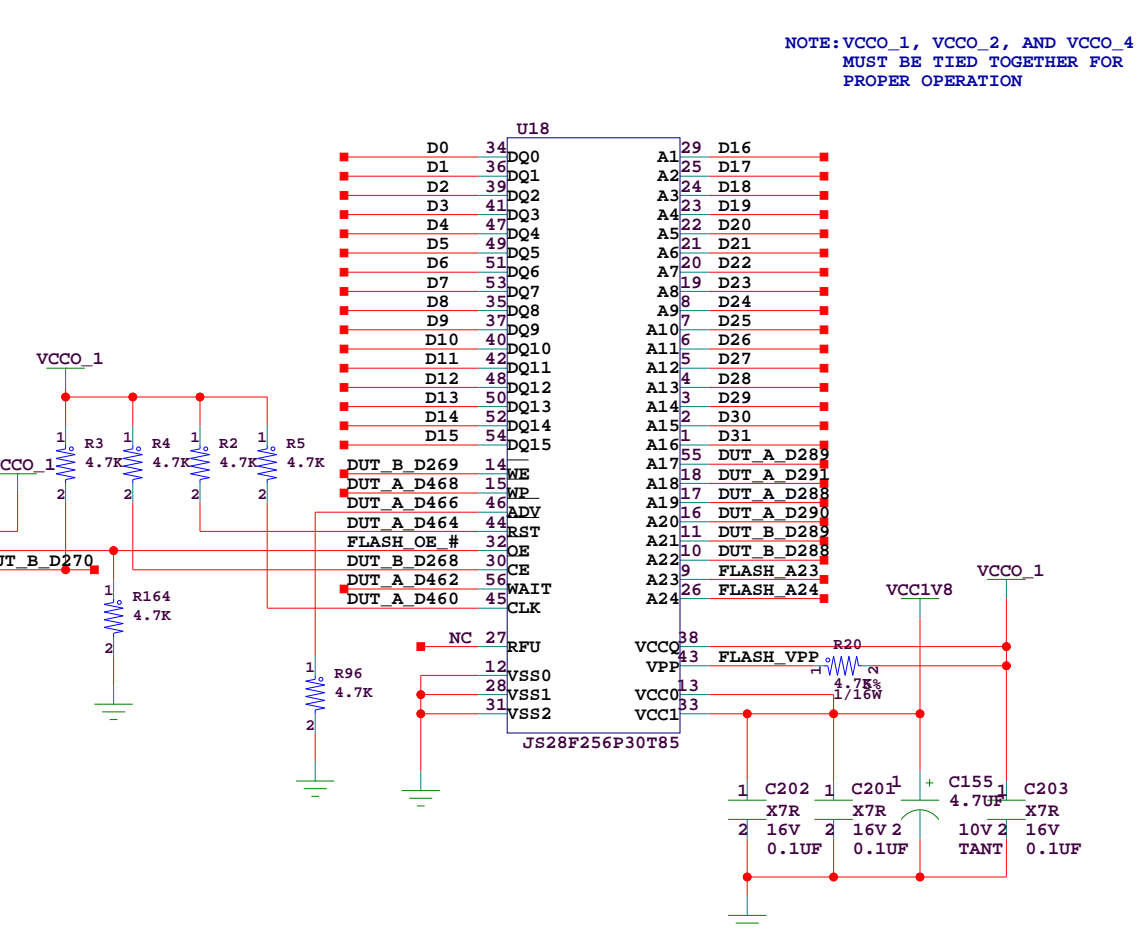
### CONFIGURATION PROM



### SPI INTERFACE

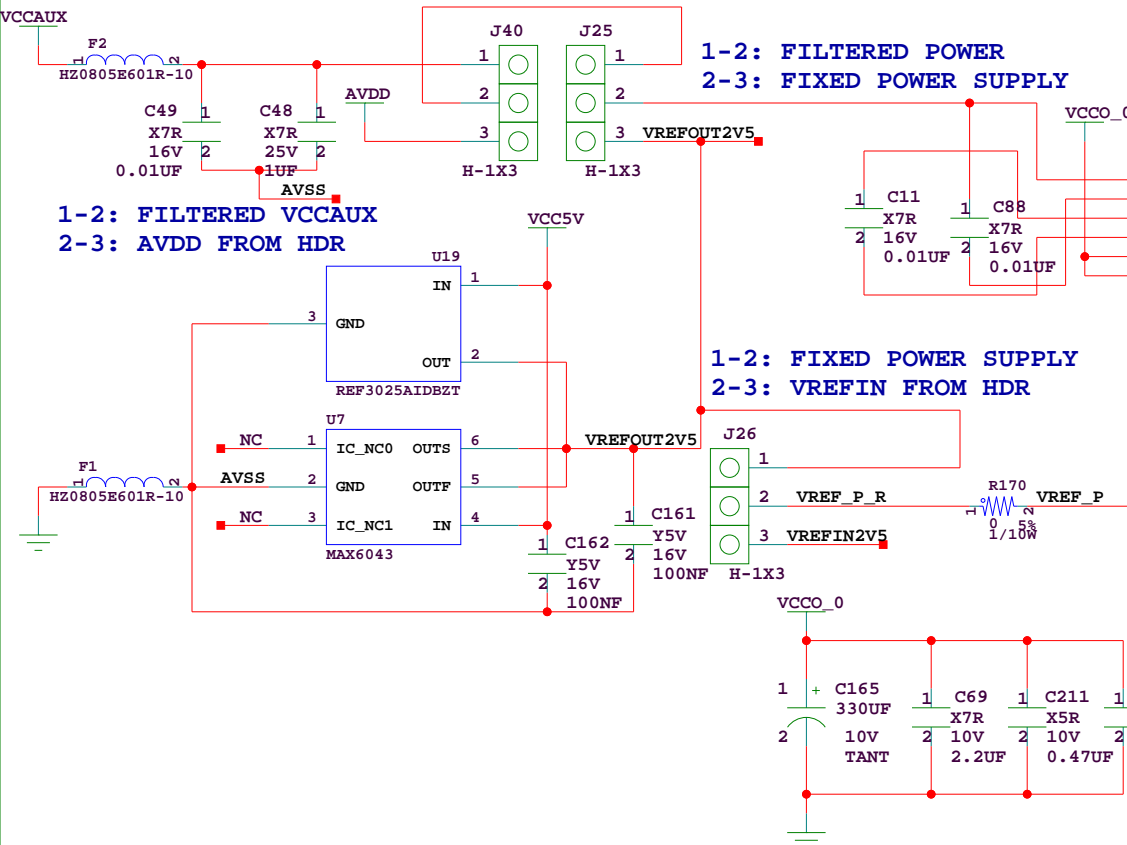


### BPI INTERFACE

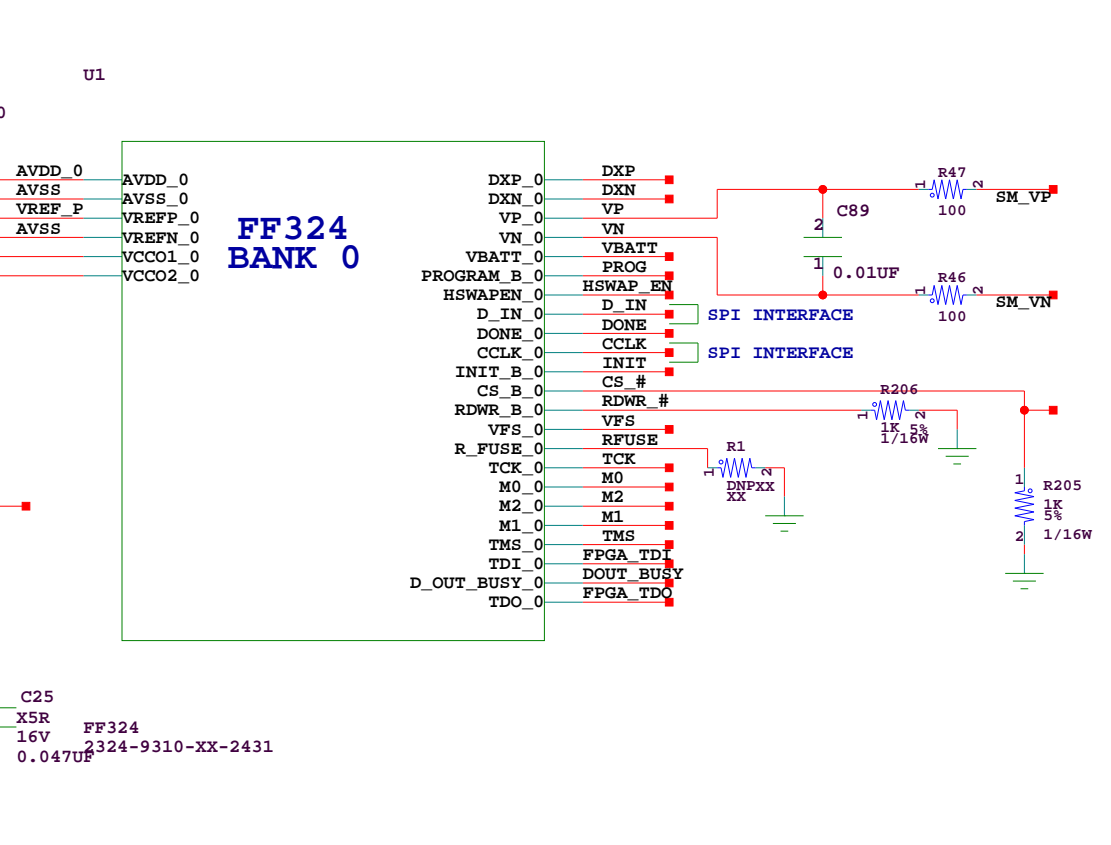


NOTE: VCC0\_1, VCC0\_2, AND VCC0\_4 MUST BE TIED TOGETHER FOR PROPER OPERATION

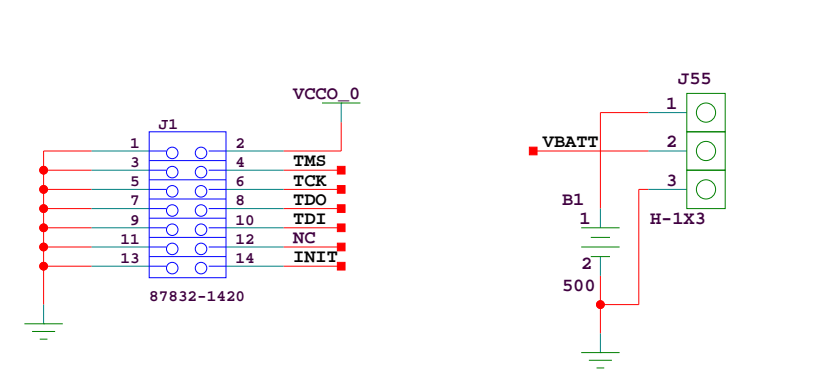
### SYSTEM MONITOR SUPPLY



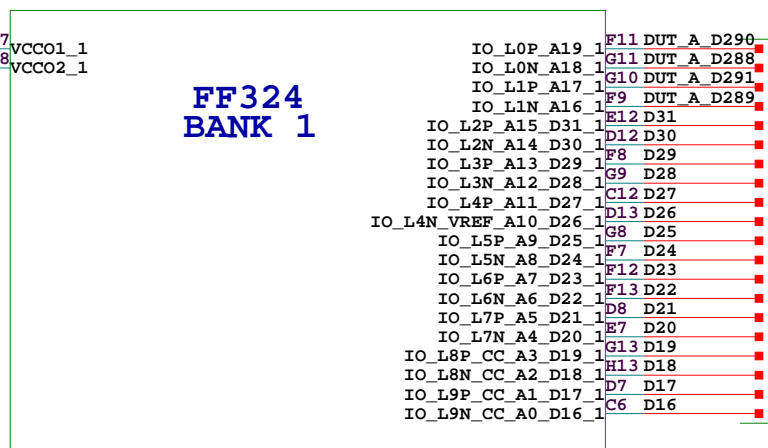
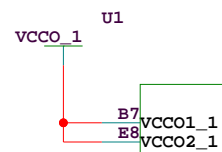
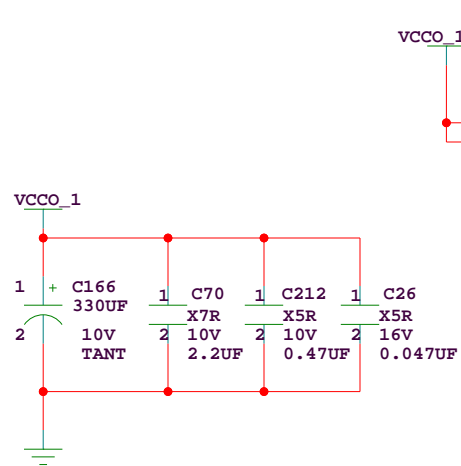
### FPGA BANK0 CONFIGURATION



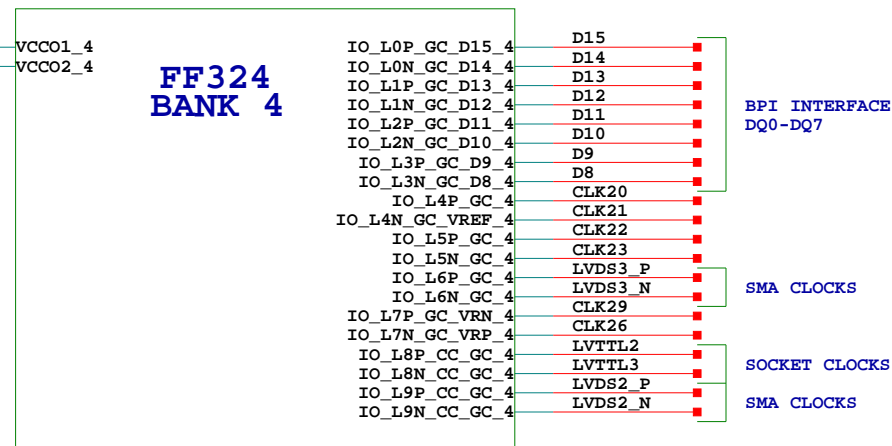
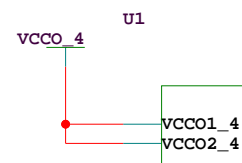
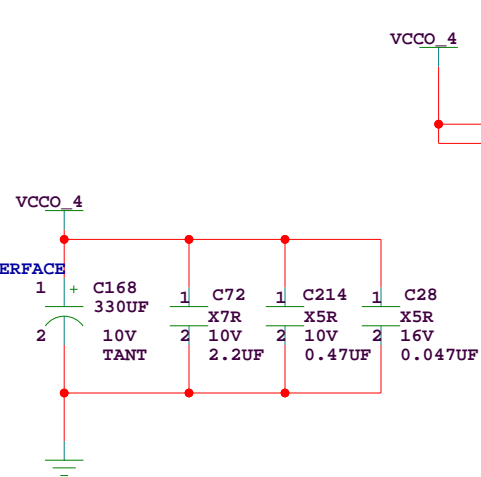
### PARALLEL 4 CABLE CONNECTOR VBATT Supply



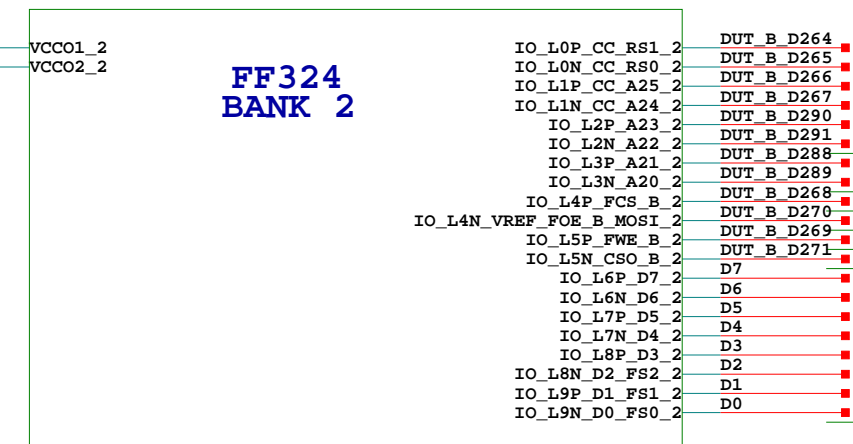
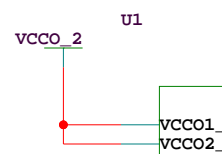
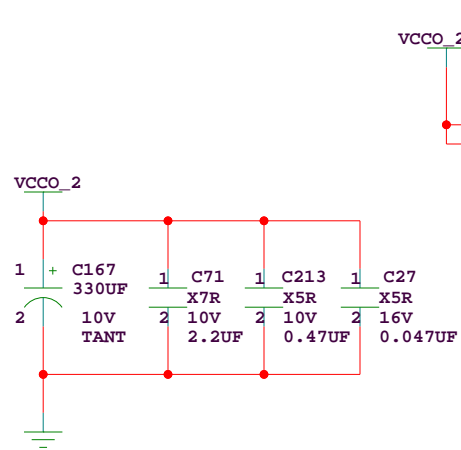
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		ART P/N	0531589-01
		FAB P/N	1280401-01
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401			
<b>CONFIGURATION</b>			
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Sheet Size:	B	Rev:	01
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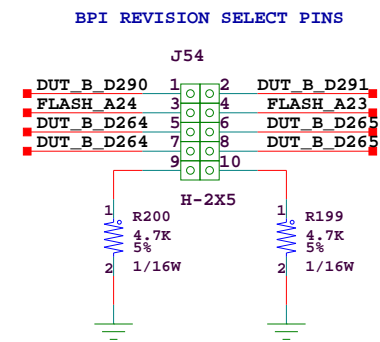
FF324  
2324-9310-XX-2431



2324-9310-XX-2431  
FF324



FF324  
2324-9310-XX-2431



- 1-3: Selects ADDR23 from FPGA to FLASH ADDR24
- 3-5: Selects RS1 from FPGA to FLASH ADDR24
- 7-9: Pulldown for RS applications
- 2-4: Selects ADDR22 from FPGA to FLASH ADDR23
- 4-6: Selects RS0 from FPGA to FLASH ADDR23
- 8-10: Pulldown for RS applications



SCH P/N 0381320-01  
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FAB P/N 1280401-01

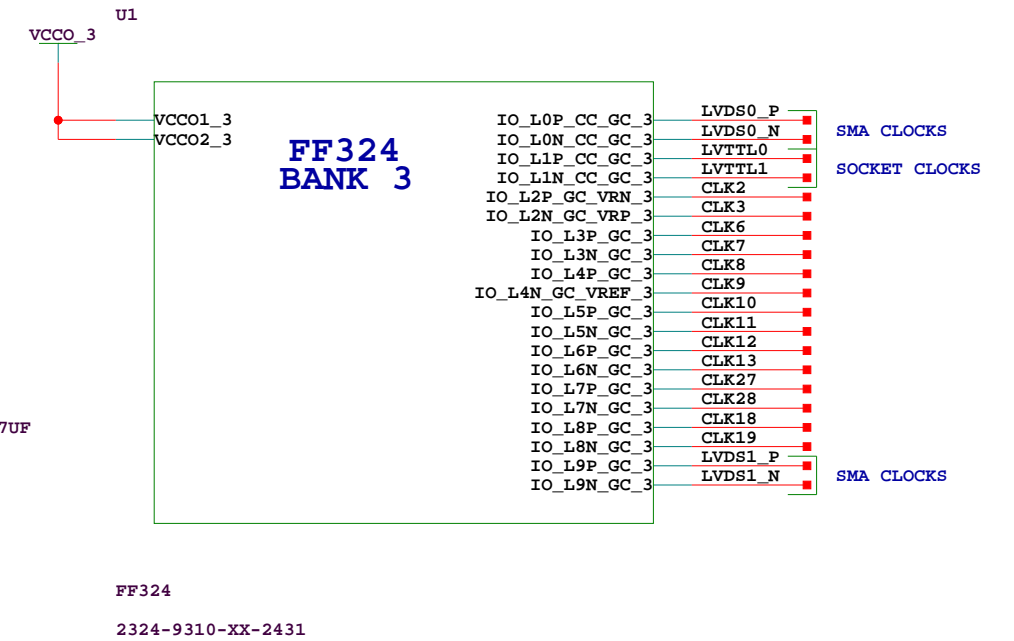
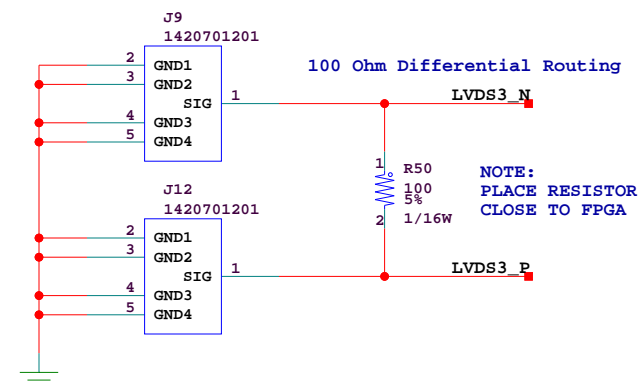
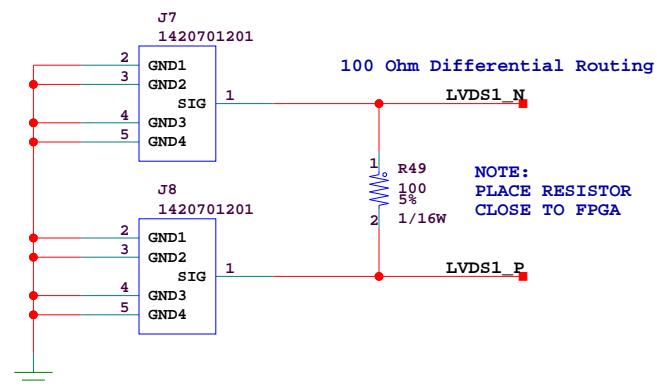
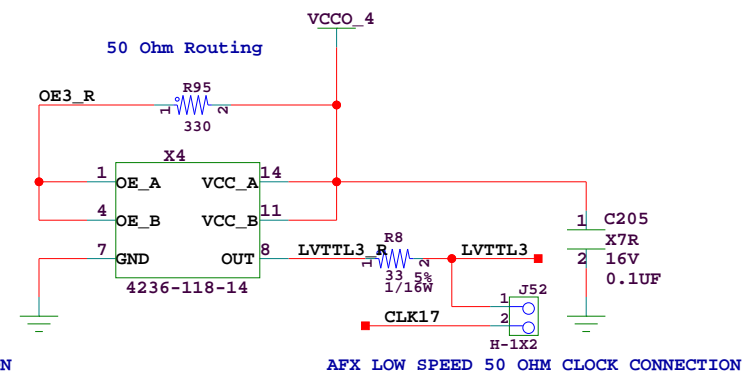
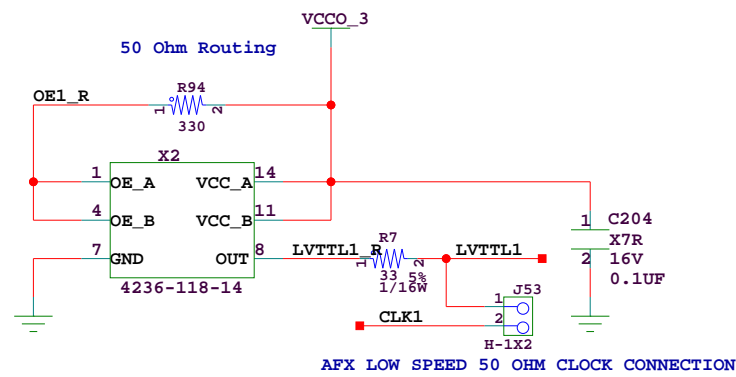
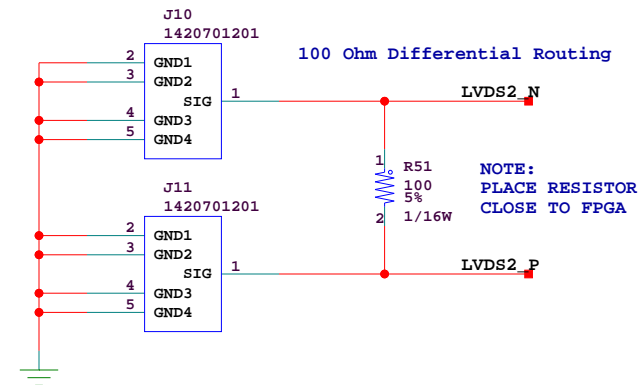
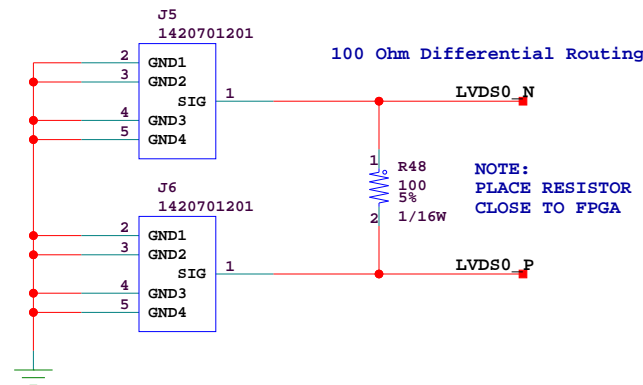
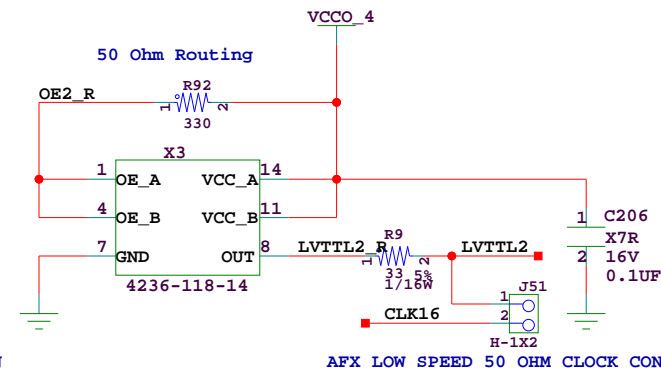
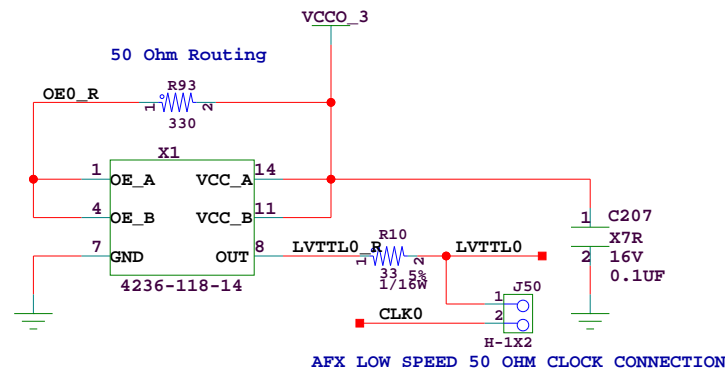
Title:  
SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401

**CONFIGURATION**

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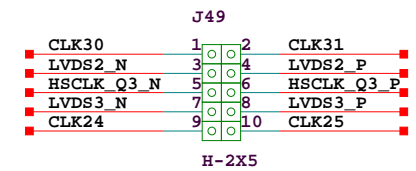
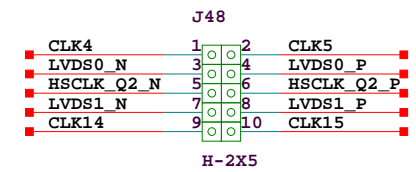
## UPPER CLOCKS

## BOTTOM CLOCKS



## AFX CLOCK CONFIGURATION

- 1-3, 2-4: LOW SPEED 50 OHM CLOCK CONNECTION
- 3-5, 4-6: HIGH SPEED 100 OHM DIFFERENTIAL CLOCK CONNECTION TO DIFFERENTIAL PAIR
- 5-7, 6-8: HIGH SPEED 100 OHM DIFFERENTIAL CLOCK CONNECTION TO DIFFERENTIAL PAIR
- 7-9, 8-10: LOW SPEED 50 OHM CLOCK CONNECTION



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Title: SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401  
**SOCKET CLOCKS, SMA DIFF CLOCKS**

Date: 7-20-2006\_10:33

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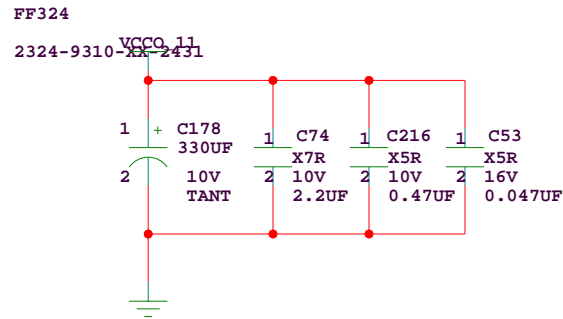
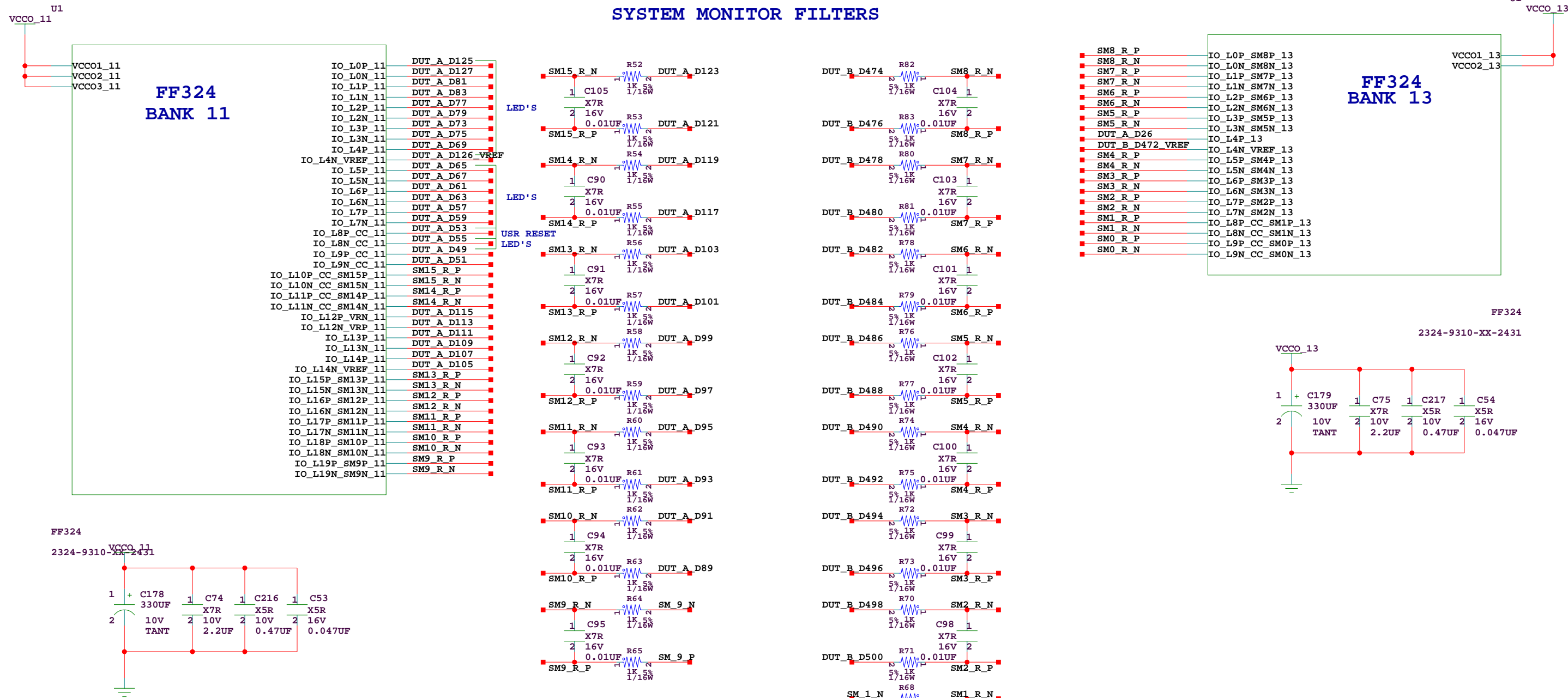
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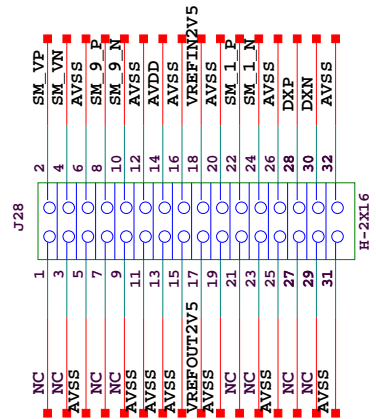
Sheet 5 of 17

Drawn By D.L.

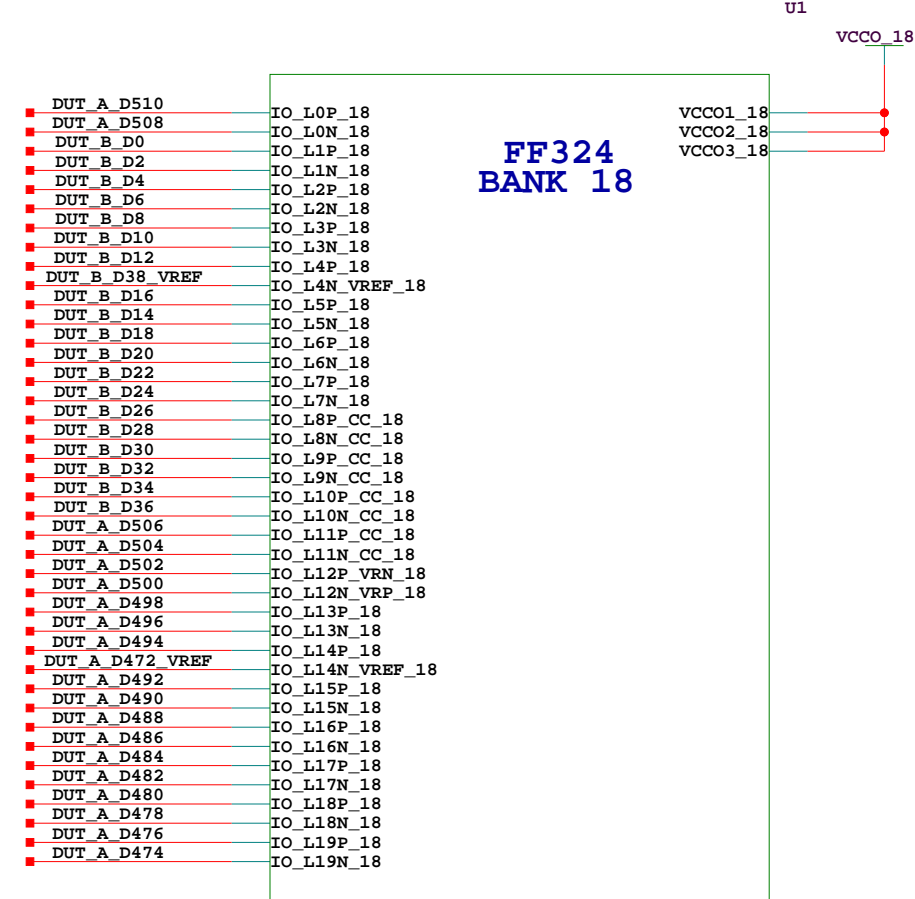
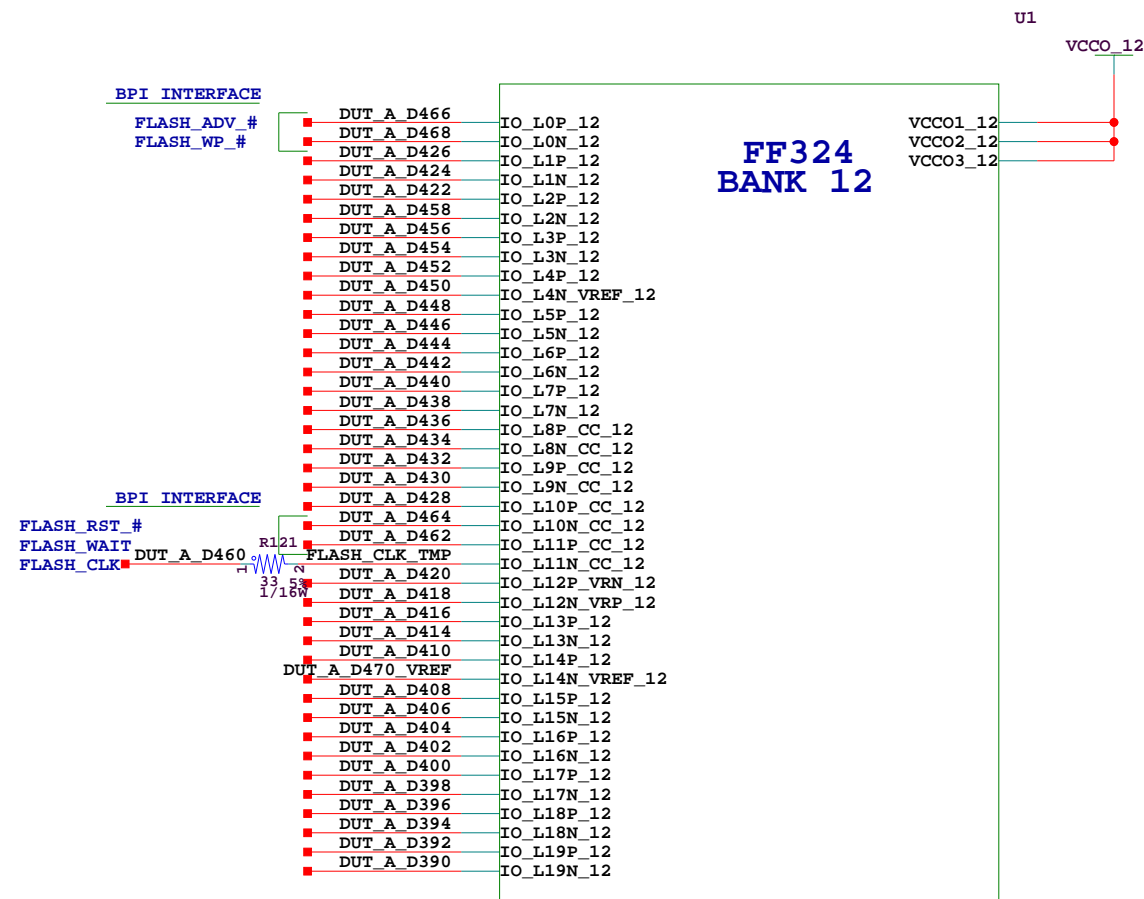
# SYSTEM MONITOR FILTERS



## SYSTEM MONITOR MALE CONNECTOR

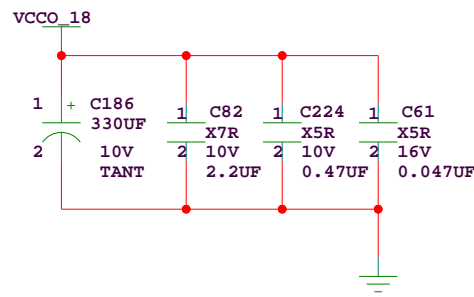
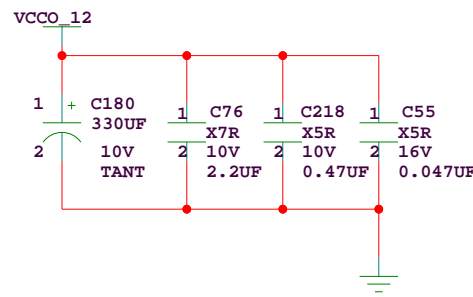


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	ART P/N	0531589-01
	FAB P/N	1280401-01
Title: SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401		
SYSTEM MONITOR		
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Sheet 6 of 17	Drawn By	D.L.



FF324  
2324-9310-XX-2431

FF324  
2324-9310-XX-2431

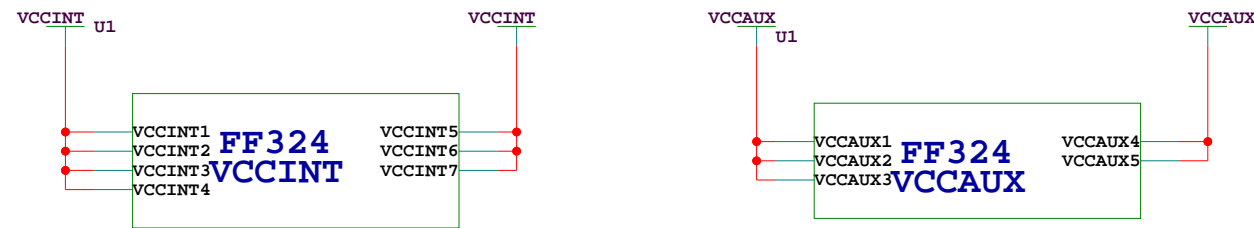
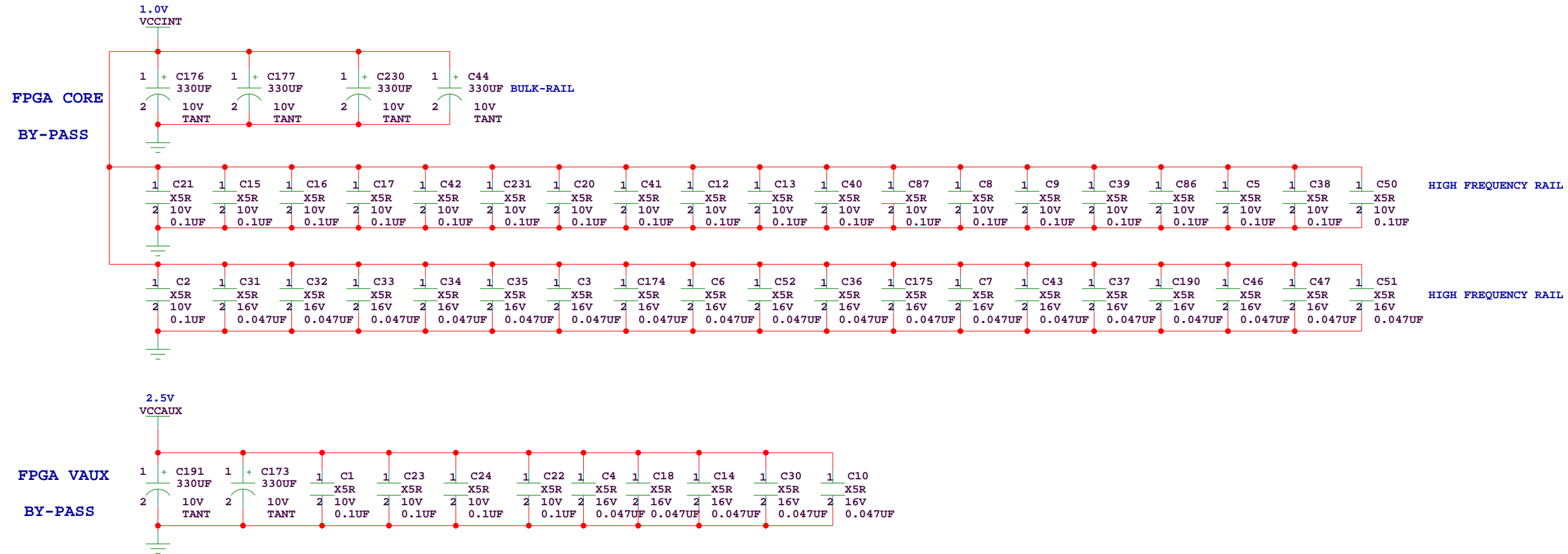


SCH P/N 0381320-01  
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Title: SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401

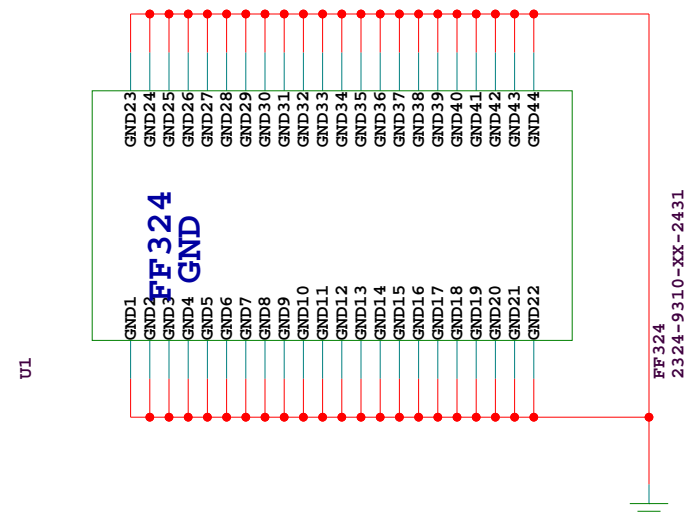
**DUT INTERFACE**

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FF324  
2324-9310-XX-2431

FF324  
2324-9310-XX-2431



U1

FF324  
2324-9310-XX-2431



SCH P/N 0381320-01  
ART P/N 0531589-01  
FAB P/N 1280401-01

Title:  
SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401

**FPGA DECOUPLING CAPACITORS**

Date: 7-20-2006\_10:33

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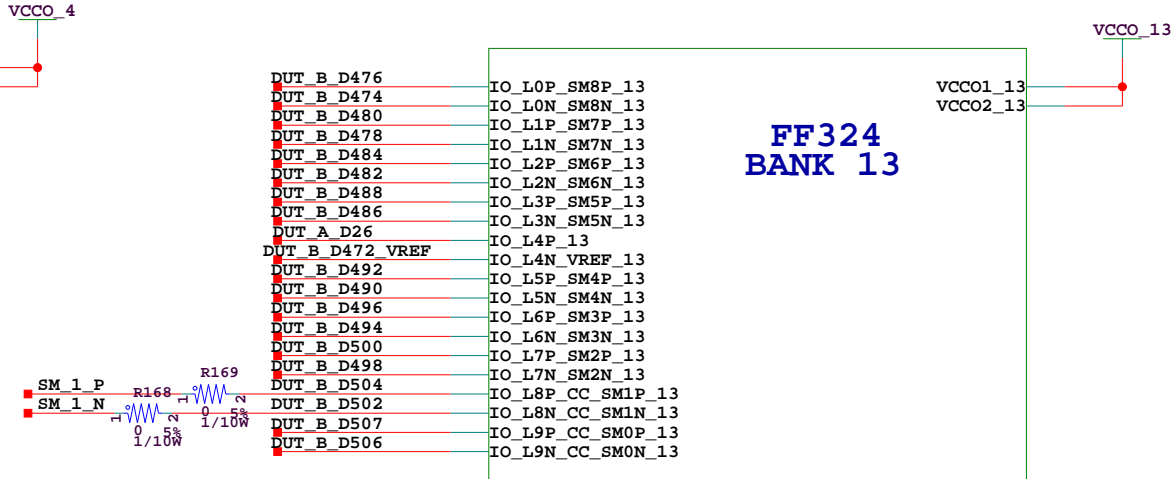
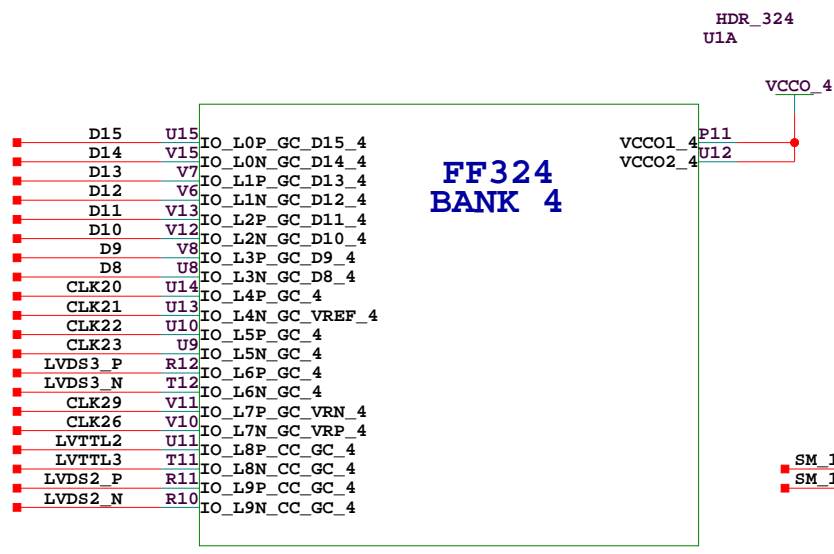
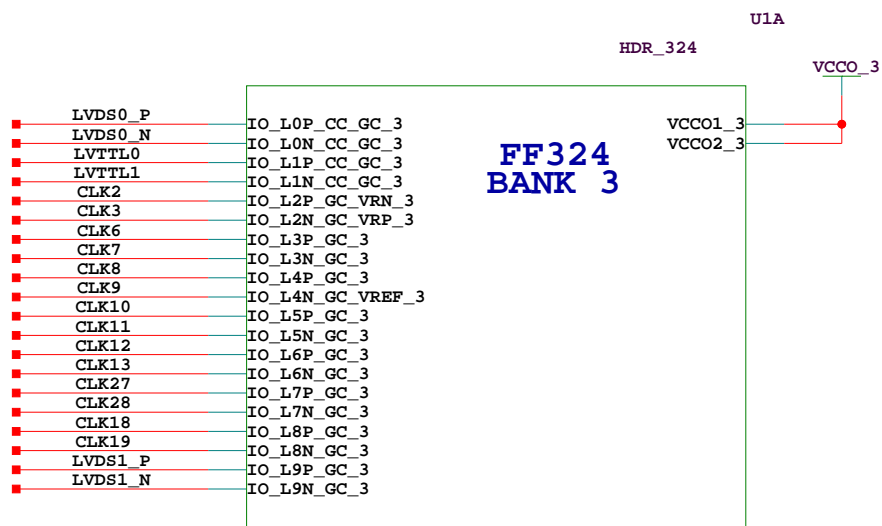
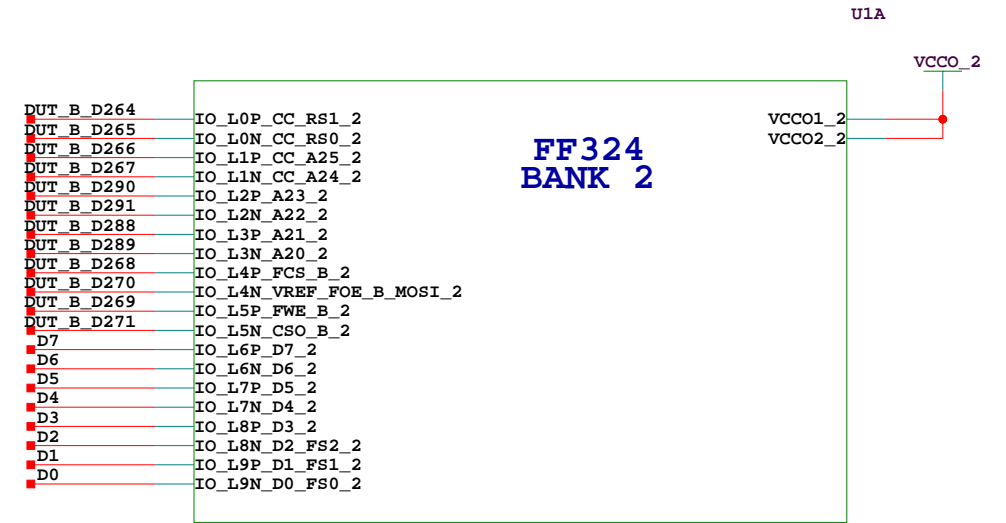
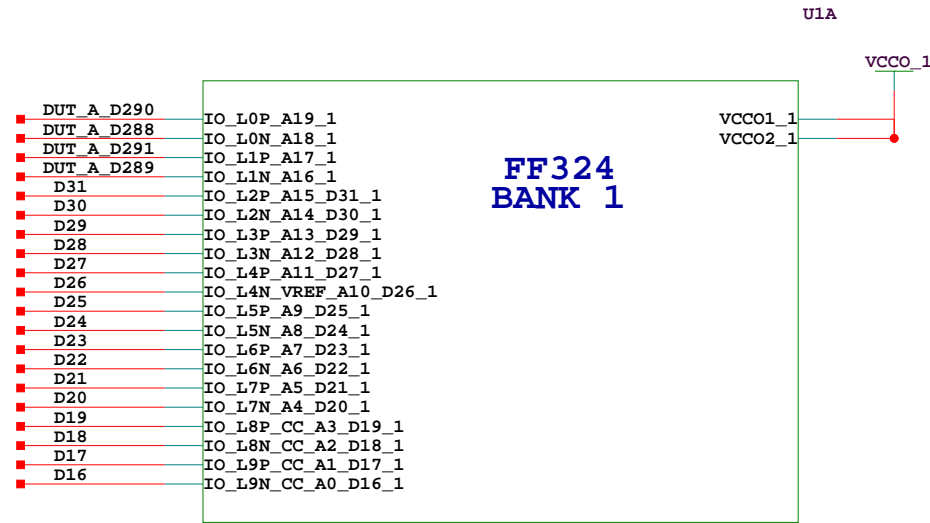
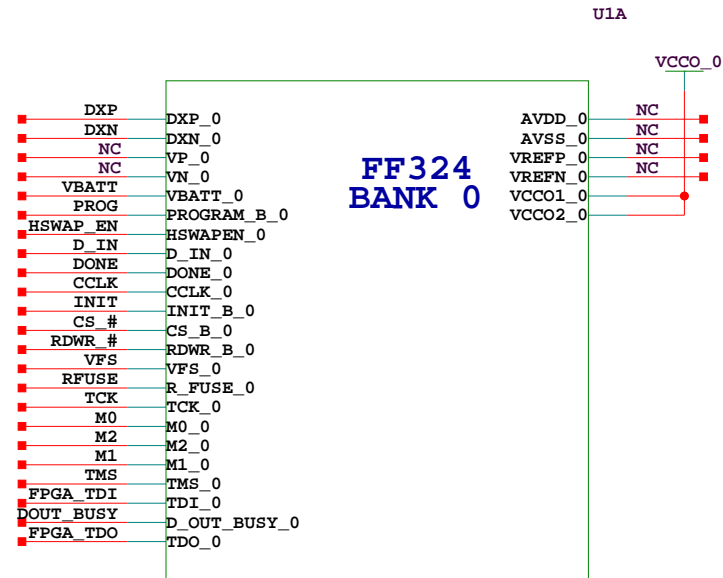
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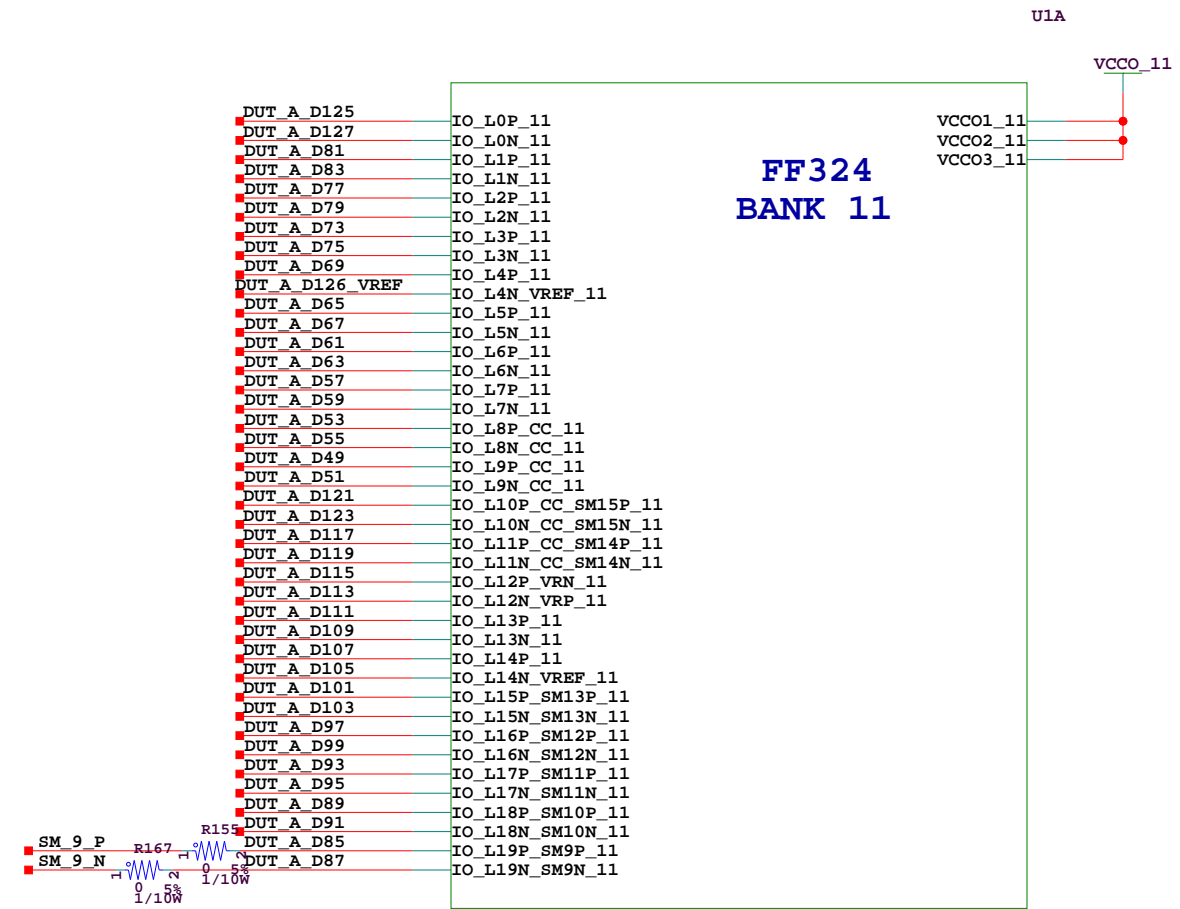
Sheet 8 of 17

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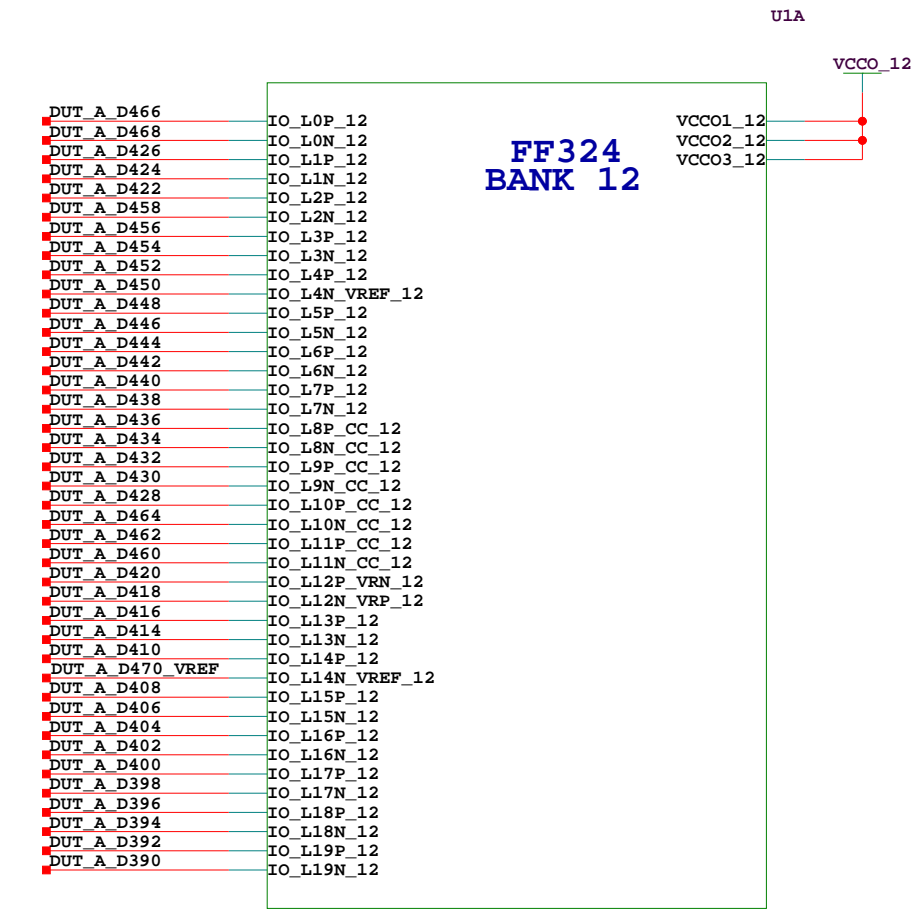




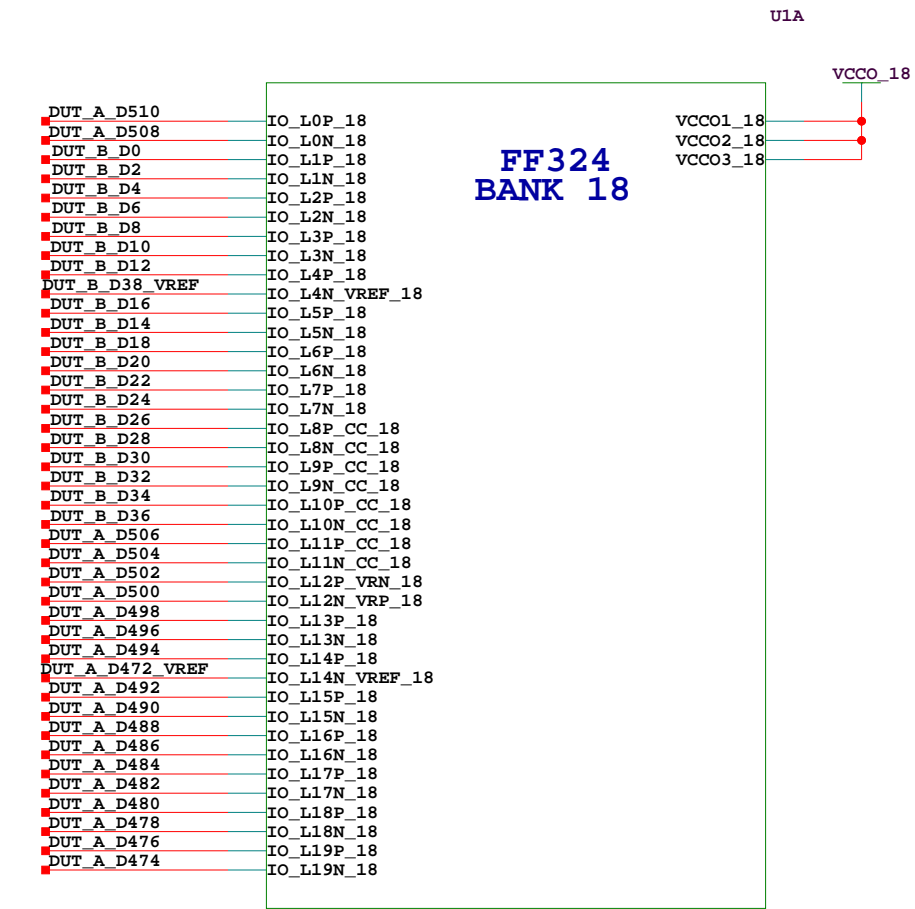
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Title: SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401			
<b>DUT TEST PINS</b>			
Date:	7-20-2006_10:33	Ver:	B
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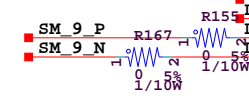
HDR\_324



HDR\_324



HDR\_324

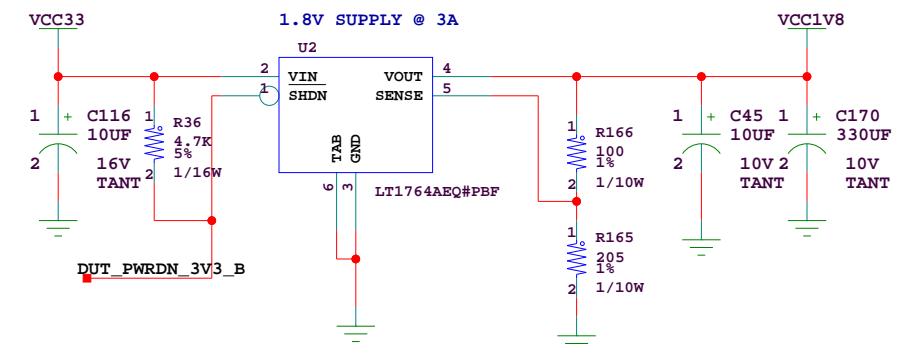
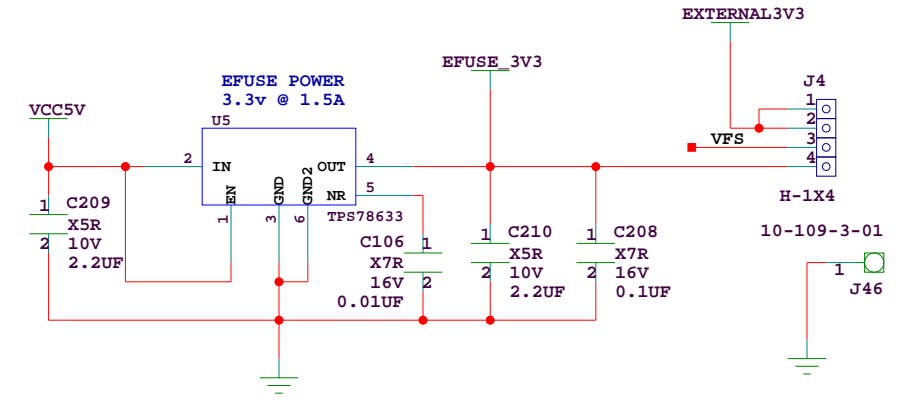
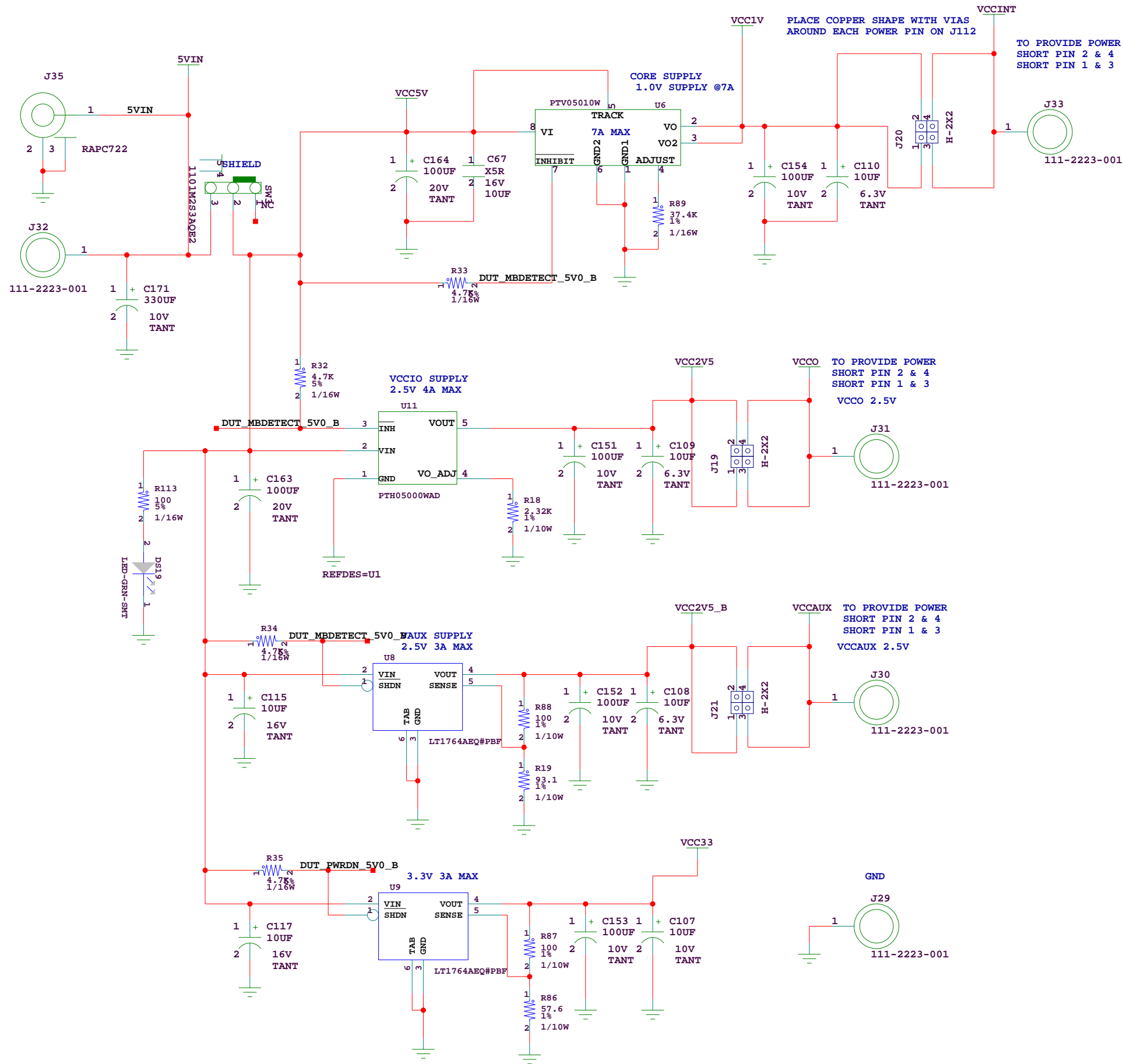


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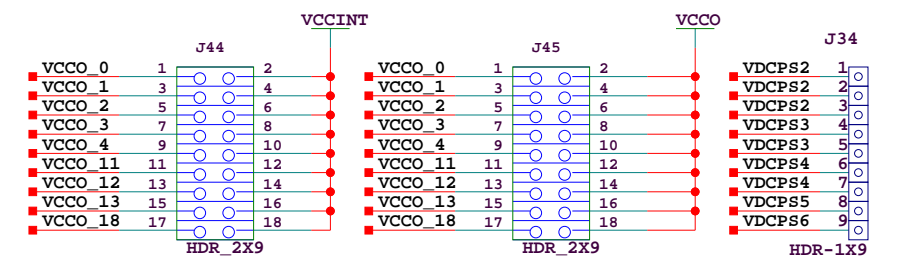
Title:  
SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401

**DUT TEST PINS**

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**VCC I/O SELECTION**

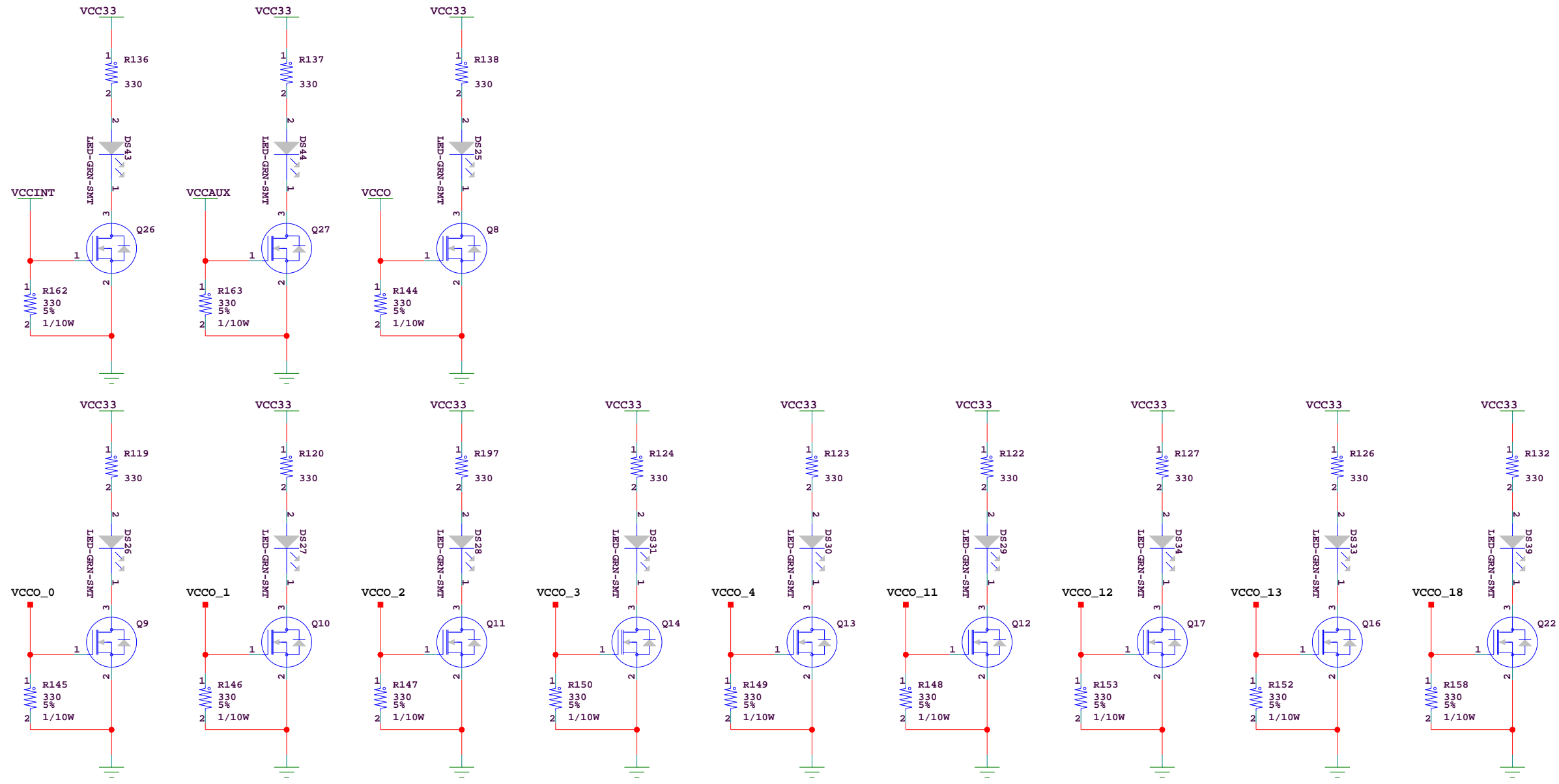



**XILINX**

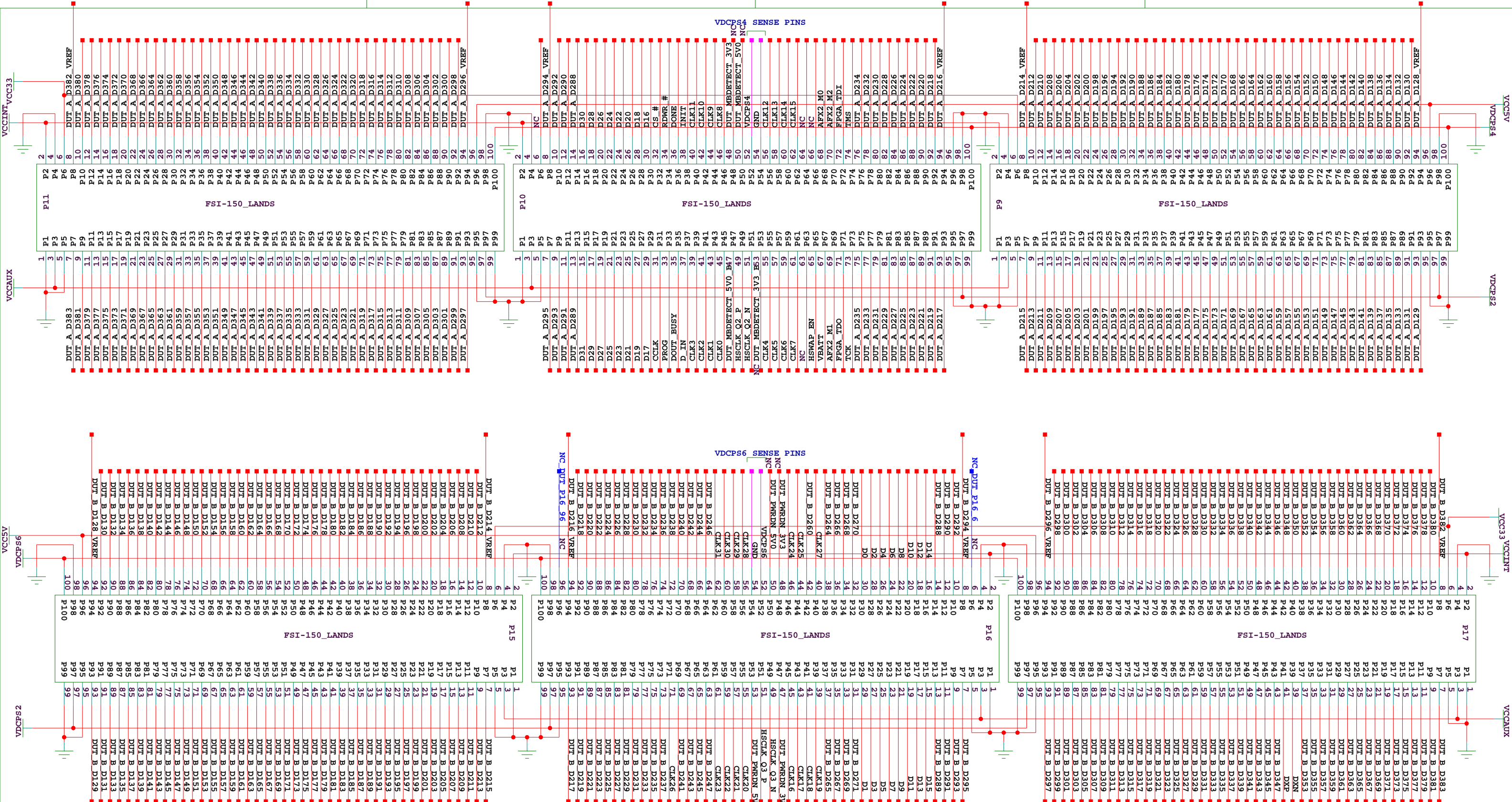
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 FAB P/N 1280401-01

Title: SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401  
**FPGA POWER SUPPLY, E-FUSE**

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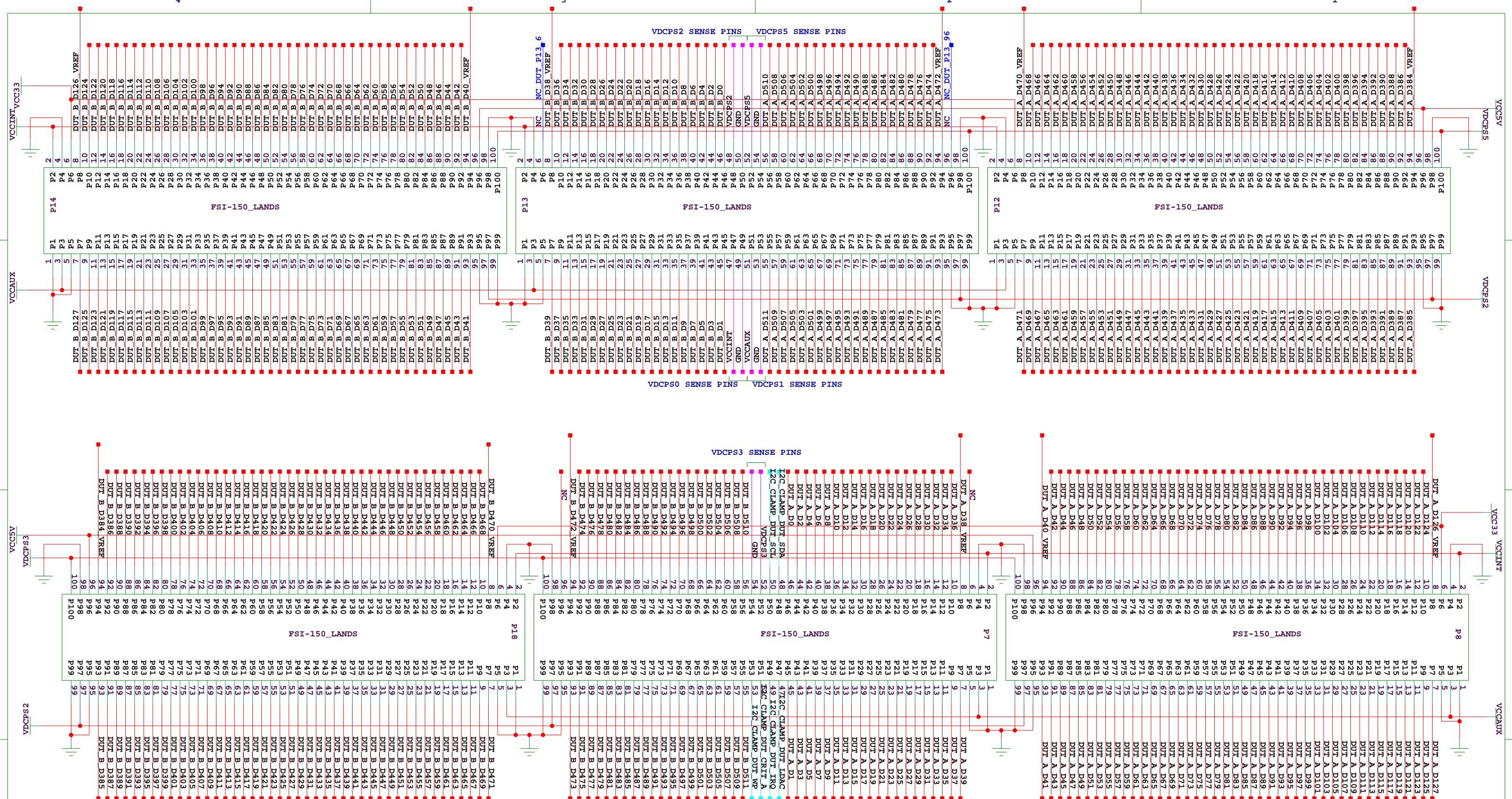
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		ART P/N	0531589-01
		FAB P/N	1280401-01
<b>Title:</b> SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401 <b>POWER LED INDICATORS</b>			
<b>Date:</b> 7-20-2006_10:33		<b>Ver:</b> B	
<b>Sheet Size:</b> B		<b>Rev:</b> 01	
<b>Sheet</b> 12	<b>of</b> 17	<b>Drawn By</b> D.L.	




SCH P/N 0381320-01  
 ART P/N 0531589-01  
 FAB P/N 1280401-01

Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401  
**AFX LANDINGS TOP AND BOTTOM**

Date: 7-20-2006_10:33	Ver: B
Sheet Size: B	Rev: 01
Sheet 13 of 17	Drawn By D.L.



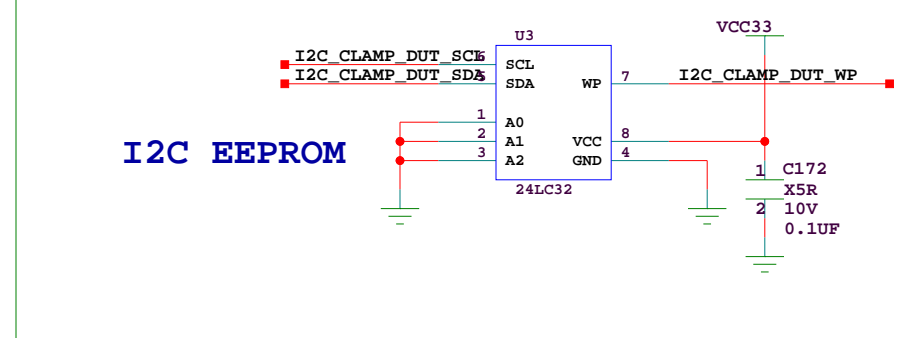
SCH P/N 0381320-01  
 ART P/N 0531589-01  
 FAB P/N 1280401-01



**Title:**  
 SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401

## AFX LANDINGS LEFT AND RIGHT

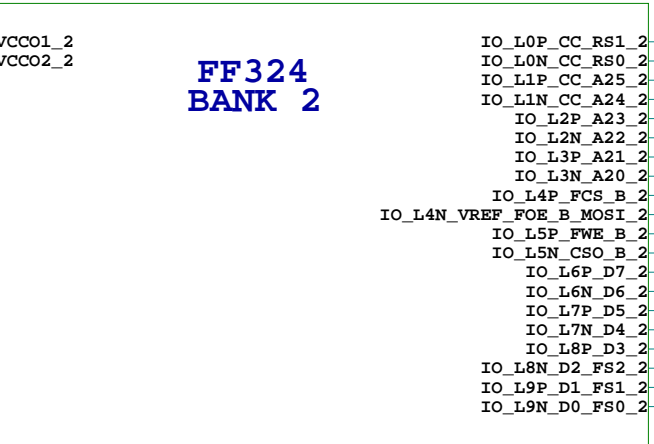
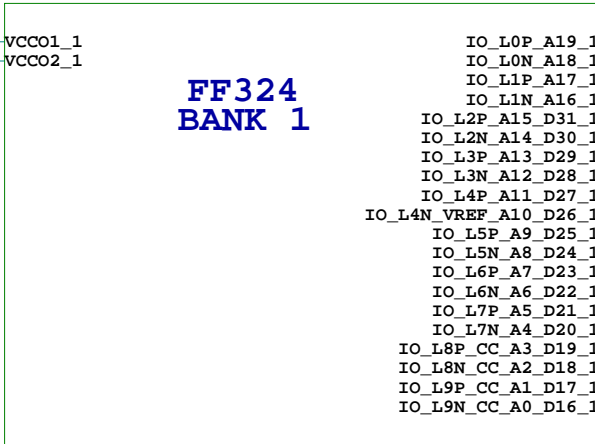
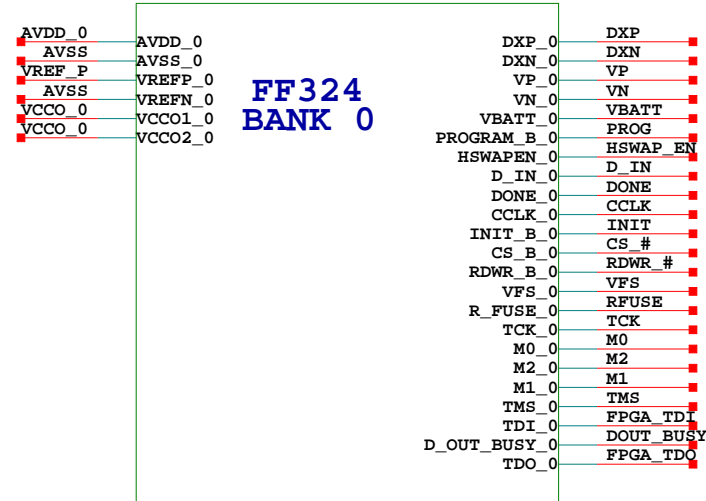
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<b>Sheet Size:</b> B	<b>Rev:</b> 01
<b>Sheet</b> 14 <b>of</b> 17	<b>Drawn By</b> D.L.



US4

US4

US4



US4

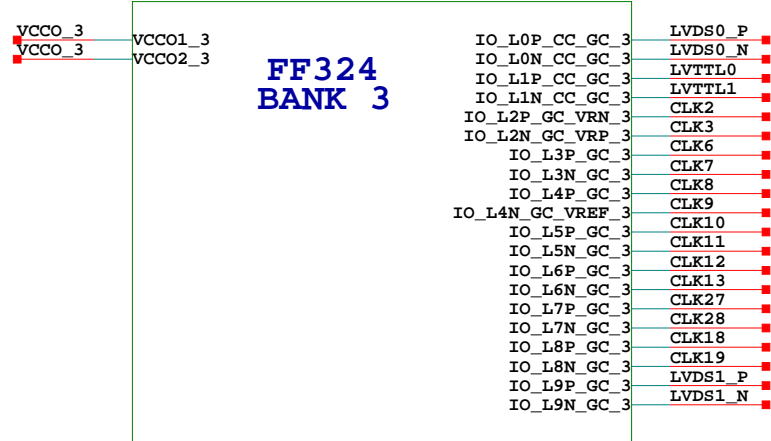
FF324\_SM

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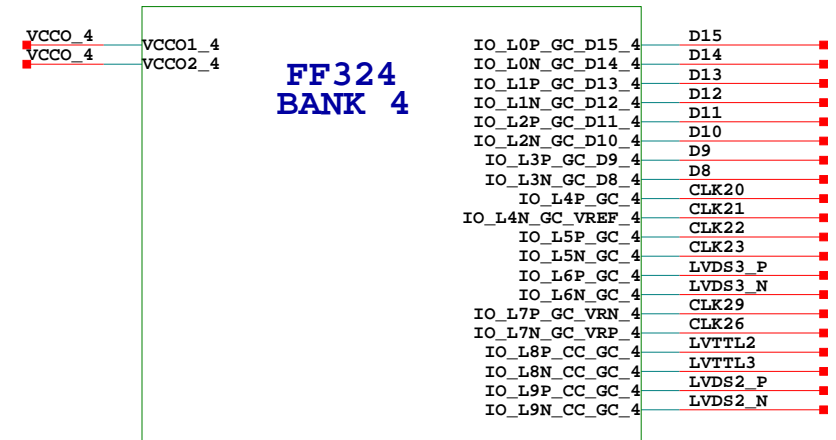
FF324\_SM

US4

FF324\_SM



FF324\_SM



FF324\_SM

**XILINX**

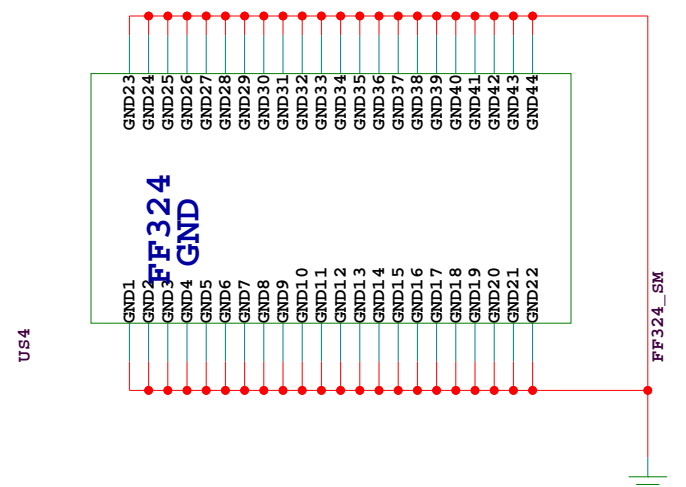
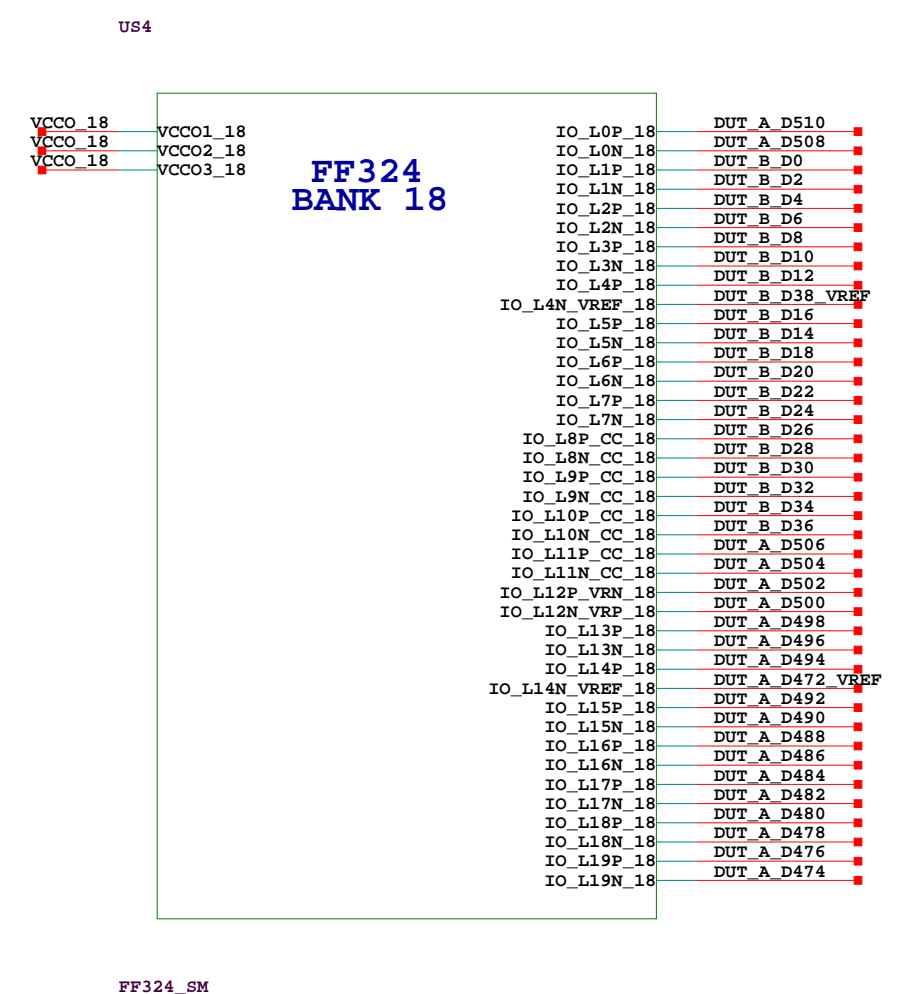
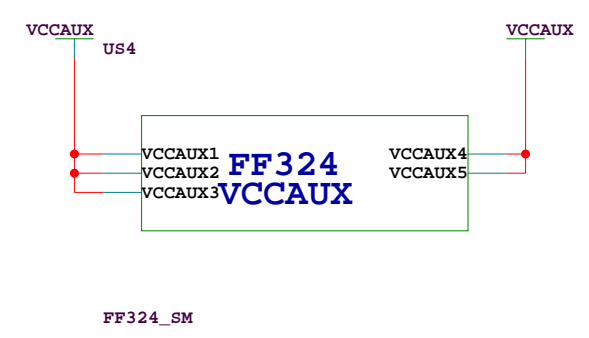
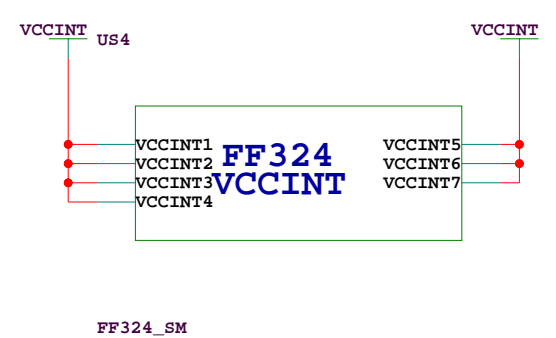
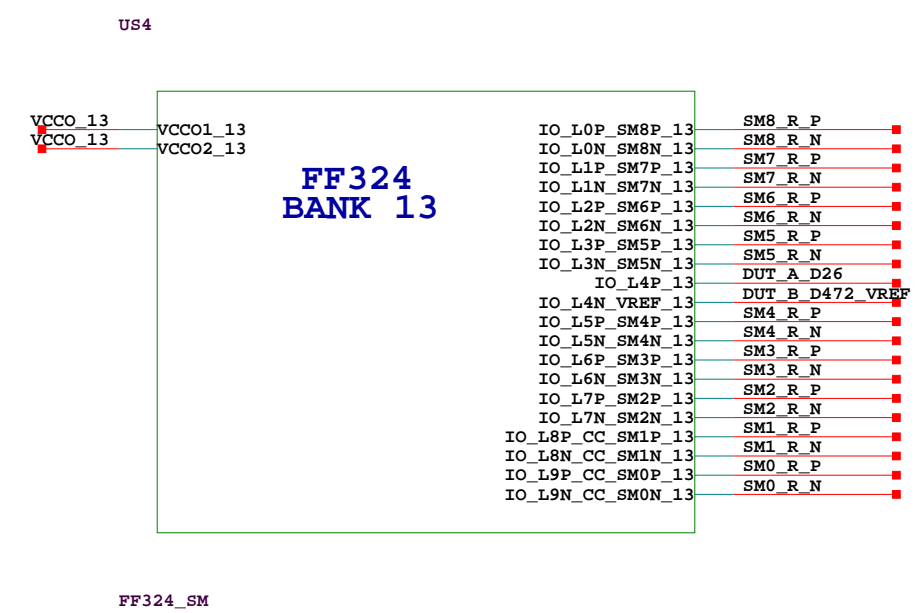
SCH P/N 0381320-01  
 ART P/N 0531589-01  
 FAB P/N 1280401-01

Title:  
 SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401

**MISC.**

Date:	7-20-2006_10:33	Ver:	B	
Sheet Size:	B	Rev:	01	
Sheet	15	of 17	Drawn By	D.L.

# TEST SOCKET



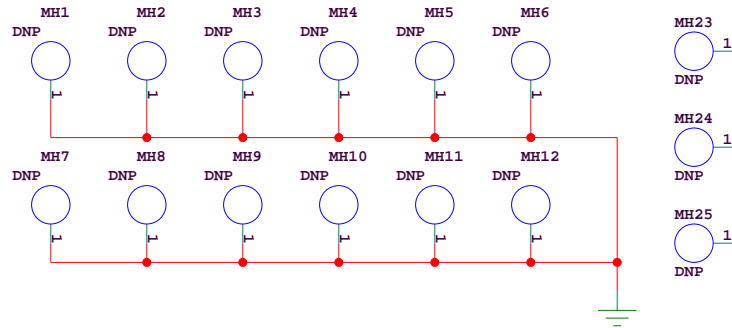
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Date: 7-20-2006_10:33		Ver: B	
Sheet Size: B		Rev: 01	
Sheet 16	of 17	Drawn By	D.L.

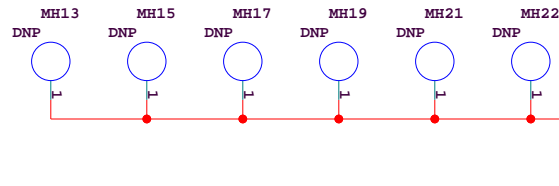


### AFXII MOUNTING HOLES

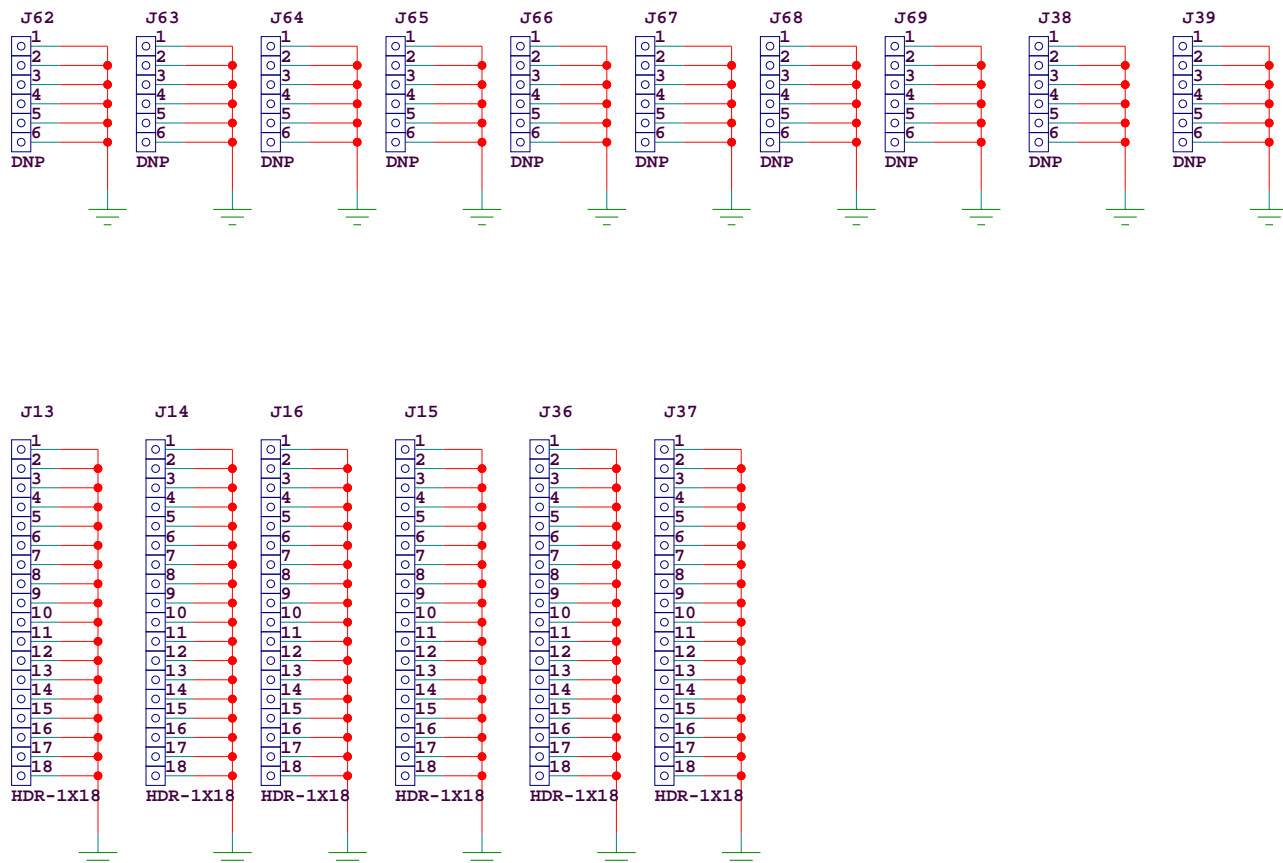
AFXII GUIDE HOLES



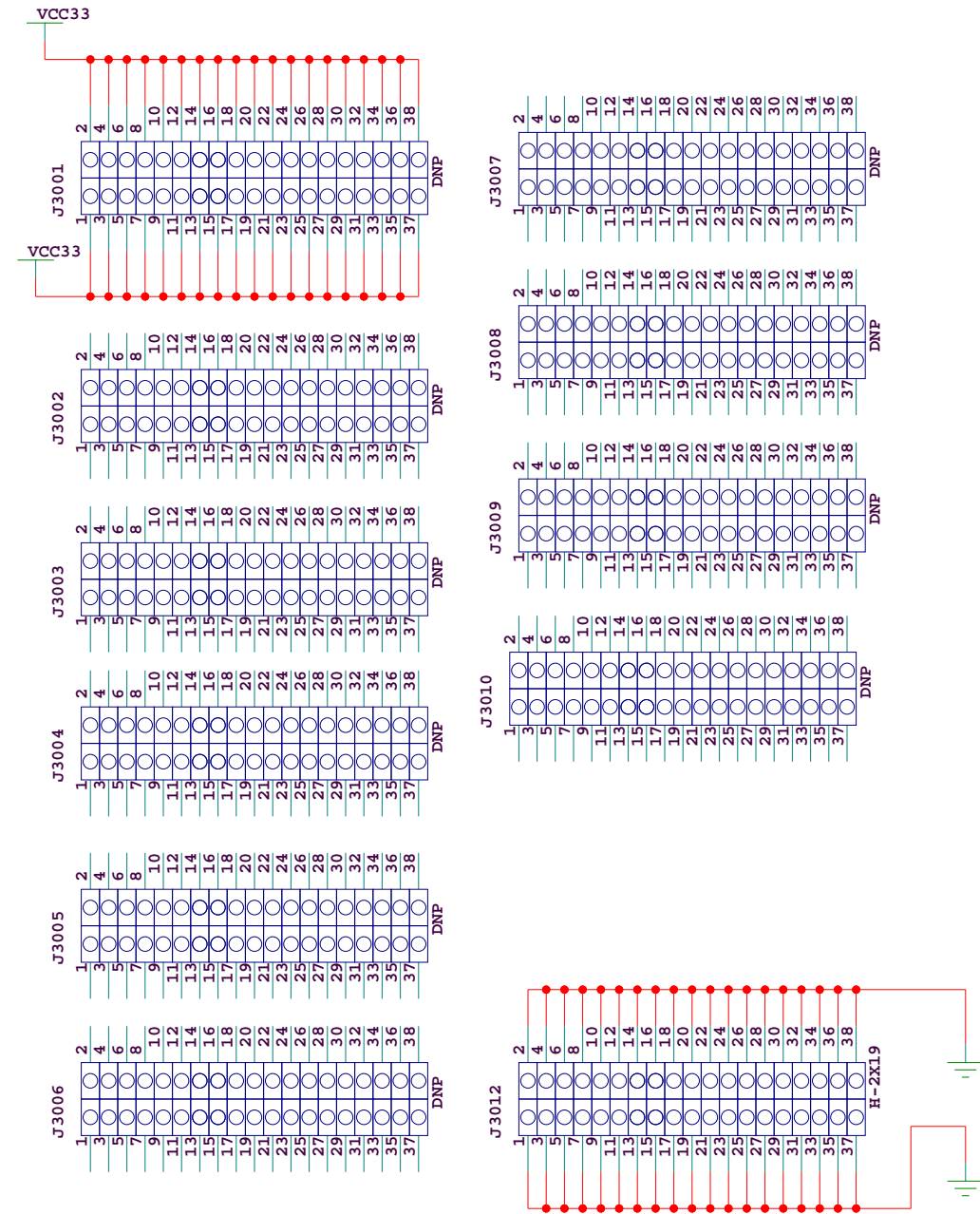
### MOUNTING HOLES



### DUT INTERLEAVE GND'S



### BREADBOARD AREA



SCH P/N 0381320-01  
 ART P/N 0531589-01  
 FAB P/N 1280401-01

Title: SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401  
**HARDWARE AND BREADBOARD AREA**

Date: 7-20-2006_10:33	Ver: B
Sheet Size: B	Rev: 01
Sheet 17 of 17	Drawn By D.L.