

PAGE 6
System Monitor Aux

PAGE 3
System Monitor

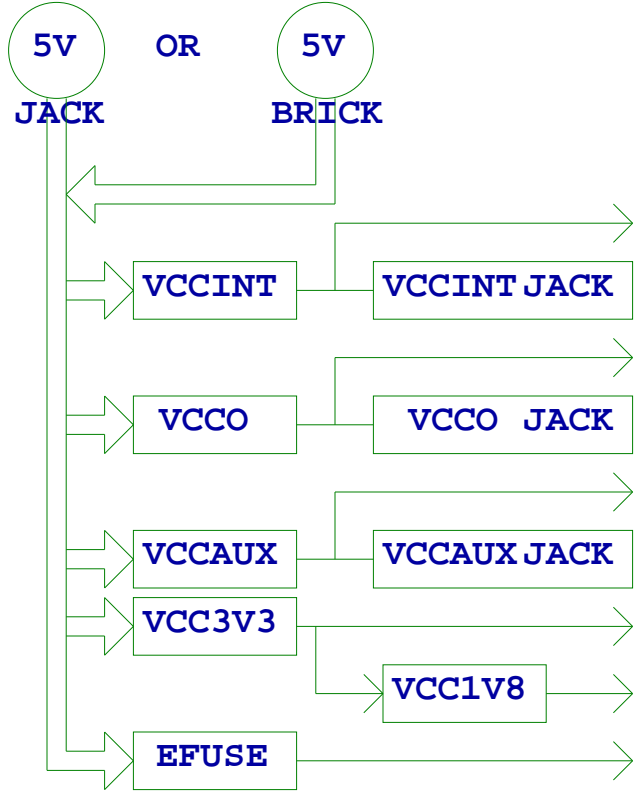
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System Ace
Upstream

PAGE 2
Upstream Connector

PAGE 5
Single Ended
Socket Clocks
2X

PAGE 5
Differential
SMA Clocks
2X

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Power Bus and Switches



Virtex 5
FF324
DUT

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Switches
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ALL DUT I/O TEST POINTS

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System Ace
Downstream

PAGE 2

Downstream Connector

PAGE 2

Single Ended
Socket Clocks
2X

PAGE 5

Differential
SMA Clocks
2X

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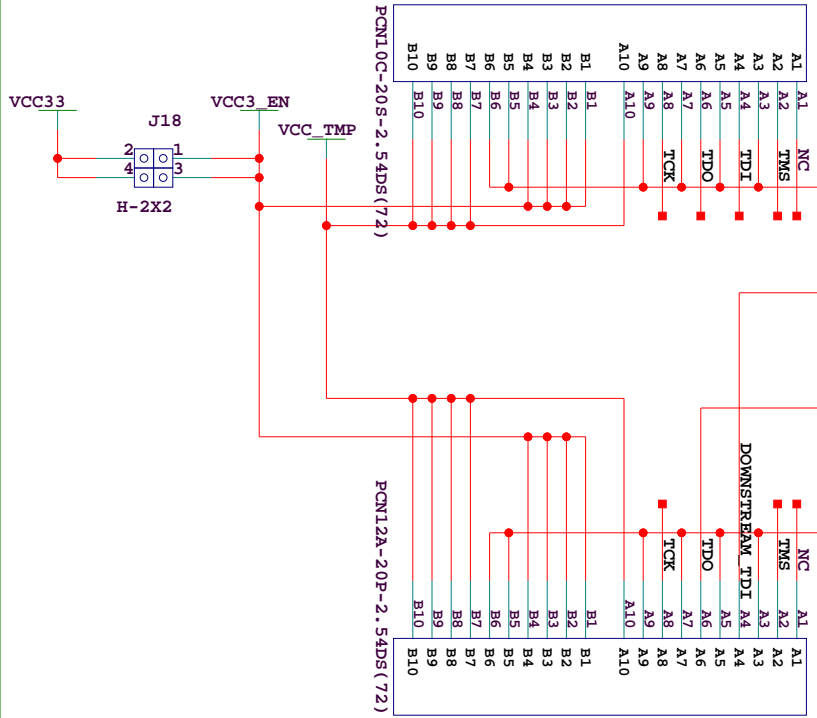
SCH P/N 0381320-01
ART P/N 0531589-01
FAB P/N 1280401-01

Title:
SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401

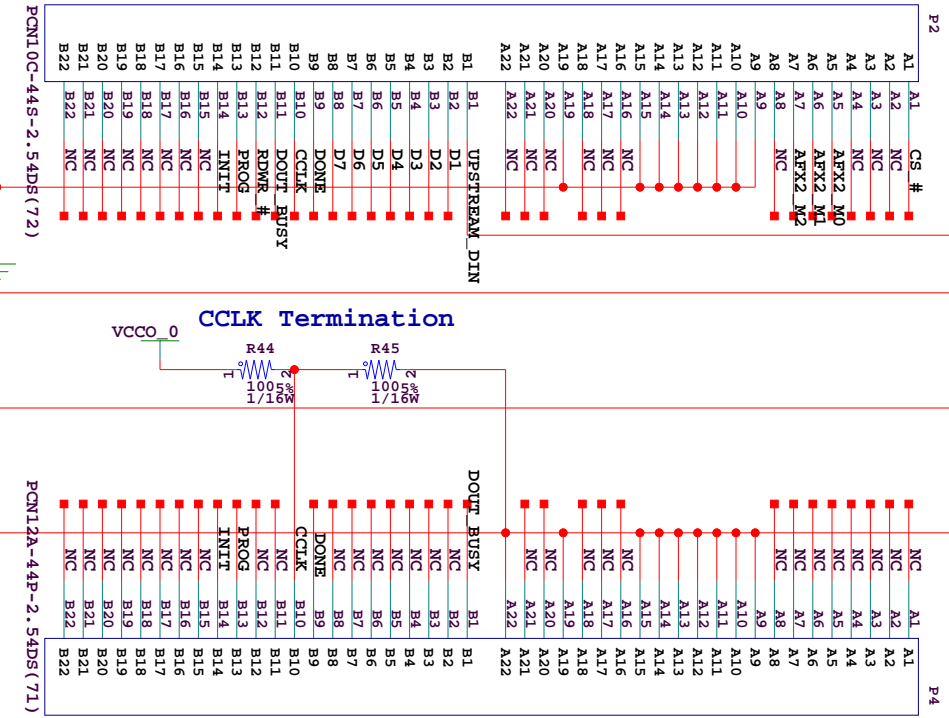
BLOCK DIAGRAM

Date: 1-11-2006_11:25	Ver: B
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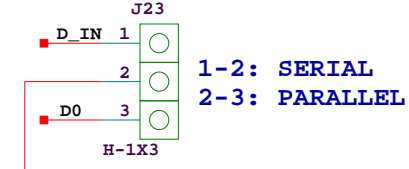
SYSTEM ACE UPSTREAM



UPSTREAM CONNECTORS

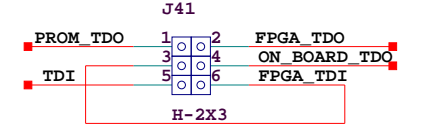


DOWNSTREAM CONFIG



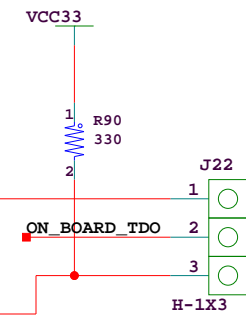
ON BOARD JTAG CHAIN SELECTION

PROM JTAG FPGA JTAG
 1-3: Enable 2-4: Enable
 3-5: Disable 4-6: Disable

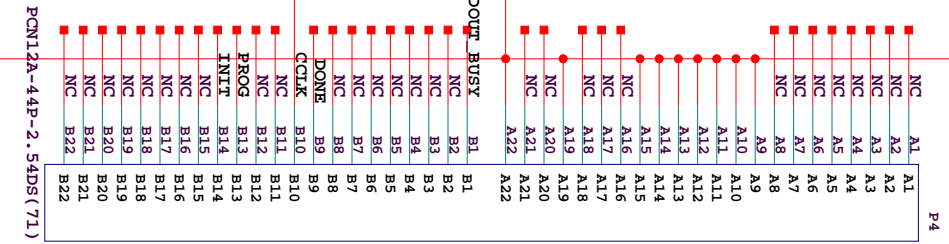
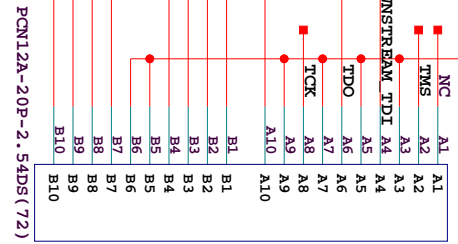


1-2: SERIAL CHAINING TO NEXT BOARD
 2-3: TERMINATION OF LAST BOARD IN THE CHAIN

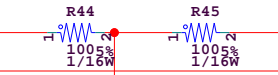
JTAG JUMPER



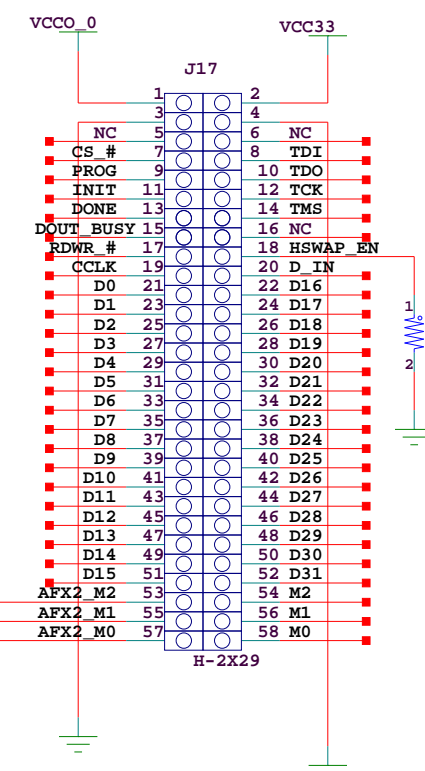
SYSTEM ACE DOWNSTREAM DOWNSTREAM CONNECTORS



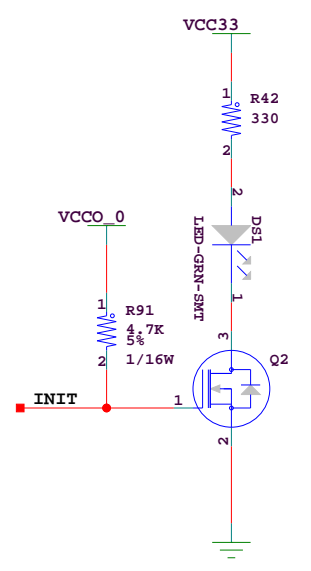
CCLK Termination



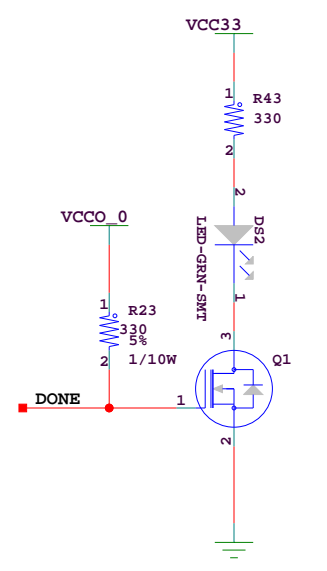
FLYING WIRE CONFIGURATION PORT



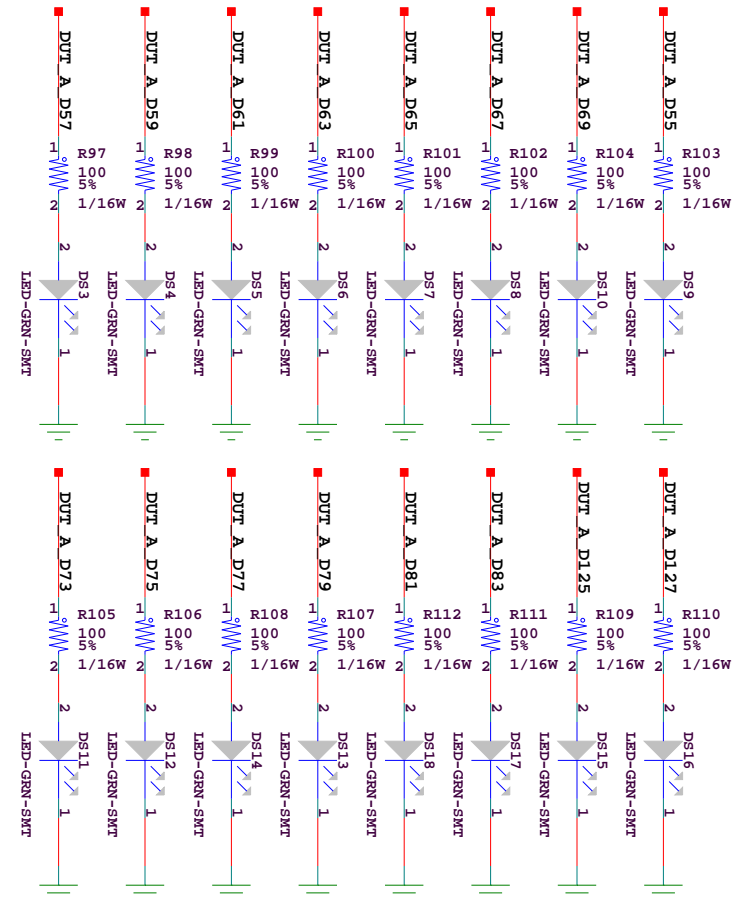
INIT LED



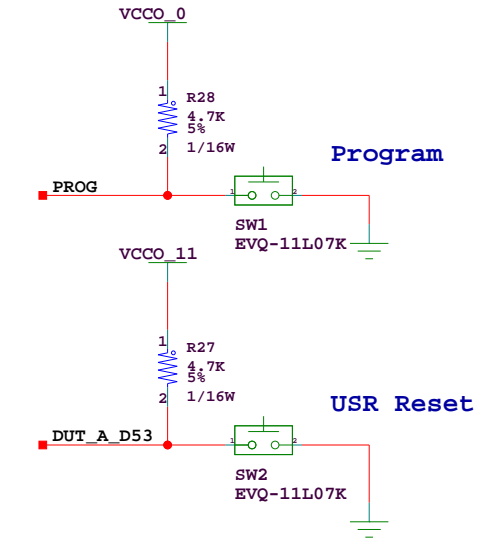
DONE LED



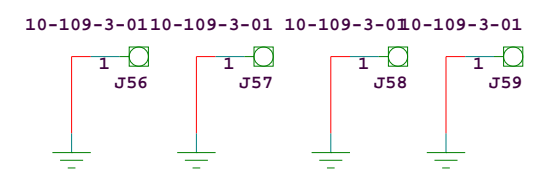
USER LED'S



SWITCHES



TEST POINTS



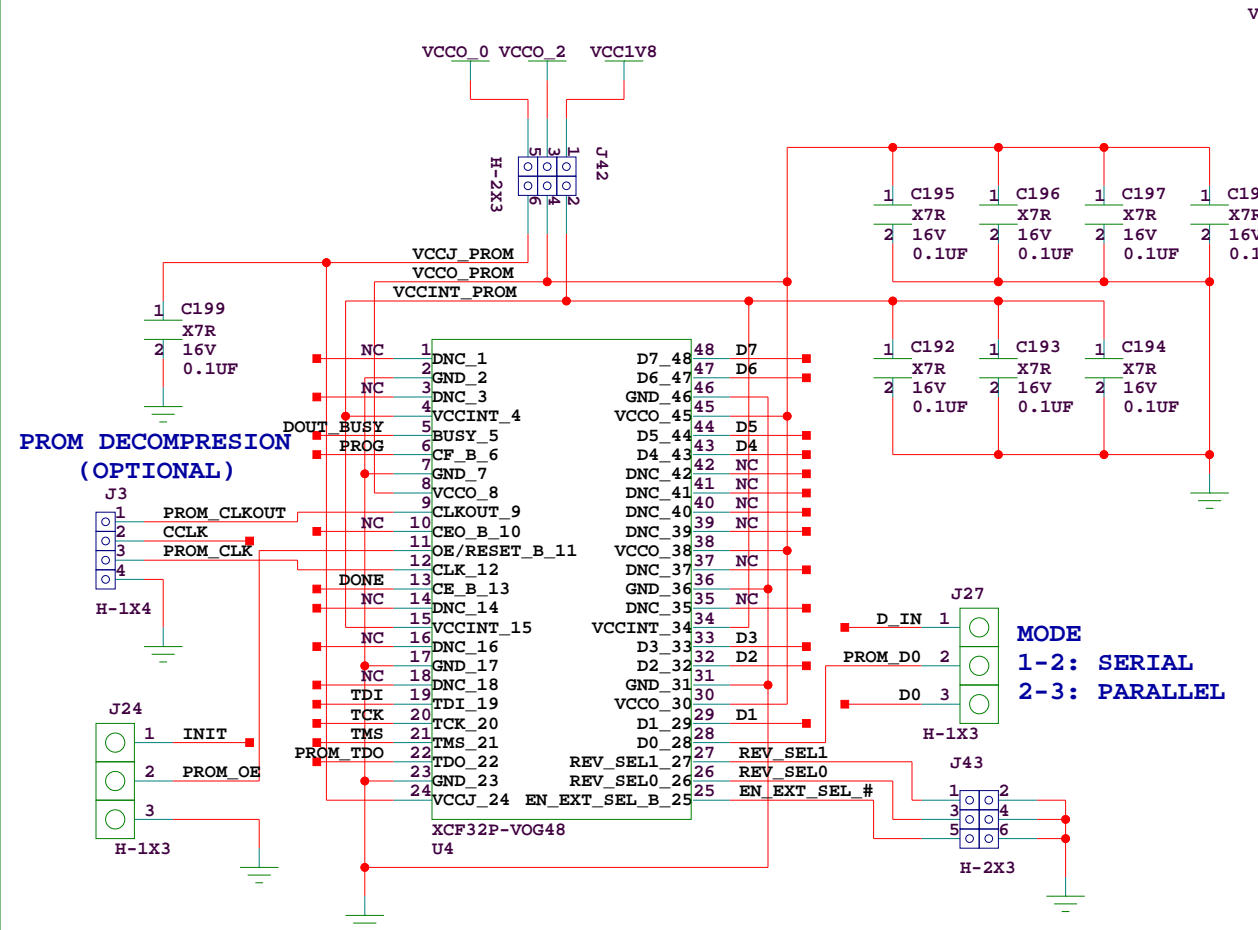
XILINX

SCH P/N 0381320-01
 ART P/N 0531589-01
 FAB P/N 1280401-01

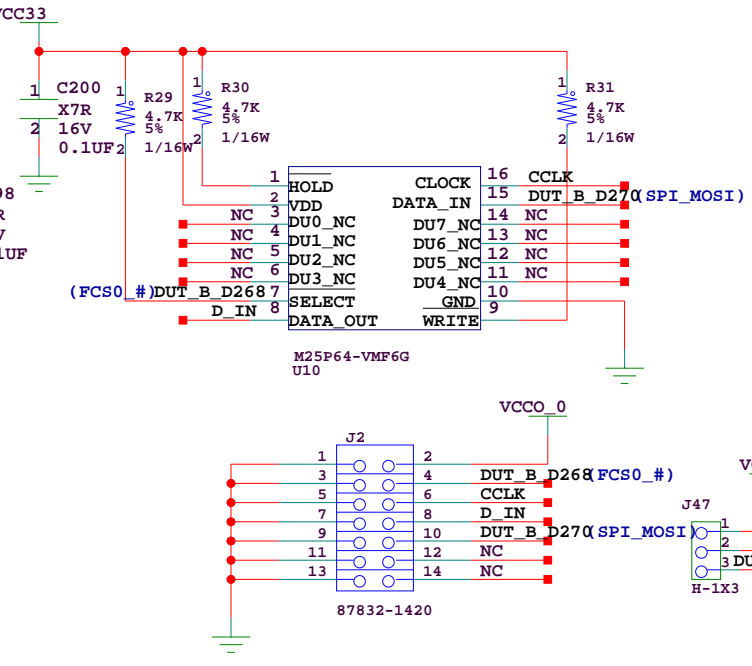
Title: SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401
DIN CONN, PORTS, STATUS LEDS, SWITCHES

Date: 7-20-2006_10:33 Ver: B
 Sheet Size: B Rev: 01
 Sheet 2 of 17 Drawn By D.L.

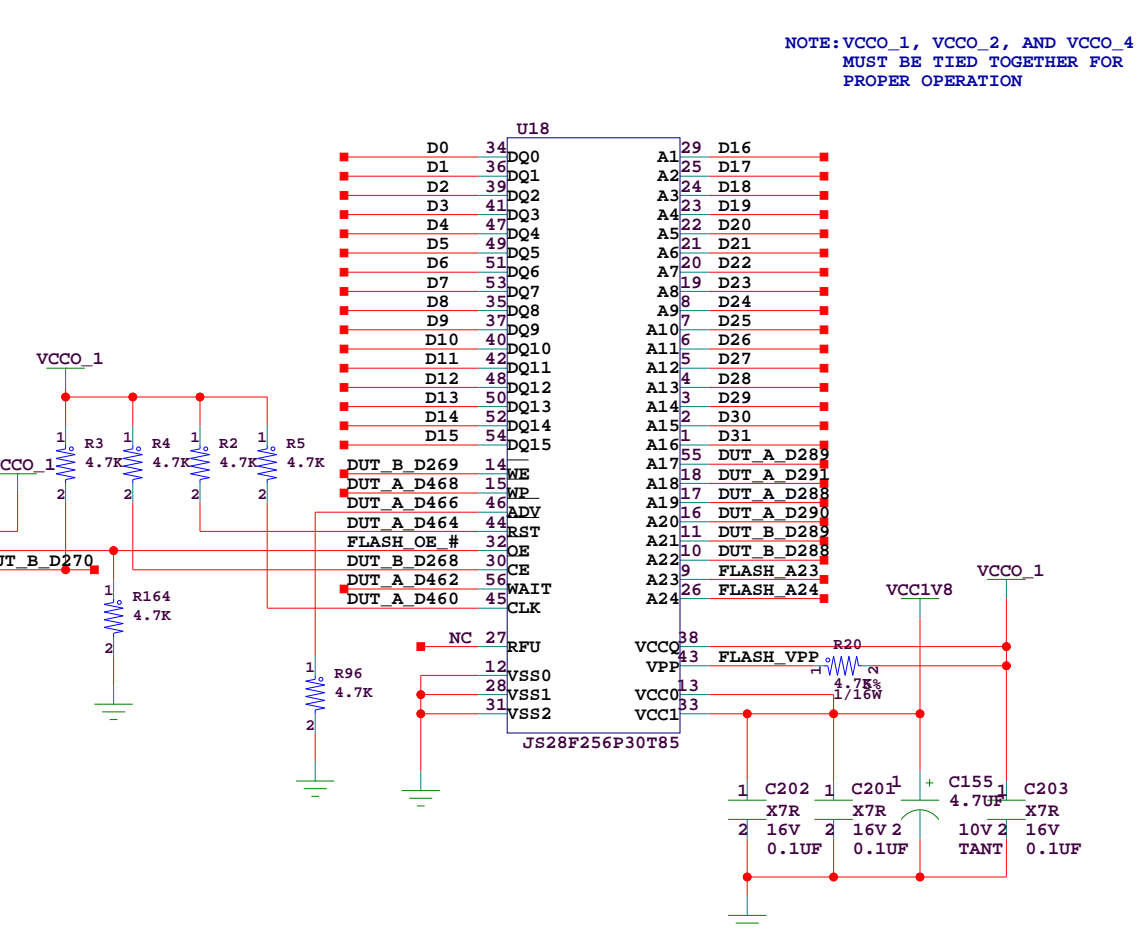
CONFIGURATION PROM



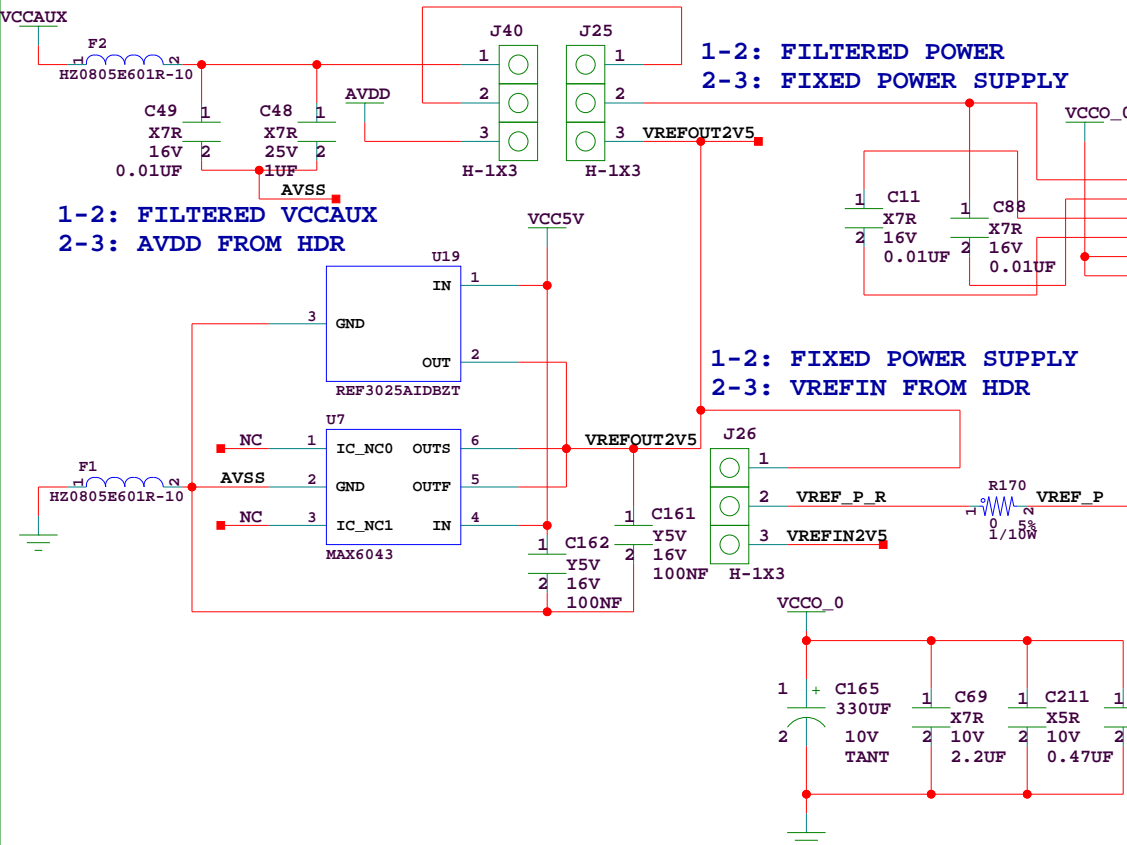
SPI INTERFACE



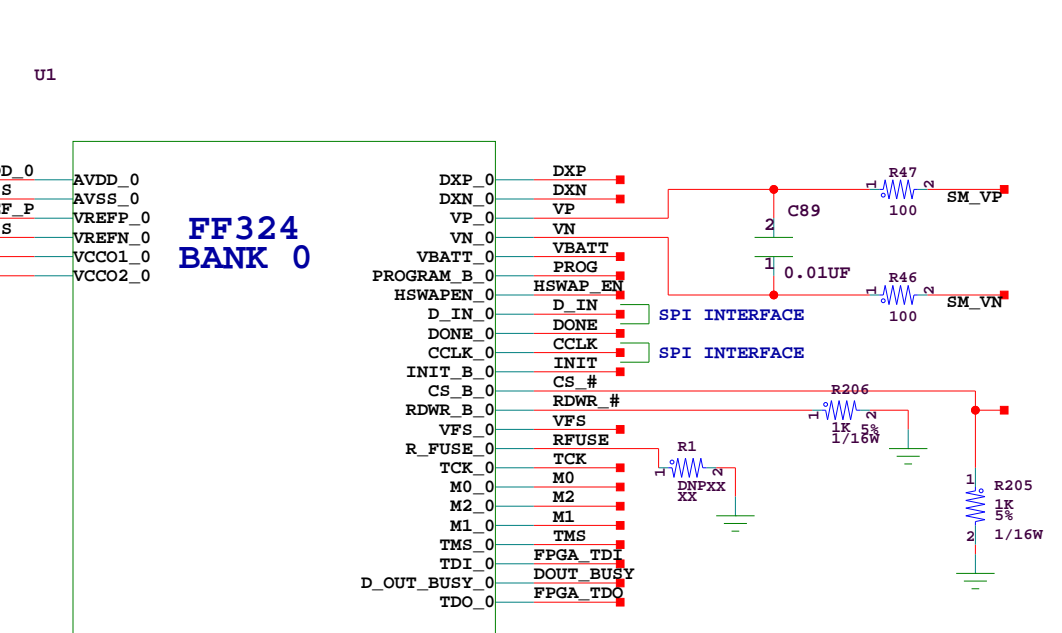
BPI INTERFACE



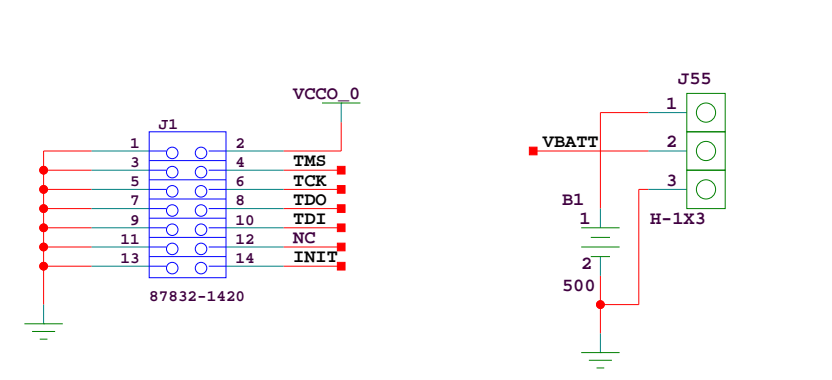
SYSTEM MONITOR SUPPLY



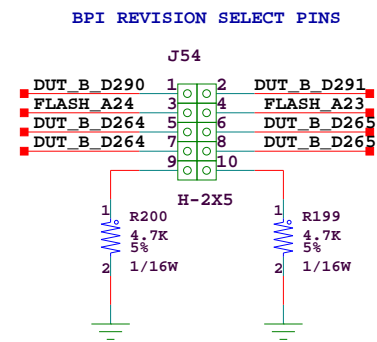
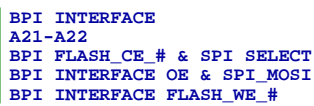
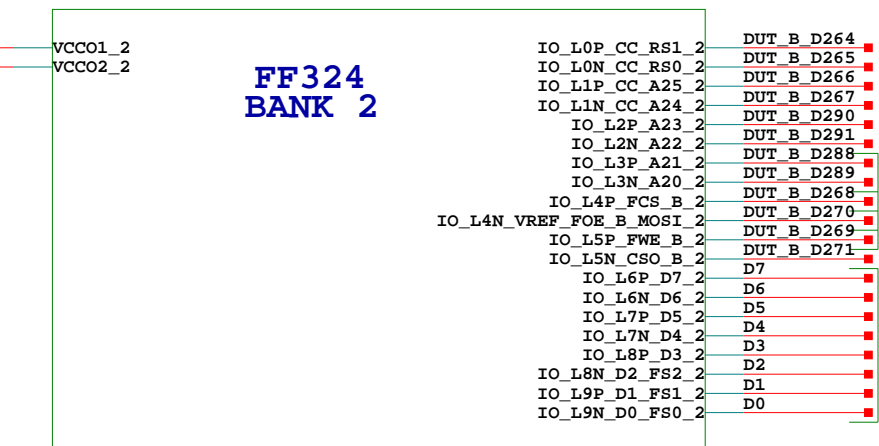
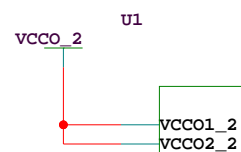
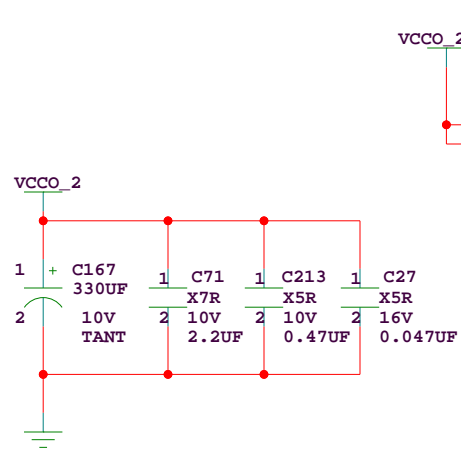
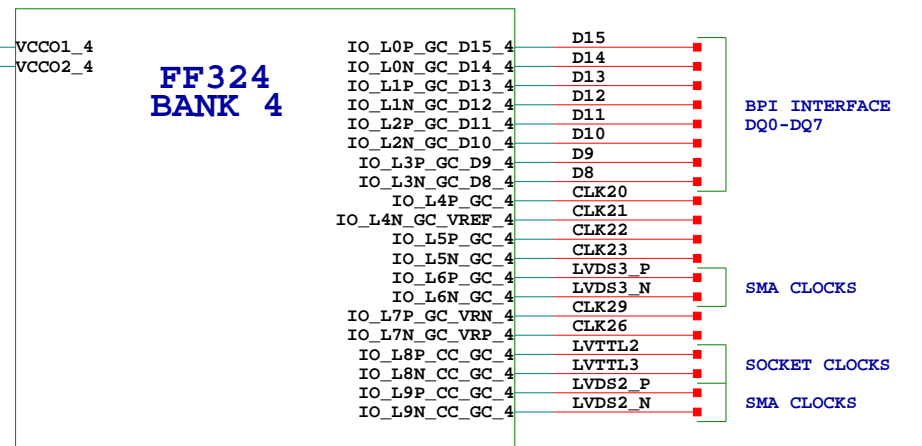
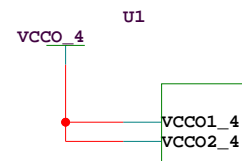
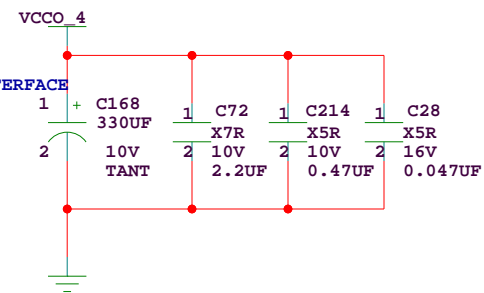
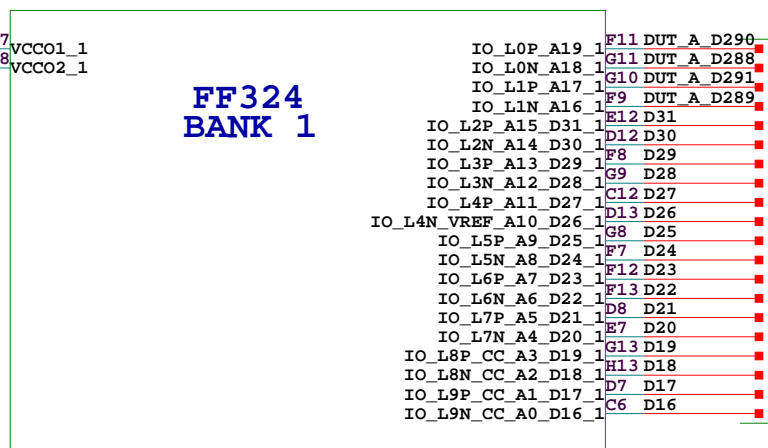
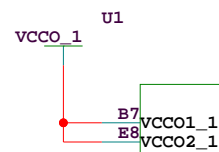
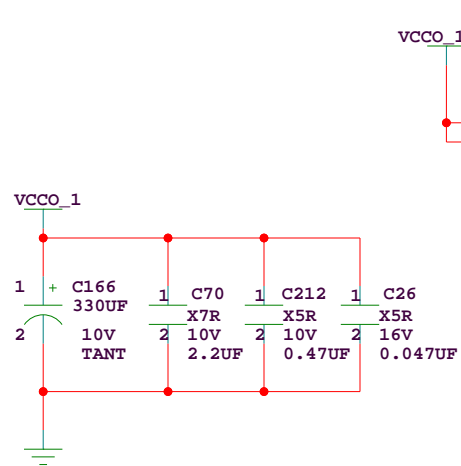
FPGA BANK0 CONFIGURATION



PARALLEL 4 CABLE CONNECTOR VBATT Supply



		SCH P/N	0381320-01
		ART P/N	0531589-01
		FAB P/N	1280401-01
Title: SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401			
CONFIGURATION			
Date:	7-24-2006_15:37	Ver:	B
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- 1-3: Selects ADDR23 from FPGA to FLASH ADDR24
- 3-5: Selects RS1 from FPGA to FLASH ADDR24
- 7-9: Pulldown for RS applications
- 2-4: Selects ADDR22 from FPGA to FLASH ADDR23
- 4-6: Selects RS0 from FPGA to FLASH ADDR23
- 8-10: Pulldown for RS applications



SCH P/N 0381320-01
ART P/N 0531589-01
FAB P/N 1280401-01

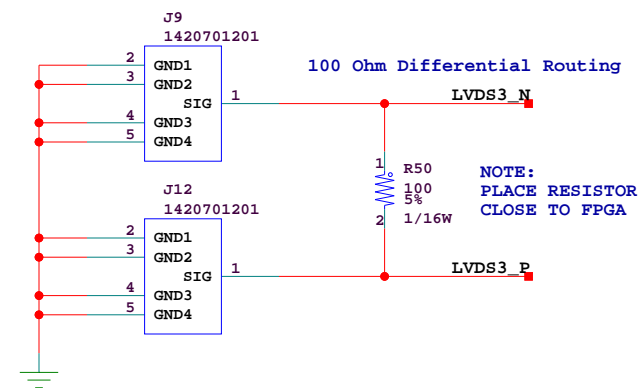
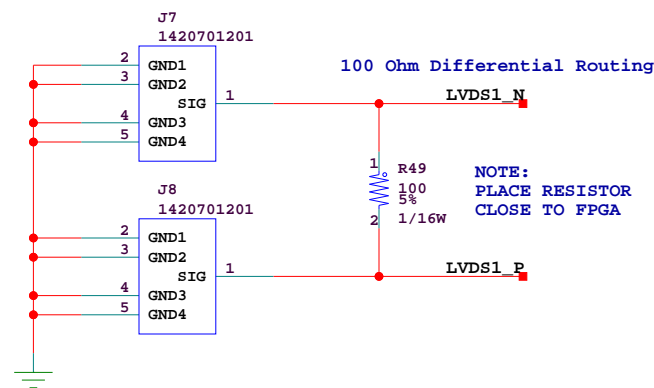
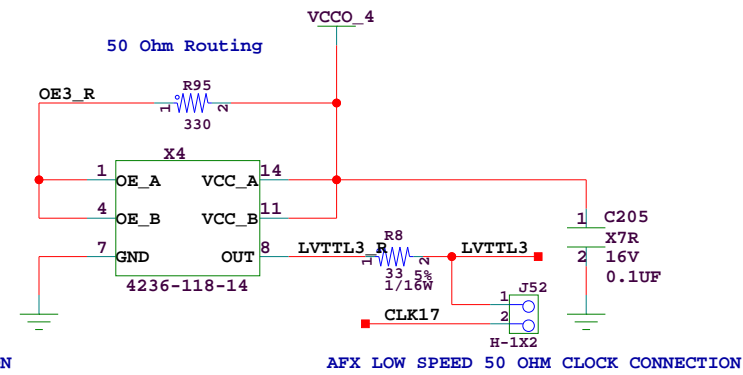
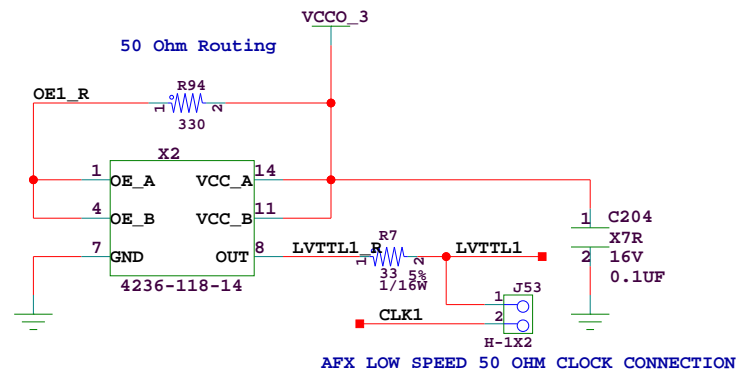
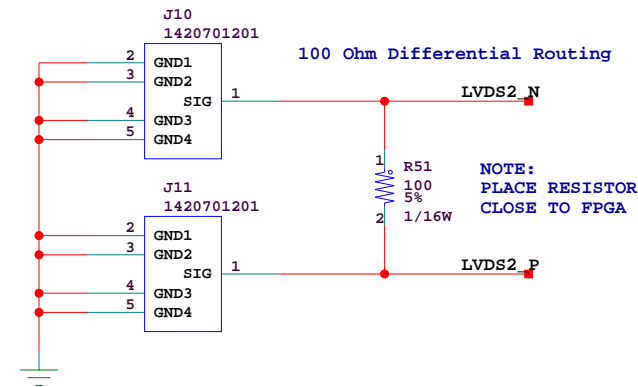
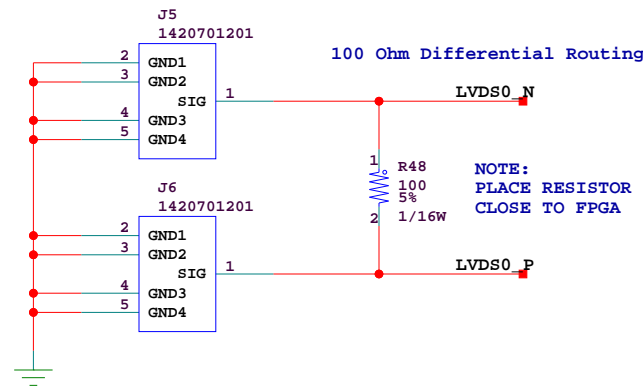
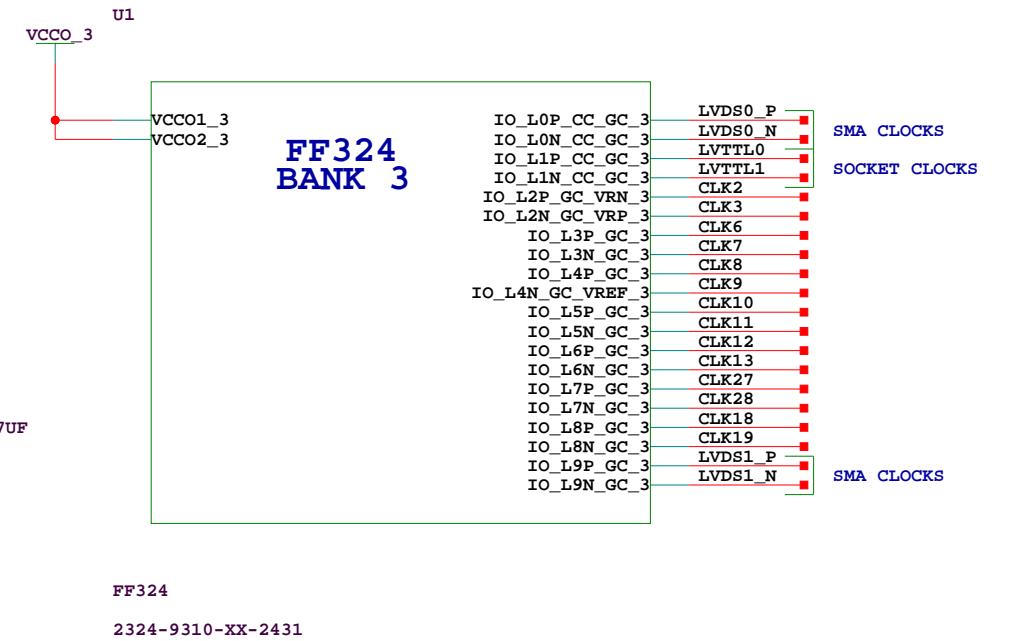
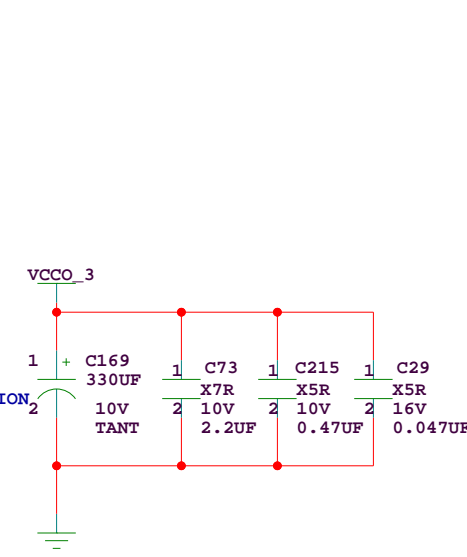
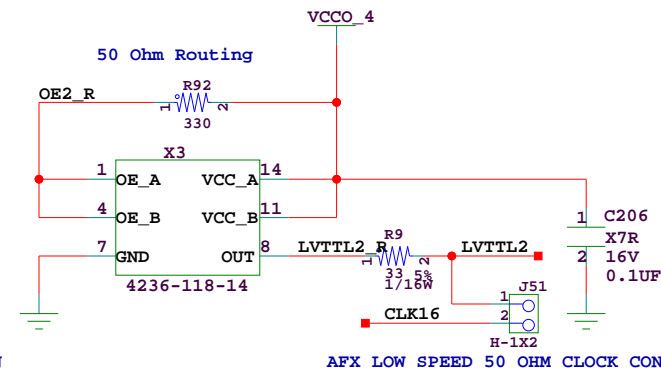
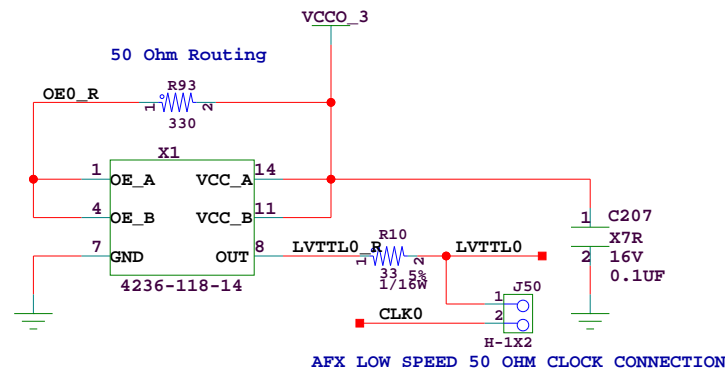
Title: SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401

CONFIGURATION

Date: 7-24-2006_13:32	Ver: B
Sheet Size: B	Rev: 01
Sheet 4 of 17	Drawn By D.L.

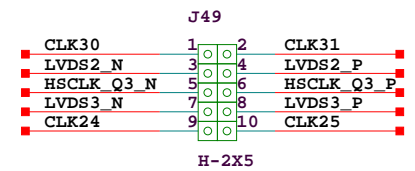
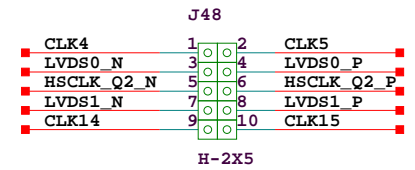
UPPER CLOCKS

BOTTOM CLOCKS



AFX CLOCK CONFIGURATION

1-3, 2-4: LOW SPEED 50 OHM CLOCK CONNECTION
 3-5, 4-6: HIGH SPEED 100 OHM DIFFERENTIAL CLOCK CONNECTION TO DIFFERENTIAL PAIR
 5-7, 6-8: HIGH SPEED 100 OHM DIFFERENTIAL CLOCK CONNECTION TO DIFFERENTIAL PAIR
 7-9, 8-10: LOW SPEED 50 OHM CLOCK CONNECTION



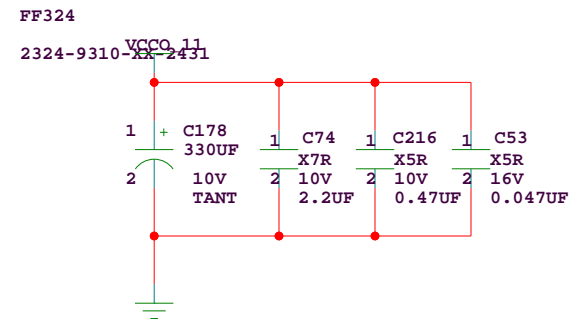
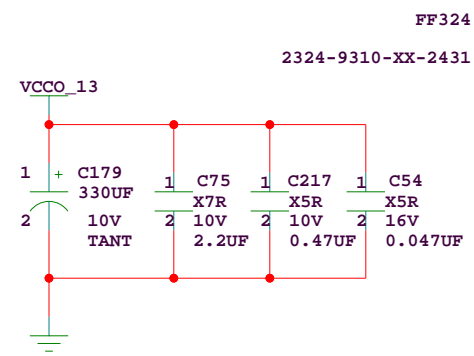
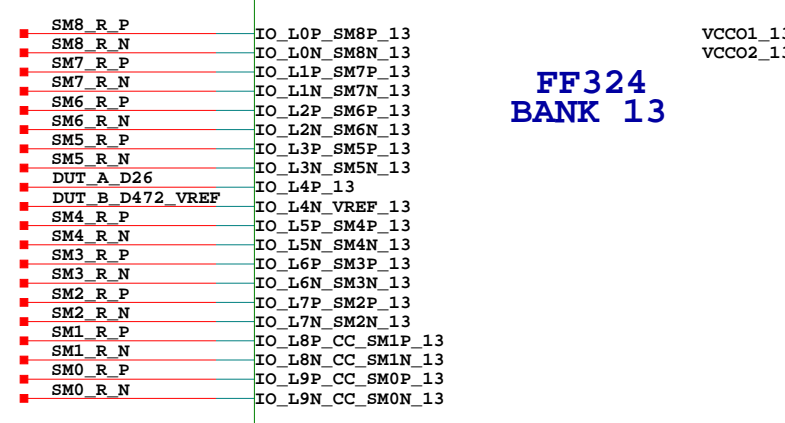
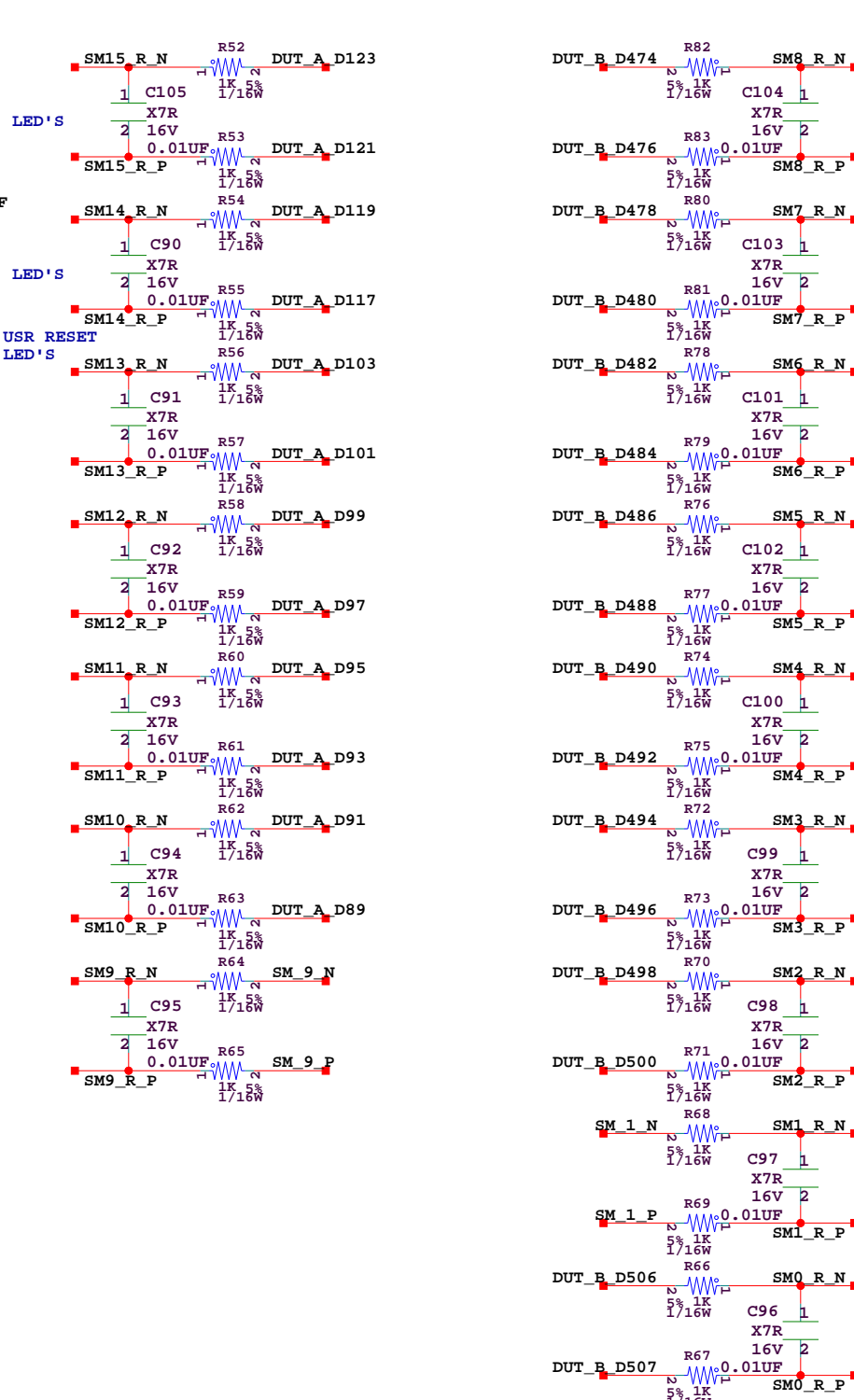
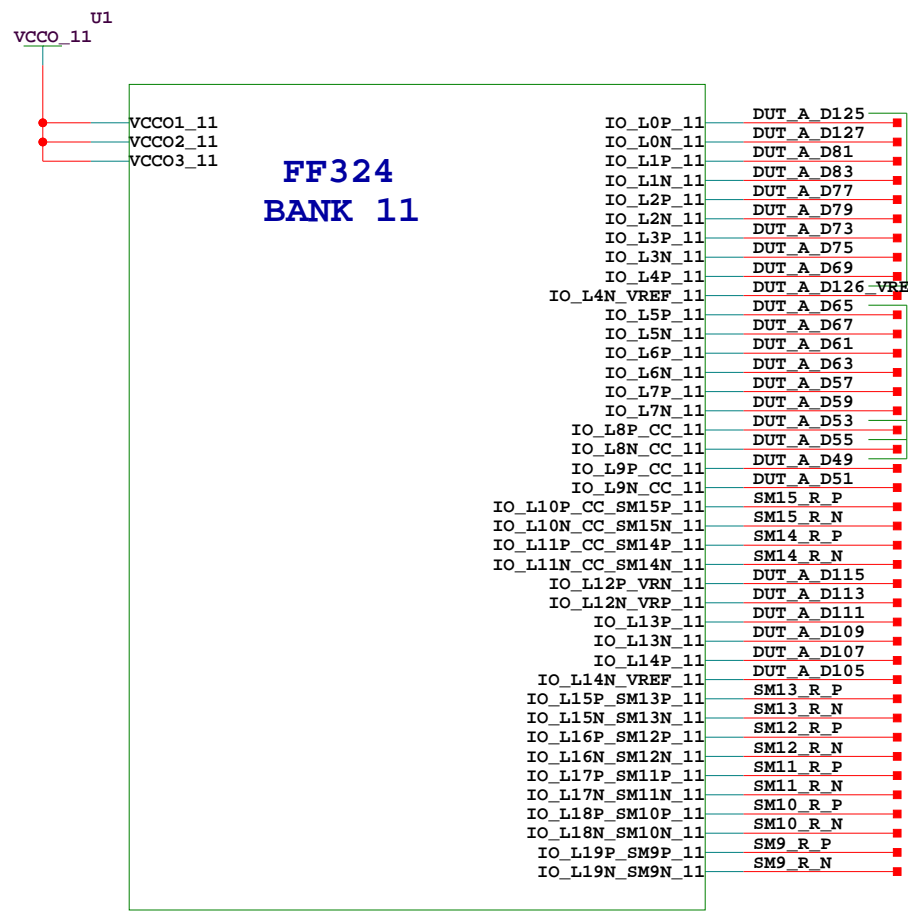
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SCH P/N 0381320-01
 ART P/N 0531589-01
 FAB P/N 1280401-01

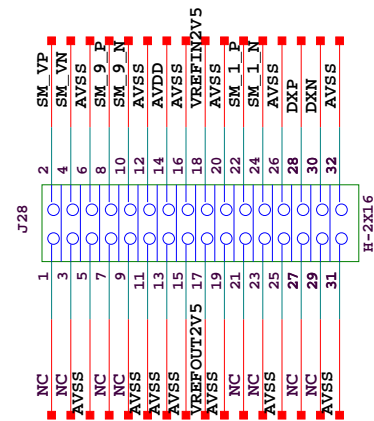
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SOCKET CLOCKS, SMA DIFF CLOCKS


Date: 7-20-2006_10:33 Ver: B
 Sheet Size: B Rev: 01
 Sheet 5 of 17 Drawn By D.L.

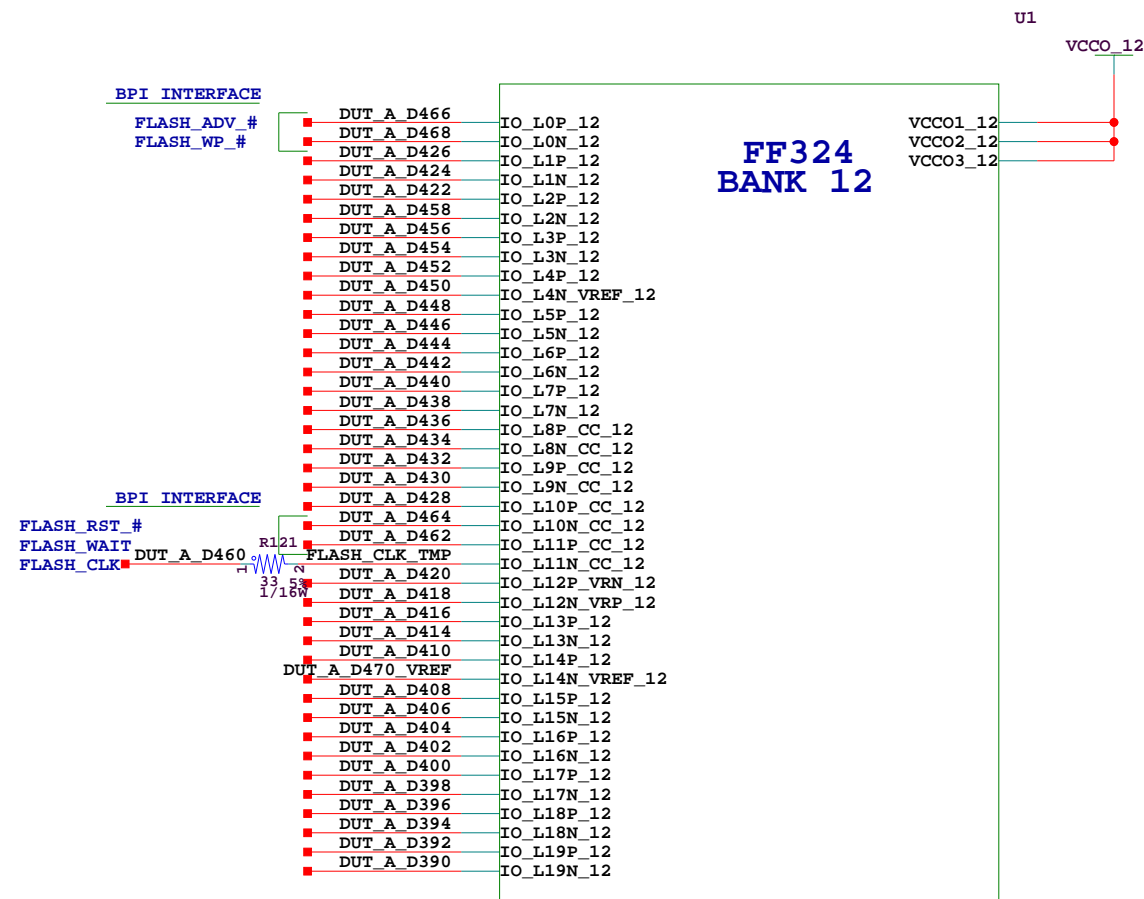
SYSTEM MONITOR FILTERS



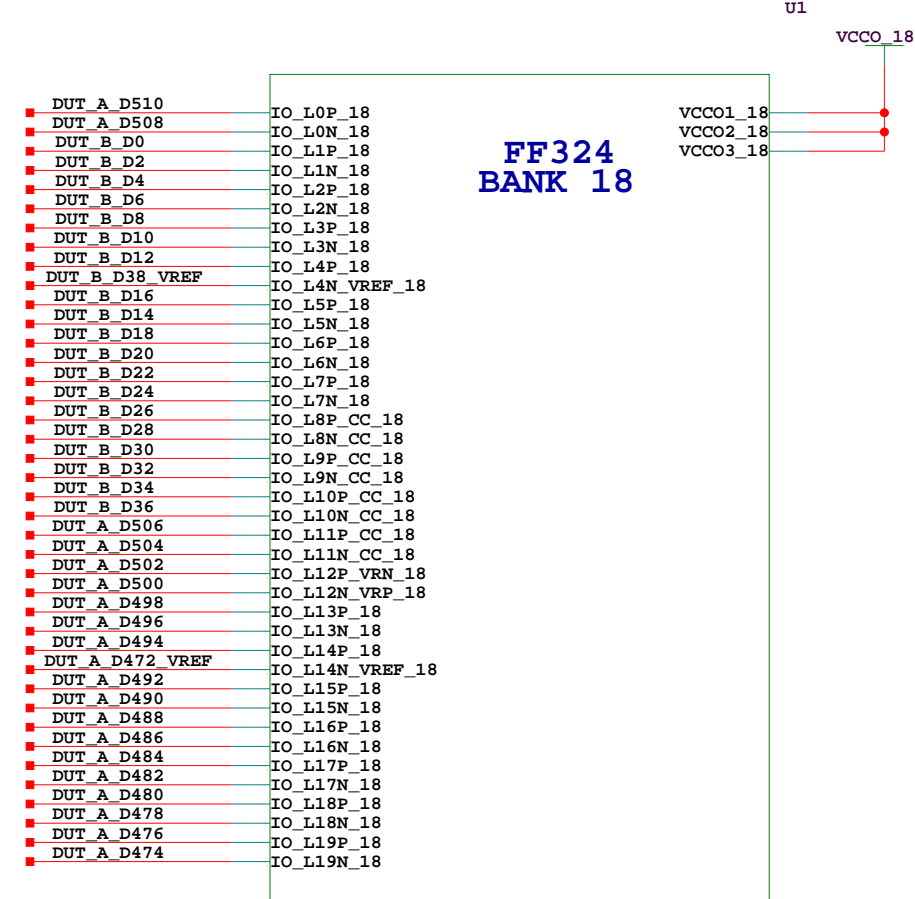
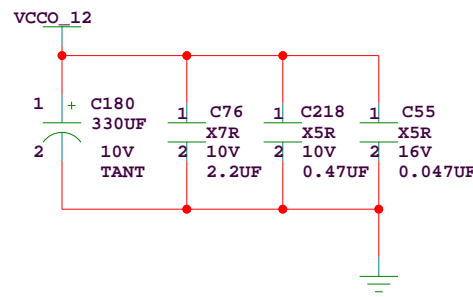
SYSTEM MONITOR MALE CONNECTOR



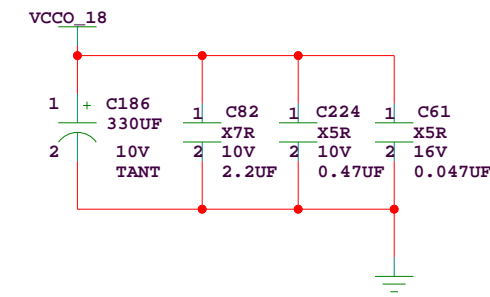
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Title: SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401			
SYSTEM MONITOR			
Date: 7-20-2006_10:33	Ver: B		
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Sheet 6 of 17	Drawn By D.L.		



FF324
2324-9310-XX-2431



FF324
2324-9310-XX-2431

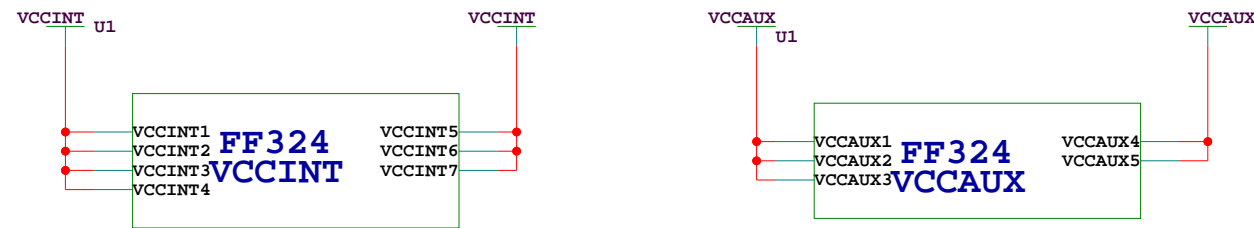
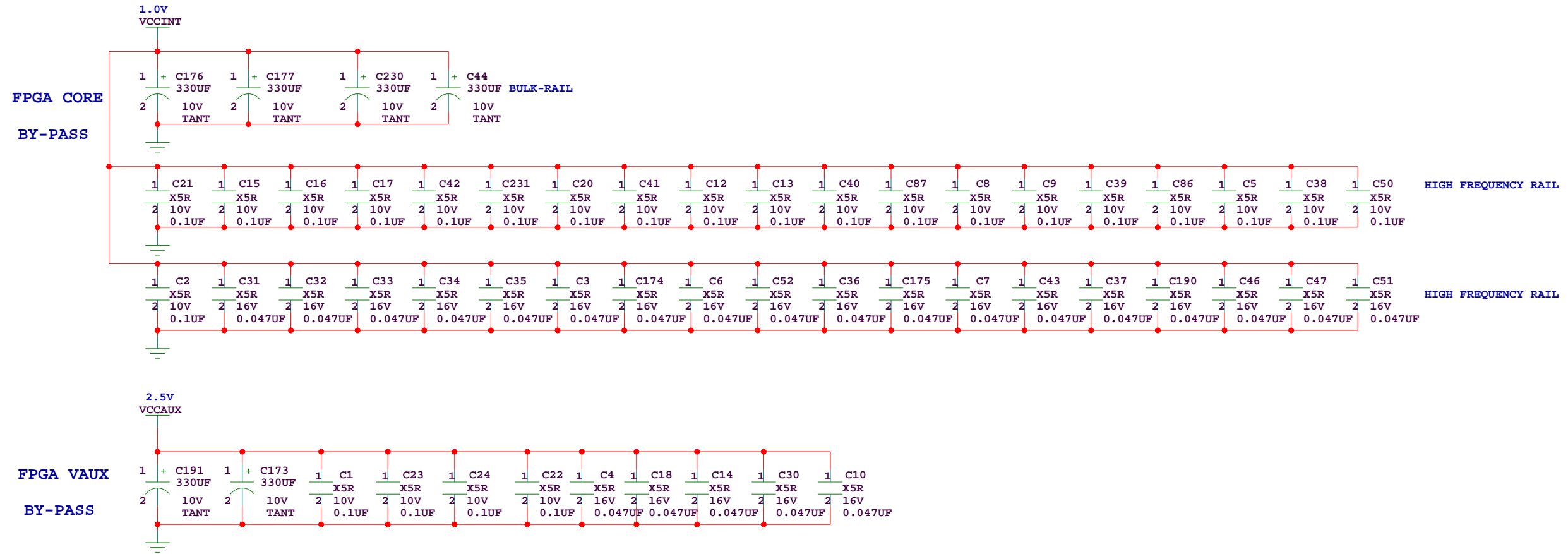


SCH P/N 0381320-01
ART P/N 0531589-01
FAB P/N 1280401-01

Title:
SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401

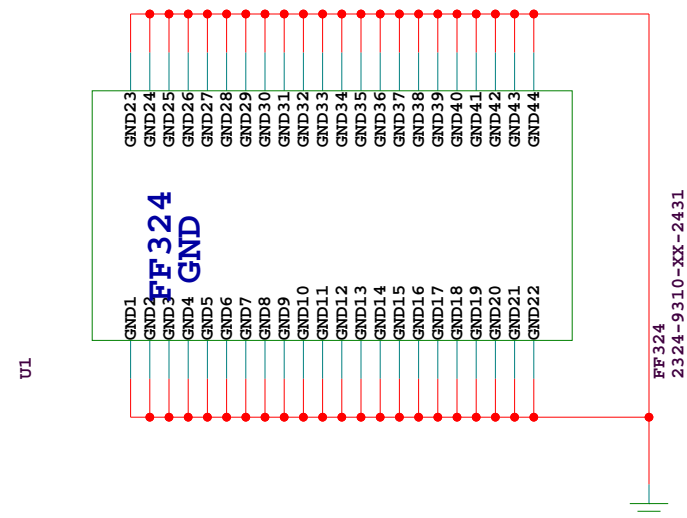
DUT INTERFACE

Date: 7-20-2006_10:33	Ver: B
Sheet Size: B	Rev: 01
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FF324
2324-9310-XX-2431

FF324
2324-9310-XX-2431



U1

FF324
2324-9310-XX-2431



SCH P/N 0381320-01
ART P/N 0531589-01
FAB P/N 1280401-01

Title:
SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401

FPGA DECOUPLING CAPACITORS

Date: 7-20-2006_10:33

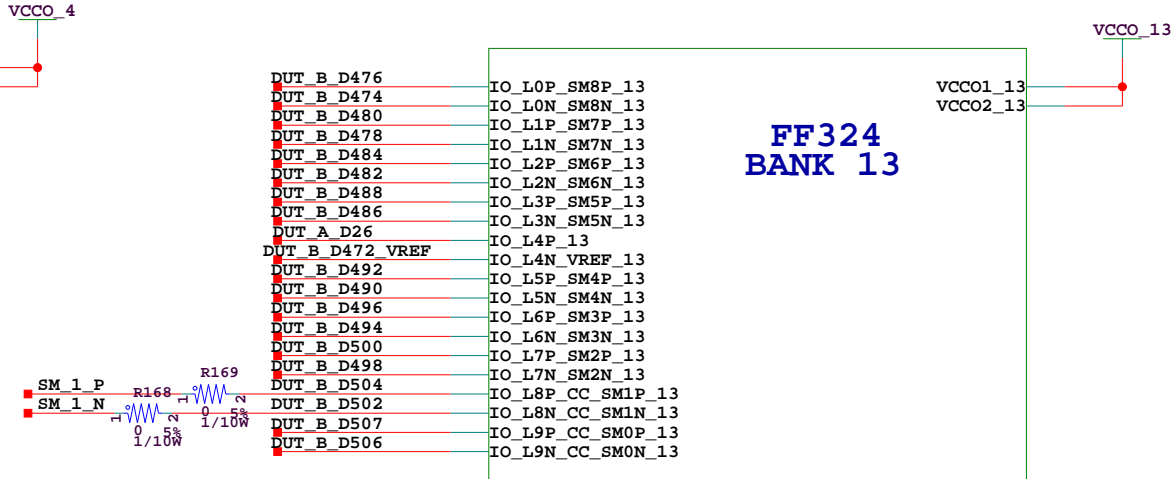
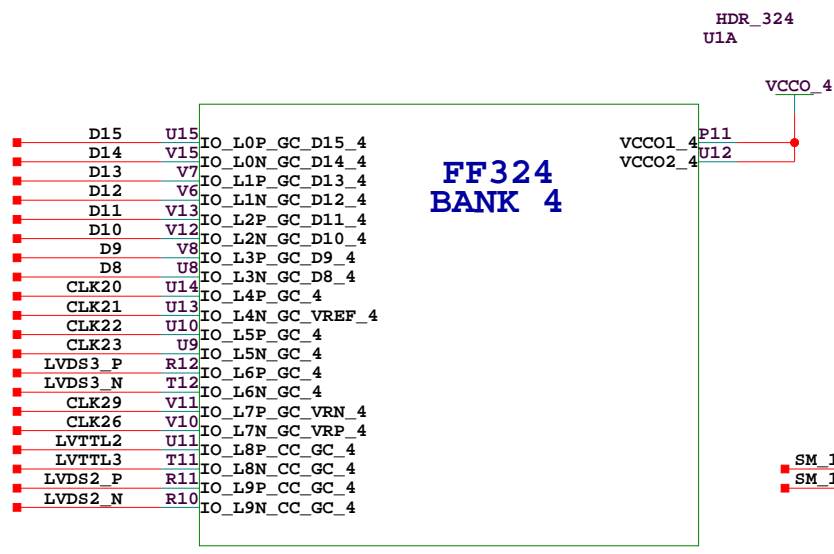
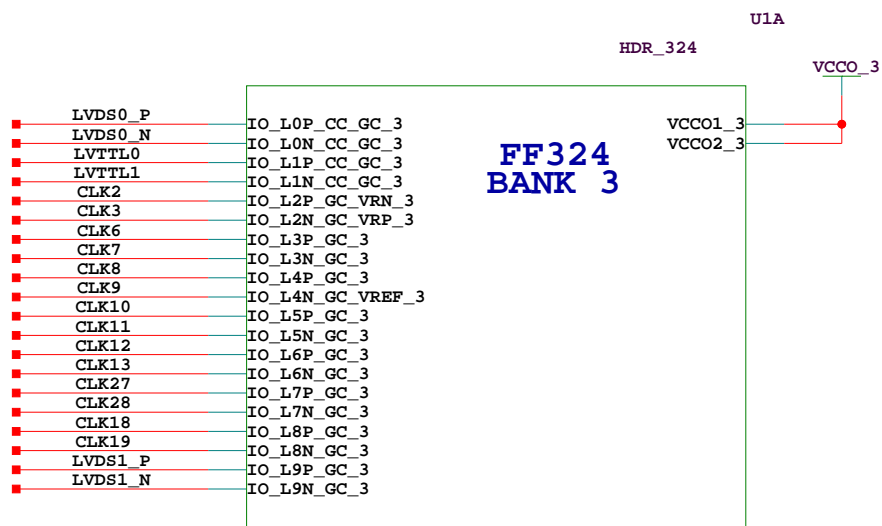
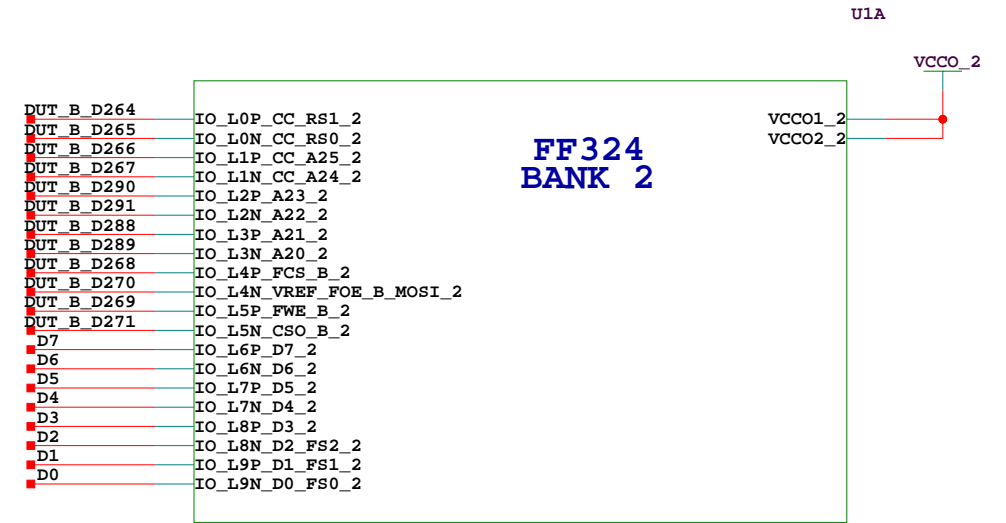
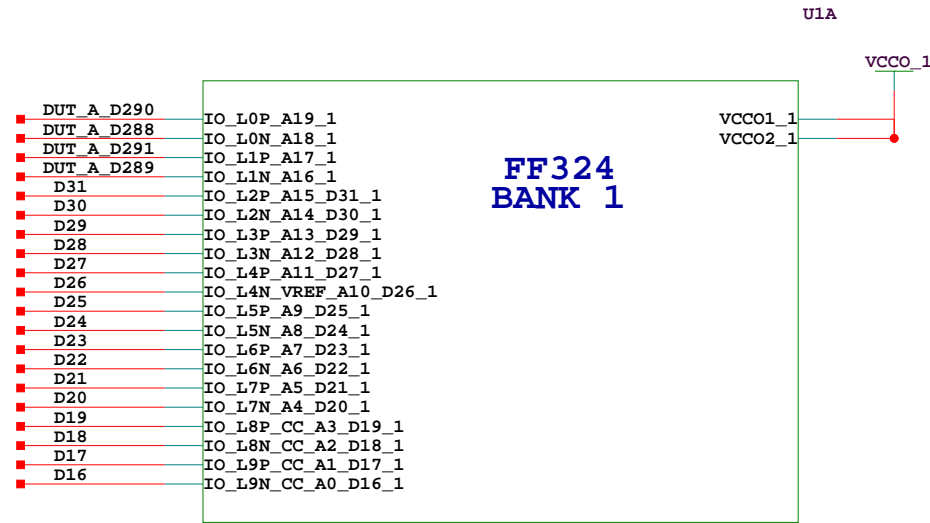
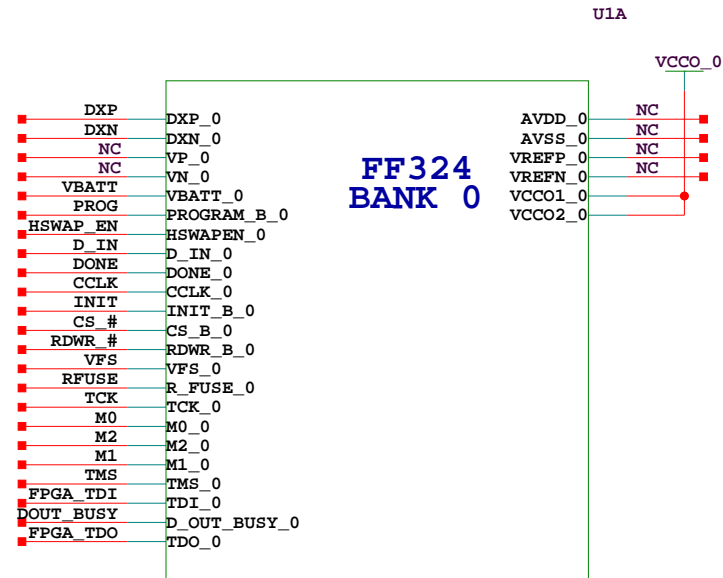
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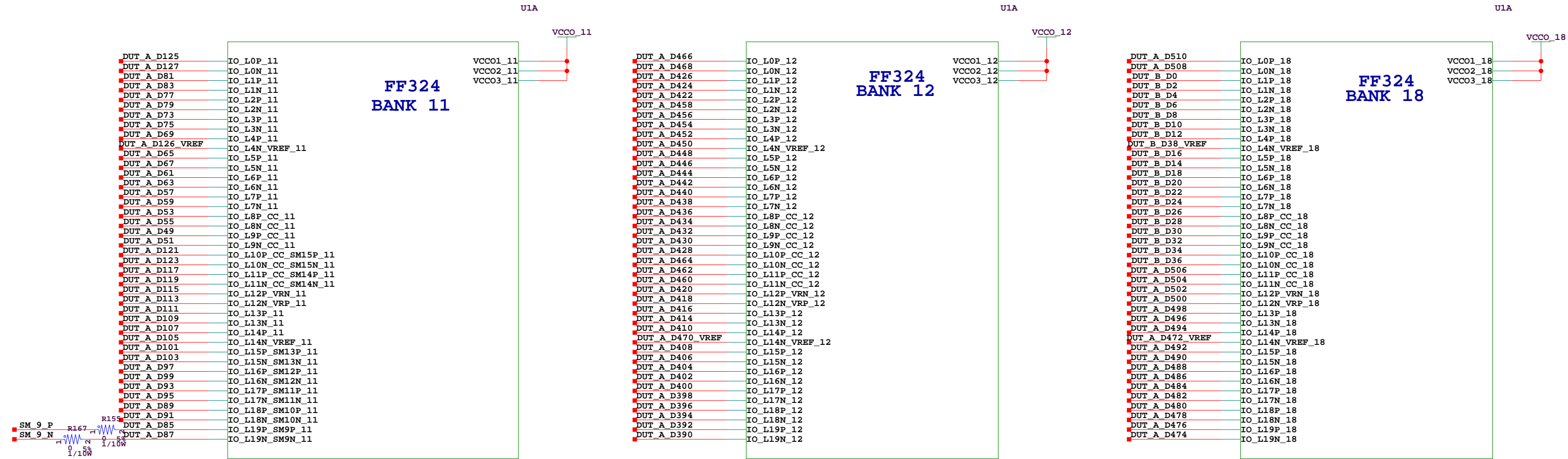
Rev: 01

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Drawn By D.L.




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		ART P/N	0531589-01
		FAB P/N	1280401-01
Title: SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401			
DUT TEST PINS			
Date: 7-20-2006_10:33		Ver: B	
Sheet Size: B		Rev: 01	
Sheet 9	of 17	Drawn By	D.L.

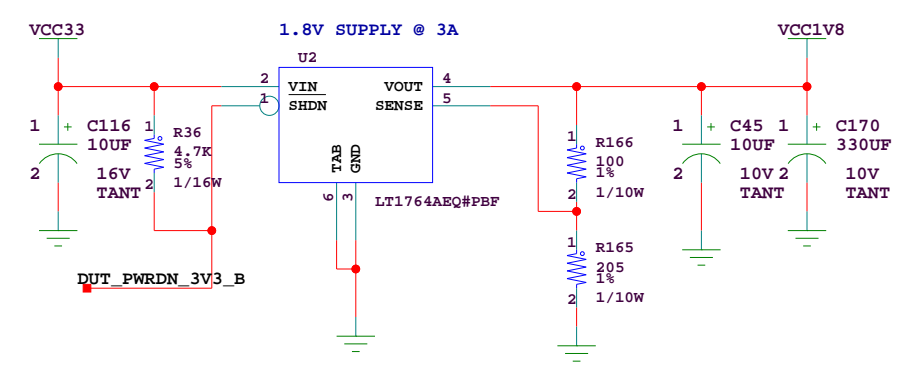
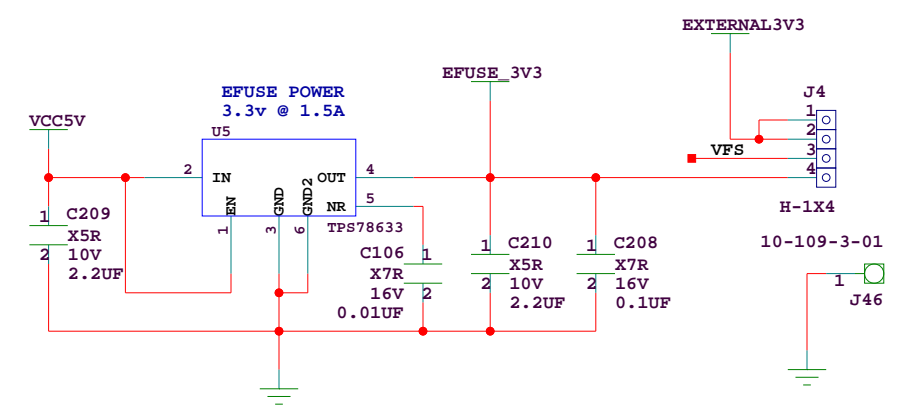
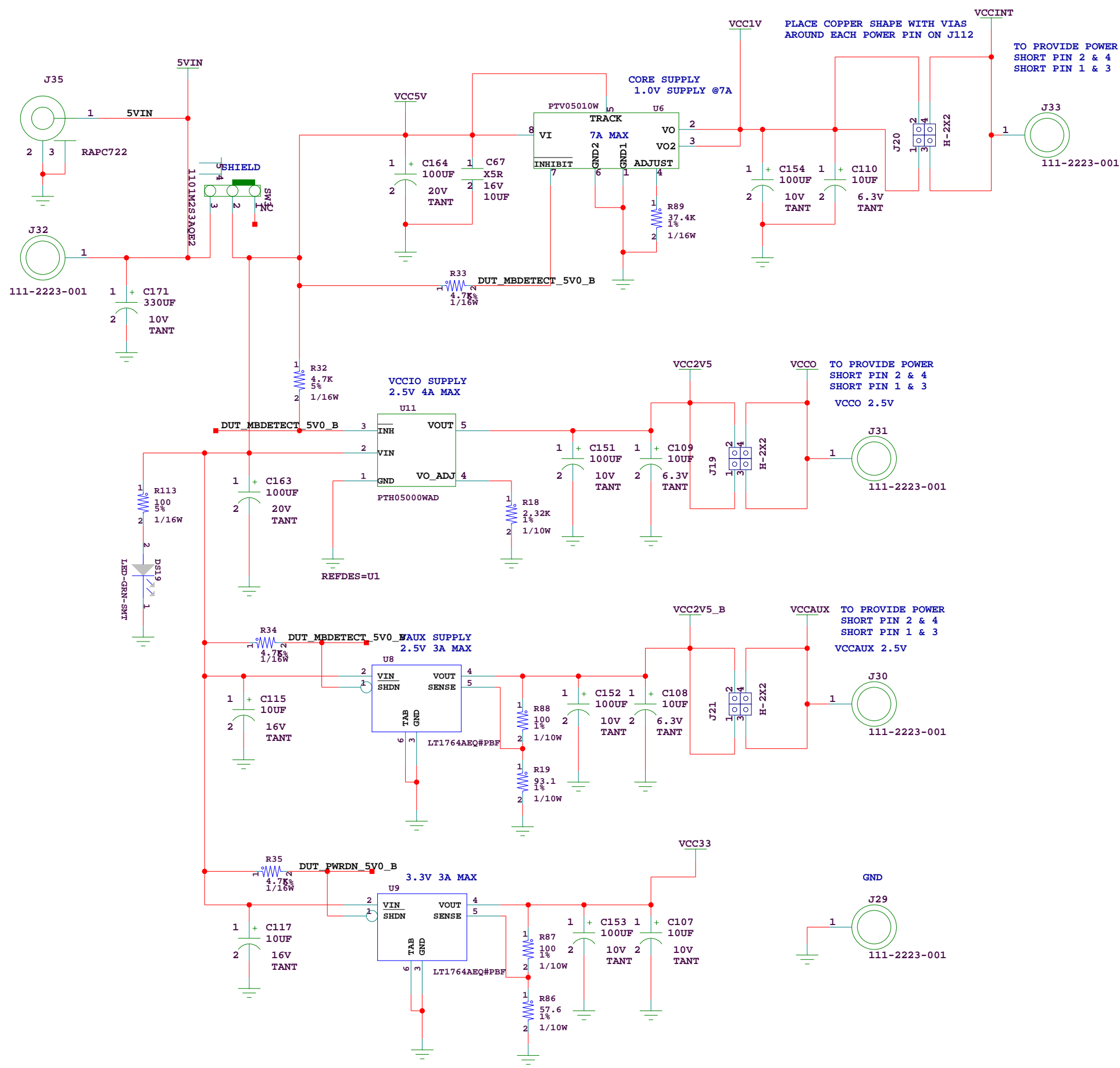


HDR_324

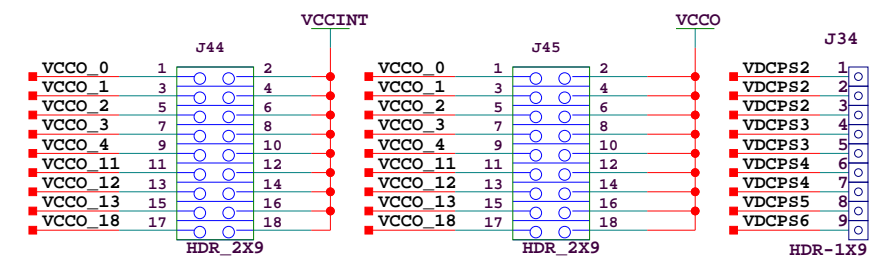
HDR_324

HDR_324

		SCH P/N	0381320-01
		ART P/N	0531589-01
		FAB P/N	1280401-01
Title: SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401 DUT TEST PINS			
Date: 7-20-2006_10:33		Ver: B	
Sheet Size: B		Rev: 01	
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VCC I/O SELECTION

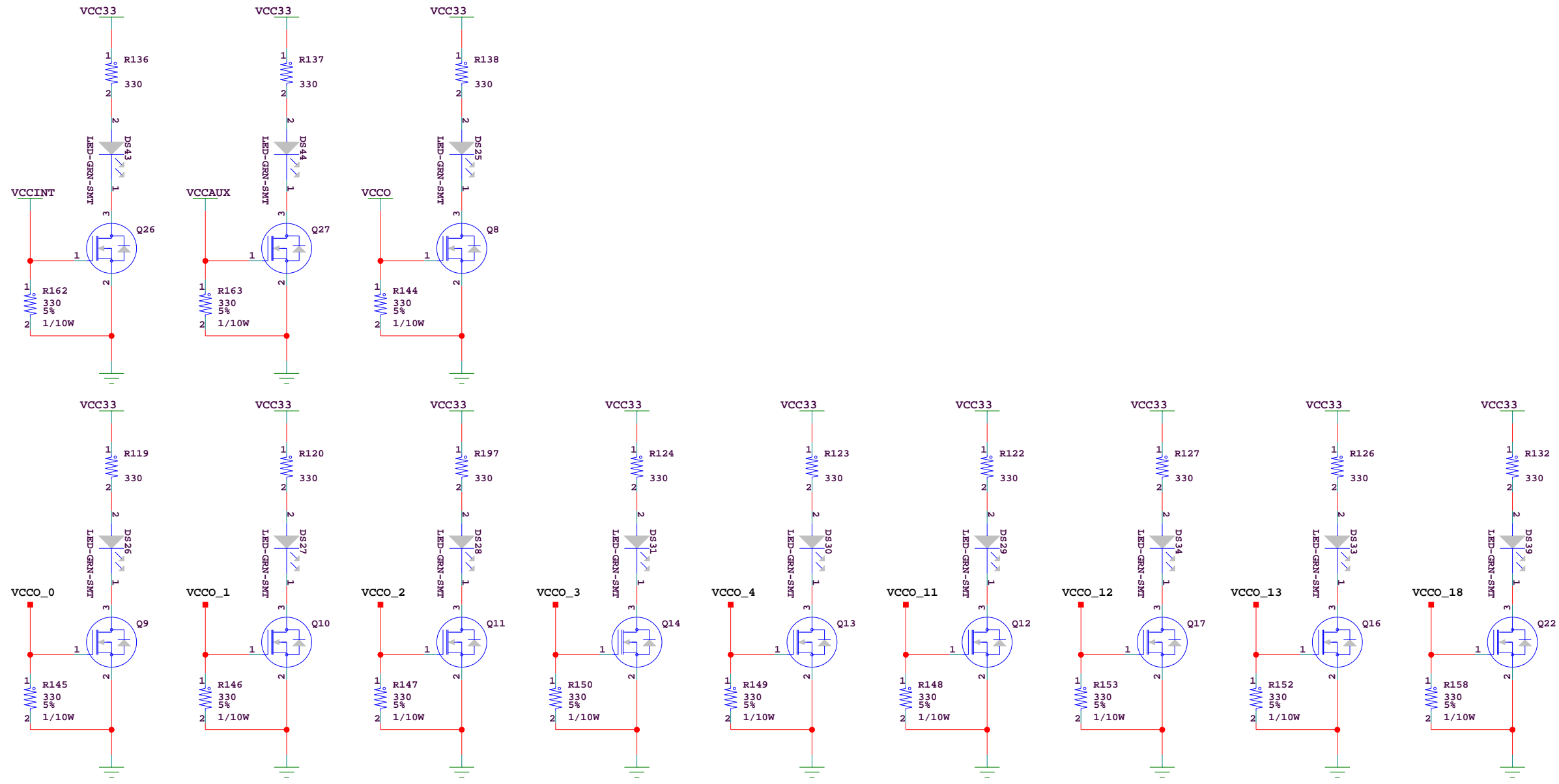



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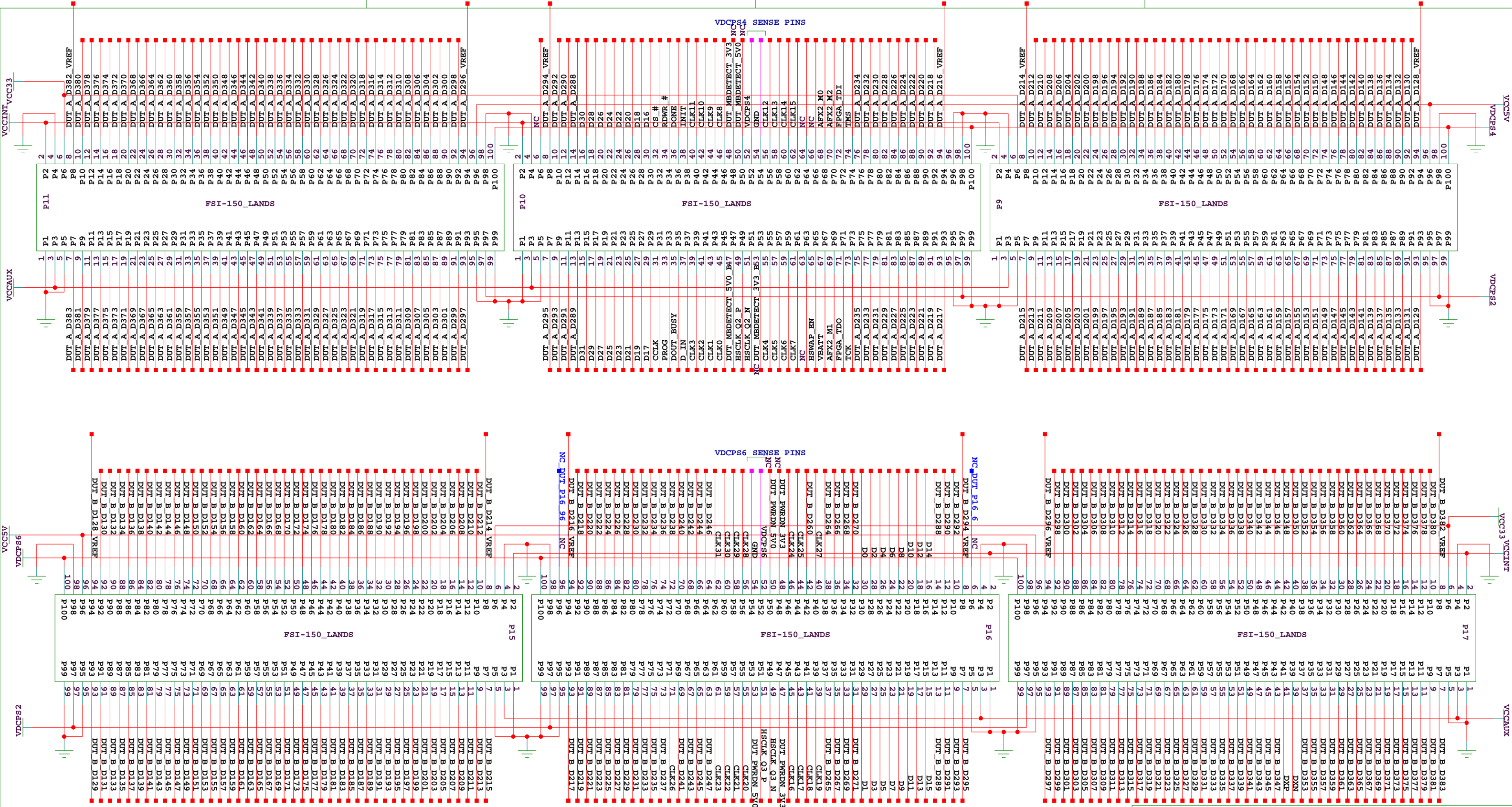
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 ART P/N 0531589-01
 FAB P/N 1280401-01

Title: SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401
FPGA POWER SUPPLY, E-FUSE

Date: 7-20-2006_10:33 Ver: B
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		ART P/N	0531589-01
		FAB P/N	1280401-01
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Date: 7-20-2006_10:33		Ver: B	
Sheet Size: B		Rev: 01	
Sheet 12	of 17	Drawn By D.L.	



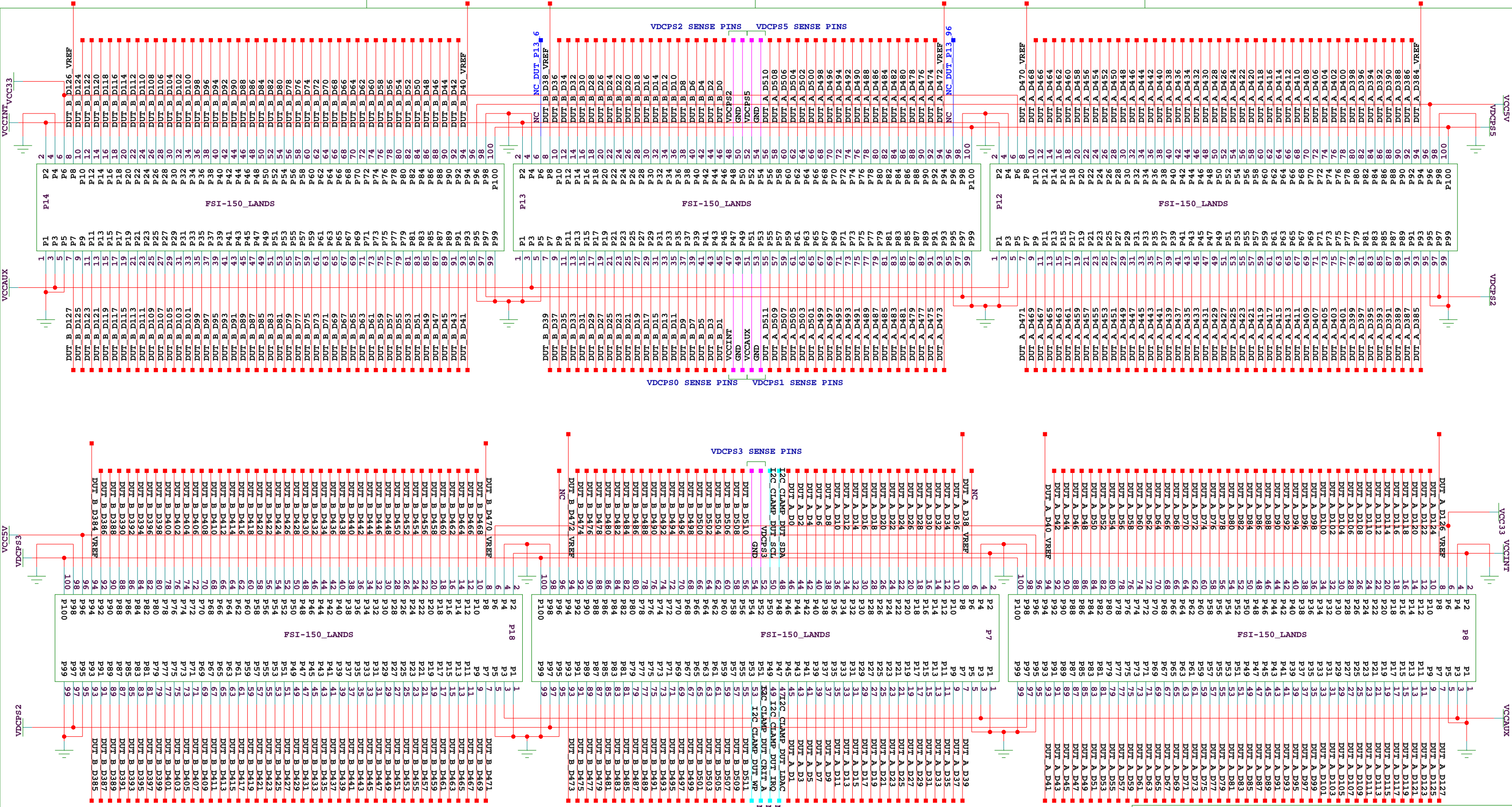
SCH P/N 0381320-01
 ART P/N 0531589-01
 FAB P/N 1280401-01

XILINX

Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401

AFX LANDINGS TOP AND BOTTOM

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Sheet 13 of 17	Drawn By D.L.





SCH P/N 0381320-01
 ART P/N 0531589-01
 FAB P/N 1280401-01

Title:
 SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401

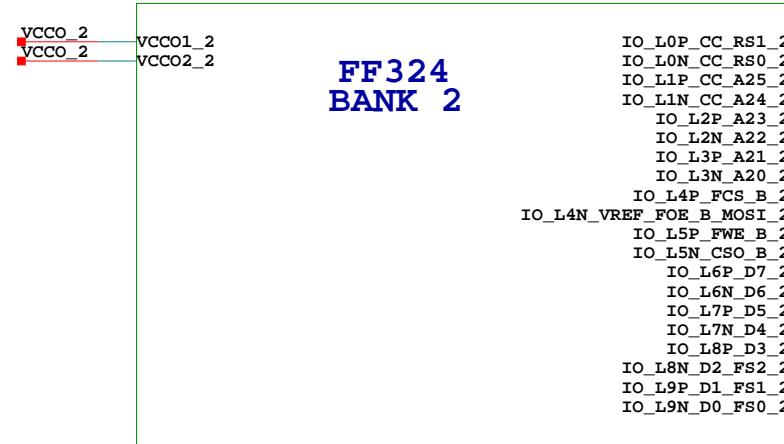
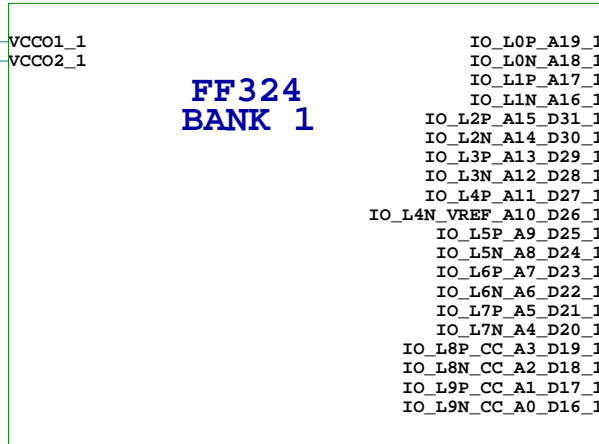
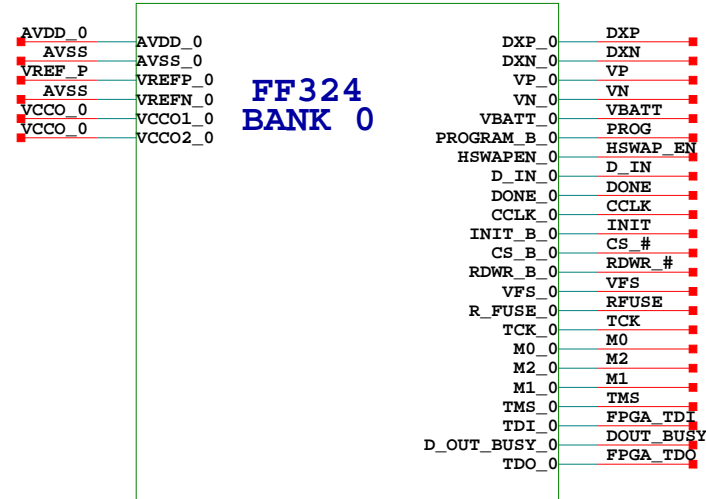
AFX LANDINGS LEFT AND RIGHT

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Sheet Size: B	Rev: 01
Sheet 14 of 17	Drawn By D.L.

US4

US4

US4



US4

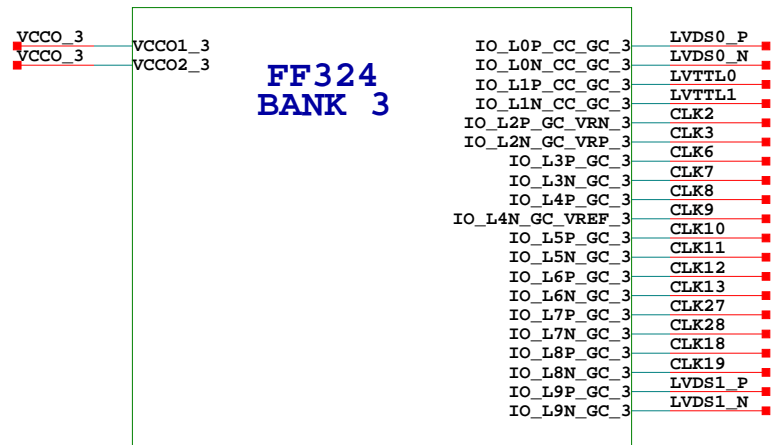
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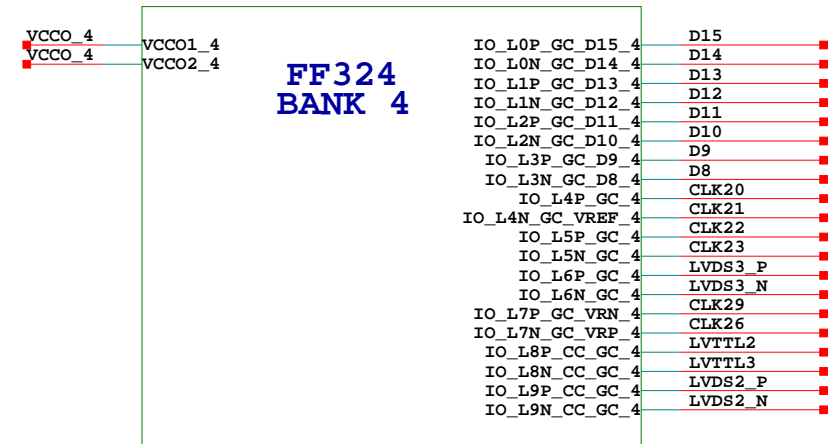
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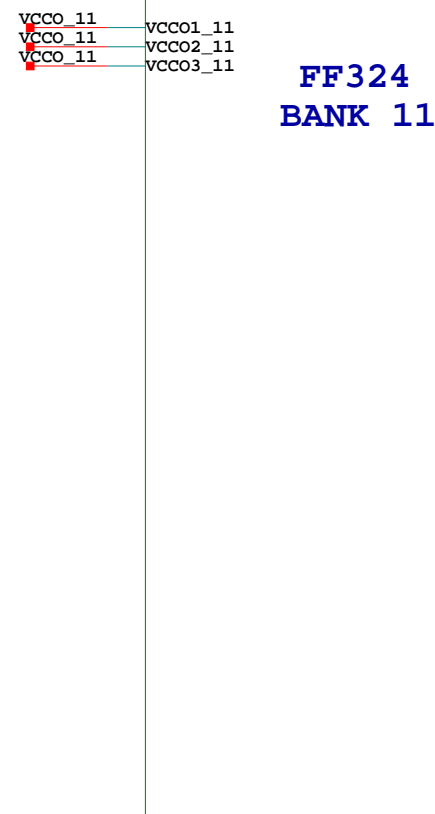
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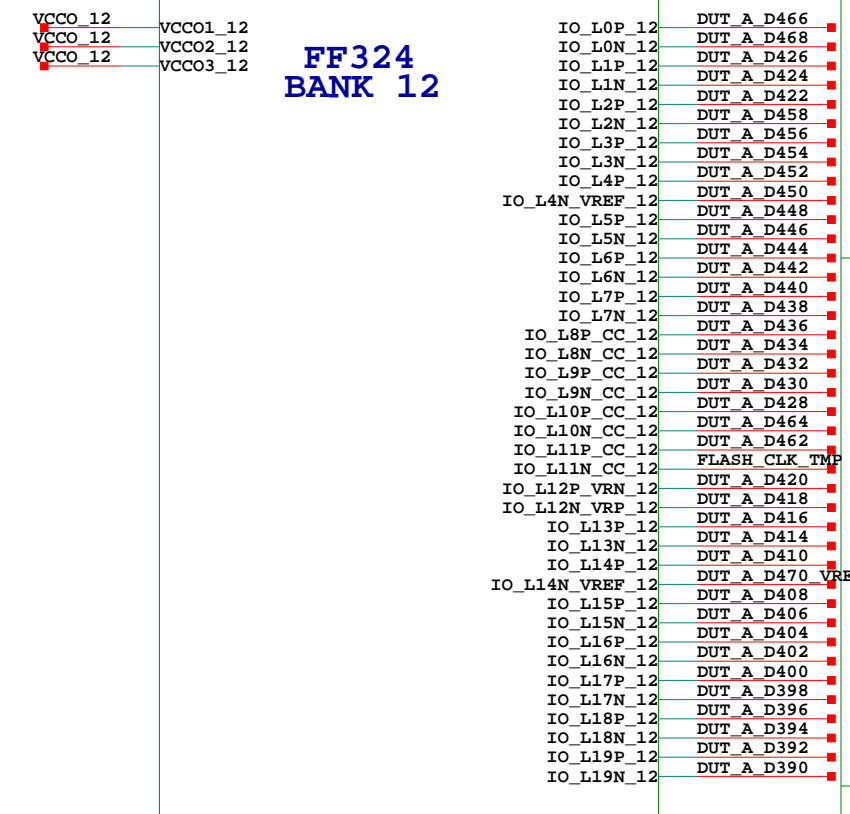
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FF324_SM



FF324_SM



FF324_SM

XILINX SCH P/N 0381320-01
 ART P/N 0531589-01
 FAB P/N 1280401-01

Title: SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401
MISC.

Date: 7-20-2006_10:33 Ver: B

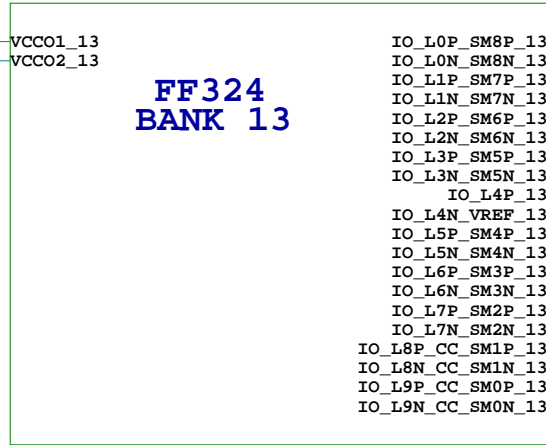
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Sheet 15 of 17 Drawn By D.L.

TEST SOCKET

US4

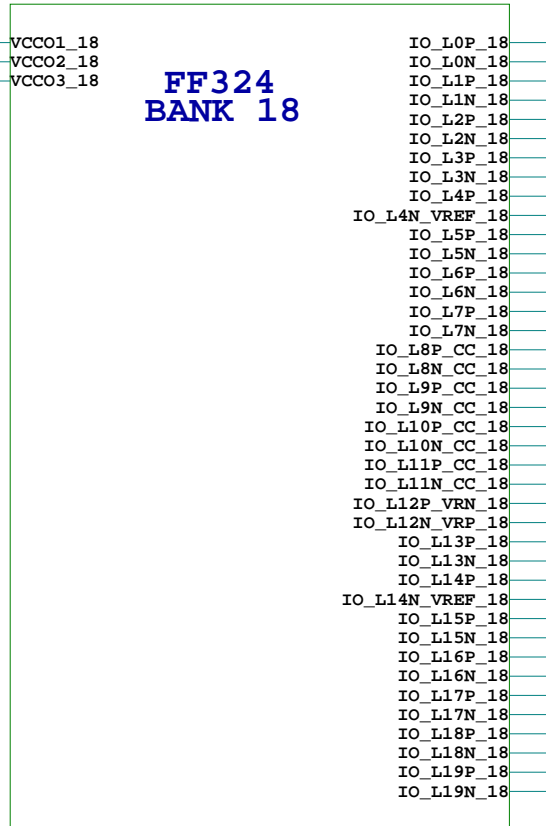
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VCCO_13



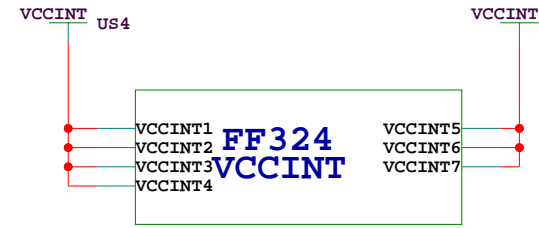
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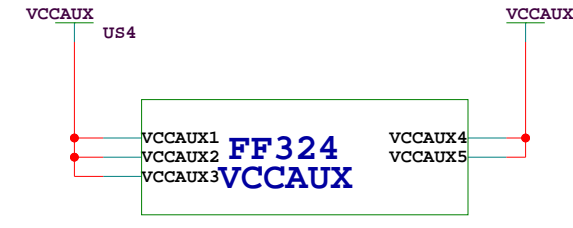
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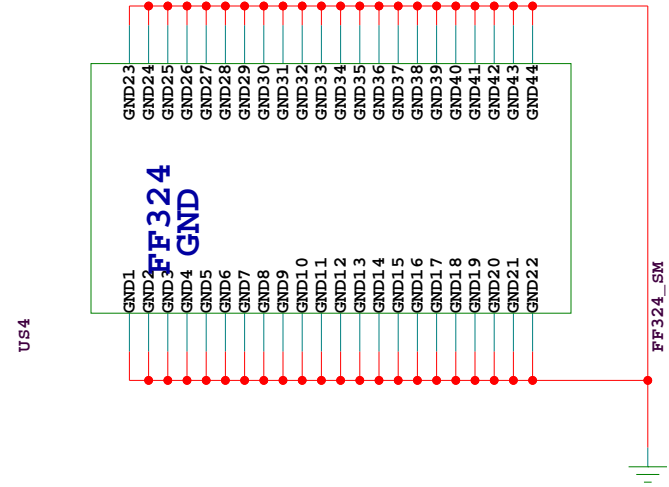
FF324_SM



FF324_SM



FF324_SM



TEST SOCKET

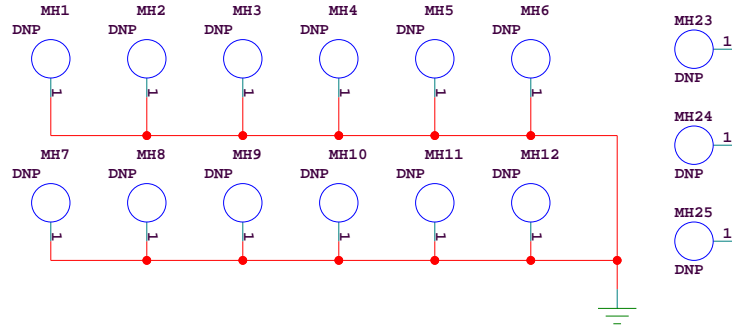
SCH P/N 0381320-01
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FAB P/N 1280401-01

Title: SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401 MISC.

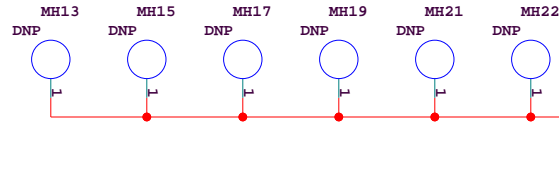
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Sheet 16 of 17	Drawn By D.L.

AFXII MOUNTING HOLES

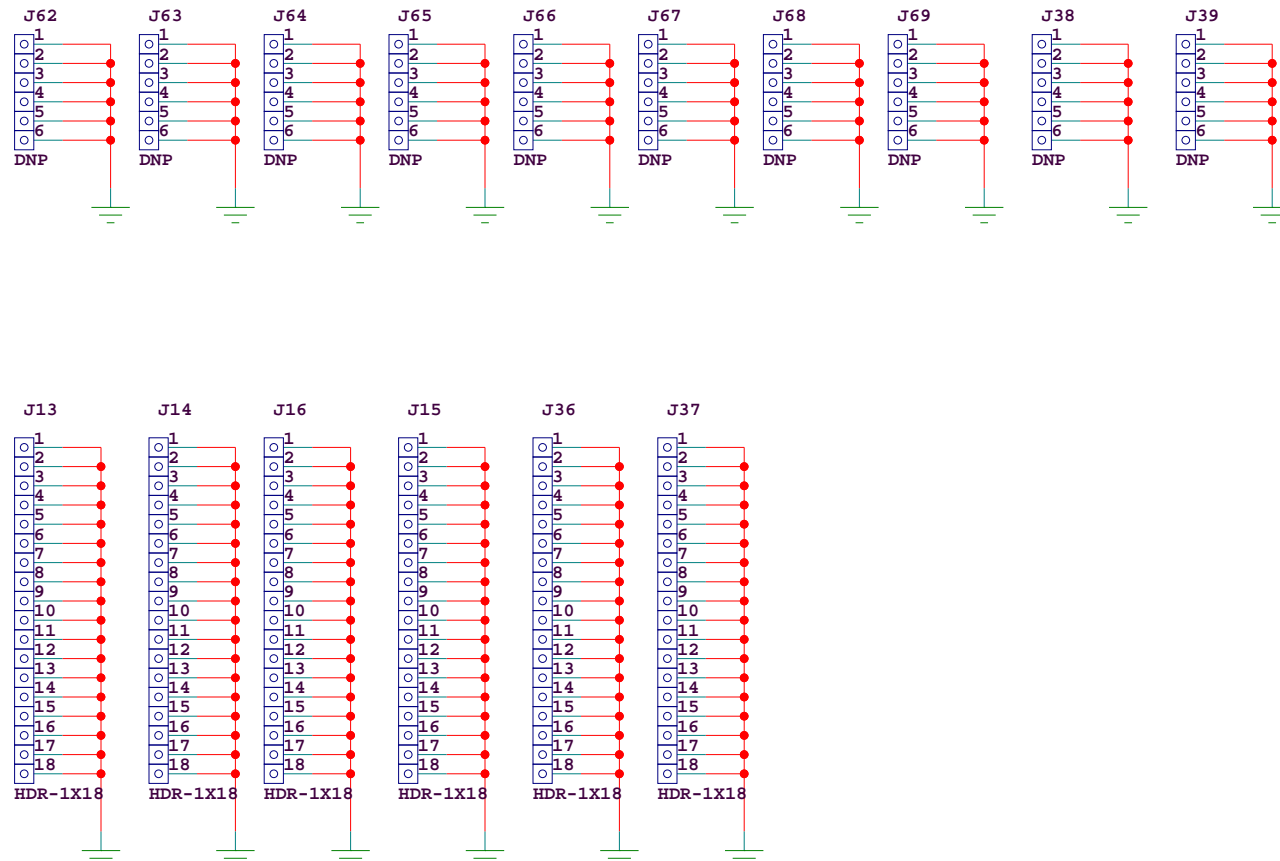
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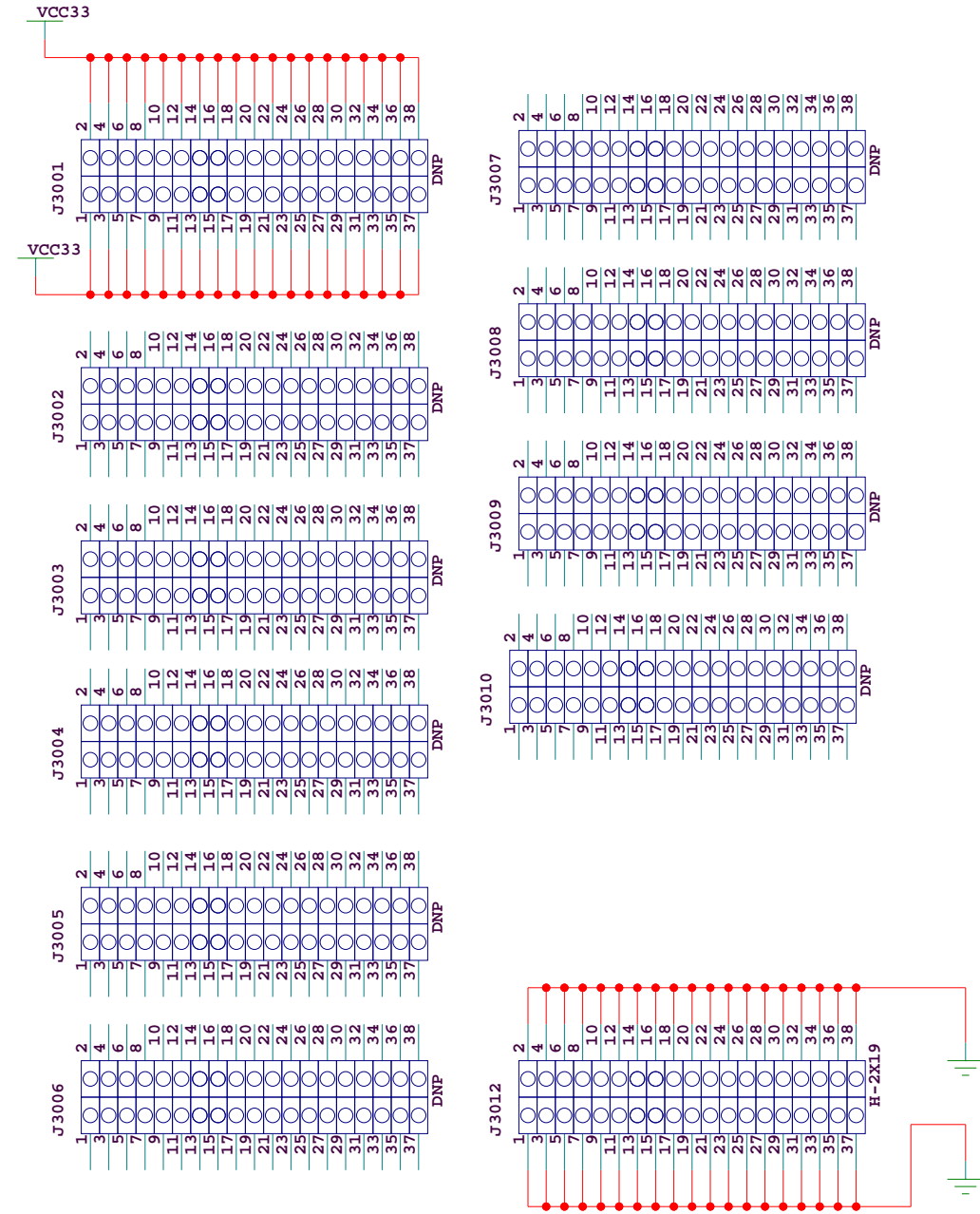
MOUNTING HOLES



DUT INTERLEAVE GND'S



BREADBOARD AREA



SCH P/N 0381320-01
 ART P/N 0531589-01
 FAB P/N 1280401-01

Title: SCHEM,ROHS COMPLIANT, VIRTEX 5 FF324 DAUGHTER, 1280401
HARDWARE AND BREADBOARD AREA

Date: 7-20-2006_10:33	Ver: B
Sheet Size: B	Rev: 01
Sheet 17 of 17	Drawn By D.L.