## Revision History

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<tr>
<th>Date</th>
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<tr>
<td>04/30/14</td>
<td>11.0</td>
<td>Recompiled for 2015.1. Removed Ethernet as per CR861391.</td>
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<tr>
<td>11/24/14</td>
<td>10.0</td>
<td>Recompiled for 2014.4.</td>
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<td>10/08/14</td>
<td>9.0</td>
<td>Recompiled for 2014.3.</td>
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<tr>
<td>06/09/14</td>
<td>8.0</td>
<td>Recompiled for 2014.2.</td>
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<td>7.0</td>
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<td>12/18/13</td>
<td>6.0</td>
<td>Recompiled for 2013.4.</td>
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<td>10/23/13</td>
<td>5.0</td>
<td>Recompiled for 2013.3. Converted to IPI, added RGMII interface and LwIP.</td>
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<td>06/19/13</td>
<td>4.0</td>
<td>Recompiled for 2013.2. AR55431, AR55531 and AR55738 fixed.</td>
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<tr>
<td>04/03/13</td>
<td>3.0</td>
<td>Recompiled for 2013.1. Added AR55431, AR55531 and AR55738. AR53420 Fixed.</td>
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<tr>
<td>02/04/13</td>
<td>2.1</td>
<td>As per AR54044, added 2012.4 device pack. Added AR53420 and AR54223.</td>
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<td>12/18/12</td>
<td>2.0</td>
<td>Recompiled for 2012.4</td>
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<tr>
<td>10/23/12</td>
<td>1.0</td>
<td>Initial Version.</td>
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Overview

» Xilinx AC701 Board
» Software Requirements
» AC701 Setup
» AC701 BIST (Built-In Self Test)
» Compile AC701 BIST Design
» Program AC701 with BIST Design
» References

Note: This presentation applies to the AC701
AC701 BIST Design Description

Description

- The Built-In System Test (BIST) application uses an IPI MicroBlaze system to verify board functionality. A UART based terminal program interface offers users a menu of tests to run.

Block Design Source

- AC701 BIST Design Files (2015.1 C) ZIP file
- Available through http://www.xilinx.com/ac701

Note: Presentation applies to the AC701
AC701 BIST Design Description

Block Design IP

- Processor and Subsystems: MicroBlaze, MicroBlaze Debug Module (MDM), Local Memory Bus (LMB), LMB BRAM Controller, Block Memory Generator, Processor System Reset, AXI Interrupt Controller
- AXI Bus: AXI Interconnect
- Memory: AXI BRAM Controller, Memory Interface Generator (MIG 7 Series)
- Peripherals: AXI IIC, AXI GPIO, AXI UART16550, XADC Wizard
- Other IP: Clocking Wizard, Constant, Concat, gte2_top

- [Designing IP Subsystems Using IP Integrator](https://www.xilinx.com) (UG994)

Note: Presentation applies to the AC701
Vivado Software Requirements


Note: Presentation applies to the AC701
AC701 Setup

» Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the AC701 board
  – Connect this cable to your PC
AC701 Setup

- Connect a USB Type-A to Mini-B cable to the USB UART connector on the AC701 board
  - Connect this cable to your PC
  - Power on the AC701 board for UART Drivers Installation
AC701 Setup

➢ Install USB UART Drivers
  – Refer to UG1033 for Installation details

Note: Presentation applies to the AC701
AC701 Setup

- Reboot your PC if necessary
- Right-click on My Computer and select Properties
  - Select the Hardware tab
  - Click on Device Manager

Note: Presentation applies to the AC701
AC701 Setup

» Expand the Ports

Hardware

– Right-click on Silicon Labs CP210x USB to UART Bridge and select Properties

Note: Presentation applies to the AC701
AC701 Setup

» Under Port Settings tab
  - Click Advanced
  - Set the COM Port to an open Com Port setting from COM1 to COM4

Note: Presentation applies to the AC701
AC701 Setup

- Refer to UG1036 for Tera Term installation
- Board Power must be on before starting Tera Term
- Start the Terminal Program
  - Select your USB Com Port
  - Set the baud to 9600

Note: Presentation applies to the AC701
AC701 Setup

- Unzip the AC701 BIST Design Files (2015.1 C) ZIP file
  - Available through http://www.xilinx.com/ac701

Note: Presentation applies to the AC701
Open a Vivado Tcl Shell:

Start → All Programs → Xilinx Design Tools → Vivado 2015.1 → Vivado 2015.1 Tcl Shell
Download the BIST bitstream

In the Vivado Tcl Shell type:

```
source C:/ac701_bist/ready_for_download/bist_download.tcl
```
AC701 BIST

View initial BIST screen

** Xilinx Artix-7 FPGA AC701 Evaluation Kit **

Choose Feature to Test:
1: UART Test
2: LED Test
3: IIC Test
4: TIMER Test
5: ROTARY Test
6: SWITCH Test
7: LCD Test
8: DDR3 External Memory Test
9: BRAM Internal Memory Test
B: BUTTON Test
0: Exit

Note: Presentation applies to the AC701
AC701 BIST

» UART Test

- Type “1” to start the UART Test
- After each test, press any key to return to the main menu

Note: Presentation applies to the AC701
AC701 BIST

- LED Test
  - Type 2 to begin LED Test
- View Walking 1’s pattern on GPIO LEDs
  - Sequence repeats twice

Note: Presentation applies to the AC701
AC701 BIST

IIC Test

- Type 3 to begin IIC Test

Note: Presentation applies to the AC701
AC701 BIST

Timer Test
- Type 4 to begin Timer Test

Note: Presentation applies to the AC701
AC701 BIST

 Rotary Test

 - Type 5 to begin Rotary Test
 - Turn the rotary switch (under the LCD) back and forth

Note: Presentation applies to the AC701
AC701 BIST

- **GPIO Switch Test**
  - Set 4-position GPIO DIP Switch (SW2)
  - Type **6** to begin GPIO Switch Test
    - Reads switch settings

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**Note:** Presentation applies to the AC701
AC701 BIST

LCD Test

- Type 7 to begin LCD Test

Note: Presentation applies to the AC701.
AC701 BIST

External Memory Test

- Type 8 to begin External Memory Test
AC701 BIST

➤ Internal Memory Test
  – Type 9 to begin BRAM Memory Test

![Tera Term VT window showing test results]

Note: Presentation applies to the AC701
AC701 BIST

Button Test

- Type B to begin Button Test

Note: Presentation applies to the AC701
Compile AC701 BIST Design
Compile AC701 BIST Design

- Open Vivado
  
  Start → All Programs → Xilinx Design Tools → Vivado 2015.1 → Vivado

- Select Open Project

**Note:** Presentation applies to the AC701
Compile AC701 BIST Design

Open the AC701 Design:

- `<Design Name>/ac701_bist.xpr`

Note: Presentation applies to the AC701
Compile AC701 BIST Design

The design is fully implemented; you can recompile, or export to SDK

– To recompile, right-click synth_1, select **Reset Runs** then **Generate Bitstream**
Compile AC701 BIST Design

➢ Once done, both the Synthesis and Implementation will have green check marks

Note: Presentation applies to the AC701
Compile AC701 BIST Design

- The BIST Design has been implemented with IP Integrator (IPI)
- Click Open Block Design

Note: Presentation applies to the AC701
Compile AC701 BIST Design

» All the IP Blocks used in the design can be seen in this view

» Click Open Implemented Design

Note: Presentation applies to the AC701
Compile AC701 BIST Design

View Implemented Design

Note: Presentation applies to the AC701
Compile AC701 BIST Design

- Select File → Export → Export Hardware
- Click OK

Note: Presentation applies to the AC701
Compile AC701 BIST Design

- Select File → Launch SDK
- Click OK

Note: Presentation applies to the AC701
Compile AC701 Software in SDK

SDK Software Compile - Build ELF files in SDK

– When done, close SDK and return to Vivado

Note: Presentation applies to the AC701
Program AC701 with BIST Design
Program AC701 with BIST Design

Click Add Sources
Program AC701 with BIST Design

Select Add or Create Design Sources

Note: Presentation applies to the AC701
Program AC701 with BIST Design

- Add bist_app.elf from the SDK tree
- Make sure Copy sources into project is deselected
- Click Finish

Note: Presentation applies to the AC701
Program AC701 with BIST Design

Right-click on bist_app.elf and select Associate ELF Files…
Program AC701 with BIST Design

- Click the button to the right; select the bist_app.elf then click OK twice

Note: Presentation applies to the AC701
Program AC701 with BIST Design

», Click Generate Bitstream

- This creates a bitstream with the BIST ELF file

Note: Presentation applies to the AC701
Program AC701 with BIST Design

» Click Open Hardware Manager

Note: Presentation applies to the AC701
Program AC701 with BIST Design

Click Open target and select Auto Connect

Note: Presentation applies to the AC701
Program AC701 with BIST Design

Select Program device → xc7a200t_0

Note: Presentation applies to the AC701
Program AC701 with BIST Design

- Program Device defaults to impl_1 bitstream
- Click Program

Note: Presentation applies to the AC701
Program AC701 with BIST Design

- BIST Application runs in the terminal window

**Note:** Presentation applies to the AC701
Program AC701 with BIST Design

Close the Project

Note: Presentation applies to the AC701
Program AC701 with BIST Design

- Repeat this process using Tcl scripts
- Open a Vivado Tcl shell and type:
  
  ```
  source C:/ac701_bist/ready_for_download/make_download_files.tcl
  ```
- This script uses Tcl commands to add the ELF files to the BIST project, then generates the BIST bitstream

Note: Presentation applies to the AC701
Program AC701 with BIST Design

- Download the BIST bitstream
- In the Vivado Tcl Shell type:
  ```
  cd C:/ac701_bist/ready_for_download
  source bist_download.tcl
  ```

Note: Presentation applies to the AC701
Program AC701 with BIST Design

BIST Application runs in the terminal window

Note: Presentation applies to the AC701
References
References

➤ IP Integrator Documentation
  – Designing IP Subsystems Using IP Integrator – UG994

➤ 7 Series Configuration
  – 7 Series FPGAs Configuration User Guide
Documentation

Artix-7

- Artix-7 FPGA Family
- Design Advisory Master Answer Record for Artix-7 FPGAs

AC701 Documentation

- Artix-7 FPGA AC701 Evaluation Kit
- AC701 Getting Started Guide – UG967
- AC701 User Guide – UG952