# Revision History

The following table shows the revision history for this document.

<table>
<thead>
<tr>
<th>Section</th>
<th>Revision Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>10/31/2019 Version 1.1</strong></td>
<td>All sections. Updated to the Vitis™ unified software platform throughout.</td>
</tr>
<tr>
<td><strong>02/15/2019 Version 1.0</strong></td>
<td>Initial Xilinx release. N/A</td>
</tr>
</tbody>
</table>
Chapter 1

Introduction

**IMPORTANT! Except where noted, this user guide applies to both the U200 and U250 cards.**

The Xilinx® Alveo™ U200/U250 Data Center accelerator cards are peripheral component interconnect express (PCIe®) Gen3 x16 compliant cards featuring the Xilinx Virtex® UltraScale+™ technology. These cards accelerate compute-intensive applications such as machine learning, data analytics, video processing, and more. The Alveo U200/U250 Data Center accelerator cards are available in passive and active cooling configurations. The following figure shows a passively cooled Alveo U200 accelerator card.
CAUTION! The Alveo U200/U250 accelerator card with passive cooling is designed to be installed into a data center server, where controlled air flow provides direct cooling. Due to the card enclosure, switches are not accessible and LEDs are not visible (except for the triple-LED module DS3 that protrudes through the left front end PCIe bracket). The card details in this user guide are provided to aid understanding of the card features. If the cooling enclosure is removed from the card and the card is powered-up, external fan cooling airflow MUST be applied to prevent over-temperature shut-down and possible damage to the card electronics. Removing the cooling enclosure voids the board warranty.

See Appendix C: Additional Resources and Legal Notices for references to documents, files, and resources relevant to the Alveo U200/U250 accelerator cards.
Block Diagram

The block diagram of the Alveo U200/U250 accelerator card is shown in the following figure.

Figure 2: Card Block Diagram

Card Features

The Alveo U200/U250 accelerator card features are listed in this section. Detailed information for each feature is provided in Chapter 3: Card Component Description.

- Alveo U200 accelerator card:
  - Virtex UltraScale+ XCU200-2FSGD2104E FPGA

- Alveo U250 accelerator card:
  - Virtex UltraScale+ XCU250-2LFIGD2104E FPGA
- Memory (four independent dual-rank DDR4 interfaces)
  - 64 gigabyte (GB) DDR4 memory
  - 4x DDR4 16 GB, 2400 mega-transfers per second (MT/s), 64-bit with error correcting code (ECC) DIMM
  - x4/x8 unregistered dual inline memory module (UDIMM) support
- Configuration options
  - 1 gigabit (Gb) Quad Serial Peripheral Interface (SPI) flash memory
  - Micro-AB universal serial bus (USB) JTAG configuration port
- 16-lane PCI Express
- Two QSFP28 connectors 100G interfaces
- USB-to-UART FT4232HQ bridge with Micro-AB USB connector
- PCIe Integrated Endpoint block connectivity
  - Gen1, 2, or 3 up to x16
- I2C bus
- Status LEDs
- Power management with system management bus (SMBus) voltage, current, and temperature monitoring
- Dynamic power sourcing based on external power supplied
- 65W PCIe slot functional with PCIe slot power only
- 150 W PCIe slot functional with 110 A max $V_{CCINT}$ current PCIe slot power and 6-pin PCIe AUX power cable connected
- 225 W PCIe slot functional with 160 A max $V_{CCINT}$ current PCIe slot power and 8-pin PCIe AUX power cable connected
- Onboard reprogrammable flash configuration memory
- Front panel JTAG and universal asynchronous receiver-transmitter (UART) access through the USB port
- FPGA configurable over USB/JTAG and Quad SPI configuration flash memory
Card Specifications

Dimensions

Height: 4.376 inch (11.115 cm)
PCB thickness (±5%): 0.062 inch (0.157 cm)
Card length, passive heat sink: 9.2 inch (23.4 cm)
Card thickness with heat sink enclosure installed:
  Passive: 1.44 inch (3.66 cm)

Note: A 3D model of this card is not available.

Environmental

Temperature
Operating: 0°C to +45°C
Storage: −25°C to +60°C

Humidity
10% to 90% non-condensing

Operating Voltage
PCIe® slot +12 V_{DC}, +3.3 V_{DC}, +3.3 V_{\text{AUXDC}}, External +12 V_{DC}

Design Flows

The preferred optimal design flow for targeting the Alveo Data Center accelerator card uses the Vitis™ unified software platform. However, traditional design flows, such as RTL or HLx are also supported using the Vivado® Design Suite tools. The following figure shows a summary of the design flows.
Requirements for the different design flows are listed in the following table.

**Table 1: Requirements to Get Started with Alveo Data Center Accelerator Card Design Flows**

<table>
<thead>
<tr>
<th></th>
<th>RTL Flow</th>
<th>HLx Flow</th>
<th>Vitis</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flow documentation</td>
<td>UG949¹</td>
<td>UG895²</td>
<td>UG1301³</td>
</tr>
<tr>
<td>Hardware documentation</td>
<td>UG1289</td>
<td>UG1289</td>
<td>N/A</td>
</tr>
<tr>
<td>Vivado tools support</td>
<td>Board support XDC</td>
<td>Board support XDC</td>
<td>N/A</td>
</tr>
<tr>
<td>Programming the FPGA</td>
<td>Vivado Hardware Manager</td>
<td>Vivado Hardware Manager</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
3. *Getting Started with Alveo Data Center Accelerator Cards (UG1301).*

For either the RTL or HLx flow, designers can start by targeting the Alveo Data Center accelerator card in the Vivado® tools. In the Vivado Design Suite, select **Create New Project → RTL Project**, and then select the Alveo Data Center accelerator U200 card as shown in the following figure.
When using the RTL flow, after you have selected the Alveo Data Center accelerator card from the Boards tab, the following figures appear. The RTL-based project can now be created.

**Figure 4: Selecting Alveo Data Center Accelerator U200 Card in Vivado Design Suite**

**Figure 5: Alveo Data Center Accelerator U200 Card New Project Summary**
Creating an MCS File and Programming the Alveo Card

For custom RTL flow, this section outlines the procedures to do the following:

- Create an MCS file (PROM image)
- Flash programming through the USB-JTAG (Micro USB) interface

Create an MCS File (PROM Image)

The Alveo accelerator card contains a Quad SPI configuration flash memory part that can be configured over USB-JTAG. This part contains a protected region, with the factory base image at the 0x00000000 address space. This base image points to the customer programmable region at a 0x01002000 address space offset.

To ensure that the PROM image is successfully loaded onto the Alveo accelerator card at power on, the starting address must be set to 0x01002000 and the interface set to spix4 when creating the MCS file. Details on adding this to the MCS file can be found in the UltraScale Architecture Configuration User Guide (UG570).
In addition, the following code must be placed in the project XDC file to correctly configure the MCS file.

```bash
# Bitstream Configuration
set_property CONFIG_VOLTAGE 1.8 [current_design]
set_property BITSTREAM.CONFIG.CONFIGFALLBACK Enable [current_design]
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property CONFIG_MODE SPIx4 [current_design]
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 85.0 [current_design]
set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN disable [current_design]
set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN Pullup [current_design]
set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR Yes [current_design]
```

### Program the Alveo Card

After the MCS file is created, see the procedure in the "Programming the FPGA Device" chapter in the *Vivado Design Suite User Guide: Programming and Debugging* (UG908) to connect to the Alveo Data Center accelerator card using the hardware manager.

1. Select **Add Configuration Device** and select the mt25qu01g-spi-x1_x2_x4 part.
2. Right-click the target to select **Program the Configuration Memory Device**.
   a. Select the MCS file target.
   b. Select **Configuration File Only**.
   c. Click **OK**.
3. After programming has completed, disconnect the card in the hardware manager, and disconnect the USB cable from the Alveo accelerator card.
4. Perform a cold reboot on the host machine to complete the card update.
Electrostatic Discharge Caution

CAUTION! ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.

To prevent ESD damage:

- Use an ESD wrist or ankle strap and ensure that it makes skin contact. Connect the equipment end of the strap to an unpainted metal surface on the chassis.
- Avoid touching the adapter against your clothing. The wrist strap protects components from ESD on the body only.
- Handle the adapter by its bracket or edges only. Avoid touching the printed circuit board or the connectors.
- Put the adapter down only on an antistatic surface such as the bag supplied in your kit.
- If you are returning the adapter to Xilinx Product Support, place it back in its antistatic bag immediately.

Installing Alveo Data Center Accelerator Cards in Server Chassis

Because each server or PC vendor's hardware is different, for physical board installation guidance, see the manufacturer's PCI Express® board installation instructions.

For programming and start-up details, see Getting Started with Alveo Data Center Accelerator Cards (UG1301).
FPGA Configuration

The Alveo U200/U250 accelerator card supports two UltraScale+™ FPGA configuration modes:

- Quad SPI flash memory
- JTAG using USB JTAG configuration port (USB J13/FT4232H U27)

The FPGA bank 0 mode pins are hardwired to $M[2:0] = 001$ master SPI mode with pull-up/down resistors.

At power up, the FPGA is configured by the Quad SPI NOR flash device (Micron MT25QU01GBBA8E12-0SIT) with the FPGA_CCLK operating at clock rate of 105 MHz (EMCCLK) using the master serial configuration mode. The Quad SPI flash memory NOR device has a capacity of 1 Gb.

If the JTAG cable is plugged in, QSPI configuration might not occur. JTAG mode is always available independent of the mode pin settings.

For complete details on configuring the FPGA, see the *UltraScale Architecture Configuration User Guide (UG570)*.

**Table 2: Configuration Modes**

<table>
<thead>
<tr>
<th>Configuration Mode</th>
<th>M[2:0]</th>
<th>Bus Width</th>
<th>CCLK Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Master SPI</td>
<td>001</td>
<td>x1, x2, x4</td>
<td>FPGA output</td>
</tr>
<tr>
<td>JTAG</td>
<td>Not applicable</td>
<td>x1</td>
<td>Not applicable</td>
</tr>
</tbody>
</table>
Card Component Description

This chapter provides a functional description of the components of the Alveo™ U200/U250 Data Center accelerator card.

**UltraScale+ FPGA**

The Alveo U200 accelerator card is populated with the Virtex® UltraScale+™ XCU200-L2FSGD2104E FPGA.

The Alveo U250 accelerator card is populated with the Virtex UltraScale+ XCU250-L2FIGD2104E FPGA.

For more information about Virtex® UltraScale+™ FPGAs, see the Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics (DS923).

**DDR4 DIMM Memory**

Four independent dual-rank DDR4 interfaces are available. The card is populated with four socketed single-rank Micron MTA18ASF2G72PZ-2G3B1IG 16GB DDR4 RDIMMs. Each DDR4 DIMM is 72 bits wide (64-bits plus support for ECC).

The detailed FPGA and DIMM pin connections for the feature described in this section are documented in the Alveo U200/U250 accelerator card XDC file.

For more details about the Micron DDR4 DIMM, see the Micron MTA18ASF2G72PZ-2G3B1IG data sheet at the Micron website: [http://www.micron.com](http://www.micron.com).

**Quad SPI Flash Memory**

The Quad SPI device provides 1 Gb of nonvolatile storage.

- Part number: MT25QU01GBBB8E12-0SIT (Micron)
• Supply voltage: 1.8V
• Datapath width: 4 bits
• Data rate: variable

For more flash memory details, see the Micron MT25QU01GBBB8E12-0SIT data sheet at the Micron website.

For configuration details, see the UltraScale Architecture Configuration User Guide (UG570). The detailed FPGA and Flash pin connections for the feature described in this section are documented in the Alveo U200/U250 accelerator card XDC file, referenced in Appendix A: Xilinx Design Constraints (XDC) File.

# USB JTAG Interface

The Alveo accelerator card provides access to the FPGA device via the JTAG interface.

FPGA configuration is available through the Vivado® hardware manager, which accesses the on-board USB-to-JTAG FT4232HQ bridge device. The micro-AB USB connector on the Alveo U200/U250 accelerator card PCIe® panel/bracket provides external device programming access.

**Note:** JTAG configuration is allowed at any time regardless of the FPGA mode pin settings consistent with the UltraScale Architecture Configuration User Guide (UG570).

For more details about the FT4232HQ device, see the FTDI website: [https://www.ftdichip.com/](https://www.ftdichip.com/).

# FT4232HQ USB-UART Interface

The FT4232HQ Quad USB-UART provides a UART connection through the micro-AB USB connector. The FPGA UART TX/RX (two-wire) connection is made through the FT4232HQ BD port. Channel BD implements a 2-wire level-shifted TX/RX UART connection to the FPGA. The FTDI FT4232HQ data sheet is available on the FTDI website: [https://www.ftdichip.com/](https://www.ftdichip.com/).

# PCI Express Endpoint

The Alveo U200/U250 accelerator card implements a 16-lane PCI Express® edge connector that performs data transfers at the rate of 2.5 giga-transfers per second (GT/s) for Gen1, 5.0 GT/s for Gen2, and 8.0 GT/s for Gen3 applications. The -2 speed grade FPGA included with the cards supports up to Gen3 x16.
QSFP28 Module Connectors

The Alveo accelerator cards host two 4-lane small form-factor pluggable (QSFP) connectors that accept an array of optical modules. Each connector is housed within a single QSFP cage assembly.

The QSFP+ connectors are accessible via the I2C interface on the Alveo U200/U250 accelerator cards. The QSFP connector’s sideband signals are accessible directly from the FPGA. The MODSELL, RESETL, MODPRSL, INTL, and LPMODE sideband signals are defined in the small form factor (SFF) specifications listed below. The components visible through the card PCIe panel/bracket top to bottom are:

- Triple status LEDs
- QSFP0
- QSFP1
- USB

For additional information about the quad SFF pluggable (28 Gb/s QSFP+) module, see the SFF-8663 and SFF-8679 specifications for the 28 Gb/s QSFP+ at the SNIA Technology Affiliates website: https://www.snia.org/sff/specifications2.

Each QSFP connector has its own clock generator.

- QSFP0 clock
  - Clock generator: Silicon Labs SI5335A-B06201-GM
  - Output CLK1A/1B: the QSFP0_CLOCK_P/N clock is an AC-coupled LVDS 156.25 MHz clock wired to the QSFP0 GTY interface

- QSFP1 clock
  - Clock generator: Silicon Labs SI5335A-B06201-GM
  - Output CLK1A/1B: the QSFP1_CLOCK_P/N clock is an AC-coupled LVDS 156.25 MHz clock wired to the QSFP1 GTY interface

The detailed FPGA and QSFP pin connections for the feature described in this section are documented in the Appendix A: Xilinx Design Constraints (XDC) File.

I2C Bus

The Alveo U200/U250 accelerator cards implement an I2C bus network (the device tree details are available in the board support package).
Status LEDs

The Alveo card is designed to operate with the passive heat sink enclosure cover installed so the DS1 and DS2 LEDs are not visible. Status light emitting diodes (LEDs) DS3, DS4, and DS5 are visible through a cutout in the PCIe end bracket. The following table defines the card status LEDs.

Table 3: Card Status LEDs

<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DS1</td>
<td>RED: POWER_GOOD</td>
</tr>
<tr>
<td>DS2</td>
<td>BLUE: DONE_0</td>
</tr>
<tr>
<td>DS3</td>
<td>ORANGE: STATUS_LED0</td>
</tr>
<tr>
<td>DS4</td>
<td>YELLOW: STATUS_LED1</td>
</tr>
<tr>
<td>DS5</td>
<td>GREEN: STATUS_LED2</td>
</tr>
</tbody>
</table>

Card Power System

Limited power system telemetry is available through the I2C IP. I2C IP is instantiated during the FPGA design process which begins after the Alveo Data Center accelerator card is selected from the Vivado Design Suite Boards tab. Refer to Design Flows for more information.
Xilinx Design Constraints (XDC) File

RTL users can reference the Vivado Design Suite User Guide: Using Constraints (UG903) for more information. The Alveo accelerator card XDC files are available for download from their respective websites along with this user guide.
Regulatory and Compliance Information

This product is designed and tested to conform to the European Union directives and standards described in this section.

CE Directives

2014/35/EC, Low Voltage Directive (LVD)
2014/30/EC, Electromagnetic Compatibility (EMC) Directive

CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

Electromagnetic Compatibility


This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

Safety

Compliance Markings

In August of 2005, the European Union (EU) implemented the EU Waste Electrical and Electronic Equipment (WEEE) Directive 2002/96/EC and later the WEEE Recast Directive 2012/19/EU. These directives require Producers of electronic and electrical equipment (EEE) to manage and finance the collection, reuse, recycling and to appropriately treat WEEE that the Producer places on the EU market after August 13, 2005. The goal of this directive is to minimize the volume of electrical and electronic waste disposal and to encourage re-use and recycling at the end of life.

Xilinx has met its national obligations to the EU WEEE Directive by registering in those countries to which Xilinx is an importer. Xilinx has also elected to join WEEE Compliance Schemes in some countries to help manage customer returns at end-of-life.

If you have purchased Xilinx-branded electrical or electronic products in the EU and are intending to discard these products at the end of their useful life, please do not dispose of them with your other household or municipal waste. Xilinx has labeled its branded electronic products with the WEEE Symbol to alert our customers that products bearing this label should not be disposed of in a landfill or with municipal or household waste in the EU.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

Appendix C

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select Help → Documentation and Tutorials.
- On Windows, select Start → All Programs → Xilinx Design Tools → DocNav.
- At the Linux command prompt, enter docnav.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the Design Hubs View tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

These documents provide supplemental material useful with this guide:
Product Websites

The most up-to-date information related to the Alveo™ U200/U250 card and documentation is available on the following websites:

1. Alveo U200 Data Center Accelerator Card
2. Alveo U250 Data Center Accelerator Card
3. Alveo Data Center Accelerator Card - Known Issues and General Information (AR 71752)

Supplemental Documents

The following Xilinx document provide supplemental material useful with this guide.

- UltraFast Design Methodology Guide for the Vivado Design Suite (UG949)
- Getting Started with Alveo Data Center Accelerator Cards (UG1301)
- Alveo U50 Data Center Accelerator Card Installation Guide (UG1370)
- Alveo Programming Cable User Guide (UG1377)
- UltraScale Architecture Configuration User Guide (UG570)
- Vivado Design Suite User Guide: Programming and Debugging (UG908)
- Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics (DS923)
- UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide (PG150)
- UltraScale Architecture PCB Design User Guide (UG583)

Additional Links

The following links provide supplemental material useful with this guide.

- Xilinx, Inc: https://www.xilinx.com
- Micron Technology: http://www.micron.com
  (MTA18ASF2G72PZ-2G3B11G, MT25QU01GBB8E12-0SIT)
  (FT4232HQ)
- SFP-DD module: SFP-DD Specification
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