Kintex-7 FPGA Connectivity Kit (Vivado Design Suite 2013.1)

Getting Started Guide

UG929 (v3.0) April 17, 2013

This document applies to the following software versions: Vivado Design Suite 2013.1 and 2013.2

XILINX®

XPM0402915-03

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/26/2012	1.0	Initial Xilinx release.
08/23/2012	1.1	Updated Figure 7, Figure 16, Figure 17, Figure 19, Figure 20, Figure 22, and Figure 24 with v1.1 screen captures. Changed ISE Design Suite Logic Edition Tools "v14.1" to "v14.1 or later" under Hardware Test Setup Requirements. Clarified step 3 through step 6 under Hardware Demonstration Setup. Clarified step 2 through step 4 and step 8 under Installing the Device Drivers. Added Next Steps.
01/07/2013	2.0	Replaced reference to USB stick with link to design files (under Hardware Test Setup Requirements and Installing the Device Drivers). Added Note preceding Hardware Demonstration Setup. Replaced reference to ISE Design Suite user guide with references to Vivado Design Suite user guides in Appendix A, Additional Resources.
04/17/13	3.0	Updated title page for Vivado Design Suite 2013.1. Changed "32-bit" to "32-bit and 64-bit" in last paragraph under Introduction. Added Notes 2 and 3 following Figure 1. Updated "UG477" to "PG054", "UG773" to "PG072", and "UG692" to "PG068" user guide references throughout document.

Table of Contents

Getting Started with the Kintex-7 FPGA Connectivity Kit

The Kintex™-7 FPGA Connectivity Kit provides a comprehensive, high-performance development and demonstration platform using the Kintex-7 FPGA family for high-bandwidth and high-performance applications in multiple market segments. The kit enables designing with DDR3, I/O expansion through FMC, and common serial standards, such as PCI Express® and 10GBASE-R through the FMC interface.

This Getting Started Guide is divided into two sections:

- Hardware Setup and Testing with the KC705 Built-in Self Test

  This section on the built in self test (BIST) familiarizes users with the KC705 board, the various switch positions, the sequence to program the FPGA, and provides a sanity check on the board's hardware components.

- Connectivity System Setup with the Targeted Reference Design

  This section provides the steps required to setup the connectivity TRD hardware, program the FPGA, load the application driver, and become familiar with the GUI.

Hardware Setup and Testing with the KC705 Built-in Self Test

The built-in self-test (BIST) tests many of the features offered by the Kintex-7 FPGA KC705 evaluation kit. The test is stored in the nonvolatile BPI Linear Flash memory, and configures the FPGA when the mode and upper flash address pins on the board are set for Master BPI.

Figure 1 provides an overview of the board features used by the BIST.

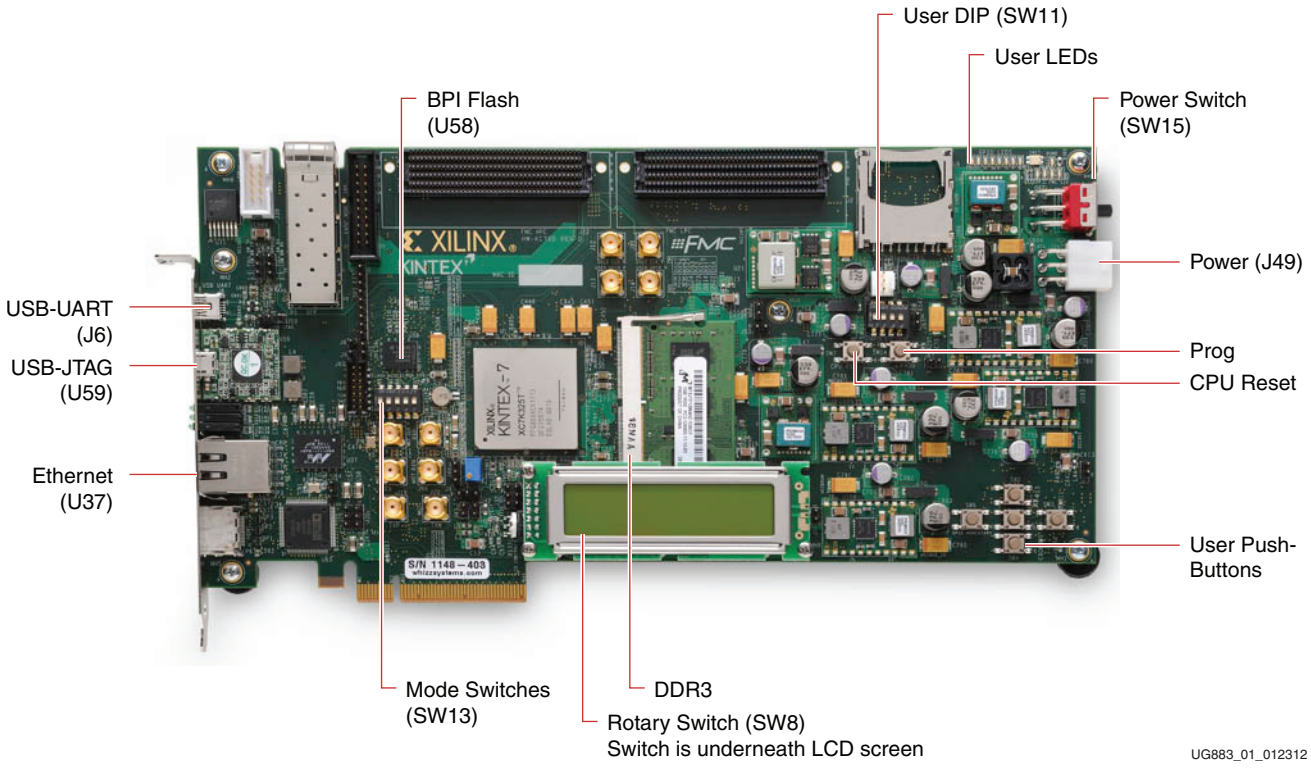

Figure 1: **KC705 Board Features**

Note: For a diagram of all the features on the KC705, see UG810, *KC705 Evaluation Board for the Kintex-7 FPGA User Guide* [Ref 8].

Hardware Test Setup Requirements

The prerequisites for testing the design in hardware are:

- KC705 Evaluation board with the Kintex-7 FPGA XC7K325T-2FFG900C device
- USB-to-Mini-B cable (for UART)
- AC power adapter (12 VDC)
- Tera Term Pro terminal program [Ref 21]

  Note: The Tera Term Pro program is used for illustrative purposes. Other programs can be used.
- USB-UART drivers from SiLabs [Ref 22]

Hardware Test Board Setup Requirements

This section details the hardware setup and use of the terminal program for running the BIST application. It contains step-by-step instructions for board bring-up.

KC705 Evaluation Board Setup

1. Set the jumpers and switches on the KC705 board as follows:
   - The mode switches (SW13) are set for Master BPI mode 010.
   - The upper flash address switches (SW13) are set to 11.
2. Verify the switch and jumper settings are set as shown in Table 1 and Figure 2.

Note: For this application, the board should be set up as a stand-alone system, with power coming from the cord and brick that comes with the KC705 evaluation kit.

Table 1: **Switch and Jumper Settings**

Switch	Setting	
SW15	Board Power slide-switch	
	..	Off
SW11	User GPIO DIP switch	
	4	Off
	3	Off
	2	Off
	1	Off
SW13	Configuration Mode switch	
	5	Off
	4	On
	3	Off
	2	On
	1	On

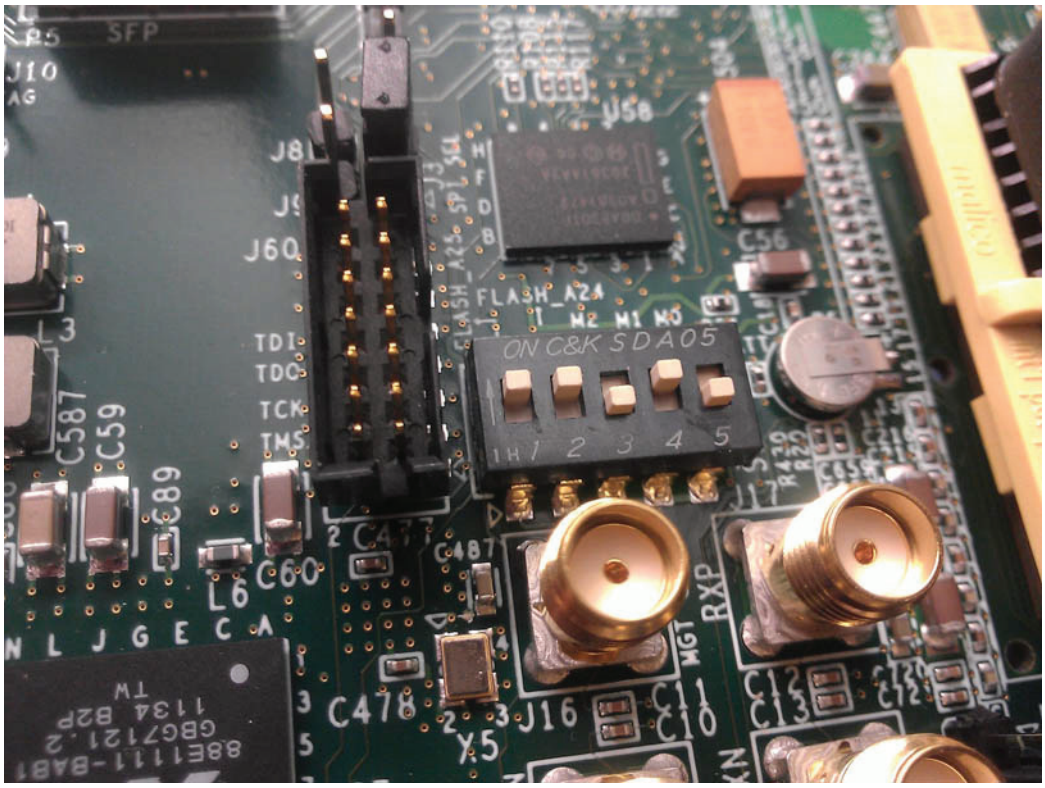

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Figure 2: **BIST Switch and Jumper Settings**

Hardware Bring-Up

This section details the steps for hardware bring-up:

1. With the board switched off, plug a USB-to-Mini-B cable into the UART port of the KC705 board and the PC (see Figure 3).
2. Install the power cable.
3. Switch the KC705 board power to ON.

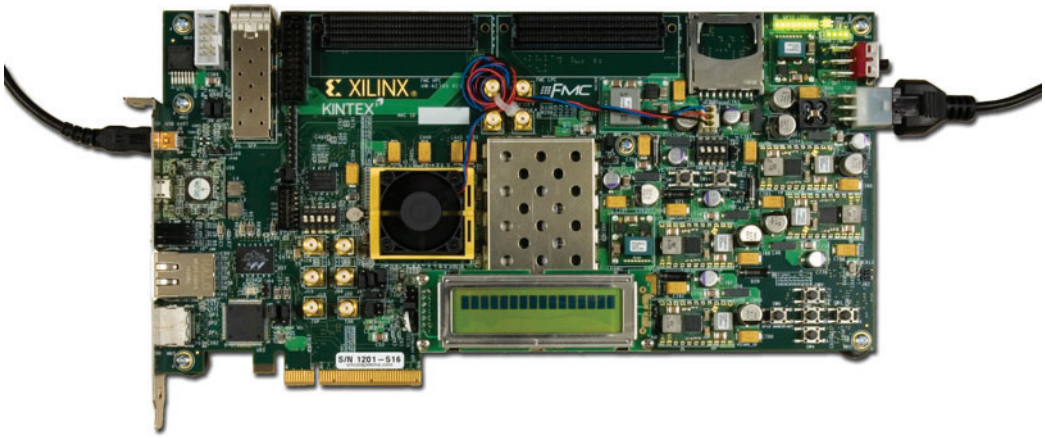

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Figure 3: **KC705 with the UART and Power Cable Attached**

Install the UART Driver

1. Run the downloaded executable UART-USB driver file listed in Hardware Test Setup Requirements, page 8. This enables UART-USB communications with a host PC (see Figure 4).

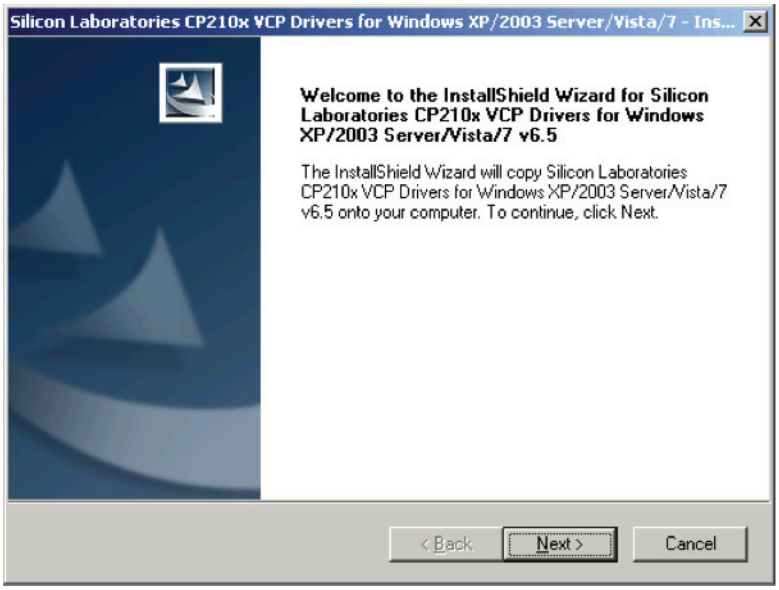

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Figure 4: **UART Cable Driver Installation**

2. Set the USB-UART connection to a known port in the Device Manager as follows:
   - Right-click **`My Computer`** and select **`Properties`**.
   - Select the **`Hardware`** tab, then click the **`Device Manager`** button.
   - Find and right-click the Silicon Labs device in the list. Then select **`Properties`**.
   - Click the **`Port Settings`** tab and the **`Advanced...`** button.
   - Select an open COM port between COM1 and COM4.

Figure 5 shows the steps needed to set the USB-UART port.

Note: Steps and diagrams refer to use with a Windows host PC with the Windows XP or Windows 7 operating system.

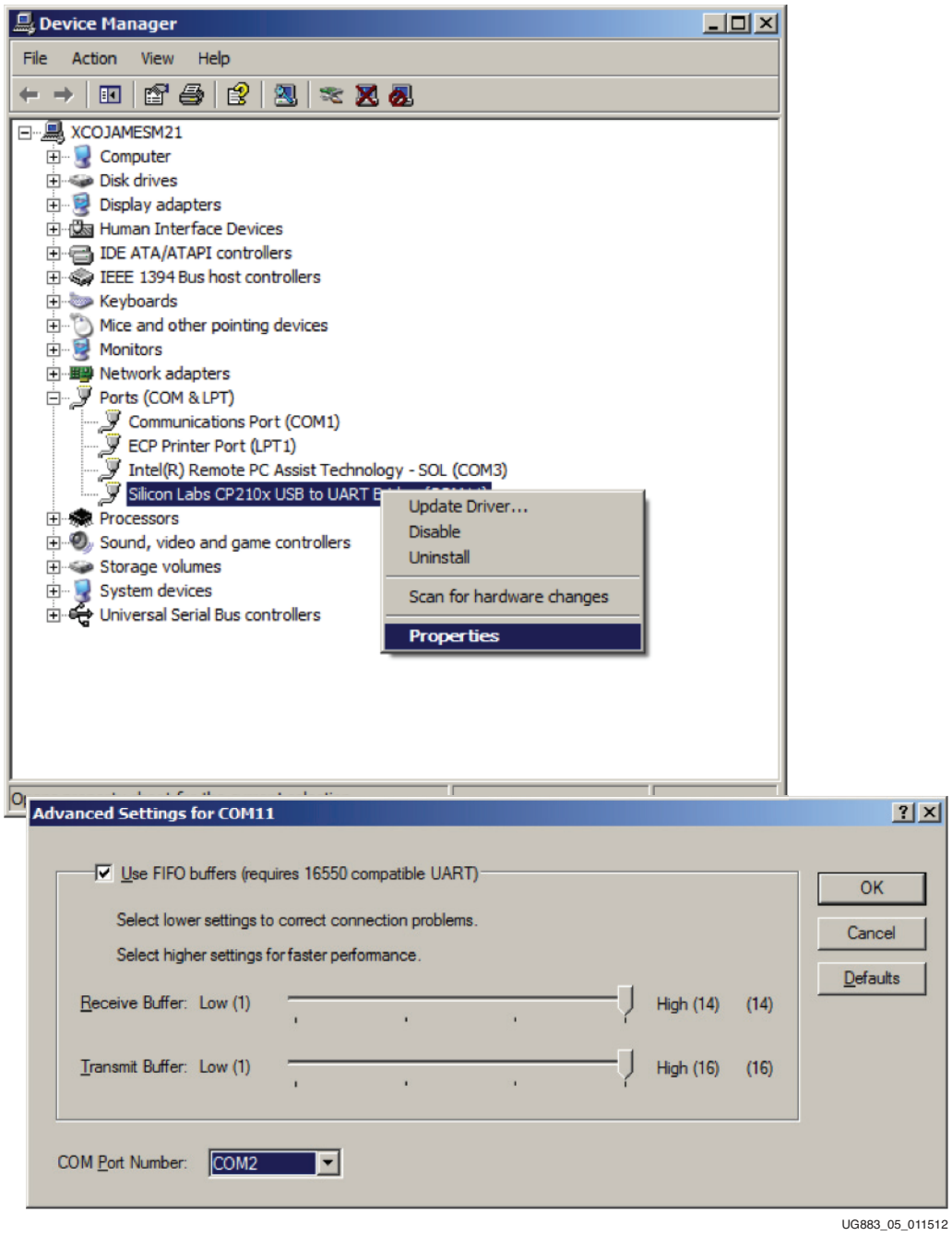

Figure 5: **Port Selection on the Device Manager Screen**

Run the BIST Application

1. Start the installed terminal program.
2. Press PROG (SW14) on the KC705 board, and view the BIST output on the terminal window (see Figure 6).

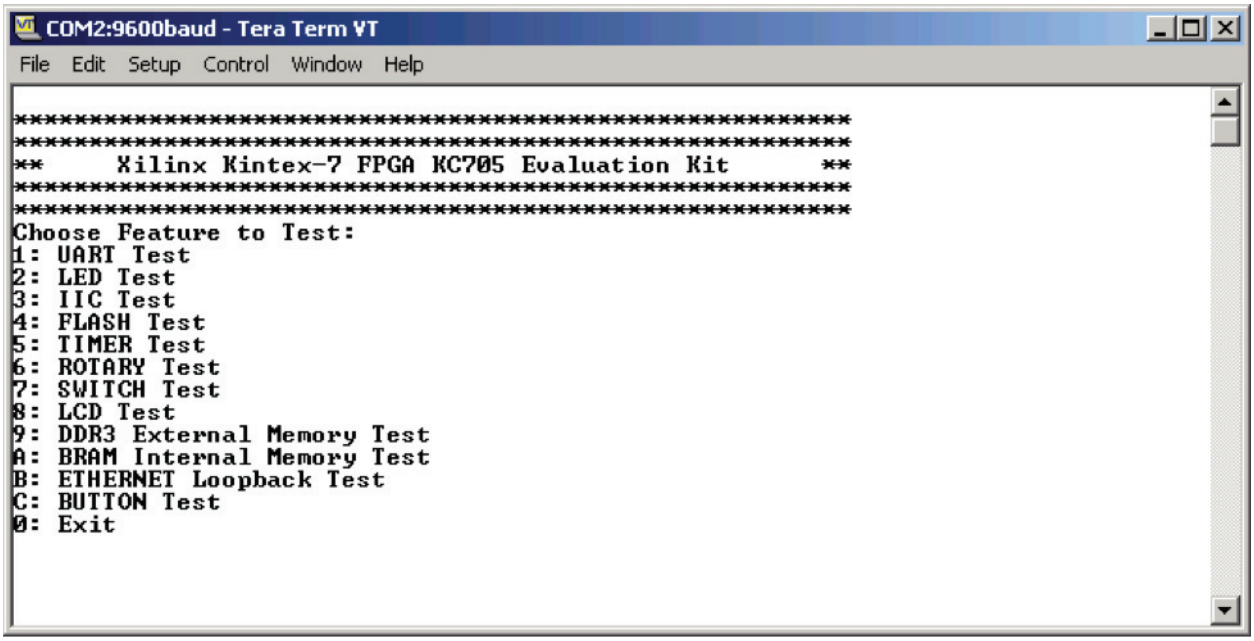

Figure 6: **BIST Main Menu**

3. Select the relevant tests to run, and observe the results.

For more information on the BIST software and additional tutorials, including how to restore the default content of the onboard nonvolatile storage, see the KC705 board information references [Ref 20].

Connectivity System Setup with the Targeted Reference Design

Introduction

Figure 7 depicts the block level overview of the Kintex-7 Connectivity Targeted Reference Design (TRD) which delivers up to 20 Gb/s of performance per direction.

The design is a dual Network Interface Card (NIC) with an x8 GEN2 PCIe endpoint, a multi-channel packet DMA from Northwest Logic, DDR3 memory for buffering, 10G Ethernet MAC and 10GBASE-R standard compatible physical layer interface. The PCIe-DMA together is responsible for movement of data between a PC system and FPGA (S2C implies data movement from PC system to FPGA and C2S implies data movement from FPGA to PC system).

DDR3 SDRAM (64-bit, 1,600 Mb/s or 800 MHz) is used for packet buffering – a virtual FIFO layer facilitates the use of DDR3 as multiple FIFOs. The virtual FIFO layer is built using the AXI Stream interconnect and AXI Virtual FIFO controller CoreGEN IPs.

Dual NIC application is built over this by use of Ten Gigabit Ethernet MAC and Ten Gigabit PCS/PMA (10GBASE-R PHY) IPs. The 10G MAC connects to the 10G BASE-R PHY over 64-bit, SDR XGMII parallel interface. Additionally, the design provides power monitoring capability based on a PicoBlaze™ engine.

For software, the design provides 32-bit and 64-bit Linux drivers for all modes of operation listed below and a graphical user interface (GUI) which controls the tests and monitors the status.

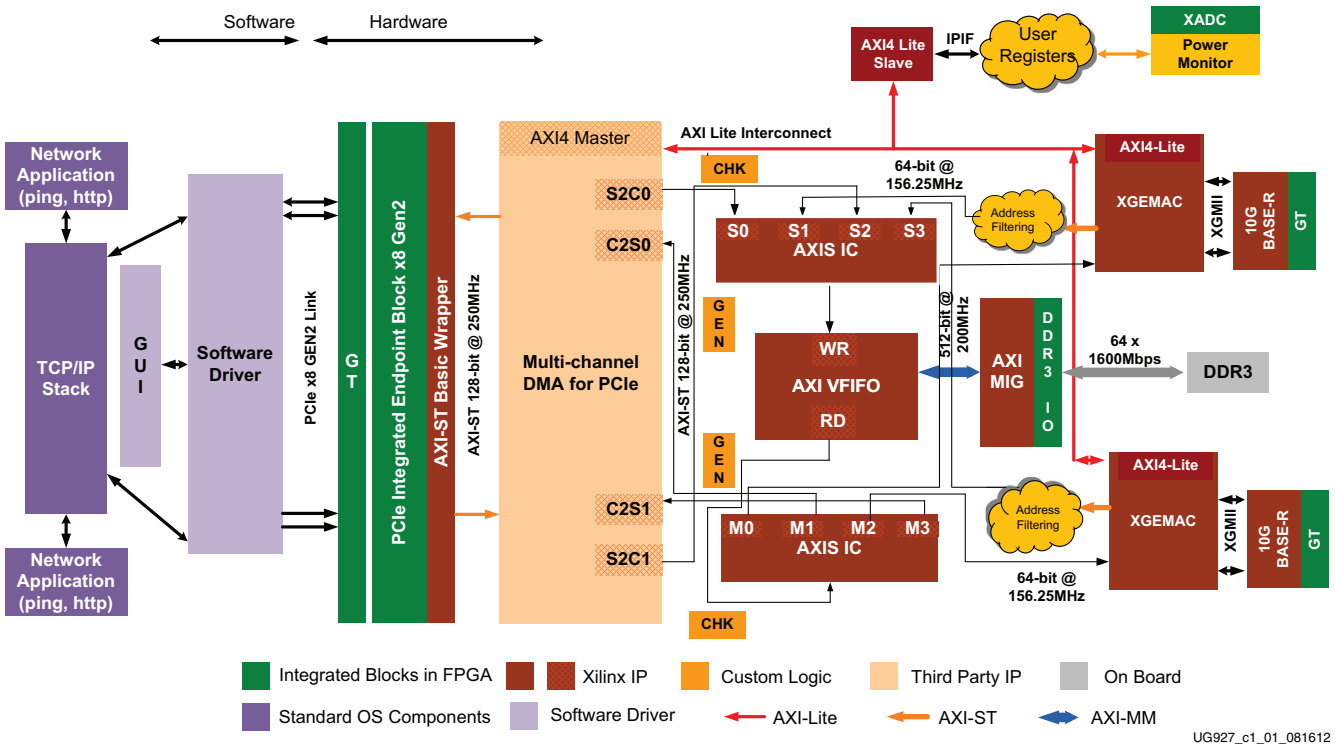

Figure 7: **Kintex-7 Connectivity TRD Block Diagram**

Notes:

1. The arrows in Figure 7 indicate AXI interface directions from master to slave. They do not indicate data flow directions.
2. The DMA netlist shipped along with this core is an evaluation netlist. For full version netlist, contact Northwest Logic [Ref 23].
3. The DMA used in the TRD is configured for x8Gen2 PCIe interface. For other supported configurations, contact Northwest Logic [Ref 23].

Features

The Kintex-7 FPGA Connectivity Targeted Reference Design features these components:

- PCI Express v2.1 compliant GEN2 x8 Endpoint operating at 5 Gb/s per lane per direction
  - PCIe transaction interface utilization engine
  - MSI and legacy interrupt support
- Bus mastering scatter-gather DMA to offload processor

- Multi-channel DMA
- AXI4 streaming interface for data
- AXI4 interface for register space access
- DMA performance engine
- Full duplex operation
  - Independent transmit and receive channels
- 10 Gigabit Ethernet MAC with 10G BASE-R PHY
  - Address filtering
  - Inter-frame gap control
  - Jumbo frame support up to 16,383 bytes in size
  - Ethernet statistics engine
  - Management interface for configuration (MDIO)
- PicoBlaze based PVT monitoring
  - Engine in hardware to monitor power by reading TI's UCD9248 power controller chip on-board KC705
  - Engine in hardware to monitor die temperature via Xilinx analog-to-digital converter
- Application demand driven power management
  - Option to change PCIe link width and link speed for reduced power consumption in lean traffic scenario

Hardware Test Setup Requirements

The prerequisites for testing the design in hardware are:

- KC705 evaluation board with XC7K325K-2-FFG900CES FPGA
- Design files
  - Design source files
  - Device driver files
  - Board design files
  - Documentation

  Design files are available at:

  http://www.xilinx.com/support/documentation/kintex-7_fpga_connectivity_kit.htm
- Vivado™ Design Suite Logic Edition Tools v2012.4 or later
- 4-pin to 6-16 12V PCIe adapter cable
- Micro USB cable
- FM-S14 FMC card with 4 SFP+ cages [Ref 25]
- Two 10G MMF SFP+ SR optical transceivers [Ref 26]
- LC to LC OM3 10G fiber optic patch cable [Ref 27]
- Fedora 16 LiveCD [Ref 24]
- PC with PCIe v2.0 slot. Recommended PCI Express Gen2 PC system motherboards are ASUS P5E (Intel X38), ASUS Rampage II Gene (Intel X58) and Intel DX58SO (Intel

X58). Note that the Intel X58 chipsets tend to show higher performance. This PC could also have Fedora Core 16 Linux OS installed on it. Note that the PC is not part of the Kintex-7 connectivity kit.

Note: This document refers to the initially released TRD version (v1_0). For subsequent releases, the design version will be upgraded but the change will not be reflected in this document.

Hardware Demonstration Setup

This section details the hardware setup and use of provided application and control GUI to help the user get started quickly with the hardware. It provides a step-by-step explanation on hardware bring-up, software bring-up, and use of the application GUI.

All procedures listed in the following sections require super user access on a Linux machine. When using Fedora 16 LiveCD provided with the kit, super user access is granted by default due to the way the kernel image is built; if LiveCD is not used contact the system administrator for super user access.

1. With the power supply turned off, ensure that switches P1 and P2 on the FM-S14 FMC card are in the ON position, as shown in Figure 8.

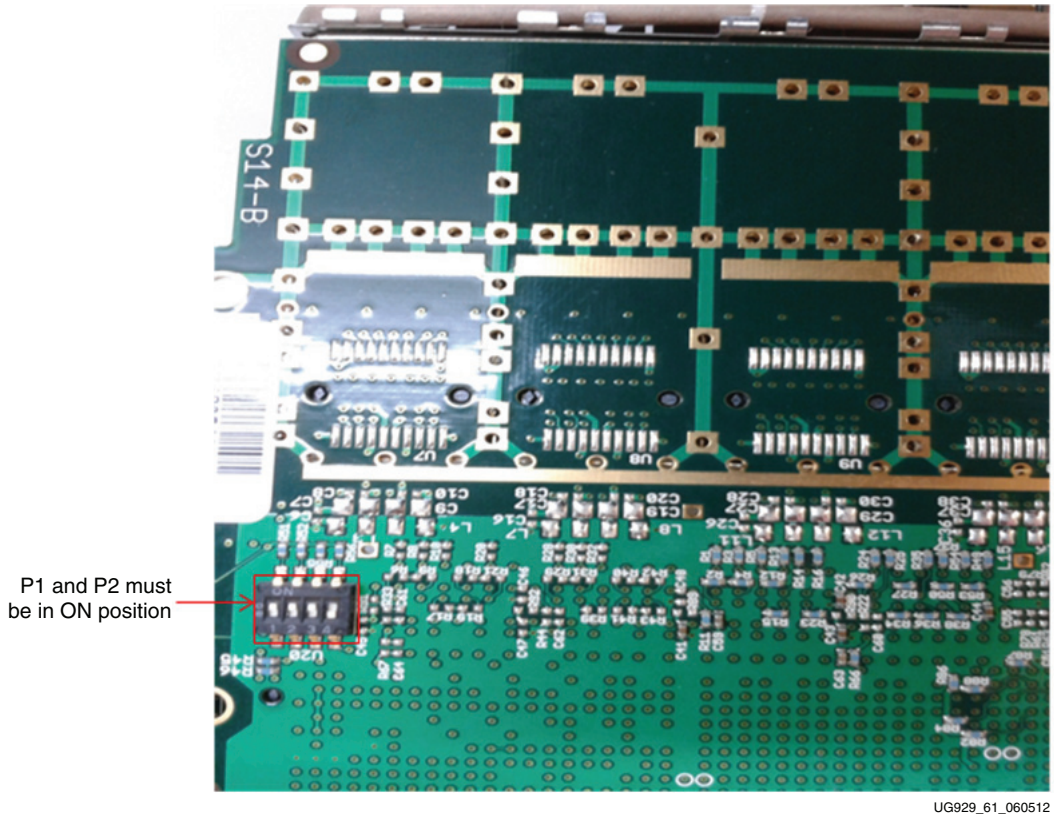

Figure 8: **DIP Switch Position on FMC Card**

2. Insert SFP+ connectors to channel 2 and channel 3 positions as shown in Figure 9.

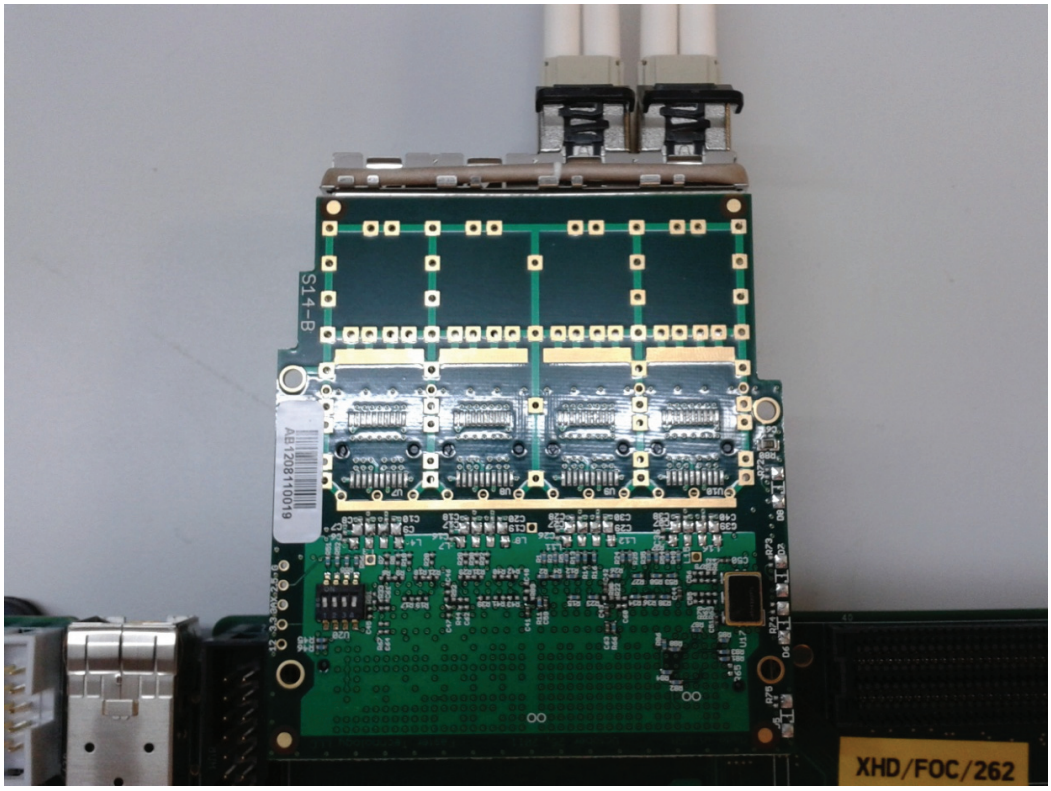

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Figure 9: **SFP+ Connector Position on FMC Card**

3. Insert the FM-S14 FMC card to the HPC slot of KC705 as shown in Figure 10. Remove the cap from the fiber optic cables and connect the fiber optic cables in a loopback fashion as shown in the figure.

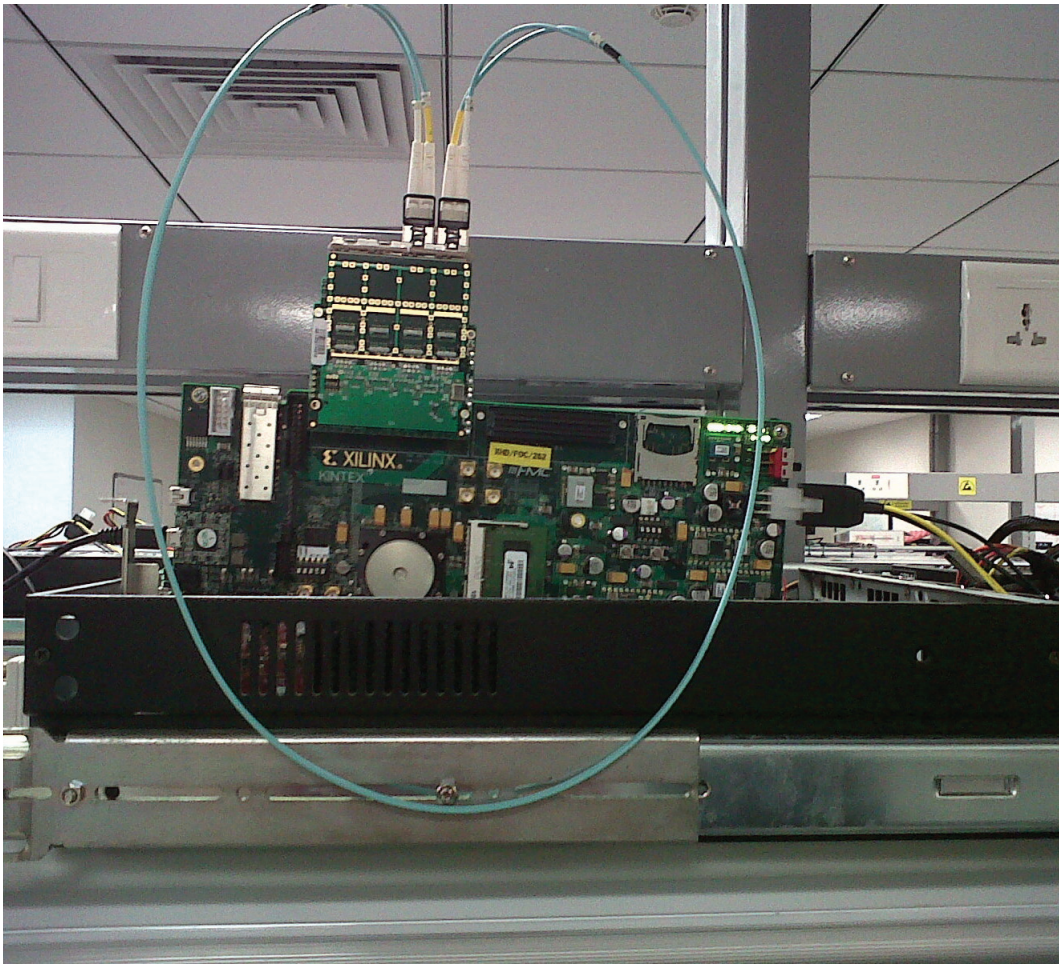

Figure 10: **Setup with Fiber Optic Cable**

4. Connect the 12V ATX power supply 4-pin disk drive type connector to the board. Note that the 6-pin ATX supply cannot be connected directly to the KC705 board and the 6-pin adapter is required.

   Caution! The 6-pin ATX supply cannot be connected directly to the KC705 board and the 6-pin adapter is required.

5. With the host system powered off, insert the KC705 board in the PCI Express® slot through the PCI Express x8 edge connector.
6. Ensure that the connections are secure so as to avoid loose contact problems. Power on the KC705 board and then the system.
7. The GPIO LEDs are located in the top right corner of the KC705 board. These LED indicators illuminate to provide the following status (LED positions are marked from left to right):

   LED position 1 – DDR3 link up

   LED position 2 – 10GBASE-R link 1 ready

LED position 3 – 10GBASE-R link 2 ready

LED position 4 – 156.25 MHz clock heart beat LED

LED position 5 – PCIe x8 link stable

LED position 6 – PCIe 250 MHz clock

LED position 7 – PCIe link up

LED positions on the KC705 board are shown in Figure 11.

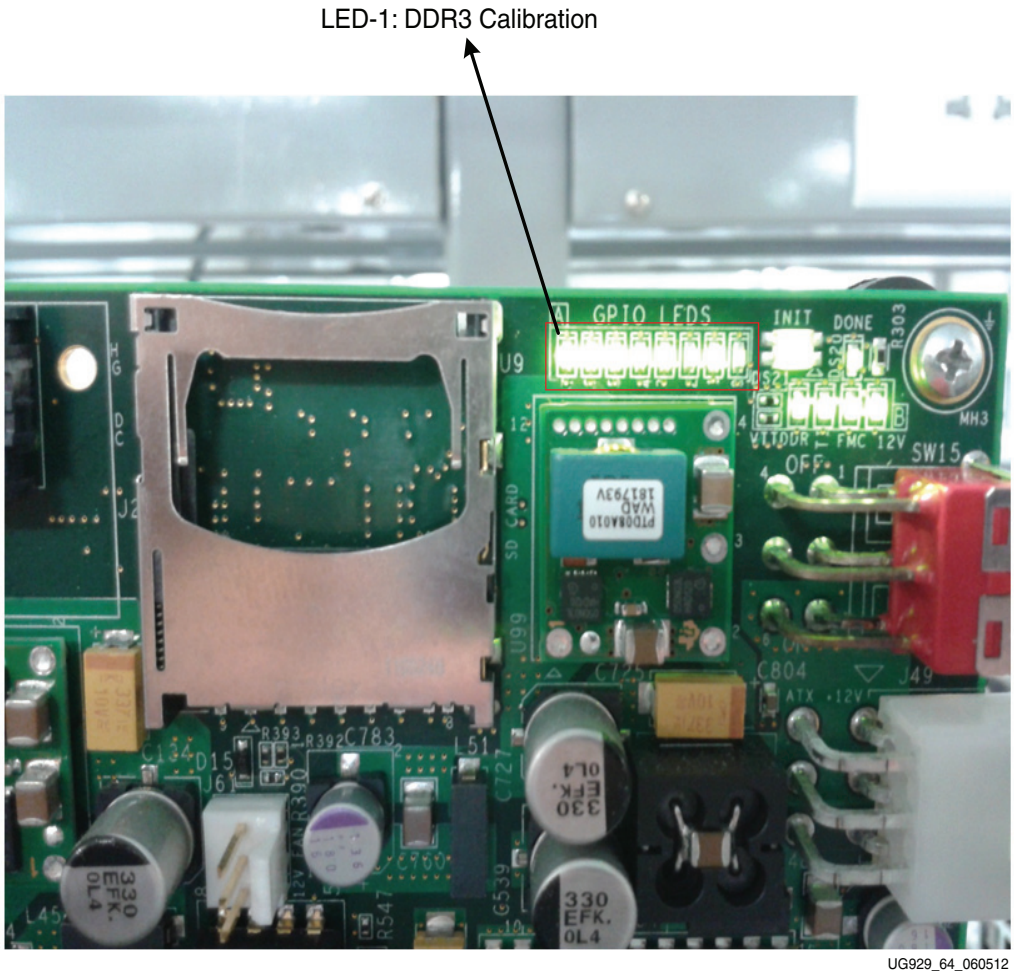

Figure 11: **LED Position on the FMC Card**

8. The LEDs on the FMC card (note that these are on the bottom side) indicate the following status:

   LED position top – FM-S14 is connected on the correct FMC connector on KC705 board

   LED position bottom – indicates clock generator on FMC is programmed to generate 312.5 MHz as required by the TRD

Installing the Device Drivers

This sections describes the steps to install the device drivers for the Kintex-7 Connectivity TRD after completion of the above hardware setup steps.

1. If Fedora 16 is installed on the PC system's hard disk, boot as a root-privileged user, proceed to step 3. Otherwise continue with step 2.
2. To boot from the Fedora 16 Live DVD provided in the kit, place the DVD in the PC's CD-ROM drive. The Fedora 16 Live Media is for Intel-compatible PCs. The DVD contains a complete, bootable 32-bit Fedora 16 environment with the proper packages installed for the TRD demonstration environment. The PC boots from the CD-ROM drive and logs into a liveuser account. This account has kernel development root privileges required to install and remove device driver modules.

   Note: Users might have to adjust BIOS boot order settings to enure that the CD-ROM drive is the first drive in the boot order. To enter the BIOS menu to set the boot order, press the DEL or F2 key when the system is powered on. Set the boot order and save the changes. (The DEL or F2 key is used by most PC systems to enter the BIOS setup. Some PCs might have a different way to enter the BIOS setup.)

   The PC should boot from the CD-ROM drive. The images in Figure 12 are seen on the monitor during boot up. (Booting from the Fedora 16 Live DVD takes few minutes and the user needs to wait for until the Fedora 16 menu pops up on the screen as shown in Figure 12.)

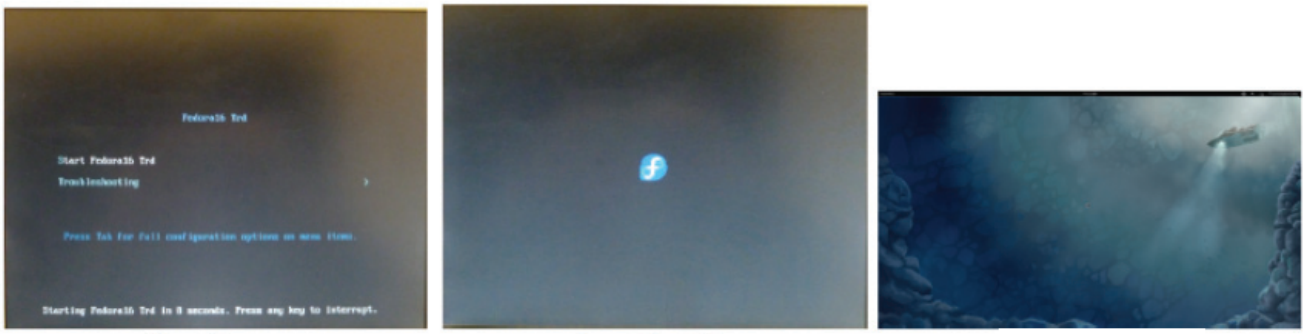

Figure 12: **Fedora 16 LiveCD Boot Sequence**

3. Copy the `k7_connectvity_trd_v1_0` folder to the home directory (or a folder of choice). Note that the user must be a root-privileged user. (Connectivity kit design files are available at http://www.xilinx.com/support/documentation/kintex-7_fpga_connectivity_kit.htm.)

   Double-click the copied `k7_connectivity_trd_v1_0` folder. The screen capture in Figure 13 shows the content of the `k7_connectivity_trd_v1_0` folder. The user needs to browse through the "Activities" tab after Fedora 16 boots up to access the "Home" directory.

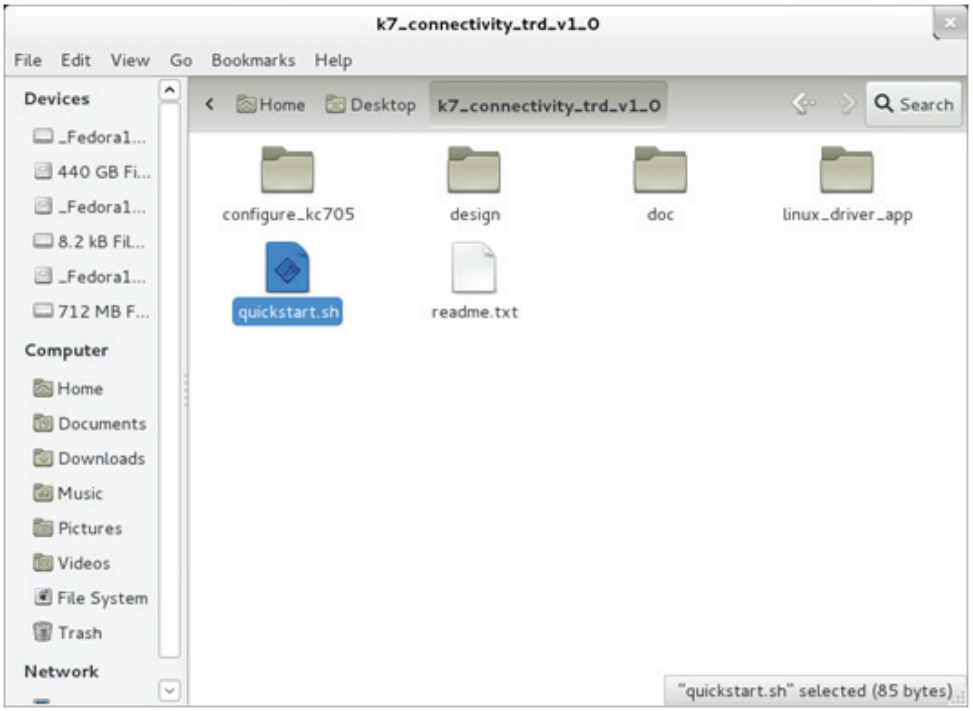

Figure 13: **Directory Structure of k7_connectivity_trd**

4. Ensure that the TRD package has the proper "execute" permission. Double click `quickstart.sh` script (see Figure 14). This script invokes the driver installation GUI. Click **Run in Terminal**.

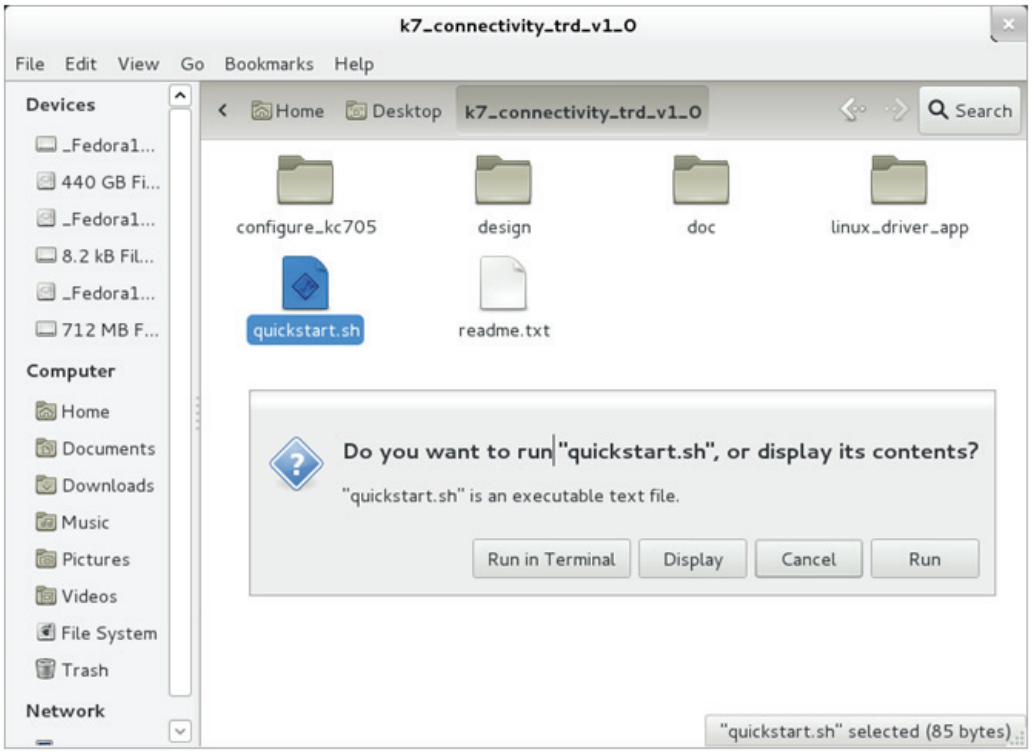

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Figure 14: **Running the Quickstart Script**

5. The GUI with driver installation option pops up as shown in Figure 15. The next steps demonstrate all modes of design operation by installing and un-installing various drivers.

   Select **GEN/CHK** performance mode driver mode as shown in Figure 15 and click **Install.**

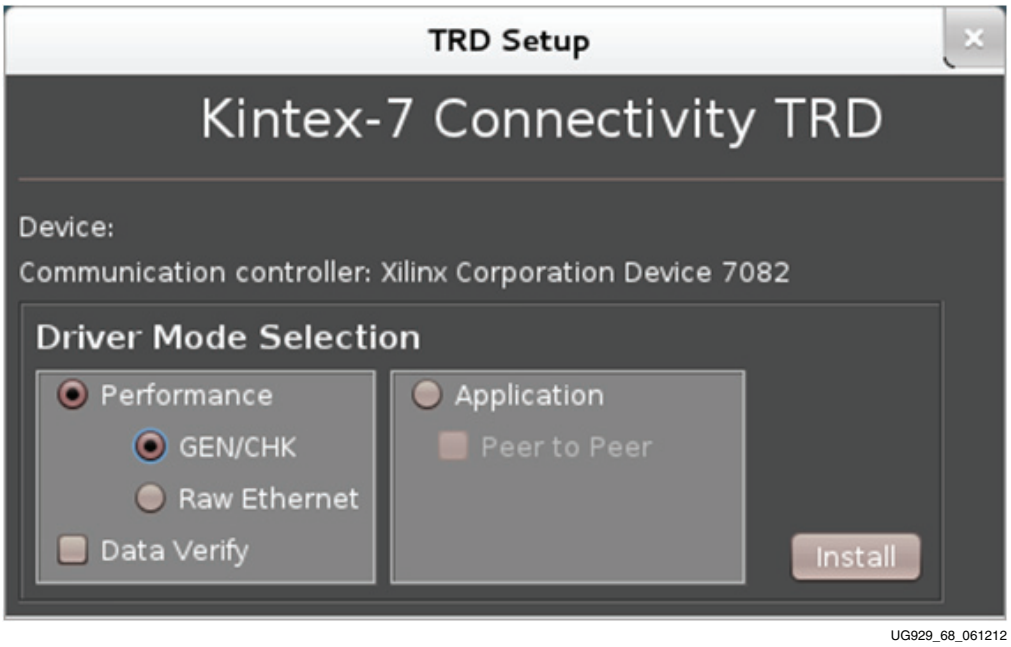

Figure 15: **Landing Page of Kintex-7 TRD**

6. After installing the GEN/CHK performance mode driver, the control and monitor user interface pops up as shown in Figure 16. The control pane shows control parameters such as test mode (loopback, generator, or checker) and packet length. The user can select PCIe link width and speed while running a test if the host machine supports link width and speed configuration capability. The System Monitor tab in the GUI also shows system power and temperature. DDR3 ready status and 10GBASE-R link status are displayed on the top left corner of the GUI.

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Figure 16: **GEN/CHK Performance Mode**

7. Click **Start** on both Data Path-0 and Data Path-1. Go to the Performance Plots tab. The Performance Plots tab shows the system-to-card and card-to-system performance numbers for a specific packet size. The user can vary packet size and see performance variation accordingly (see Figure 17).

Figure 17: **GEN/CHK Performance Mode Plots**

8. Close the GUI – a pop up message asks whether you want to un-install the drivers. Click on **Yes**. This process opens the landing page of the Kintex-7 Connectivity TRD. (Driver un-installation requires the GUI to be closed first.)
9. Select **Raw Ethernet** performance as shown in Figure 18. Click **Install**.

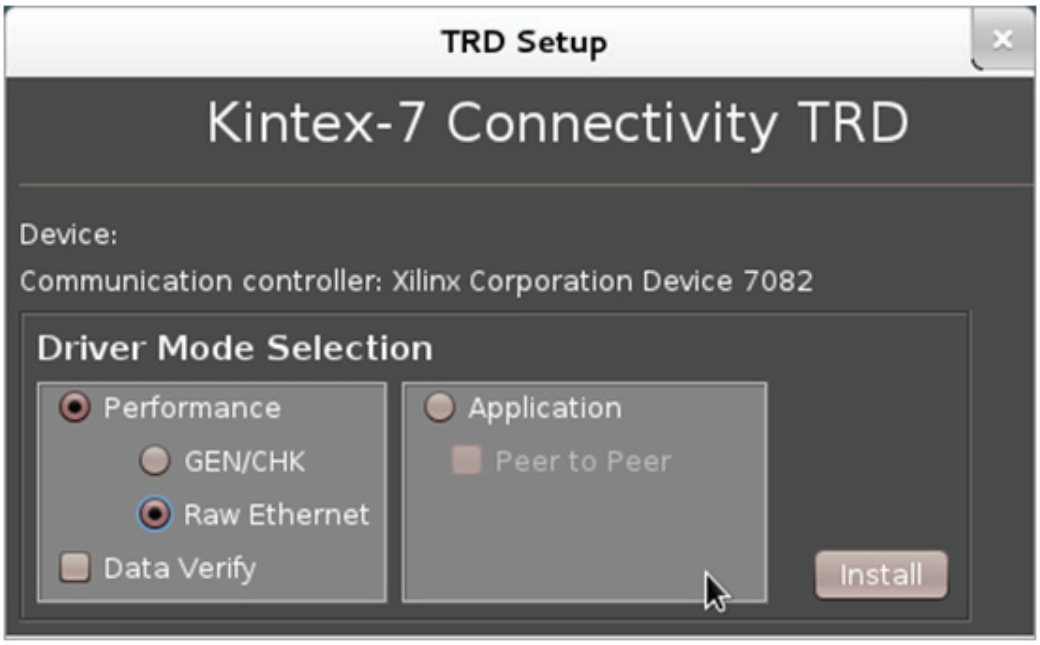

Figure 18: **Raw Ethernet Driver Installation**

10. The GUI for raw Ethernet mode driver is invoked. The user can configure packet size in raw Ethernet mode and can control PCIe link width and speed change if the host machine supports this. The System Monitor tab monitors system power and temperature (see Figure 19).

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Figure 19: **Raw Ethernet Driver GUI**

11. Click **Start** on both Data Path-0 and Data Path-1. Navigate to the Performance Plots tab to see performance on system-to-card and card-to-system (see Figure 20).

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Figure 20: **Raw Ethernet Driver Performance Plots**

12. Close the GUI – this un-installs driver and opens the Kintex-7 Connectivity TRD landing page. Note that driver un-installation requires the GUI to be closed first.
13. Select the Application mode driver as shown in Figure 21. For using peer-peer option refer to Appendix 8 of UG927, *Kintex-7 FPGA Connectivity TRD User Guide* [Ref 1]. Click **Install**.

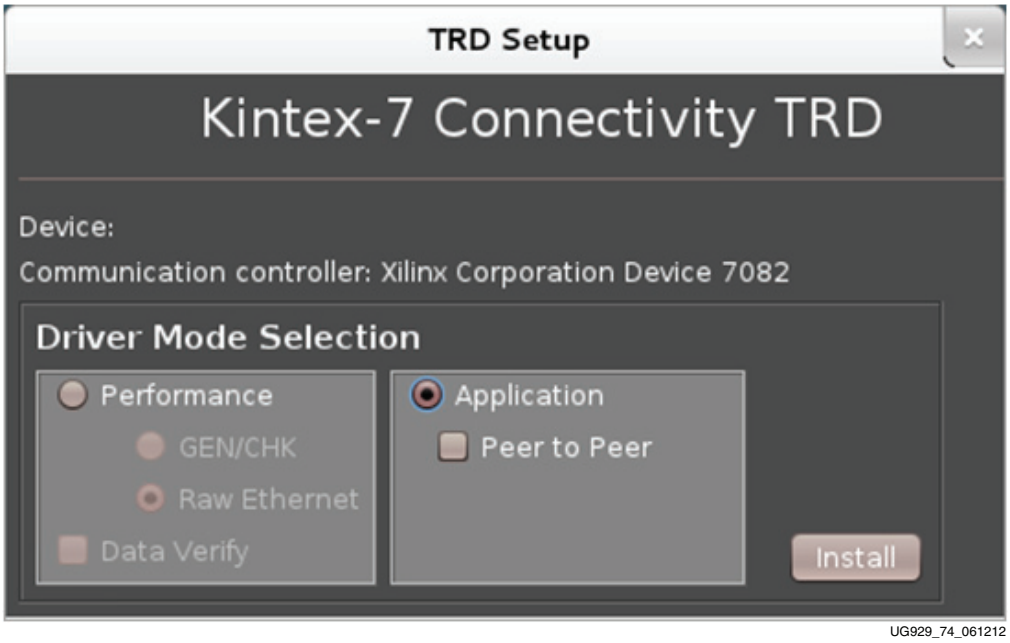

Figure 21: **Application Mode Driver Installation**

14. The GUI is invoked after the driver is installed. However, in application mode, the user cannot start or stop a test – the traffic is generated by the networking stack. The system monitor shows the system power and temperature (see Figure 22).

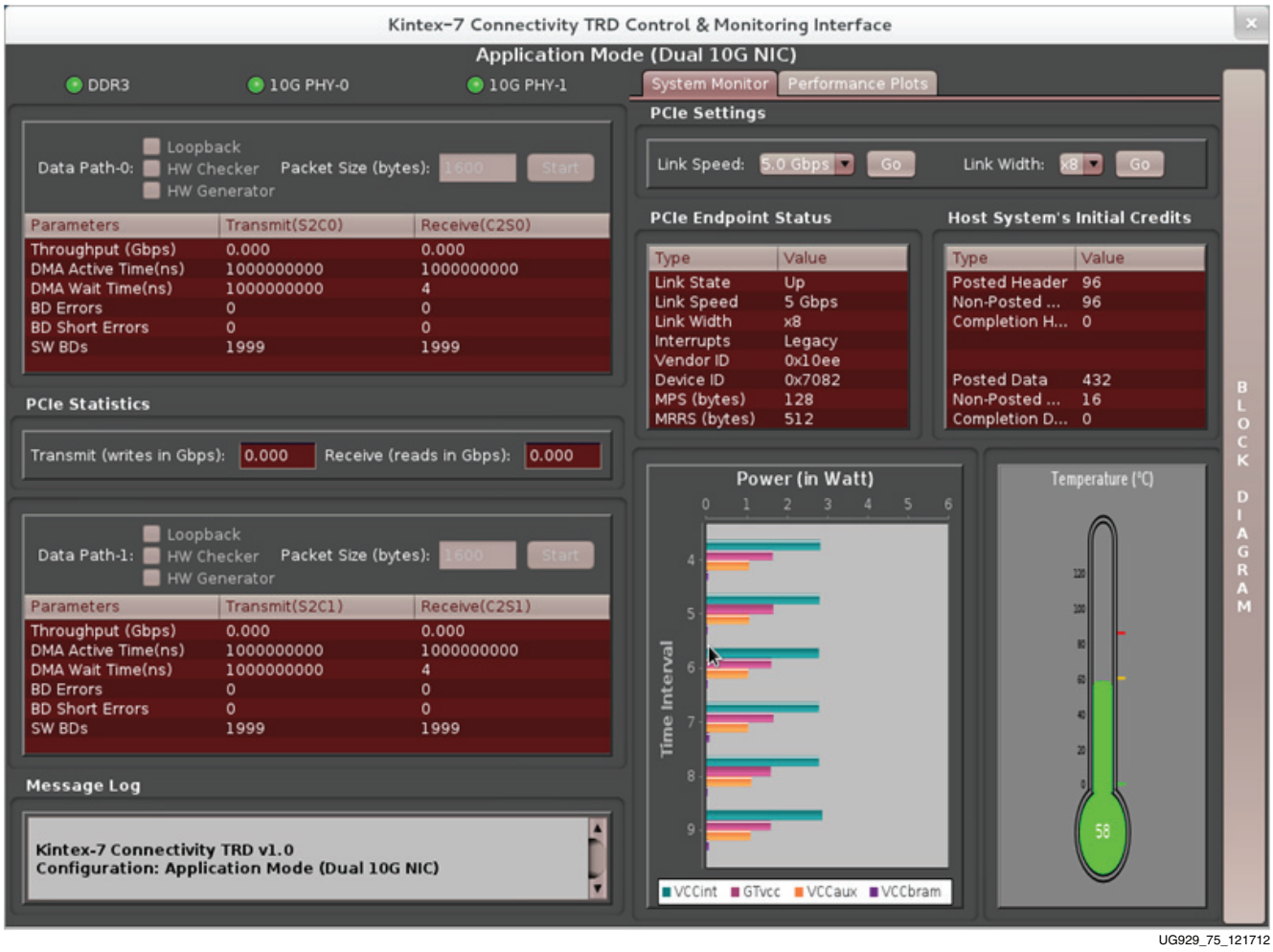

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Figure 22: **Application Mode Driver GUI**

15. Open another terminal on the host machine and run ping (see Figure 23) using the following command:

```
$ ping 10.60.0.1
$ ping 10.60.1.1
```

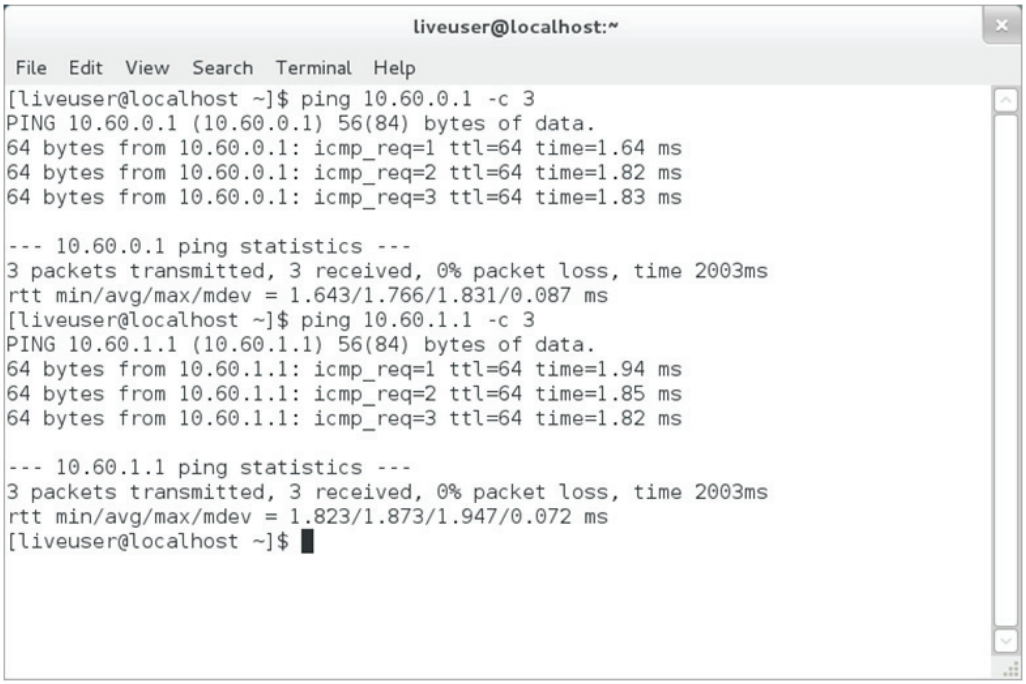

Figure 23: **Ping application on Application Mode Driver**

16. The user can click on the Block Diagram option to view the design block diagram as shown in Figure 24.
17. Close the GUI – this un-installs driver and opens the Kintex-7 Connectivity TRD landing page. Note that driver un-installation requires the GUI to be closed first.

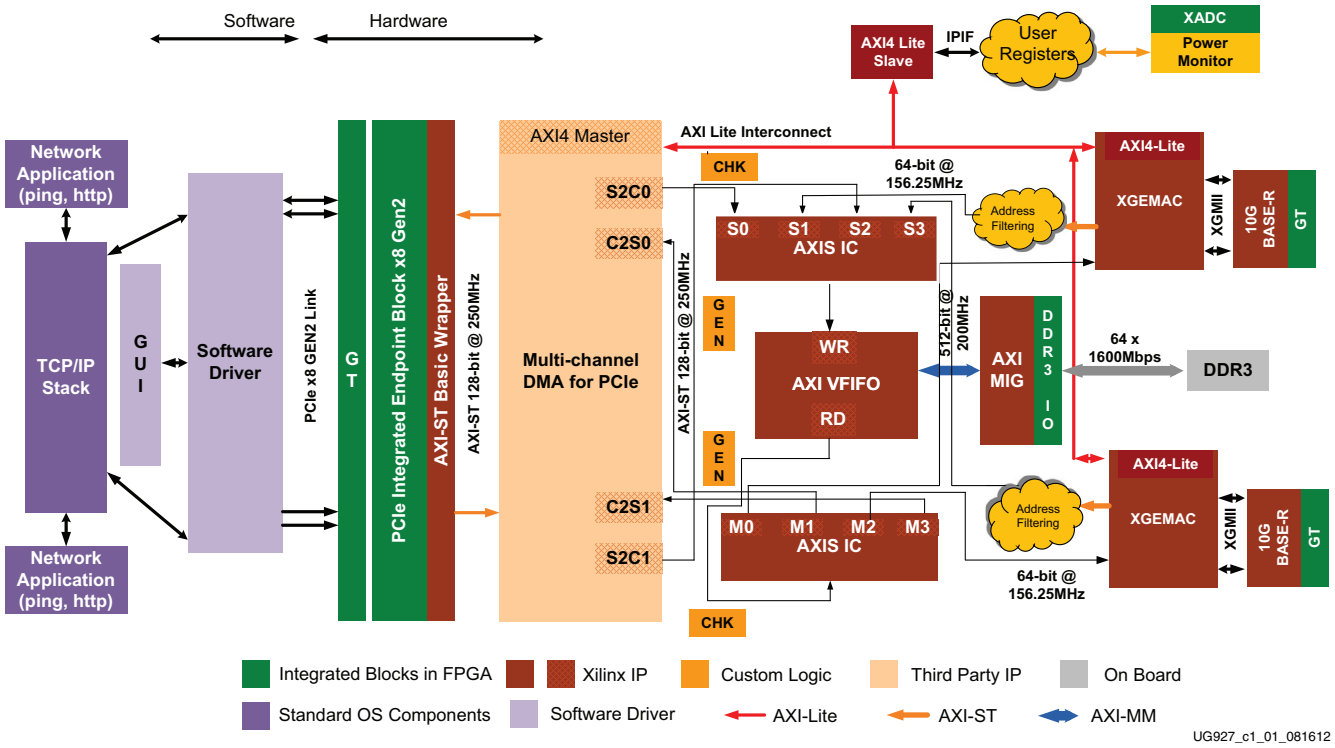

Figure 24: **Design Block Diagram**

Next Steps

With the steps in this getting started guide completed, the user has achieved a simple hardware bring-up of the Kintex-7 Connectivity TRD and initial hands-on experience with the connectivity kit.

User can now go to http://www.xilinx.com/products/boards-and-kits to get the Kintex-7 Connectivity TRD user guide and learn how to use this design as a platform to develop their own system.

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Appendix A

Additional Resources

Xilinx Resources

To search the Answer database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx Support website at:

http://www.xilinx.com/support

For a glossary of technical terms used in Xilinx documentation, see:

http://www.xilinx.com/support/documentation/sw_manuals/glossary.pdf

References

These documents provide supplemental material useful with this user guide.

1. UG911, *Vivado Design Suite Migration Methodology Guide*
2. UG900, *Vivado Design Suite User Guide: Logic Simulation*
3. UG904, *Vivado Design Suite User Guide: Implementation*
4. PG054, *7 Series FPGAs Integrated Block for PCI Express User Guide*
5. UG626, *Synthesis and Simulation Product Guide*
6. WP350, *Understanding Performance of PCI Express Systems*
7. UG476, *7 Series FPGAs GTX Transceivers User Guide*
8. UG810, *KC705 Evaluation Board for the Kintex-7 FPGA User Guide*
9. UG586, *7 Series FPGAs Memory Interface Solutions User Guide*
10. UG883, *Kintex-7 FPGA Base Targeted Reference Design Getting Started Guide*
11. PG072, *LogiCORE IP 10-Gigabit Ethernet MAC Product Guide*
12. PG068, *LogiCORE IP Ten Gigabit Ethernet PCS/PMA Product Guide*
13. AXI Interconnect IP: http://www.xilinx.com/products/intellectual-property/axi_interconnect.htm
14. PG035, *LogiCORE IP AXI4-Stream Interconnect Product Guide*
15. PG038, *LogiCORE IP AXI VFIFO Controller Product Guide*
16. AR 50555, *Kintex-7 FPGA Connectivity Kit and Targeted Reference Design - Release Notes and Known Issues Master Answer Record*

Additional Useful Sites for Boards and Kits

17. Updated information about the Kintex-7 FPGA Base Connectivity and Kintex-7 FPGA KC705 Evaluation kit
www.xilinx.com/kc705

18. Design advisories by software release for Kintex-7 FPGA KC705 Evaluation kit
    http://www.xilinx.com/support/#nav=sd-nav-link-179661&tab=tab-bk
19. KC705 support website
    http://www.xilinx.com/products/boards-and-kits/EK-K7-KC705-G.htm

Third Party Resources

Documents associated with other software, tool, and IP used by the connectivity TRD are available at these vendor websites:

20. Tera Term Pro program:
    http://hp.vector.co.jp/authors/VA002416/teraterm.html
21. Drivers on the Silicon Labs site:
    http://www.silabs.com/Support%20Documents/Software/CP210x_VCP_Win_XP_S2K3_Vista_7.exe
22. Northwest Logic DMA back end core:
    http://www.nwlogic.com/products/pci-express-solution
23. Fedora project:
    http://fedoraproject.org

    Fedora is a Linux-based operating system used in the development of this TRD.
24. FM-S14 FMC:
    Faster Technology FM-S14
    http://www.fastertechnology.com/fm_s14.html
25. 10G MMF SFP+ SR Optical Transceivers:
    Avago AFBR-703SDZ
    http://www.avagotech.com/pages/en/fiber_optics/ethernet/10_gbe/afbr-703sdz/
26. LC to LC OM3 10G fiber optic patch cable:
    Amphenol Cables on Demand™ (ACD) FO-10GGBLCX20-001
    http://www.cablesondemand.com/category/FO10GGBMM/URvars/Catalog/Library/InfoManage/10-GIGABIT_MULTIMODE_CABLES_...htm

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Appendix B

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