## Revision History

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<td>10/08/14</td>
<td>10.0</td>
<td>Recompiled for 2014.3.</td>
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<td>06/09/14</td>
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<td>8.0</td>
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<td>10/23/13</td>
<td>6.0</td>
<td>Recompiled for 2013.3. Converted to IPI.</td>
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<td>06/19/13</td>
<td>5.0</td>
<td>Recompiled for 2013.2. AR55738, AR55939 and AR55531 fixed.</td>
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<td>05/10/13</td>
<td>4.1</td>
<td>Added AR55939.</td>
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<td>04/03/13</td>
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<td>02/22/13</td>
<td>3.1</td>
<td>Added AR53420.</td>
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<td>12/18/12</td>
<td>3.0</td>
<td>Recompiled for 2012.4. AR53392.</td>
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<td>10/23/12</td>
<td>2.0</td>
<td>Recompiled for 2012.3. AR51180 fixed. AR52368.</td>
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<tr>
<td>09/20/12</td>
<td>1.0</td>
<td>Initial version for 2012.2. AR50886. AR51180. AR51758.</td>
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Overview

- Xilinx KC705 Board
- Software Requirements
- KC705 Setup
- KC705 BIST (Built-In Self Test)
- Compile KC705 BIST Design
- Program KC705 with BIST Design
- Run the LwIP Ethernet Design
- References

Note: This presentation applies to the KC705
KC705 BIST Design Description

» Description
  - The Built-In System Test (BIST) application uses an IPI MicroBlaze system to verify board functionality. A UART based terminal program interface offers users a menu of tests to run.

» Block Design Source
  - KC705 BIST Design Files (2014.3 C) ZIP file
  - Available through http://www.xilinx.com/kc705

Note: Presentation applies to the KC705
KC705 BIST Design Description

Block Design IP

- Processor and Subsystems: MicroBlaze, MicroBlaze Debug Module (MDM), Local Memory Bus, LMB BRAM Controller, Block Memory Generator, Proc Sys Reset, AXI Interrupt Controller
- AXI Bus: AXI Interconnect, AXI Timer
- Memory: AXI BRAM Controller, MIG 7 Series, AXI DMA
- Peripherals: AXI Ethernet, AXI EMC, AXI IIC, AXI GPIO, AXI UART 16550, XADC Wizard
- Other IP: Clocking Wizard, Constant, Concat, Slice, gte2_top
  - [Designing IP Subsystems Using IP Integrator](https://www.xilinx.com/support/documentation/ug994.pdf) (UG994)

Note: Presentation applies to the KC705
Xilinx KC705 Board
Vivado Software Requirements

  - Combined installer

Note: Presentation applies to the KC705
Connect a USB Type-A to Mini-B cable to the USB UART connector on the KC705 board
- Connect this cable to your PC
KC705 Setup

Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the KC705 board

- Connect this cable to your PC
- Power on the KC705 board for UART Drivers Installation
KC705 Setup

» Install USB UART Drivers
  – Refer to UG1033 for details on installing the USB to UART Drivers

Note: Presentation applies to the KC705
KC705 Setup

- Reboot your PC if necessary
- Right-click on My Computer and select Properties
  - Select the Hardware tab
  - Click on Device Manager

Note: Presentation applies to the KC705
KC705 Setup

Expand the Ports

Hardware

- Right-click on Silicon Labs CP210x USB to UART Bridge and select Properties

Note: Presentation applies to the KC705
KC705 Setup

- Under Port Settings tab
  - Click Advanced
  - Set the COM Port to an open Com Port setting from COM1 to COM4

Note: Presentation applies to the KC705
KC705 Setup

- Refer to [UG1036](#) regarding Tera Term installation
- Board Power must be on before starting Tera Term
- Start the Terminal Program
  - Select your USB Com Port
  - Set the baud to 9600

![Tera Term Setup](https://via.placeholder.com/350)

Note: Presentation applies to the KC705
KC705 Setup

- Unzip the KC705 BIST Design Files (2014.3 C) ZIP file
  - Available through http://www.xilinx.com/kc705

Note: Presentation applies to the KC705
Open a Vivado Tcl Shell:

Start → All Programs → Xilinx Design Tools → Vivado 2014.3 → Vivado 2014.3 Tcl Shell
KC705 BIST

- Download the BIST bitstream
- In the Vivado Tcl Shell type:
  ```
  cd C:/kc705_bist/ready_for_download
  source bist_download.tcl
  ```

Note: Presentation applies to the KC705
KC705 BIST

View initial BIST screen

Note: Presentation applies to the KC705
KC705 BIST

UART Test

- Type “1” to start the UART Test
- After each test, press any key to return to the main menu

Note: Presentation applies to the KC705
**KC705 BIST**

- LED Test
  - Type 2 to begin LED Test

- View Walking 1’s pattern on GPIO LEDs
  - Sequence repeats twice

**Note:** Presentation applies to the KC705
KC705 BIST

- IIC Test
  - Type 3 to begin IIC Test
KC705 BIST

- Flash Test
  - Type 4 to begin Flash test

Note: SW1 must not be set to JTAG mode (xx101) for this test
KC705 BIST

Timer Test

- Type 5 to begin Timer Test

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**Note:** Presentation applies to the KC705
KC705 BIST

Rotary Test
- Type 6 to begin Rotary Test
- Turn the rotary switch (under the LCD) back and forth
- Push the rotary switch inwards to actuate the push button switch

Note: Presentation applies to the KC705
**KC705 BIST**

- **GPIO Switch Test**
  - Set 4-position GPIO DIP Switch (SW4)
  - Type 7 to begin GPIO Switch Test
    - Reads switch settings

**Note:** Presentation applies to the KC705
KC705 BIST

LCD Test

- Type 8 to begin LCD Test

Note: Presentation applies to the KC705
External Memory Test

- Type 9 to begin External Memory Test

TEST2: Testing for stuck together bank/row/col bits
    Clearing memory to zeros...
    Writing and Reading...
Test Complete Status = SUCCESS

TEST3: Testing for maximum bank/row/col noise
    This test performs 16 word writes followed by 16 word reads
    Each 64 bytes inverts the bank/row/col address
    Initializing Memory to 0xA5A5A5A5...
    Writing and Reading...
Test Complete Status = SUCCESS

TEST4: Testing for Inverse Data at Address
    Writing...
    Reading...
Test Complete Status = SUCCESS

Number of errors in this pass = 0

axi_7series_ddrx test iteration #1 has PASSED!
Total number of errors for all iterations = 0
### Program finished successfully ###
Press any key to return to main menu

Note: Presentation applies to the KC705
KC705 BIST

- Internal Memory Test
  - Type A to begin BRAM Memory Test

Note: Presentation applies to the KC705
**Ethernet Test**

- Type B to begin AXI Ethernet Test

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**Note:** Presentation applies to the KC705
KC705 BIST

► Button Test
  – Type C to begin Button Test

Note: Presentation applies to the KC705
Compile KC705 BIST Design
Compile KC705 BIST Design

➤ Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2014.3 → Vivado

➤ Select Open Project

Note: Presentation applies to the KC705
Compile KC705 BIST Design

Open the KC705 Design:
- `<Design Name>\kc705_bist\kc705_bist.xpr`

Note: Presentation applies to the KC705
Compile KC705 BIST Design

The design is fully implemented; you can recompile, or export to SDK

- To recompile, right-click `synth_1`, select **Reset Runs** then **Generate Bitstream**

Note: Presentation applies to the KC705
Compile KC705 BIST Design

Once done, both the Synthesis and Implementation will have green check marks

Note: Presentation applies to the KC705
Compile KC705 BIST Design

- The BIST Design has been implemented with IP Integrator (IPI)
- Click Open Block Design

Note: Presentation applies to the KC705
Compile KC705 BIST Design

- All the IP Blocks used in the design can be seen in this view
- Click Open Implemented Design

Note: Presentation applies to the KC705
Compile KC705 BIST Design

› View Implemented Design

Note: Presentation applies to the KC705
Compile KC705 BIST Design

- Select File → Export → Export Hardware
- Click OK

Note: Presentation applies to the KC705
Compile KC705 BIST Design

- Select File → Launch SDK
- Click OK

Note: Presentation applies to the KC705
Compile KC705 Software in SDK

SDK Software Compile - Build ELF files in SDK
- Project builds automatically
- When done, close SDK and return to Vivado

Note: Presentation applies to the KC705
Program KC705 with BIST Design
Program KC705 with BIST Design

Select Add Sources

Note: Presentation applies to the KC705
Program KC705 with BIST Design

Select Add or Create Design Sources

Note: Presentation applies to the KC705
Program KC705 with BIST Design

- Add bist_app.elf and lwip_echo_server.elf from the SDK tree
- Make sure Copy sources into project is deselected
- Click Finish
Program KC705 with BIST Design

Right-click on one of the ELF files and select Associate ELF files.
Program KC705 with BIST Design

- Click the button to the right; select the bist_app.elf then click OK twice

**Note:** Presentation applies to the KC705
Program KC705 with BIST Design

- Select Generate Bitstream
  - This creates a bitstream with the BIST ELF file

**Note:** Presentation applies to the KC705
Program KC705 with BIST Design

Click Open Hardware Manager

Note: Presentation applies to the KC705
Program KC705 with BIST Design

- Click Open Target and select Auto Connect

Note: Presentation applies to the KC705
Program KC705 with BIST Design

Select Program device → xc7k325t_0

Note: Presentation applies to the KC705
Program KC705 with BIST Design

- Program Device defaults to impl_1 bitstream
- Click Program

Note: Presentation applies to the KC705
Program KC705 with BIST Design

» BIST Application runs in the terminal window

**Note:** Presentation applies to the KC705
Program KC705 with BIST Design

- Close the Project

Note: Presentation applies to the KC705
Program KC705 with BIST Design

- Repeat this process using Tcl scripts
- Open a Vivado Tcl shell and type:
  ```
  cd C:/kc705_bist/ready_for_download
  source make_download_files.tcl
  ```
- This script uses Tcl commands to add the ELF files to the BIST project, then generate both the BIST and LwIP bitstreams
Program KC705 with BIST Design

- Download the BIST bitstream
- In the Vivado Tcl Shell type:

  ```bash
  source C:/kc705_bist/ready_for_download/bist_download.tcl
  ```

Note: Presentation applies to the KC705
Program KC705 with BIST Design

» BIST Application runs in the terminal window

Note: Presentation applies to the KC705
Run the LwIP Ethernet Design
Connect an Ethernet cable to the KC705

- Connect this cable to your PC
- Not shown, the UART should be connected
Run the LwIP Ethernet Design

- From the Windows Control Panel, open Network Connections
- Right-click on the Gigabit Ethernet Adapter and select Properties

**Note:** Presentation applies to the KC705
Run the LwIP Ethernet Design

» Click Configure
  – Set the Media Type to Auto for 1 Gbps then click OK
Run the LwIP Ethernet Design

- Reopen the properties after the last step
- Set your host (PC) to this IP Address:

```
192.168.1.2
255.255.255.0
```

Note: Presentation applies to the KC705
Run the LwIP Ethernet Design

- Download the LwIP bitstream
- In the Vivado Tcl Shell type:

  ```
  source C:/kc705_bist/ready_for_download/lwip_download.tcl
  ```
Run the LwIP Ethernet Design

- View LwIP echo server screen

--- lwIP TCP echo server ---
TCP packets sent to port 6001 will be echoed back
Board IP: 192.168.1.10
Netmask: 255.255.255.0
Gateway: 192.168.1.1
auto-negotiated link speed: 1000
TCP echo server started @ port 7

Note: Presentation applies to the KC705
Run the LwIP Ethernet Design

From a DOS window on the PC Host, enter the command:

ping 192.168.1.10

- Ping from PC host 192.168.1.2 to KC705 target 192.168.1.10

![Ping result from DOS window]

Note: Presentation applies to the KC705
References
References

IP Integrator Documentation

– Vivado Design Suite Tcl Command Reference Guide

– Designing IP Subsystems Using IP Integrator

7 Series Configuration

– 7 Series FPGAs Configuration User Guide
Documentation

Kintex-7
  - Kintex-7 FPGA Family
  - Design Advisory Master Answer Record for Kintex-7 FPGAs
    • http://www.xilinx.com/support/answers/42946.htm

KC705 Documentation
  - Kintex-7 FPGA KC705 Evaluation Kit
  - KC705 Getting Started Guide
  - KC705 User Guide