Kintex-7 FPGA KC724 Characterization Kit IBERT

Getting Started Guide

Vivado Design Suite 2014.1

UG931 (v5.0) April 16, 2014

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/23/2012	1.0	Initial Xilinx release.
07/02/2013	2.0	Updated for Vivado Design Suite 2013.2 release. Updated Extracting the Project Files, GTX Transceiver Clock Connections, Setting Up the Vivado Design Suite, Starting the SuperClock-2 Module, Viewing GTX Transceiver Operation, Closing the IBERT Demonstration, and Creating the GTX IBERT Core. Updated Figure 1-1 and Figure 1-10 through Figure 1-35.
10/23/2013	3.0	Updated disclaimer and copyright. Updated for the Vivado Design Suite 2013.3 release. Updated filenames in Extracting the Project Files and throughout the document. Added Appendix A, Additional Resources.
12/18/2013	4.0	Updated for the Vivado Design Suite 2013.4 release.
04/16/2014	5.0	Updated for the Vivado Design Suite 2014.1 release. Added note to GTX TX/RX Loopback Connections. Updated Step 4 in Starting the SuperClock-2 Module. Updated In Case of RX Bit Errors. Added a note to Step 5 in Creating the GTX IBERT Core.

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Chapter 1

KC724 IBERT Getting Started Guide

Overview

This document describes setting up the KC724 Kintex®-7 FPGA GTX Transceiver Characterization Board to run the Integrated Bit Error Ratio Test (IBERT) demonstration using the Vivado® Design Suite. The designs that are required to run the IBERT demonstration are stored in a Secure Digital (SD) memory card that is provided with the KC724 board. The demonstration shows the capabilities of the Kintex-7 XC7K325T FPGA GTX transceiver.

The KC724 board is described in detail in the *KC724 Kintex-7 FPGA GTX Transceiver Characterization Board User Guide* (UG932) [Ref 1].

The IBERT demonstrations operate one GTX Quad at a time. The procedure consists of:

1. Setting Up the KC724 Board, page 6.
2. Extracting the Project Files, page 7.
3. Connecting the GTX Transceivers and Reference Clocks, page 8.
4. Configuring the FPGA, page 13.
5. Setting Up the Vivado Design Suite, page 14.
6. Starting the SuperClock-2 Module, page 17
7. Viewing GTX Transceiver Operation, page 23.
8. Closing the IBERT Demonstration, page 24.

Requirements

The hardware and software required to run the GTX IBERT demonstrations are:

- KC724 Kintex-7 FPGA GTX Transceiver Characterization Board, including:
    - One SD card containing the IBERT demonstration designs
    - One Samtec BullsEye cable
    - Eight SMA female-to-female (F-F) adapters
    - Six 50Ω SMA terminators
    - GTX transceiver power supply module (installed on board)
    - SuperClock-2 module, Rev 1.0 (installed on board)
    - Active BGA Heatsink (installed on FPGA)
    - 12V DC power adapter
    - USB cable, standard-A plug to micro-B plug
- Host PC with:
    - SD card reader
    - USB ports
- Xilinx® Vivado Design Suite 2014.1

The hardware and software required to rebuild the IBERT demonstration designs are:

- Xilinx Vivado Design Suite 2014.1
- PC with a version of the Windows operating system supported by Xilinx Vivado Design Suite

Setting Up the KC724 Board

This section describes how to set up the KC724 board.

Caution! The KC724 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board, such as using a grounding strap and static dissipative mat.

When the KC724 board ships from the factory, it is configured for the GTX IBERT demonstrations described in this document. If the board has been re-configured it must be returned to the default set-up before running the IBERT demonstrations.

1. Move all jumpers and switches to their default positions. The default jumper and switch positions are listed in the *KC724 Kintex-7 FPGA GTX Transceiver Characterization Board User Guide* (UG932) [Ref 1].
2. Install the GTX transceiver power module by plugging it into connectors J66 and J97.
3. Install the SuperClock-2 module:
    a. Align the three metal standoffs on the bottom side of the module with the three mounting holes in the SUPERCLOCK-2 MODULE interface of the KC724 board.
    b. Using three 4-40 x 0.25 inch screws, firmly screw down the module from the bottom of the KC724 board.
    c. On the SuperClock-2 module, place a jumper across pins 2–3 (2V5) of the CONTROL VOLTAGE header, J18, and place another jumper across Si570 INH header J11.

d. Screw down a 50Ω SMA terminator onto each of the six unused Si5368 clock output SMA connectors: J7, J8, J12, J15, J16 and J17.

Extracting the Project Files

The Vivado Design Suite project files required to run the IBERT demonstrations are located in `rdf0184-kc724-ibert-2014-1.zip` on the SD card provided with the KC724 board. They are also available online at the Kintex-7 FPGA KC724 Characterization Kit documentation website.

The zip file contains these files:

- Bit Files

  `kc724_ibert_q115_125.bit`

  `kc724_ibert_q116_125.bit`

  `kc724_ibert_q117_125.bit`

  `kc724_ibert_q118_125.bit`

- Probe Files

  `kc724_ibert_115_debug_nets.ltx`

  `kc724_ibert_116_debug_nets.ltx`

  `kc724_ibert_117_debug_nets.ltx`

  `kc724_ibert_118_debug_nets.ltx`

- Tcl Scripts

  `add_scm2.tcl`

  `setup_scm2_125_00.tcl`

The Tcl scripts are used to help merge the IBERT and SuperClock-2 source code (described in Creating the GTX IBERT Core) and to set up the SuperClock-2 module to run at 125.00 MHz (described in the Setting Up the Vivado Design Suite).

To copy the files from the Secure Digital memory card:

1. Connect the Secure Digital memory card to the host computer.
2. Locate the file `rdf0184-kc724-ibert-2014-1.zip` on the Secure Digital memory card.
3. Unzip the files to a working directory on the host computer.

Running the GTX IBERT Demonstration

The GTX IBERT demonstration operates one GTX Quad at a time. This section describes how to test GTX Quad 115. The remaining GTX Quads are tested following a similar series of steps.

Connecting the GTX Transceivers and Reference Clocks

Figure 1-1 shows the locations for GTX transceiver Quads 115, 116, 117, and 118 on the KC724 board.

Note: Figure 1-1 is for reference only and might not reflect the current revision of the board.

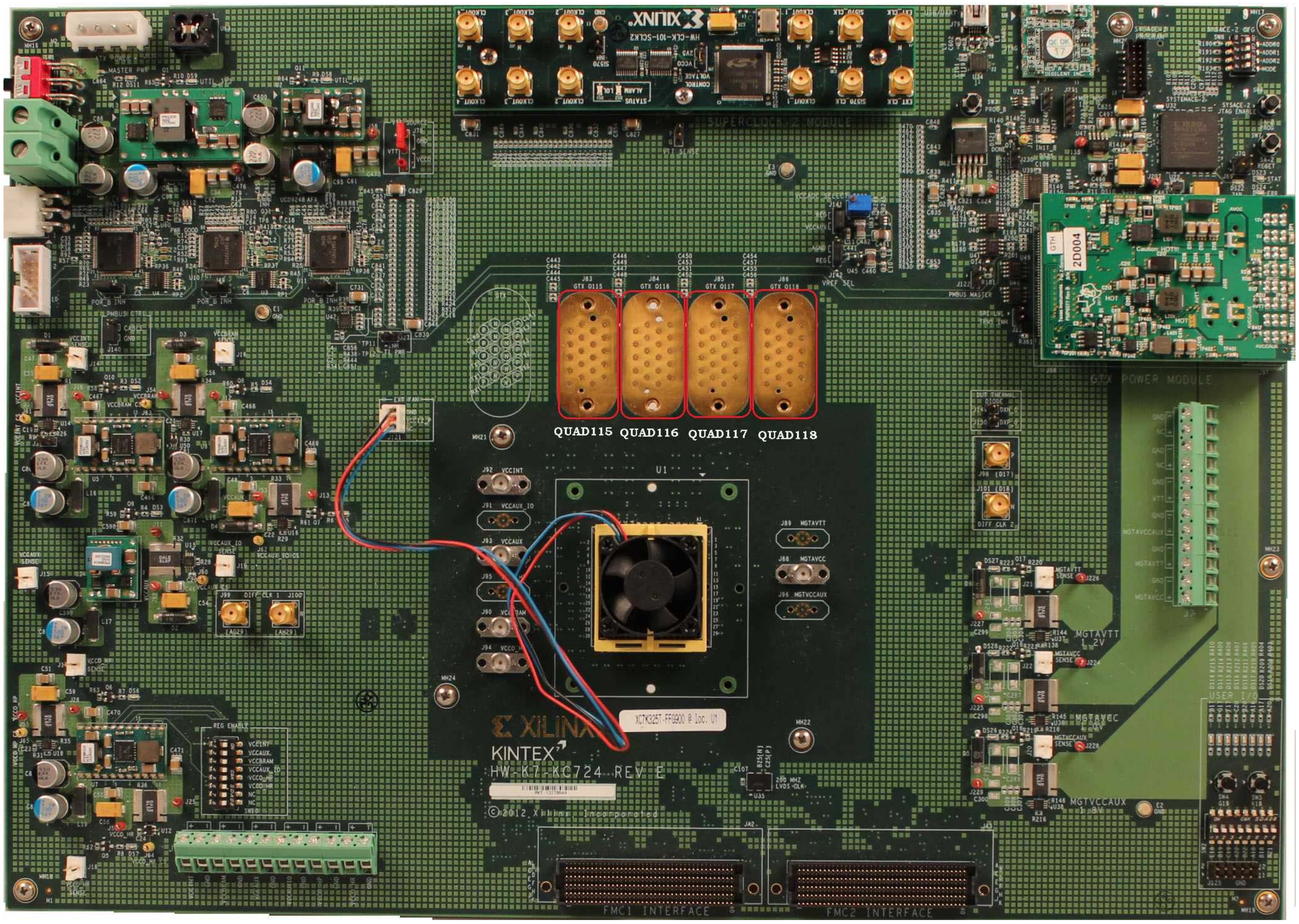

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Figure 1-1: **GTX Quad Locations**

All GTX transceiver pins and reference clock pins are routed from the FPGA to a connector pad that interfaces with Samtec BullsEye connectors. Figure 1-2 **A** shows the connector pad. Figure 1-2 **B** shows the connector pinout.

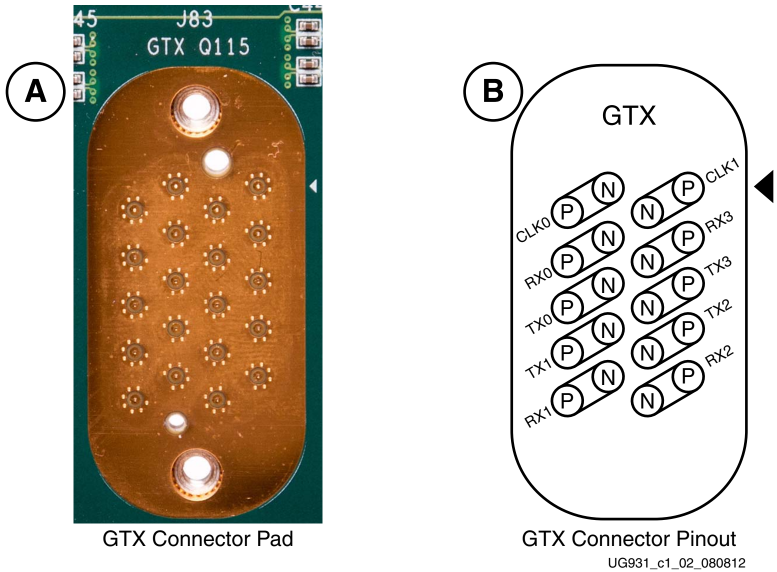

Figure 1-2: **A – GTX Connector Pad. B – GTX Connector Pinout**

The SuperClock-2 module provides LVDS clock outputs for the GTX transceiver reference clocks in the IBERT demonstrations. Figure 1-3 shows the locations of the differential clock SMA connectors on the clock module which can be connected to the reference clock cables.

Note: Figure 1-3 is for reference only and might not reflect the current revision of the board.

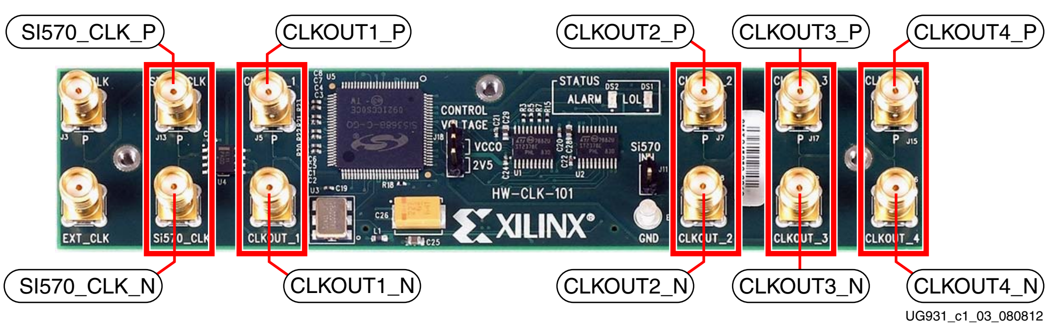

Figure 1-3: **SuperClock-2 Module Output Clock SMA Locations**

The four SMA pairs labeled CLKOUT provide LVDS clock outputs from the Si5368 clock multiplier/jitter attenuator device on the clock module. The SMA pair labeled Si570_CLK provides LVDS clock output from the Si570 programmable oscillator on the clock module.

Note: The Si570 oscillator does not support LVDS output on the Rev B and earlier revisions of the SuperClock-2 module.

For the GTX IBERT demonstration, the output clock frequencies are preset to 125.000 MHz. For more information on the SuperClock-2 module, see the *HW-CLK-101-SCLK2 SuperClock-2 Module User Guide* (UG770) [Ref 2].

Attach the GTX Quad Connector

Before connecting the BullsEye cable assembly to the board, firmly secure the blue elastomer seal provided with the cable assembly to the bottom of the connector housing if it is not already inserted (see Figure 1-4).

Note: Figure 1-4 is for reference only and might not reflect the current version of the connector.

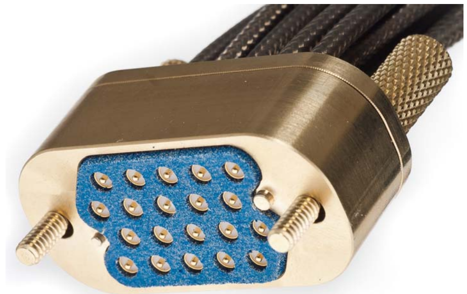

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Figure 1-4: **BullsEye Connector with Elastomer Seal**

Attach the Samtec BullsEye connector to GTX Quad 115 (Figure 1-5), aligning the two indexing pins on the bottom of the connector with the guide holes on the board. Hold the connector flush with the board and fasten it by tightening the two captive screws.

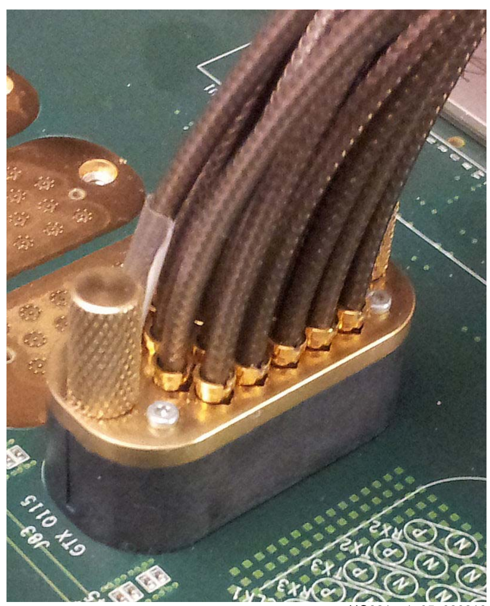

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Figure 1-5: **BullsEye Connector Attached to Quad 115**

GTX Transceiver Clock Connections

Refer to Figure 1-2, page 9 to identify the P and N coax cables that are connected to the CLK0 reference clock inputs. Connect these cables to the SuperClock-2 Module as follows:

- CLK0_P coax cable → SMA connector J7 (CLKOUT1_P) on the SuperClock-2 Module
- CLK0_N coax cable → SMA connector J8 (CLKOUT1_N) on the SuperClock-2 Module

Note: Any one of the five differential outputs from the SuperClock-2 Module can be used to source the GTX reference clock. CLKOUT1_P and CLKOUT1_N are used here as an example.

GTX TX/RX Loopback Connections

Refer to Figure 1-2, page 9 to identify the P and N coax cables that are connected to the four receivers (RX0, RX1, RX2 and RX3) and the four transmitters (TX0, TX1, TX2 and TX3). Use eight SMA female-to-female (F-F) adapters (Figure 1-6), to connect the transmit and receive cables as shown in Figure 1-7:

- TX0_P → SMA F-F Adapter → RX0_P
- TX0_N → SMA F-F Adapter → RX0_N
- TX1_P → SMA F-F Adapter → RX1_P
- TX1_N → SMA F-F Adapter → RX1_N
- TX2_P → SMA F-F Adapter → RX2_P
- TX2_N → SMA F-F Adapter → RX2_N
- TX3_P → SMA F-F Adapter → RX3_P
- TX3_N → SMA F-F Adapter → RX3_N

Note: To ensure good connectivity, it is recommended that the adapters be secured with a wrench; however, do not over tighten the SMAs.

Figure 1-6: **SMA F-F Adapter**

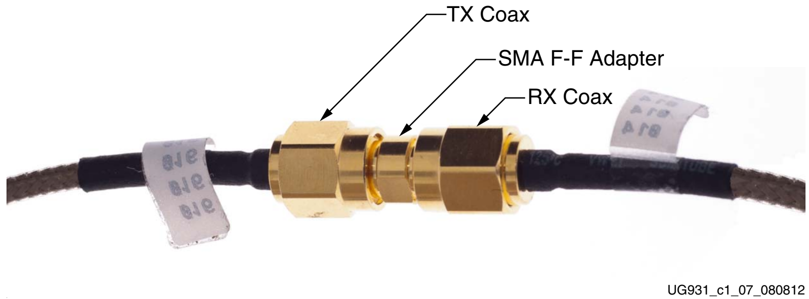

Figure 1-7: **TX-To-RX Loopback Connection Example**

Figure 1-8 shows the KC724 board with the cable connections required for the Quad 115 GTX IBERT demonstration.

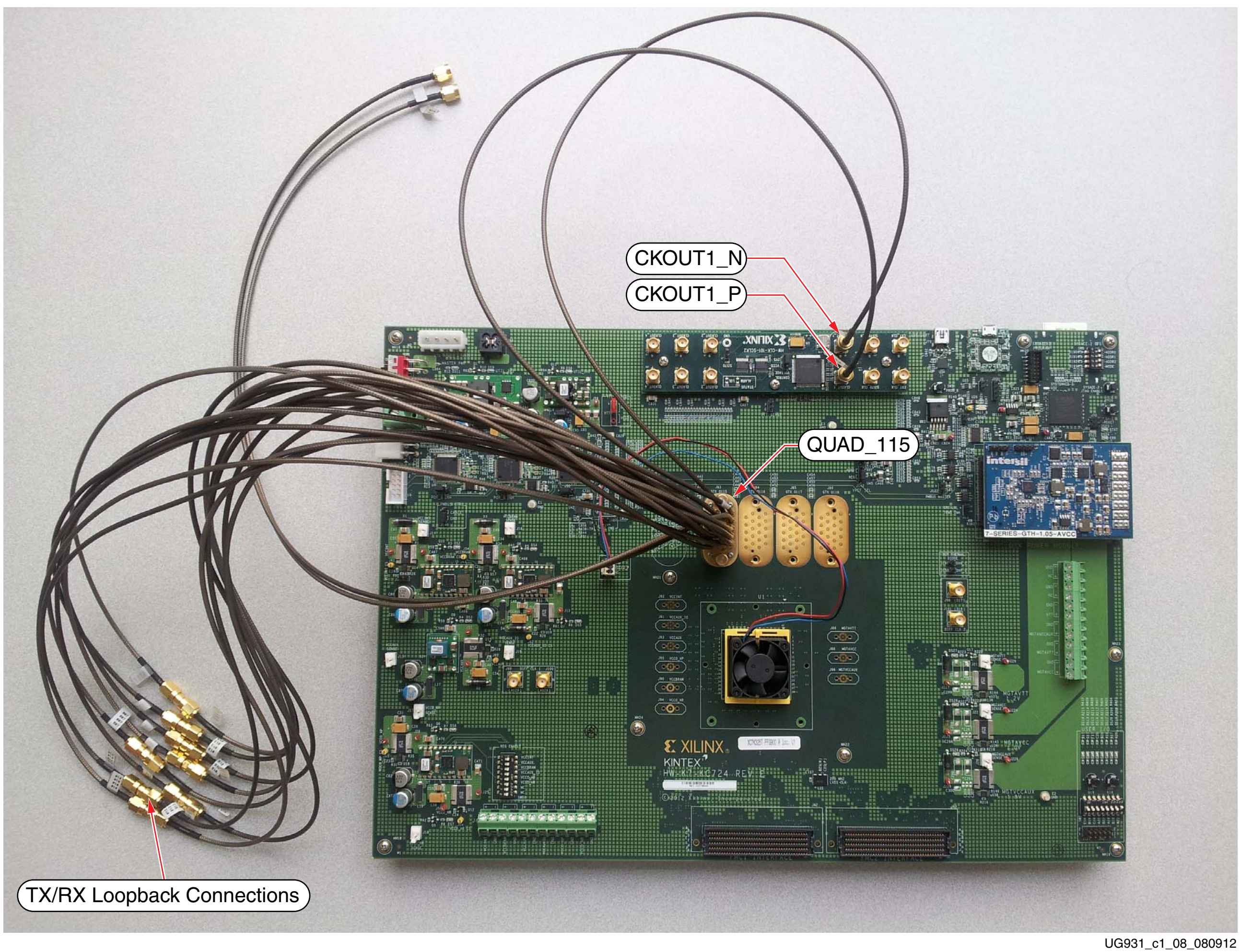

Figure 1-8: **Cable Connections for Quad 115 GTX IBERT Demonstration**

Configuring the FPGA

This section describes how to configure the FPGA using the SD card included with the board. The FPGA can also be configured through the Vivado Design Suite using the `.bit` files available on the SD card and online (as collection `rdf0184-kc724-ibert-2014-1.zip`) at the Kintex-7 FPGA KC724 Characterization Kit documentation website.

To configure from the SD card:

1. Insert the SD card provided with the KC724 board into the SD card reader slot located on the bottom-side (upper-right corner) of the KC724 board.
2. Plug the 12V output from the power adapter into connector J2 on the KC724 board.
3. Connect the host computer to the KC724 board using a standard-A plug to micro-B plug USB cable. The standard-A plug connects to a USB port on the host computer and the micro-B plug connects to U8, the Digilent USB JTAG configuration port on the KC724 board.
4. Select the GTX IBERT demonstration with the System ACE™ SD controller SASD CFG switch, SW8. The setting on this 4-bit DIP switch (Figure 1-9) selects the file used to configure the FPGA. A switch is in the ON position if set to the far right and in the OFF position if set to the far left. For the Quad 115 GTX IBERT demonstration, set ADR2 = ON, ADR1 = ON, and ADR0 = ON. The MODE bit (switch position 4) is not used and can be set either ON or OFF.

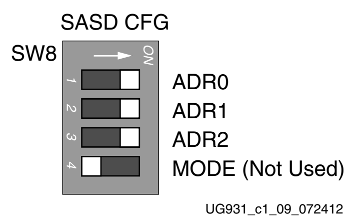

Figure 1-9: **Configuration Address DIP Switch (SW8)**

There is one IBERT demonstration design for each GTX Quad on the KC724 board, for a total of four IBERT designs. Four other demonstration designs are included that show other board features (the use of these designs are described in the README file within the SD card). All eight designs are organized and stored on the SD card as shown in Table 1-1.

Table 1-1: **SD Card Contents and Configuration Addresses**

Demonstration Design	ADR2	ADR1	ADR0
GTX Quad 115	ON	ON	ON
GTX Quad 116	ON	ON	OFF
GTX Quad 117	ON	OFF	ON
GTX Quad 118	ON	OFF	OFF
LED Scroll	OFF	ON	ON
DIP Switches	OFF	ON	OFF
Push Buttons	OFF	OFF	ON
USB/UART	OFF	OFF	OFF

5. Place the main power switch SW1 to the ON position.

Setting Up the Vivado Design Suite

1. Start the Vivado Design Suite on the host computer and click **Flow** > **Open Hardware Manager** (highlighted in Figure 1-10).

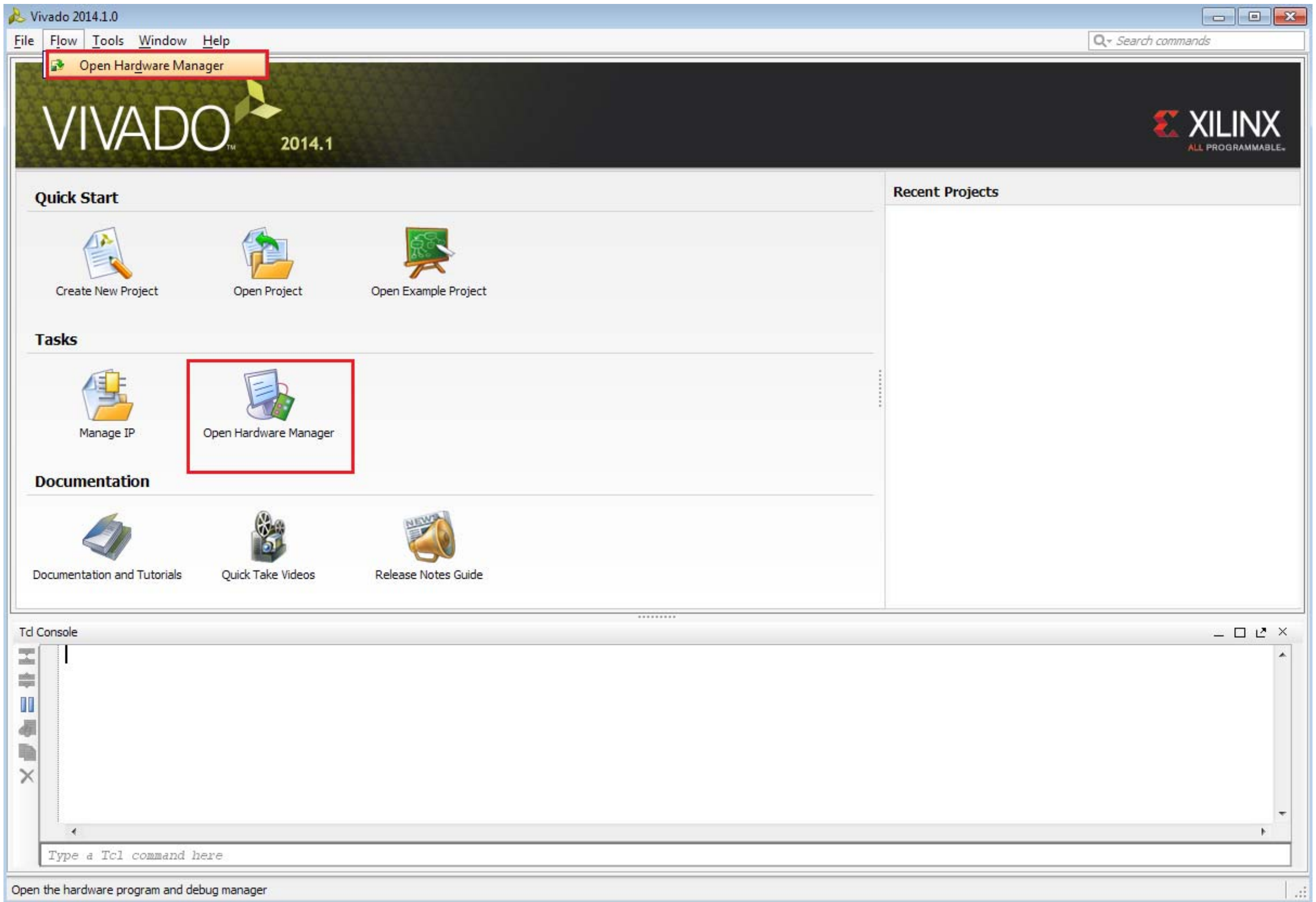

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Figure 1-10: **Vivado Design Suite, Open Hardware Manager**

2. In the Hardware Manager window (Figure 1-11), click **Open a new hardware target**.

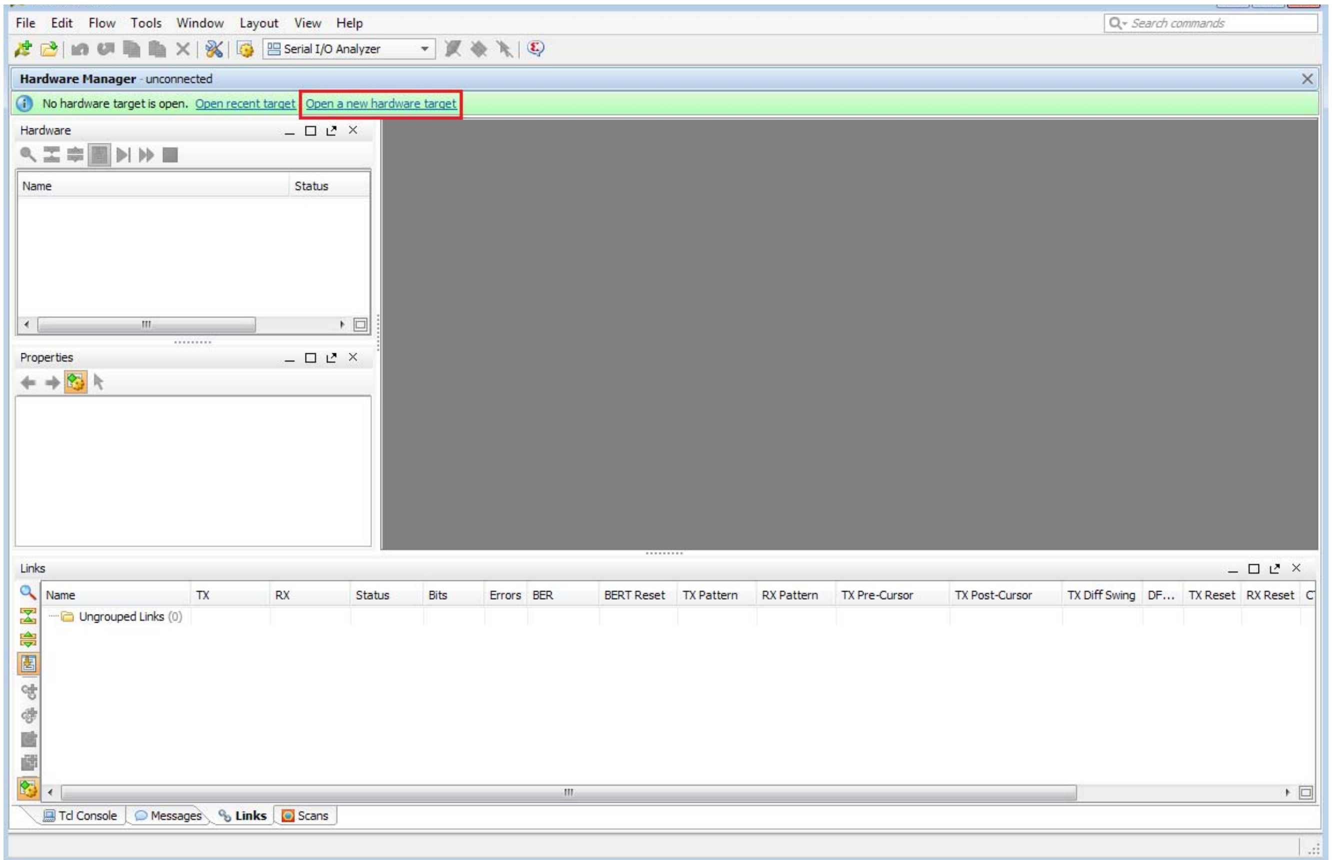

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Figure 1-11: **Open a New Hardware Manager**

3. An Open Hardware Target wizard opens. Click **Next** in the first window.
4. In the Hardware Server Settings window, select **Local server (target is on local machine)**. Click **Next** to open the server and connect to the Xilinx TCF JTAG cable.

5. In the Select Hardware Target window, the xilinx_tcf cable appears under Hardware Targets, and the JTAG chain contents of the selected cable appear under Hardware Devices (Figure 1-12). Select the **xilinx_tcf** target and keep the JTAG Clock Frequency at the default value (15 MHz), click **Next**.

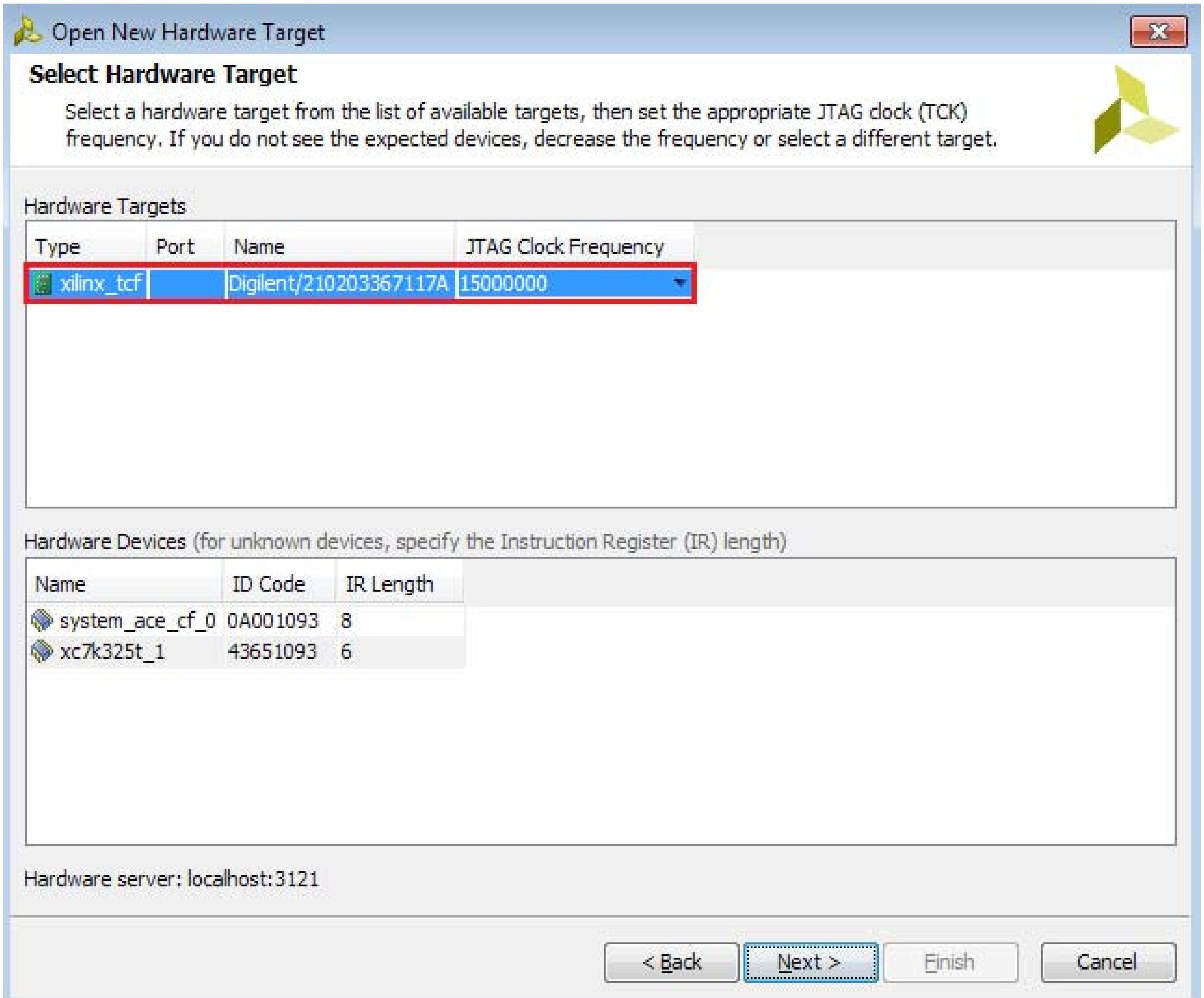

Figure 1-12: **Select Hardware Target**

6. In the Open Hardware Target Summary window, click **Finish**. The wizard closes and the Vivado Design Suite opens the hardware target.

Starting the SuperClock-2 Module

The IBERT demonstration designs use an integrated VIO core to control the clocks on the SuperClock-2 module. The SuperClock-2 module features two clock-source components: 1) An always-on Si570 crystal oscillator and, 2) an Si5368 jitter-attenuating clock multiplier. Outputs from either device can be used to drive the transceiver reference clocks. To start the SuperClock-2 Module:

1. The Vivado Design Suite Hardware window shows the System ACE and the XC7K325T device. The XC7K325T device will be reported as programmed when an SD card is used to program the FPGA during power reset (Figure 1-13). If the SD card is not available to program the XC7K235T device, select the device, and in the Hardware Device Properties window, enter the file path to the programming and the probes files associated with the Q115 IBERT design. The files are in the extracted IBERT files:

   `kc724_ibert_q115_125.bit`

   `kc724_ibert_115_debug_nets.ltx`

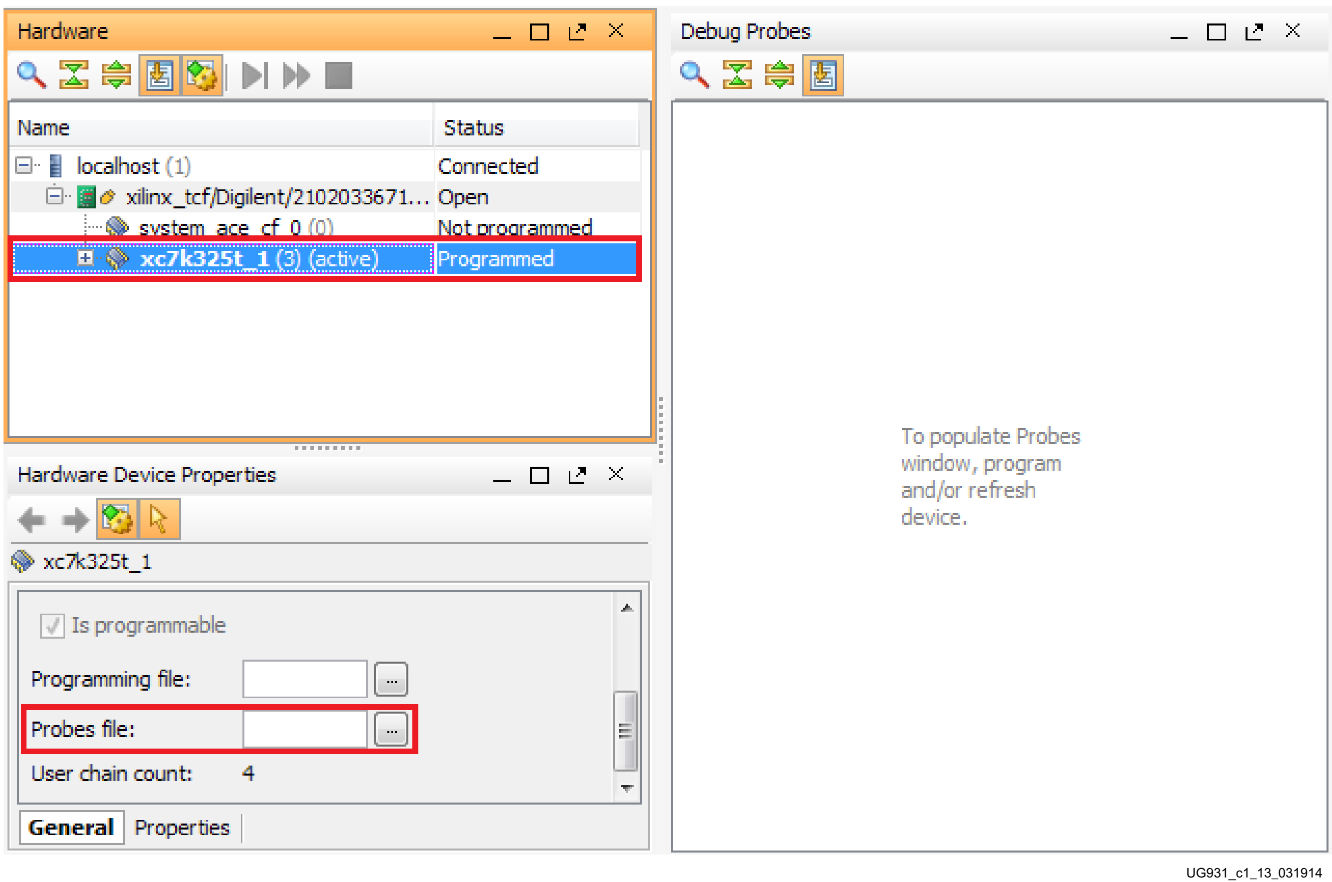

Figure 1-13: **Adding the Probes File**

2. In the Hardware window, right-click **XC7K325T_1** and select **Refresh Device** (Figure 1-14).

Note: If the FPGA was not programmed using the SD card, provide both the programming and the probes files, and then select **Program Device**.

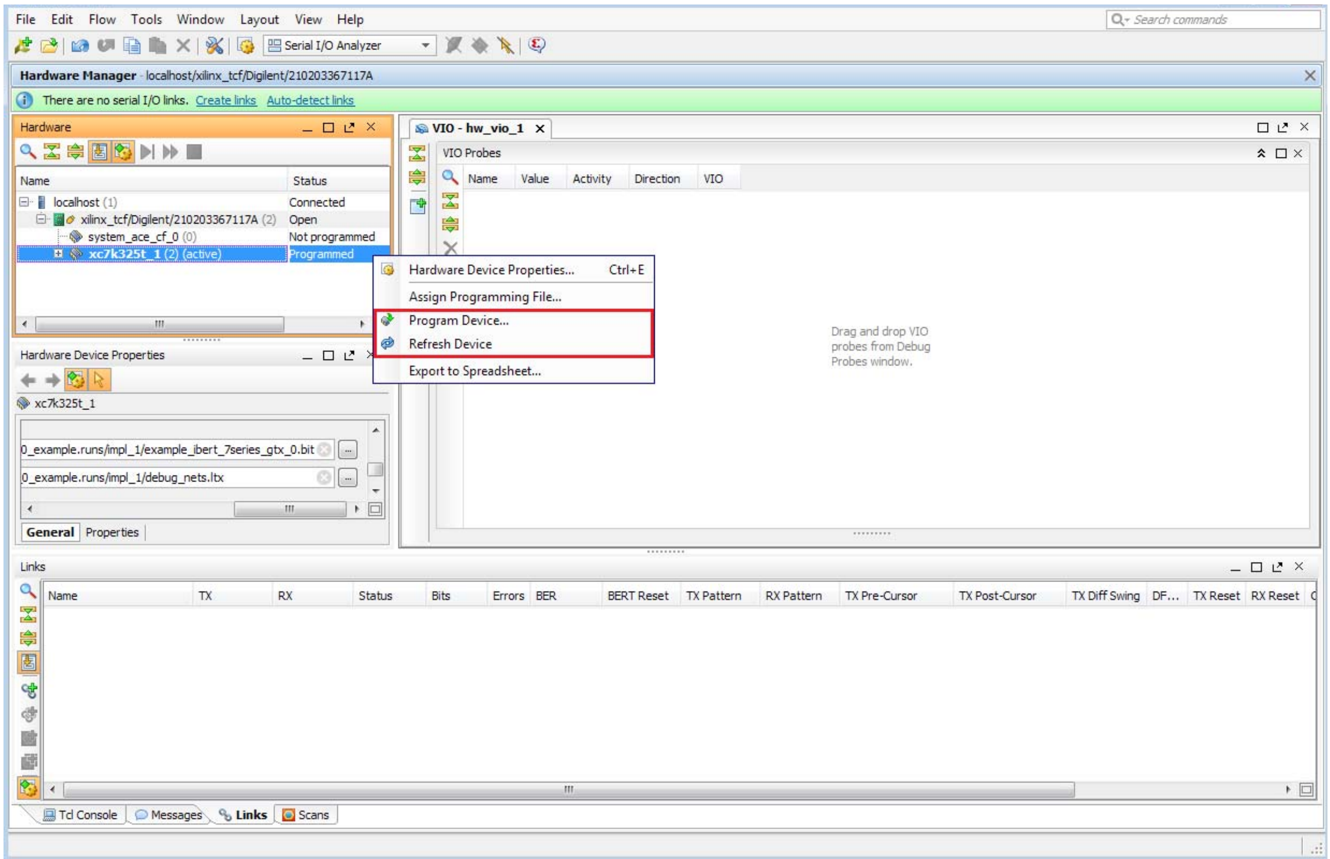

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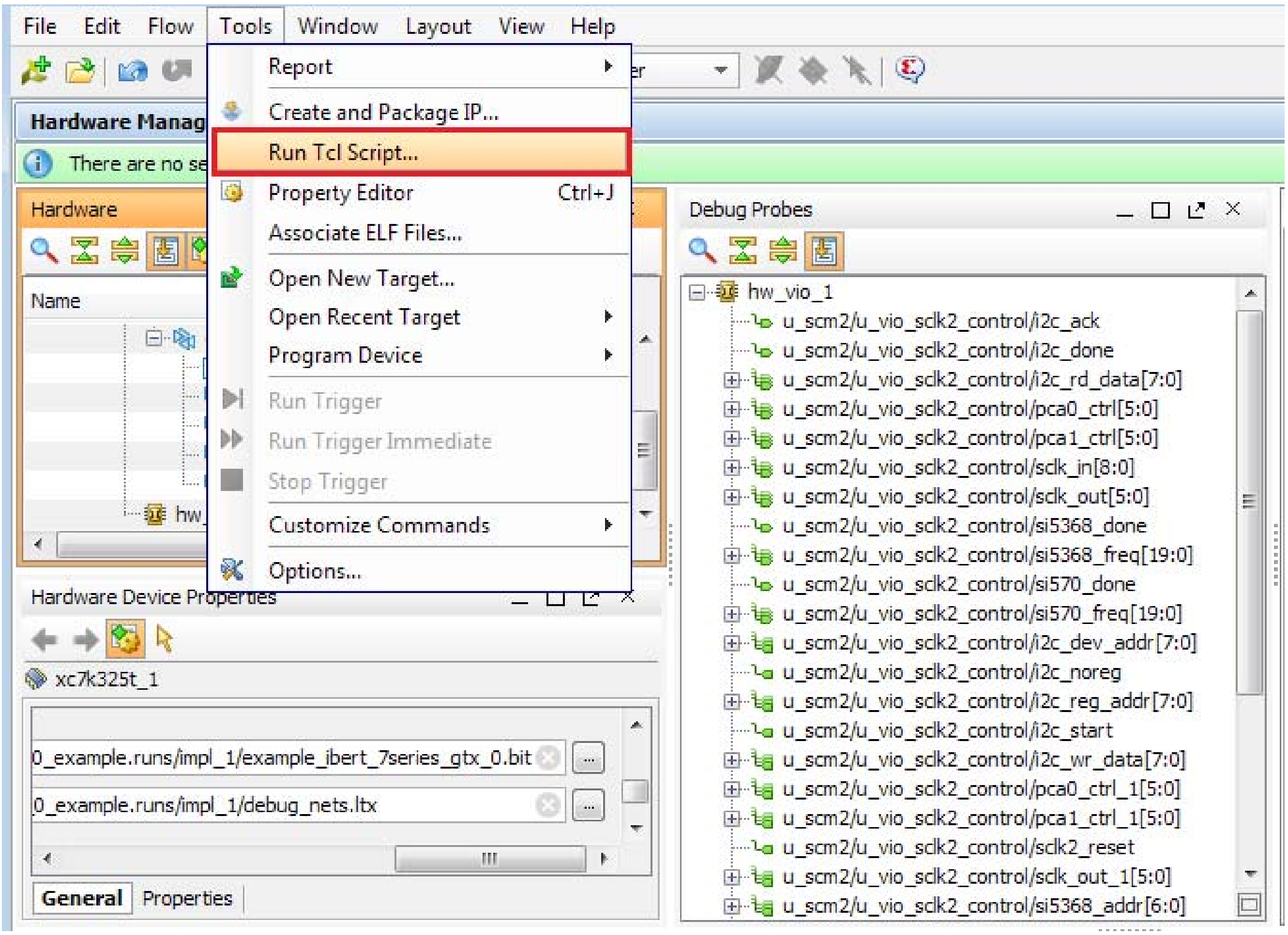
Figure 1-14: **Program/Refresh Device**

3. Vivado Design Suite reports that the XC7K325T is programmed and displays the SuperClock-2 VIO core and the IBERT core. To configure the SuperClock-2 module, click **Tools** > **Run Tcl Script** (Figure 1-15). In the Run Script window, navigate to the `setup_scm2_125_00.tcl` script in the extracted files and click **OK**.



ug931_c1_15_121113

Figure 1-15: **Run Tcl Script**

4. To view the SuperClock-2 settings in the VIO core, select the probe signal from the Debug Probes window and drag it to the VIO-hw_vio_1 window. For example, the frequencies, ROM addresses, and start signals are selected (Figure 1-16).

   Note: The ROM address values for the Si5368 and Si570 devices (i.e., Si5368 ROM Addr and Si570 ROM Addr) are preset to 19 to produce an output frequency of 125.000 MHz. Entering a different ROM address changes the reference clock(s) frequency. The complete list of pre-programmed SuperClock-2 frequencies and their associated ROM addresses is provided in Table 1-2, page 24.

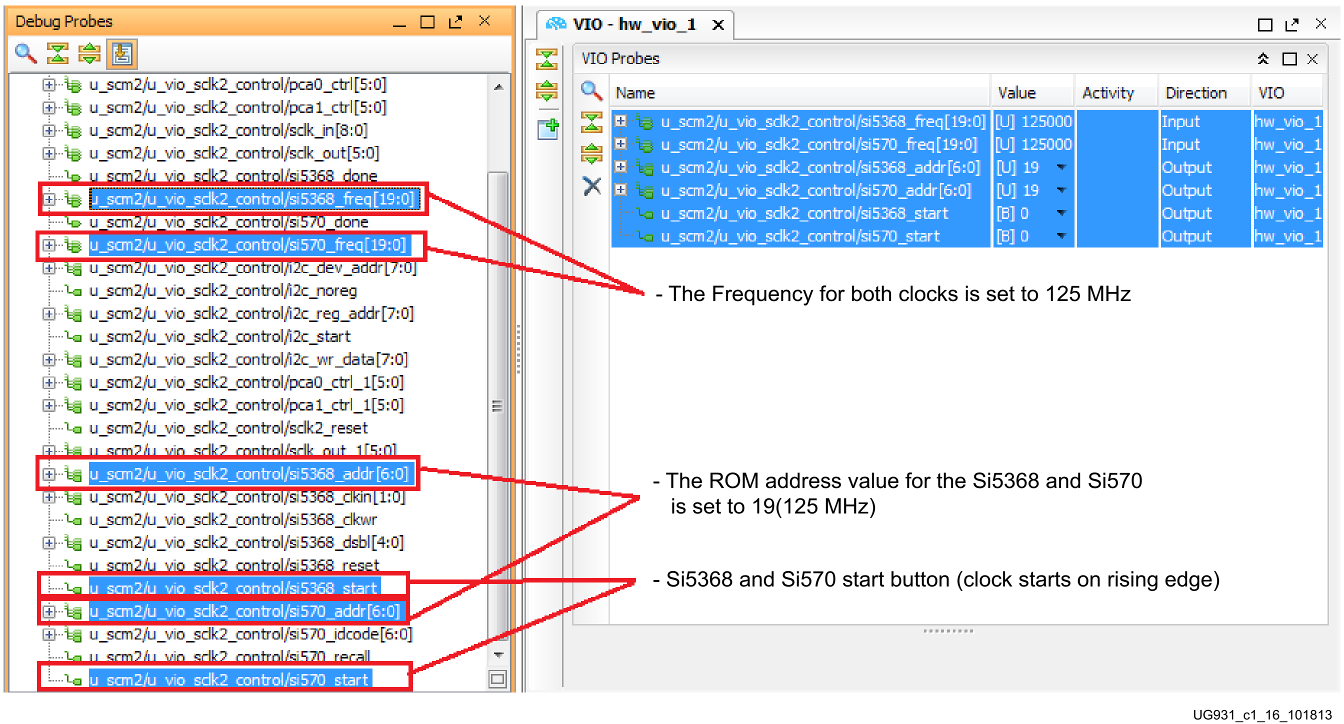


Figure 1-16: **SuperClock-2 Module VIO Core**

5. To view the GTX transceiver operation, click **Layout** > **Serial I/O Analyzer**. From the top of the Hardware Manager window, select **Auto-Detect Links** to display all available links automatically. Links can also be created manually in the Links window by right-clicking and selecting **Create Links,** or by clicking the Create Links button (Figure 1-17).

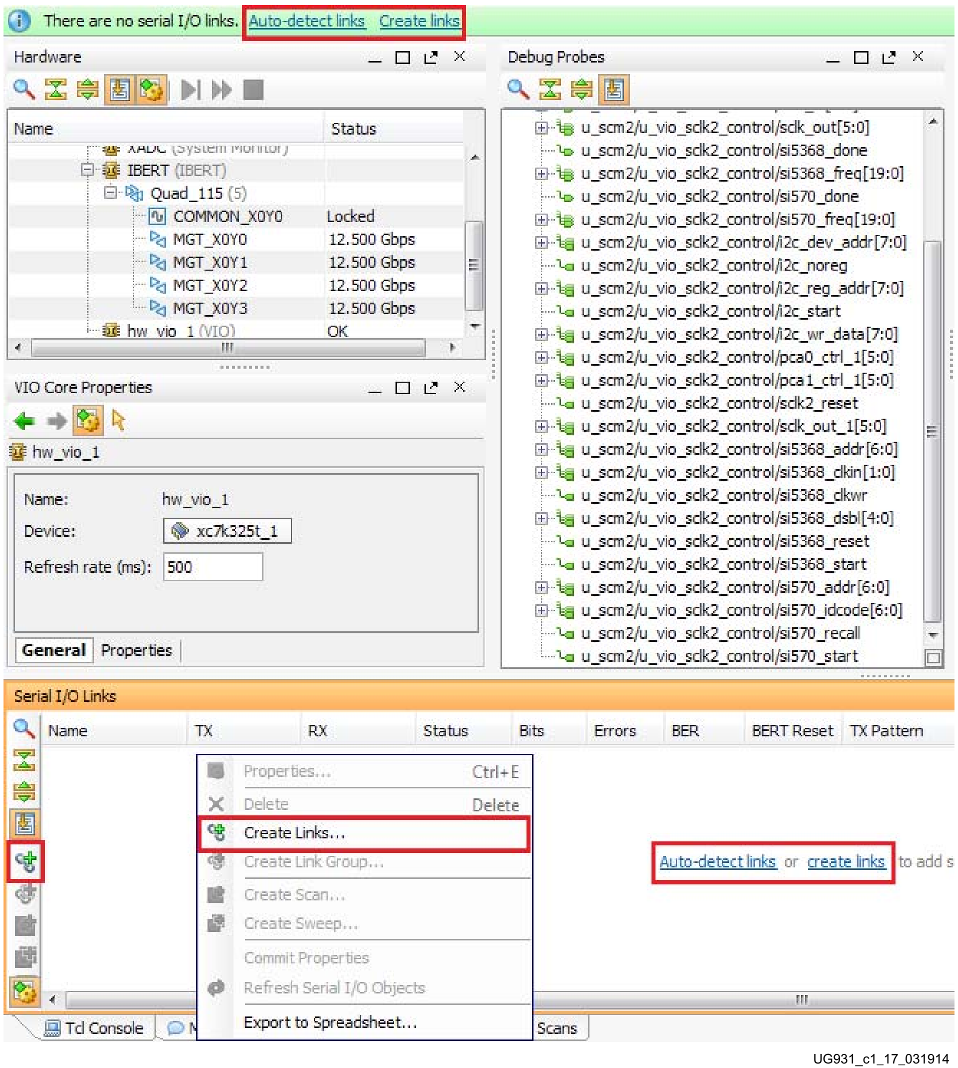


Figure 1-17: **Serial I/O Analyzer - Create Links**

6. If links are created manually, the Create Links window is displayed. The options in this window are used to link any TX GT to any RX GT. To create links, select the TX GT and RX GT from the two lists then click the Add (+) button. For this project, connect the following links (Figure 1-18):
   - MGT_X0Y0/TX to MGT_X0Y0/RX
   - MGT_X0Y1/TX to MGT_X0Y1/RX
   - MGT_X0Y2/TX to MGT_X0Y2/RX
   - MGT_X0Y3/TX to MGT_X0Y3/RX

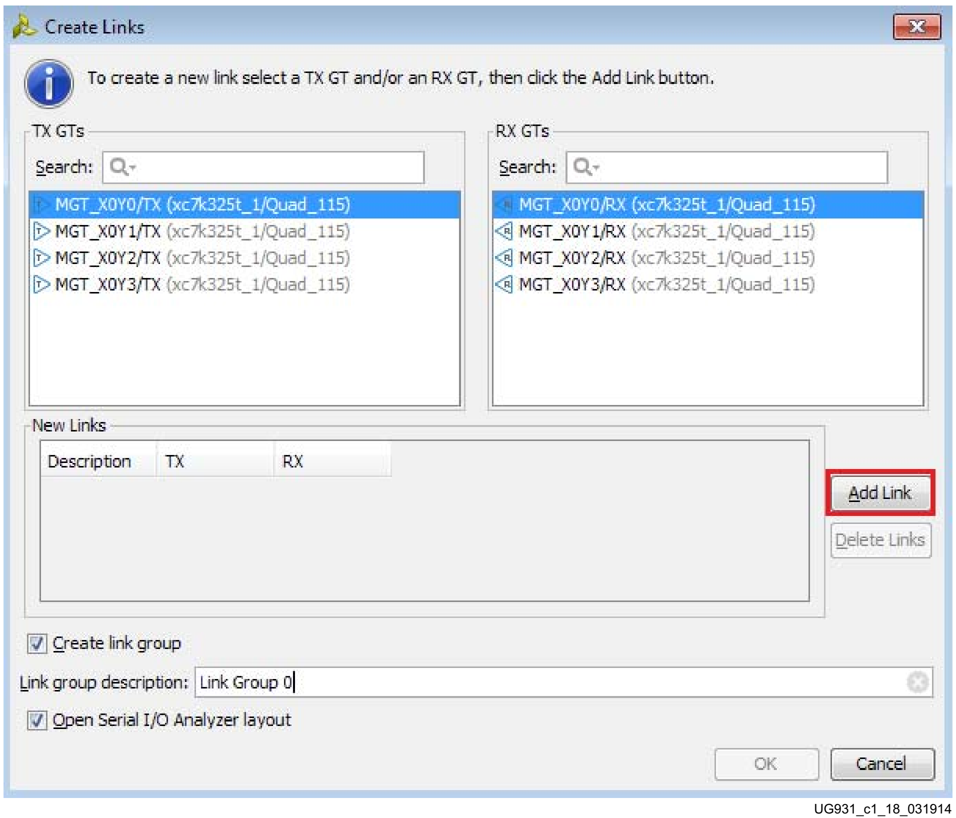


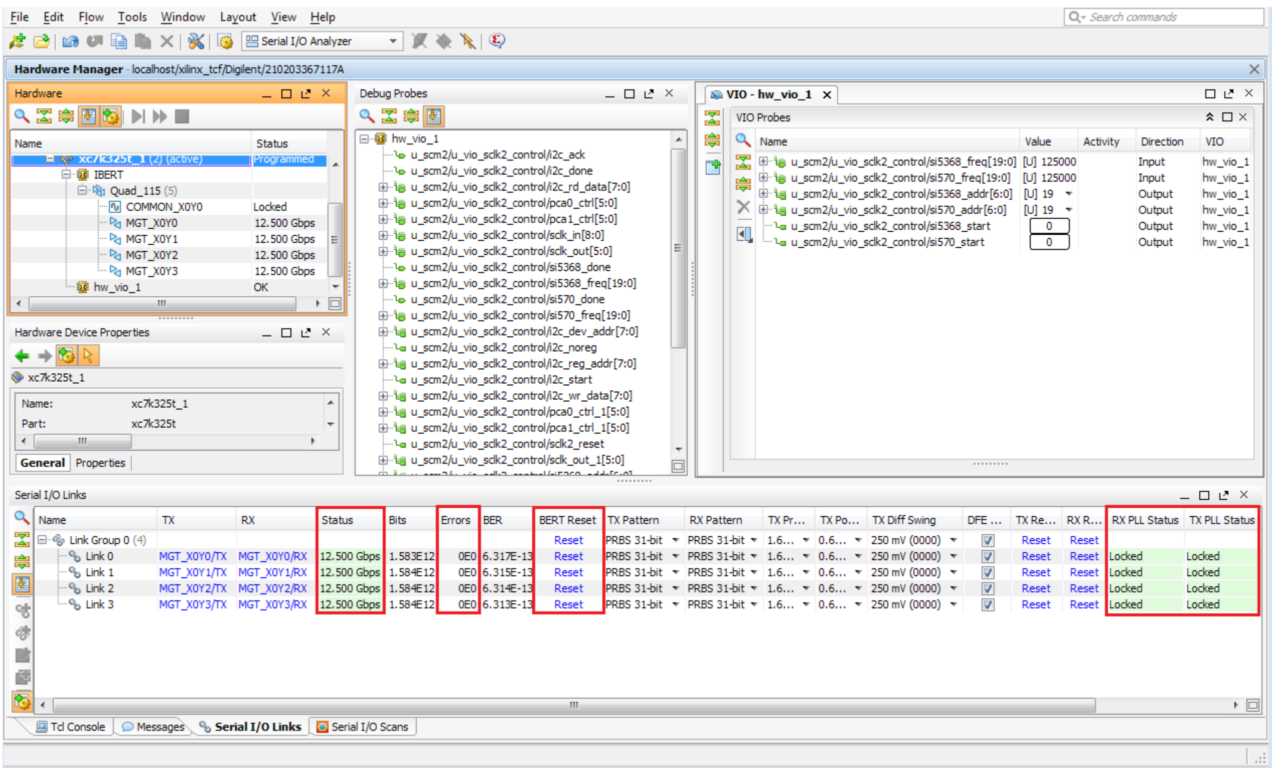
Figure 1-18: **Create Links Window**

Viewing GTX Transceiver Operation

After completing step 6 in Starting the SuperClock-2 Module, the IBERT demonstration is configured and running. The status and test settings are displayed on the **Links** tab in the Links window shown in Figure 1-19.

Note the line rate, TX differential output swing, and RX bit error count:

- The line rate for all four GTX transceivers is 12.5 Gb/s (see **MGT Link Status** in Figure 1-19).
- The GTX transmitter differential output swing is preset to 250 mV.
- Verify that there are no bit errors.



UG931_c1_19_022514

Figure 1-19: **Serial I/O Analyzer Links**

In Case of RX Bit Errors

If there are initial bit errors after linking, or as a result of changing the TX or RX pattern, click the respective BERT **Reset** button to zero the count.

If the **MGT Link Status** shows **No Link** for one or more transceivers, click the respective **TX Reset** button followed by **BERT Reset** (Figure 1-19).

Additional information on the Vivado Design Suite and IBERT core can be found in *Vivado Design Suite User Guide: Programming and Debugging* (UG908) [Ref 3] and in *LogiCORE IP Integrated Bit Error Ratio Tester (IBERT) for 7 Series GTX Transceivers Product Guide for Vivado Design Suite* (PG132) [Ref 4].

Closing the IBERT Demonstration

To stop the IBERT demonstration:

1. Close the Vivado Design Suite by selecting **File** > **Exit**.
2. Place the main power switch SW1 in the off position.

SuperClock-2 Frequency Table

Table 1-2 lists the addresses for the frequencies that are programmed into the SuperClock-2 read-only-memory (ROM).

Table 1-2: **Si570 and Si5368 Frequency Table**

Address	Protocol	Frequency (MHz)	Address	Protocol	Frequency (MHz)	Address	Protocol	Frequency (MHz)
0	100GE/40GE/10 GE	161.130	30	OBSAI	307.200	60	XAUI	156.250
1	Aurora	81.250	31	OBSAI	614.400	61	XAUI	312.500
2	Aurora	162.500	32	OC-48	19.440	62	XAUI	625.000
3	Aurora	325.000	33	OC-48	77.760	63	Generic	66.667
4	Aurora	650.000	34	OC-48	155.520	64	Generic	133.333
5	CE111	173.370	35	OC-48	311.040	65	Generic	166.667
6	CPRI™	61.440	36	OC-48	622.080	66	Generic	266.667
7	CPRI	122.880	37	OTU-1	166.629	67	Generic	333.333
8	CPRI	153.630	38	OTU-1	333.257	68	Generic	533.333
9	CPRI	245.760	39	OTU-1	666.514	69	Generic	644.000
10	CPRI	491.520	40	OTU-1	666.750	70	Generic	666.667
11	Display Port	67.500	41	OTU-2	167.330	71	Generic	205.000
12	Display Port	81.000	42	OTU-2	669.310	72	Generic	210.000
13	Display Port	135.000	43	OTU-3	168.050	73	Generic	215.000
14	Display Port	162.000	44	OTU-4	174.690	74	Generic	220.000
15	Fibrechannel	106.250	45	PCIe®	100.000	75	Generic	225.000
16	Fibrechannel	212.500	46	PCIe	125.000	76	Generic	230.000
17	Fibrechannel	425.000	47	PCIe	250.000	77	Generic	235.000
18	GigE	62.500	48	SATA	75.000	78	Generic	240.000
19	GigE	125.000	49	SATA	150.000	79	Generic	245.000
20	GigE	250.000	50	SATA	300.000	80	Generic	250.000
21	GigE	500.000	51	SATA	600.000	81	Generic	255.000
22	GPON	187.500	52	SDI	74.250	82	Generic	260.000
23	Interlaken	132.813	53	SDI	148.500	83	Generic	265.000
24	Interlaken	195.313	54	SDI	297.000	84	Generic	270.000
25	Interlaken	265.625	55	SDI	594.000	85	Generic	275.000
26	Interlaken	390.625	56	SMPTE435M	167.063	86	Generic	280.000

Table 1-2: **Si570 and Si5368 Frequency Table *(Cont'd)***

Address	Protocol	Frequency (MHz)	Address	Protocol	Frequency (MHz)	Address	Protocol	Frequency (MHz)
27	Interlaken	531.250	57	SMPTE435M	334.125	87	Generic	285.000
28	OBSAI	76.800	58	SMPTE435M	668.250	88	Generic	290.000
29	OBSAI	153.600	59	XAUI	78.125	89	Generic	295.000
90	Generic	300.000	103	Generic	365.000	116	Generic	430.000
91	Generic	305.000	104	Generic	370.000	117	Generic	435.000
92	Generic	310.000	105	Generic	375.000	118	Generic	440.000
93	Generic	315.000	106	Generic	380.000	119	Generic	445.000
94	Generic	320.000	107	Generic	385.000	120	Generic	450.000
95	Generic	325.000	108	Generic	390.000	121	Generic	455.000
96	Generic	330.000	109	Generic	395.000	122	Generic	460.000
97	Generic	335.000	110	Generic	400.000	123	Generic	465.000
98	Generic	340.000	111	Generic	405.000	124	Generic	470.000
99	Generic	345.000	112	Generic	410.000	125	Generic	475.000
100	Generic	350.000	113	Generic	415.000	126	Generic	480.000
101	Generic	355.000	114	Generic	420.000	127	Generic	485.000
102	Generic	360.000	115	Generic	425.000			

Creating the GTX IBERT Core

The Vivado Design Suite 2014.1 is required to rebuild the designs shown here.

This section provides a procedure to create a single Quad GTX IBERT core with integrated SuperClock-2 controller. The procedure assumes Quad 115 and 12.5 Gb/s line rate, but cores for any of the GTX Quads with any supported line rate can be created following the same series of steps.

For more details on generating IBERT cores, see *Vivado Design Suite User Guide: Programming and Debugging* (UG908) [Ref 3].

1. Start the Vivado Design Suite.
2. In the Vivado Design Suite window, click **Manage IP** (highlighted in Figure 1-20) and select **New IP Location**.

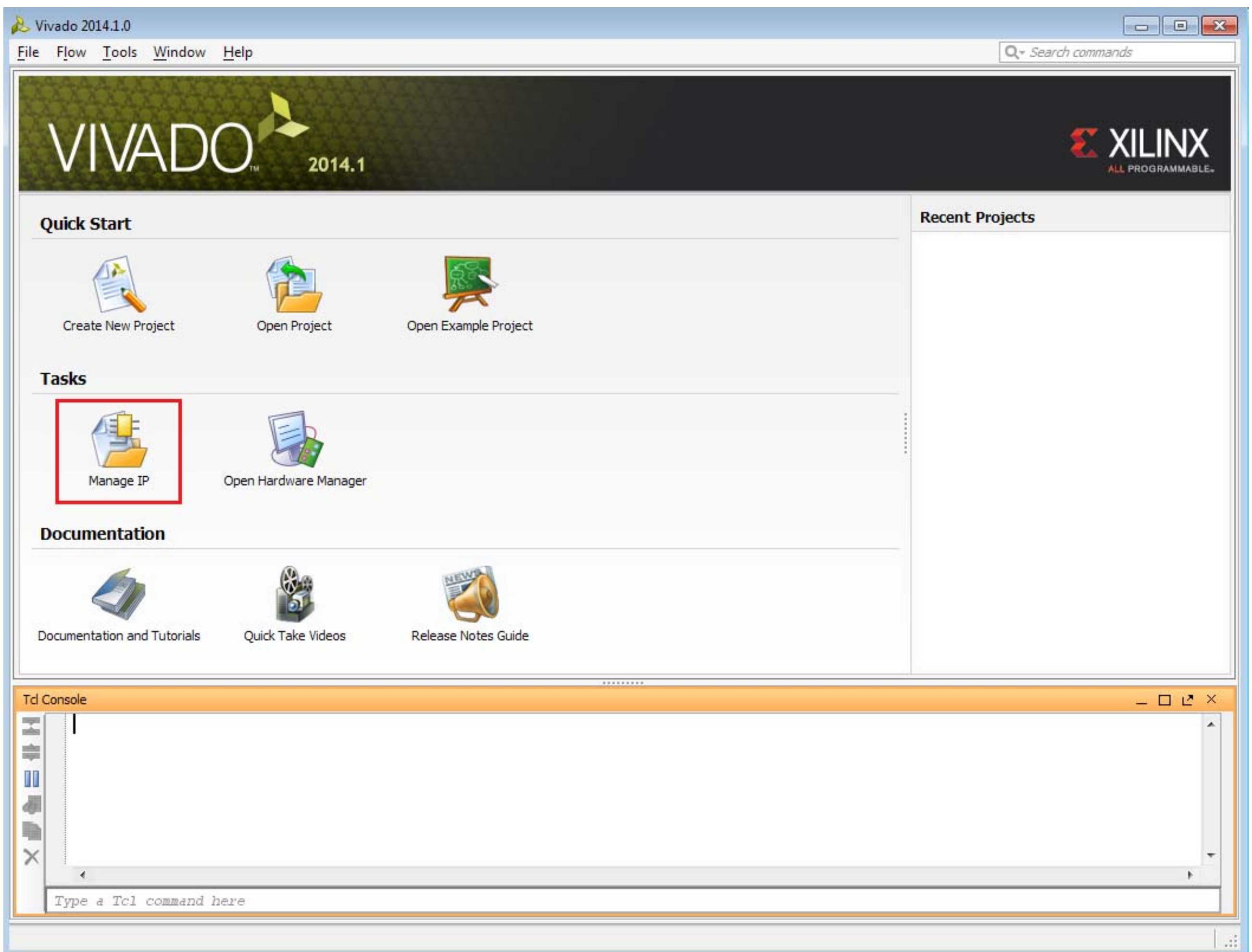


Figure 1-20: **Vivado Design Suite Initial Window**

3. When the Create a New Customized IP Location dialog window opens (not shown), click **Next**.
4. In the Manage IP Settings window, select a part by clicking the (...) button next to the Part field. A Select Device window is displayed. Use the drop-down menu items to narrow the choices. Select the **xc7k325tffg900-3** device (Figure 1-21). Click **OK**.

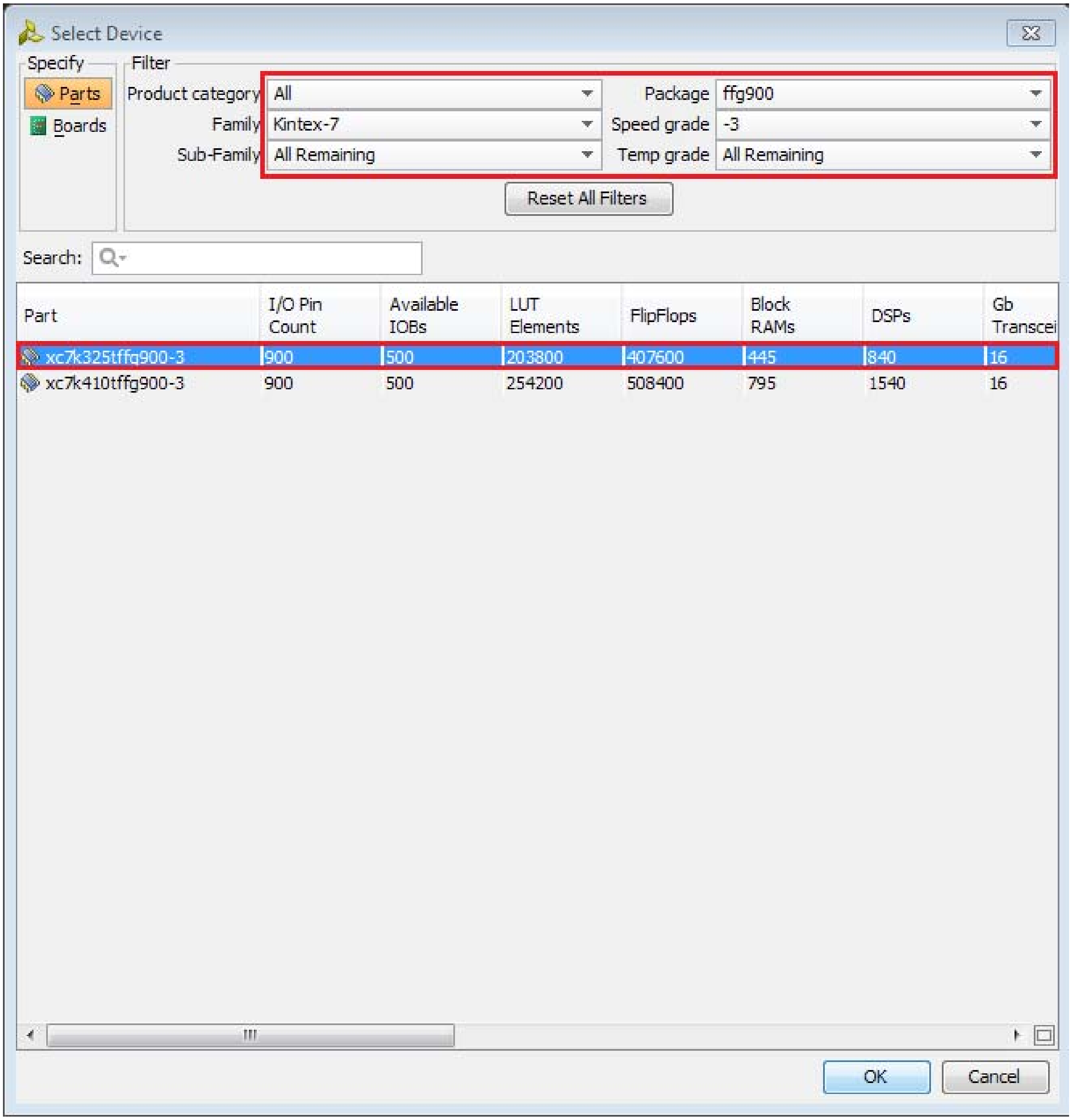


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Figure 1-21: **Select Device**

5. Back on the Manage IP Catalog window, select **Verilog** for Target language, **Vivado Simulator** for Target simulator, **Mixed** for Simulator language, and a directory to save the customized IP (Figure 1-22). Click **Finish.**

   Note: Make sure the directory name does not include spaces.

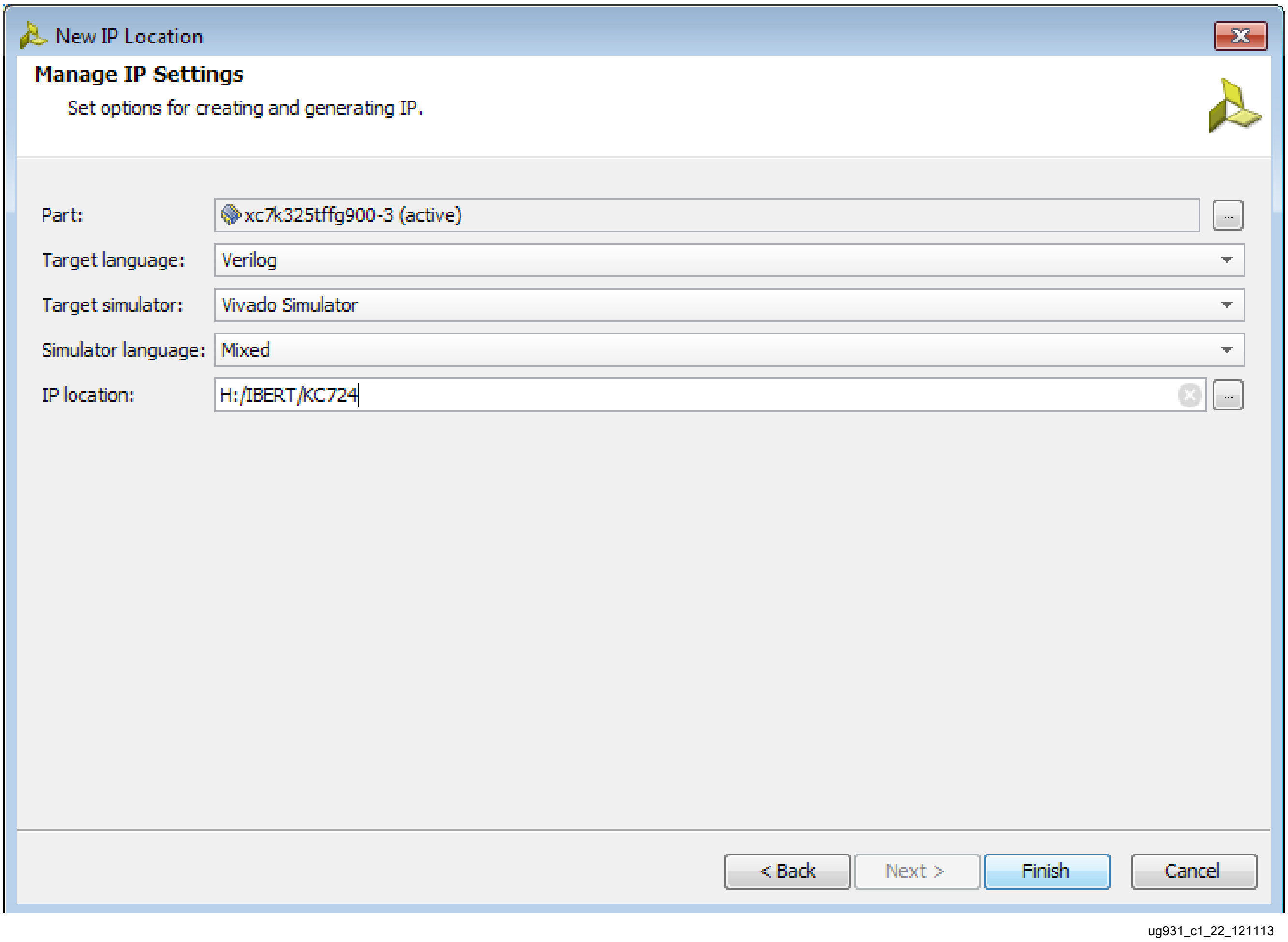


Figure 1-22: **Manage IP Settings**

6. In the IP Catalog window, open the **Debug & Verification** folder, open the **Debug** folder, and double-click **IBERT 7 Series GTX** (Figure 1-23).

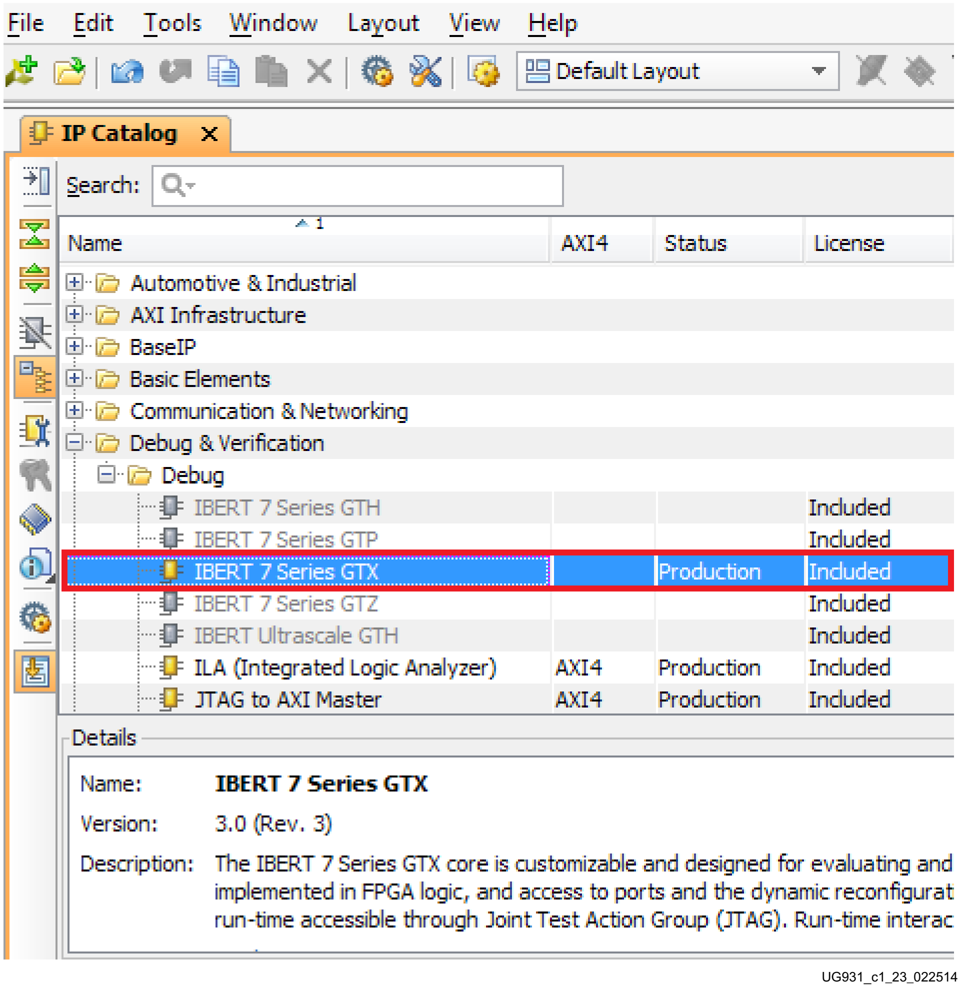
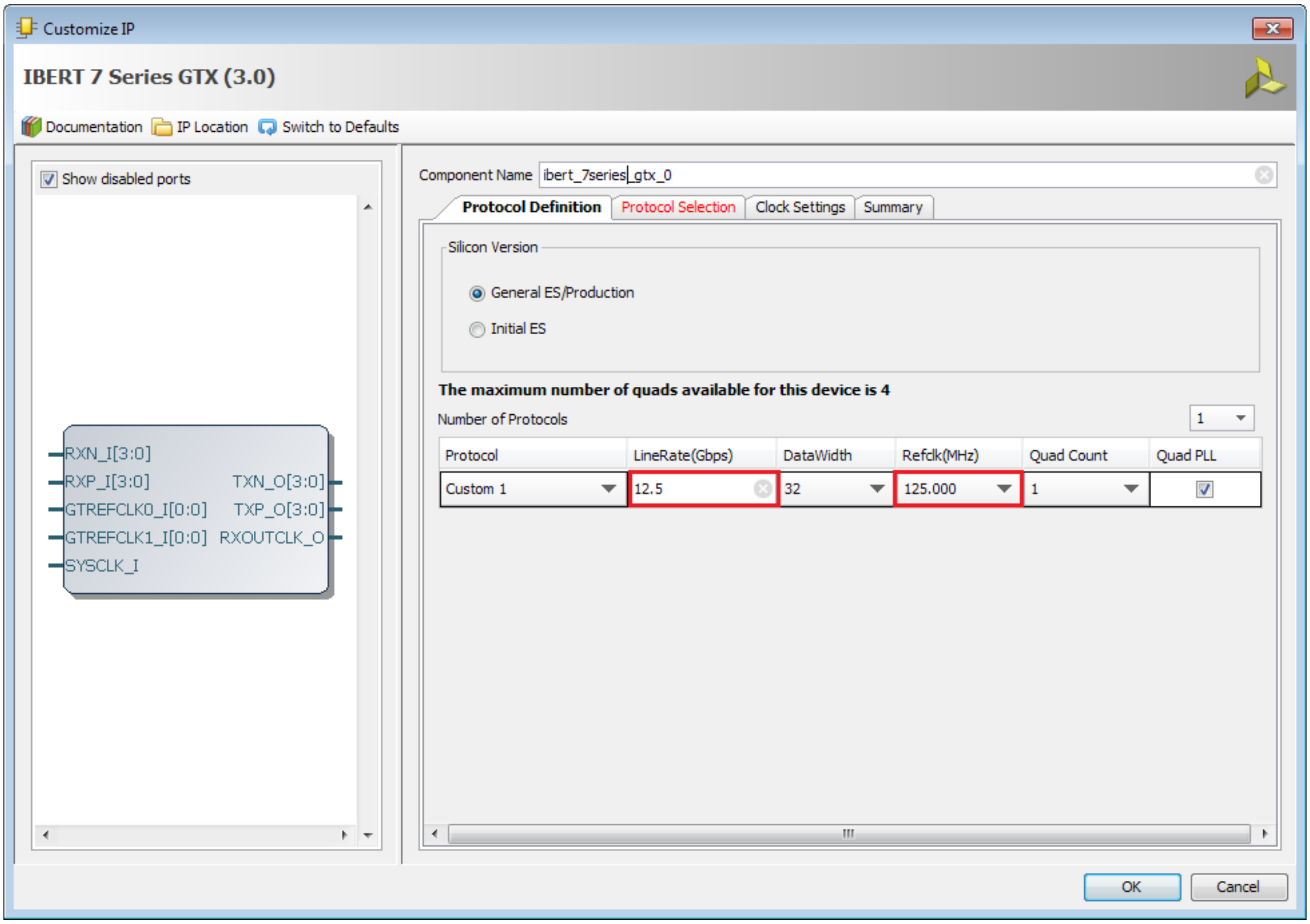


Figure 1-23: **IP Catalog**

7. A Customize IP window opens. In the **Protocol Definition** tab, change LineRate(Gb/s) to **12.5** and change Refclk (MHz) to **125.00**. Keep defaults for other fields (Figure 1-24).



ug931_c1_24_121113

Figure 1-24: **Customize IP - Protocol Definition**

8. In the **Protocol Selection** tab, use the Protocol Selected drop-down menu next to QUAD_115 to select **Custom 1 / 12.5 Gbps** (Figure 1-25).

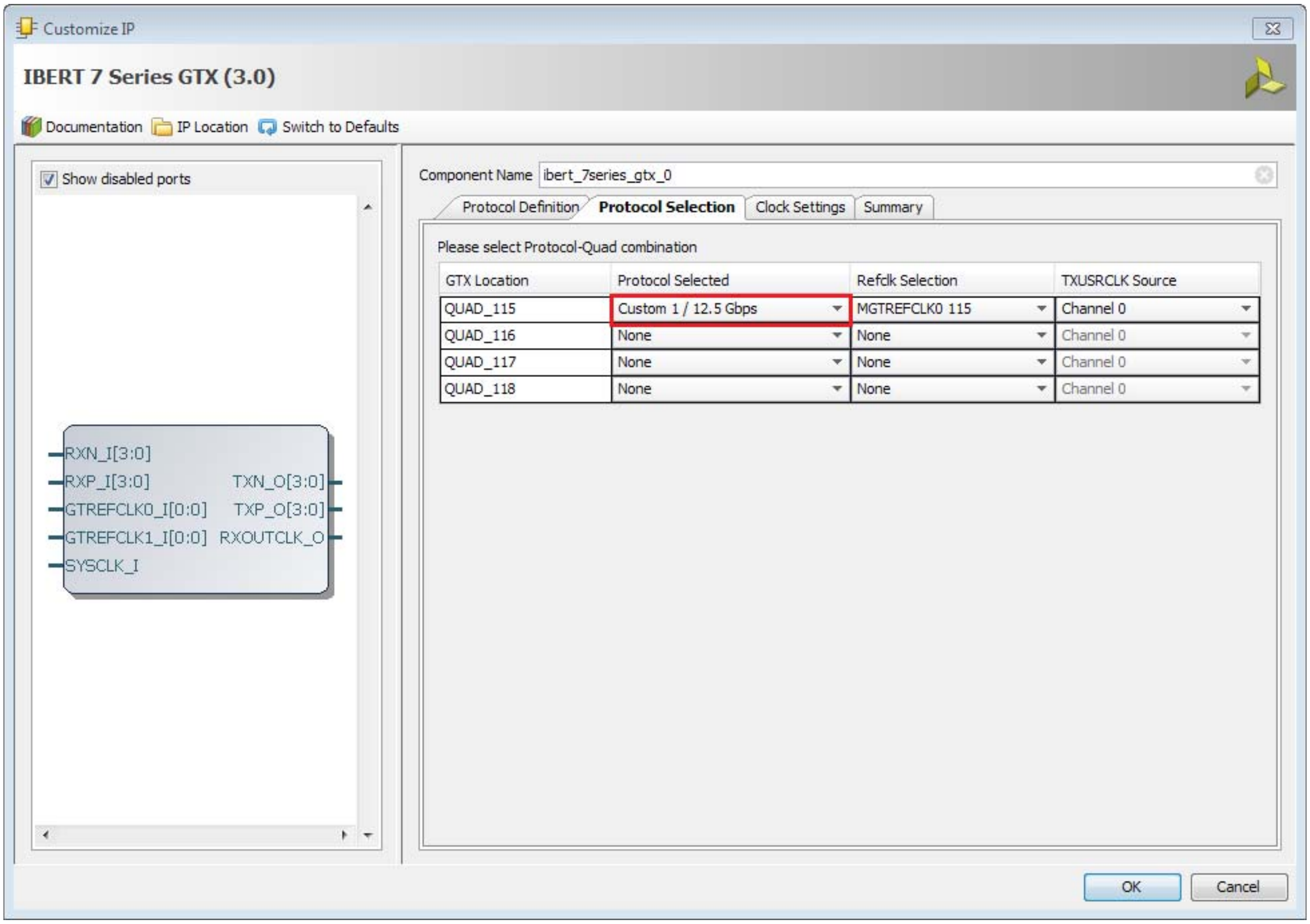


Figure 1-25: **Customize IP - Protocol Selection**

9. In the **Clock Settings** tab, select **DIFF SSTL15** for the I/O Standard, enter **C25** for the P Package Pin, enter **B25** for the N Package Pin (the FPGA pins that the system clock connects to), and make sure the Frequency (MHz) is set to **200.00** (Figure 1-26). Click **OK**. Click **Generate** in the next window to generate the output products.

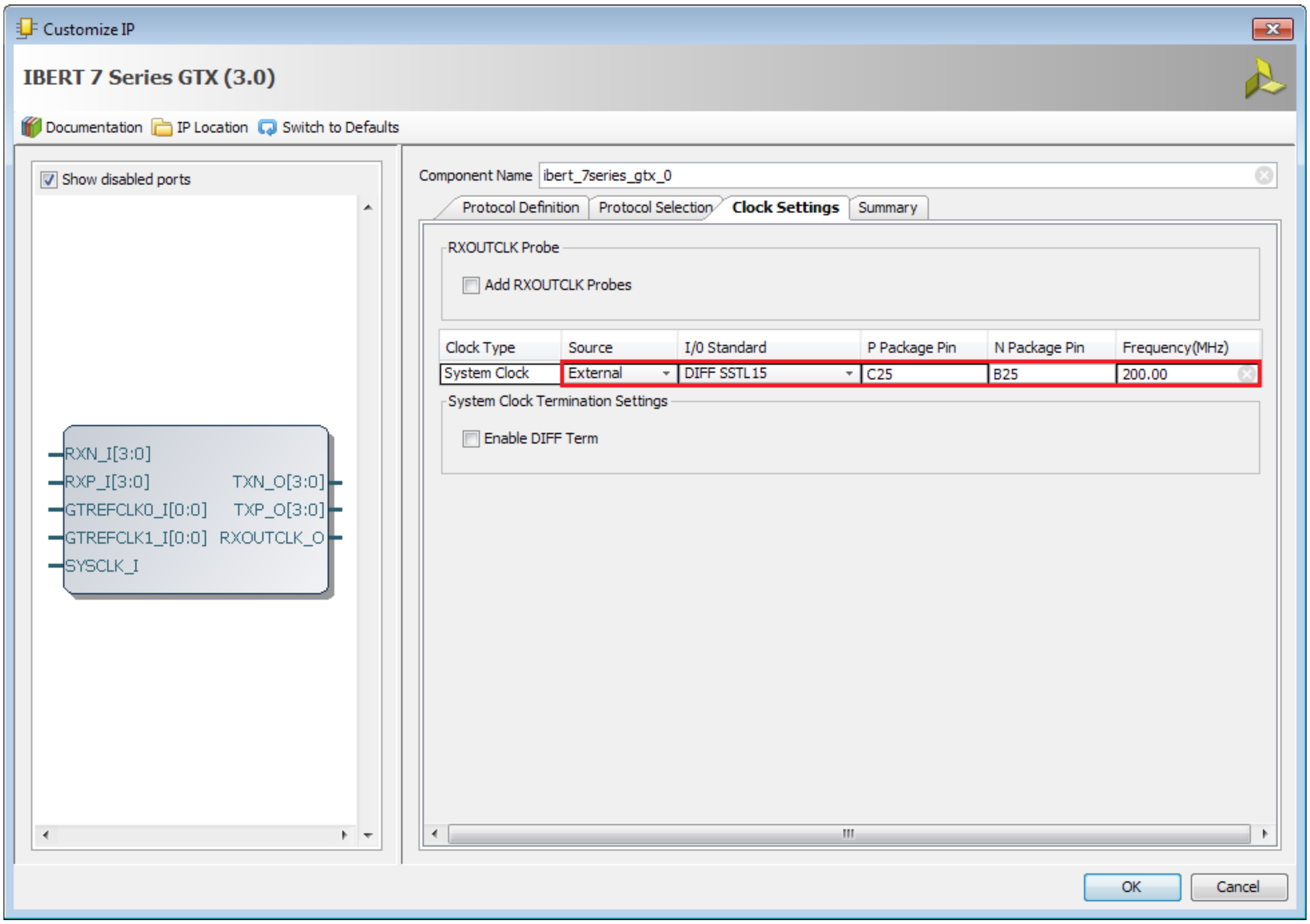


Figure 1-26: **Customize IP - Clock Settings**

10. Back on the Manage IP Catalog window, in the Sources window, right-click the **IBERT IP** and select **Open IP Example Design** (Figure 1-27). Specify a location to save the design, click **OK**, and the design opens in a new Vivado Design Suite window.

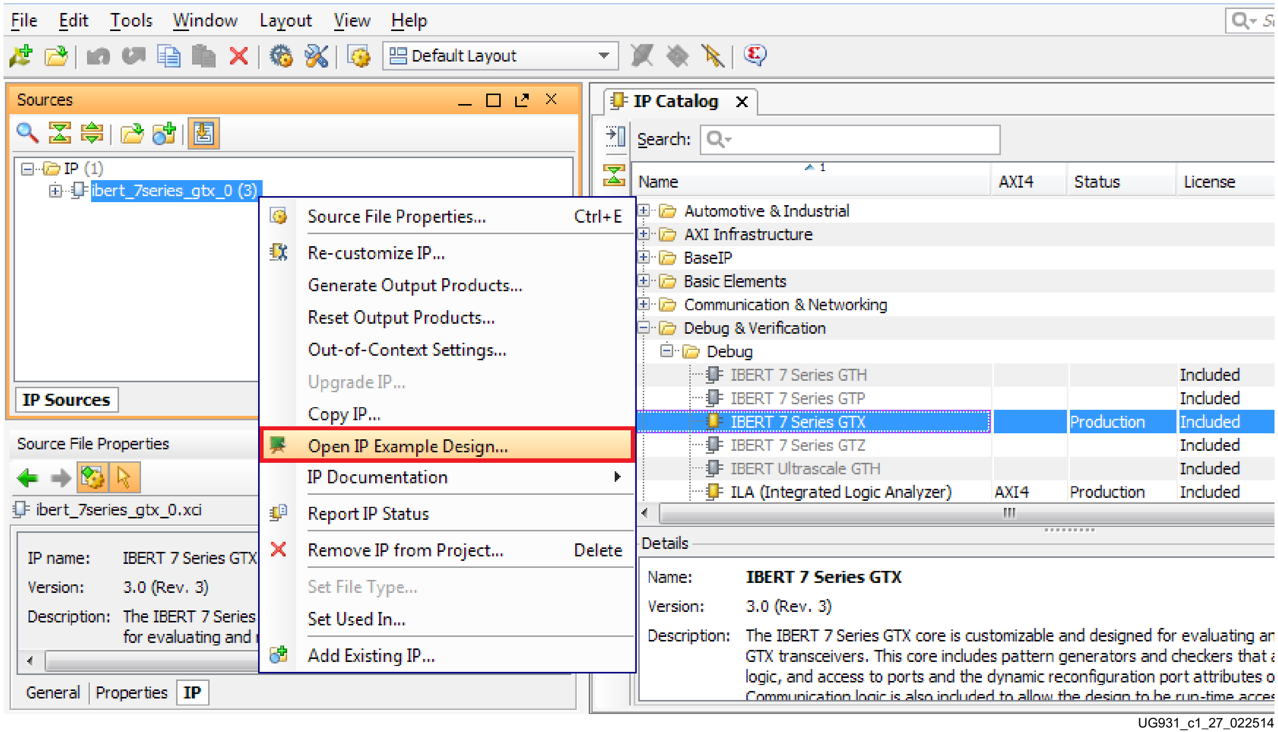


Figure 1-27: **Open IP Example Design**

11. In the new window, select **Tools** > **Run Tcl Script.** In the Run Script window, navigate to `add_scm2.tcl` in the extracted files and click **OK**. The SuperClock-2 Module Design Sources and Constraints are automatically added to the example design (Figure 1-28).

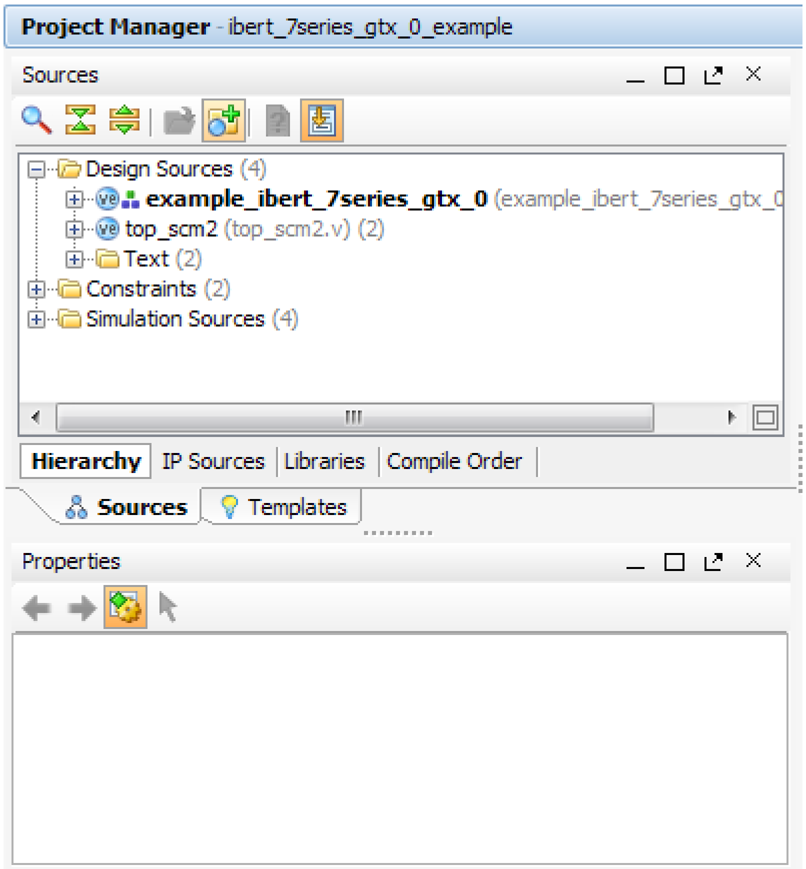


Figure 1-28: **Sources after Running add_scm2.tcl**

12. The SuperClock-2 source code needs to be added to the example IBERT wrapper. Double-click `ibert_7series_gtx_0.v` in Design Sources to open the Verilog code of the example. Add the top-level ports from `top_scm2.v` to the module declaration and instantiate the `top_scm2` module in the example IBERT wrapper (Figure 1-29). The code is also available in `scm2_merge_source.txt`. Click **File** > **Save File**.

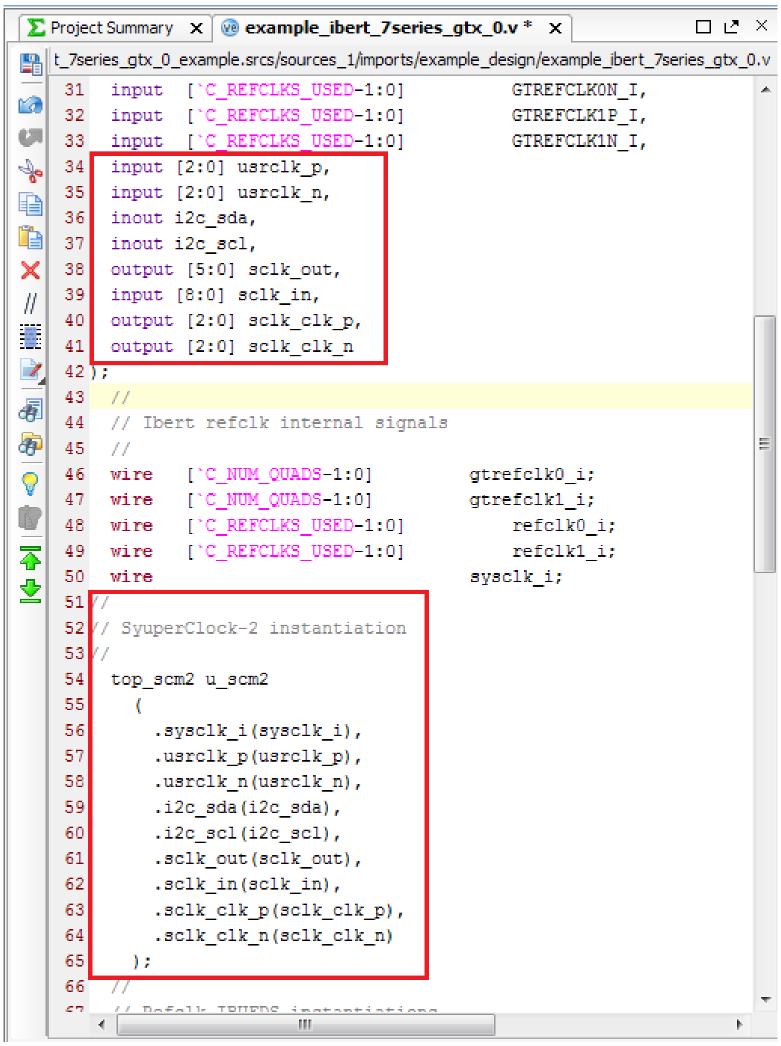


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Figure 1-29: **SuperClock-2 in the Example IBERT Wrapper**

13. In the Sources window, Design Sources should now reflect that the SuperClock-2 module is part of the example IBERT design.

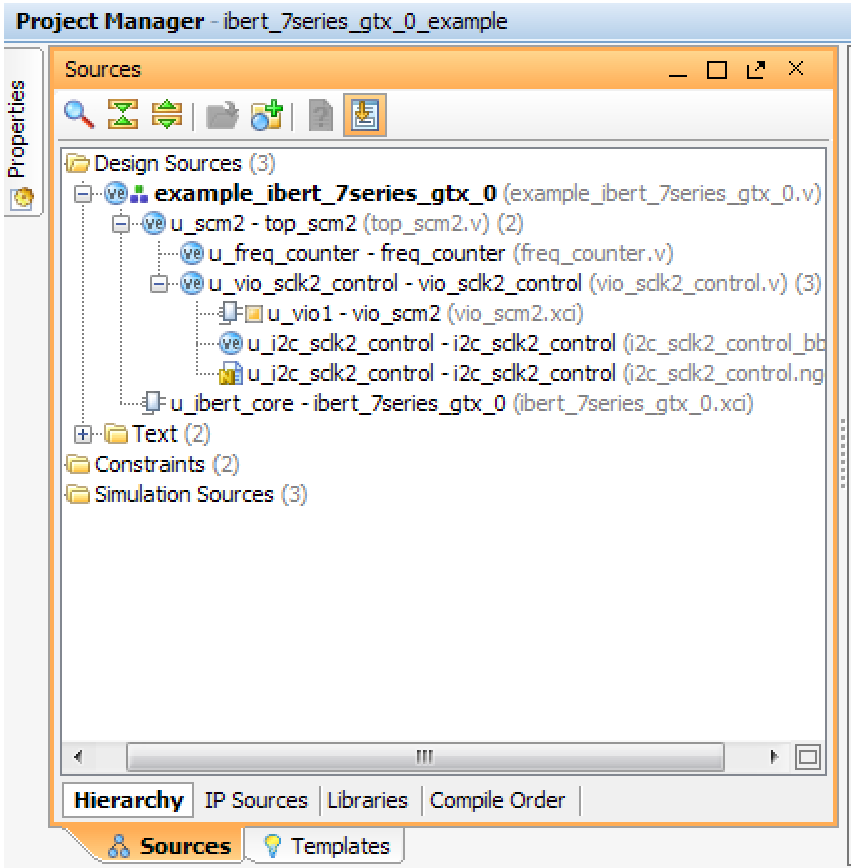

Figure 1-30: **Design Sources File Hierarchy**

14. Click **Run Synthesis** in the Flow Navigator to synthesize the design.

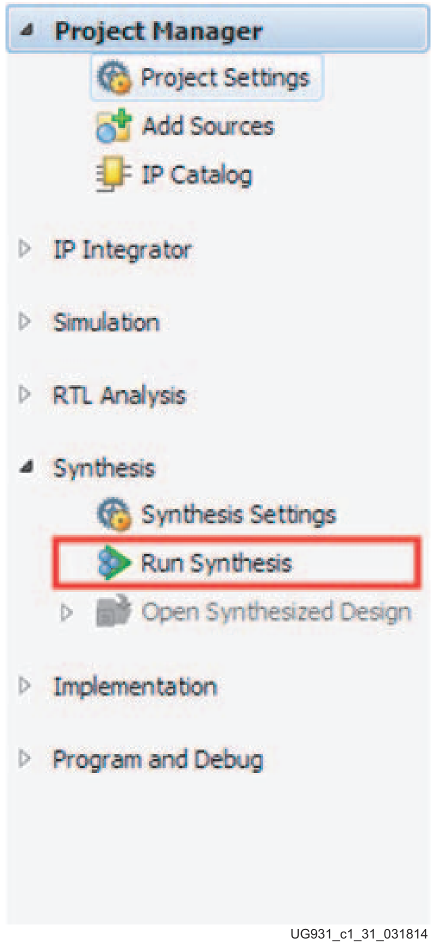

Figure 1-31: **Run Synthesis**

15. When the synthesis is done a Synthesis Completed window opens. Select **Open Synthesized Design** and click **OK** (Figure 1-32).

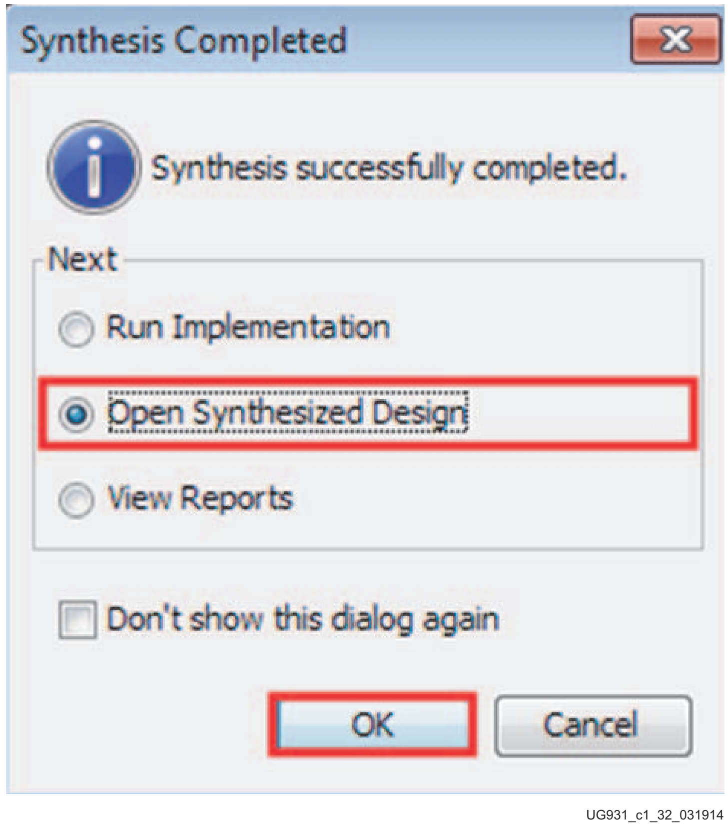

Figure 1-32: **Synthesis Completed**

16. When the Synthesized Design opens, select **dbg_hub** in the Netlist window, and then select the **Debug Core Options** tab in the Cell Properties window and change C_USER_SCAN_CHAIN* to **2** (Figure 1-33). Click **File** > **Save File Constraints**.

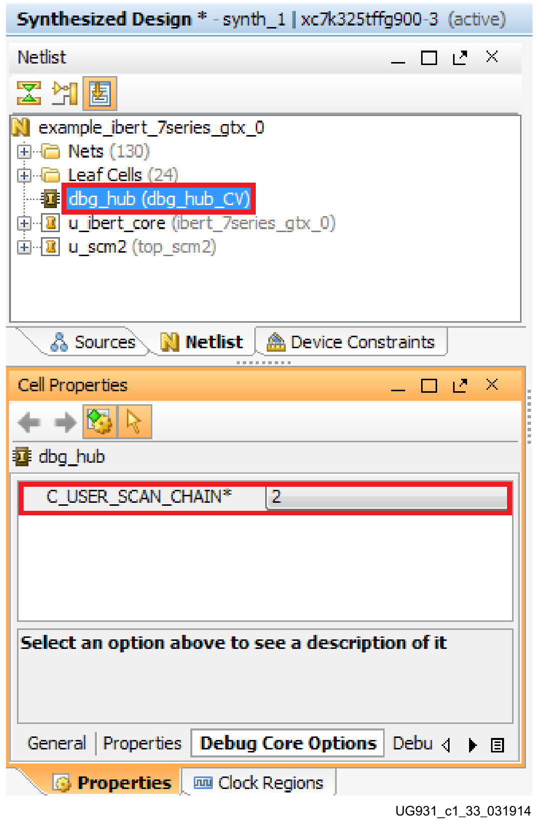

Figure 1-33: **Debug Core Options for dbg_hub**

17. In the Program Manager window under Program and Debug, click **Generate Bitstream**. A window pops up asking if it is Okay to launch implementation. Click **Yes**.

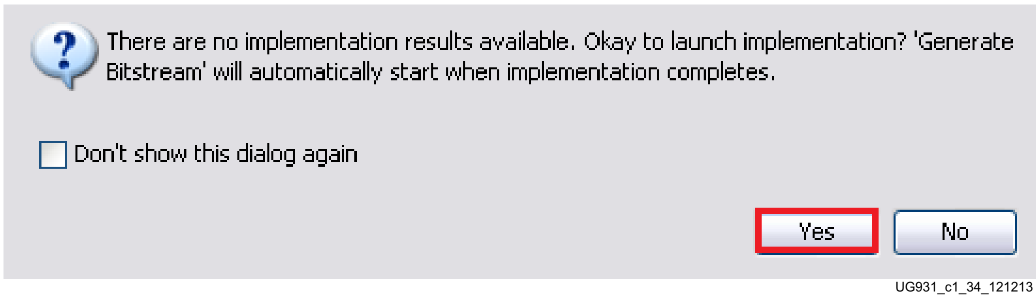

Figure 1-34: **Generate Bitstream**

18. When the Bitstream Generation Completed dialog window appears, click **Cancel** (Figure 1-35).

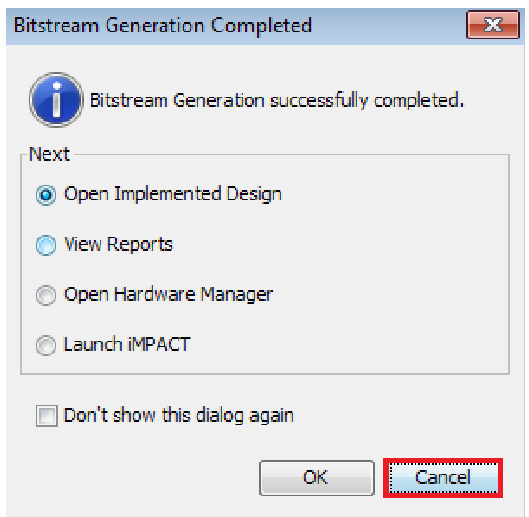

Figure 1-35: **Bitstream Generation Completed**

19. Navigate to the `..\ibert_7series_gtx_0\ibert_7series_gtx_0_example\ibert_7series_gtx_0_example.runs\impl_1` directory to locate the generated bitstream.

Appendix A

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website.

For continual updates, add the Answer Record to your myAlerts.

For definitions and terms, see the Xilinx Glossary.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

The most up to date information related to the KC724 board and its documentation is available on these websites:

Kintex-7 FPGA KC724 Characterization Kit

Kintex-7 FPGA KC724 Characterization Kit documentation

Kintex-7 FPGA KC724 Characterization Kit Answer Record (AR 43390)

These documents provide supplemental material useful with this guide:

1. *KC724 Kintex-7 FPGA GTX Transceiver Characterization Board User Guide* (UG932)
2. *HW-CLK-101-SCLK2 SuperClock-2 Module User Guide* (UG770)
3. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
4. *LogiCORE IP Integrated Bit Error Ratio Tester (IBERT) for 7 Series GTX Transceivers Product Guide for Vivado Design Suite* (PG132)

Appendix B

Warranty

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