KC724 IBERT
Getting Started Guide
(ISE Design Suite 14.3)

UG930 (v1.0) October 23, 2012

This document applies to the following software versions: ISE Design Suite 14.3 and 14.4
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Revision History
The following table shows the revision history for this document.

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<td>Initial Xilinx release.</td>
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Overview

This document provides a procedure for setting up the KC724 Kintex™-7 FPGA GTX Transceiver Characterization Board to run the Integrated Bit Error Ratio Test (IBERT) demonstration using the ISE Design Suite. The designs that are required to run the IBERT demonstration are stored in a Secure Digital (SD) memory card that is provided with the KC724 board. The demonstration shows the capabilities of the Kintex-7 XC7K325T FPGA GTX transceiver.

The KC724 board is described in detail in UG932, KC724 Kintex-7 FPGA GTX Transceiver Characterization Board User Guide.

The IBERT demonstrations operate one GTX Quad at a time. The procedure consists of:

1. Setting Up the KC724 Board.
2. Extracting the Project Files.
3. Connecting the GTX Transceivers and Reference Clocks.
4. Configuring the FPGA.
5. Setting Up the ChipScope Pro Software.
7. Closing the IBERT Demonstration.
Requirements

The hardware and software required to run the GTX IBERT demonstrations are:

- KC724 Kintex-7 FPGA GTX Transceiver Characterization Board including:
  - One SD card containing the IBERT demonstration designs
  - One Samtec BullsEye cable
  - Eight SMA female-to-female (F-F) adapters
  - Six 50Ω SMA terminators
  - GTX transceiver power supply module (installed on board)
  - SuperClock-2 module, Rev 1.0 (installed on board)
  - Active BGA Heatsink (installed on FPGA)
  - 12V DC power adapter
  - USB cable, standard-A plug to micro-B plug
- Host PC with:
  - SD card reader
  - USB ports
  - Xilinx® ChipScope™ Pro software, version 14.3 or higher. Software is available at: [http://www.xilinx.com/chipscopepro](http://www.xilinx.com/chipscopepro)

The hardware and software required to rebuild the IBERT demonstration designs are:

- Xilinx ISE® Design Suite version 14.3 or higher
- PC with a version of the Windows operating system supported by Xilinx ISE Design Suite

Setting Up the KC724 Board

This section describes how to set up the KC724 board.

**Caution!** The KC724 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

When the KC724 board ships from the factory, it is configured for the GTX IBERT demonstrations described in this document. If the board has been re-configured it must be returned to the default set-up before running the IBERT demonstrations.

1. Move all jumpers and switches to their default positions. The default jumper and switch positions are listed in [UG932, KC724 Kintex-7 FPGA GTX Transceiver Characterization Board User Guide](http://www.xilinx.com).
2. Install the GTX transceiver power module by plugging it into connectors J66 and J97.
3. Install the SuperClock-2 module:
   a. Align the three metal standoffs on the bottom side of the module with the three mounting holes in the SUPERCLOCK-2 MODULE interface of the KC724 board.
   b. Using three 4-40 x 0.25 inch screws, firmly screw down the module from the bottom of the KC724 board.
   c. On the SuperClock-2 module, place a jumper across pins 2–3 (2V5) of the CONTROL VOLTAGE header, J18, and place another jumper across Si570 INH header J11.
d. Screw down a 50Ω SMA terminator onto each of the six unused Si5368 clock output SMA connectors: J7, J8, J12, J15, J16 and J17.

Extracting the Project Files

The ChipScope Pro Software .cpj project files for the IBERT demonstrations are located in kc724_cpj.zip on the SD card provided with the KC724 board. They are also available online along with .bit files for all four designs (as collection rdf0183_<ISE version>.zip) at:

http://www.xilinx.com/kc724

kc724_cpj.zip contains four project files: kc724_q115.cpj, kc724_q116.cpj, kc724_q117.cpj, and kc724_q118.cpj. These files are used to load pre-saved MGT/IBERT and SuperClock-2 module control settings for the GTX demonstrations.

To copy the files from the Secure Digital memory card:

1. Connect the Secure Digital memory card to the host computer.
2. Locate the file kc724_cpj.zip on the Secure Digital memory card.
3. Unzip the files to a working directory on the host computer.

Running the GTX IBERT Demonstration

The GTX IBERT demonstration operates one GTX Quad at a time. This section describes how to test GTX Quad 115. The remaining GTX Quads are tested following a similar series of steps.

Connecting the GTX Transceivers and Reference Clocks

Figure 1-1 shows the locations for GTX transceiver Quads 115, 116, 117, and 118 on the KC724 board.

Note: Figure 1-1 is for reference only and might not reflect the current revision of the board.
All GTX transceiver pins and reference clock pins are routed from the FPGA to a connector pad which interfaces with Samtec BullsEye connectors. **Figure 1-2 A** shows the connector pad. **Figure 1-2 B** shows the connector pinout.
Running the GTX IBERT Demonstration

The SuperClock-2 module provides LVDS clock outputs for the GTX transceiver reference clocks in the IBERT demonstrations. Figure 1-3 shows the locations of the differential clock SMA connectors on the clock module which can be connected to the reference clock cables.

**Note:** The image in Figure 1-3 is for reference only and might not reflect the current revision of the board.

**Figure 1-2: A – GTX Connector Pad. B – GTX Connector Pinout**

The four SMA pairs labeled CLKOUT provide LVDS clock outputs from the Si5368 clock multiplier/jitter attenuator device on the clock module. The SMA pair labeled Si570_CLK provides LVDS clock output from the Si570 programmable oscillator on the clock module.

**Note:** The Si570 oscillator does not support LVDS output on the Rev B and earlier revisions of the SuperClock-2 module.

For the GTX IBERT demonstration, the output clock frequencies are preset to 125.000 MHz. For more information regarding the SuperClock-2 module, refer to [UG770, HW-CLK-101-SCLK2 SuperClock-2 Module User Guide](www.xilinx.com).

**Attach the GTX Quad Connector**

Before connecting the BullsEye cable assembly to the board, firmly secure the blue elastomer seal provided with the cable assembly to the bottom of the connector housing if
it isn’t already inserted (see Figure 1-4).

**Note:** Figure 1-4 is for reference only and might not reflect the current version of the connector.

![BullsEye Connector with Elastomer Seal](image1.png)

**Figure 1-4:** BullsEye Connector with Elastomer Seal

Attach the Samtec BullsEye connector to GTX Quad 115 (Figure 1-5), aligning the two indexing pins on the bottom of the connector with the guide holes on the board. Hold the connector flush with the board and fasten it by tightening the two captive screws.

![BullsEye Connector Attached to Quad 115](image2.png)

**Figure 1-5:** BullsEye Connector Attached to Quad 115

**GTX Transceiver Clock Connections**

Refer to Figure 1-2, page 9 to identify the P and N coax cables that are connected to the CLK1 reference clock inputs. Connect these cables to the SuperClock-2 Module as follows:

- CLK1_P coax cable → SMA connector J5 (CLKOUT1_P) on the SuperClock-2 Module
- CLK1_N coax cable → SMA connector J6 (CLKOUT1_N) on the SuperClock-2 Module

**Note:** Any one of the five differential outputs from the SuperClock-2 Module can be used to source the GTX reference clock. CLKOUT1_P and CLKOUT1_N are used here as an example.
GTX TX/RX Loopback Connections

Refer to Figure 1-2, page 9 to identify the P and N coax cables that are connected to the four receivers (RX0, RX1, RX2 and RX3) and the four transmitters (TX0, TX1, TX2 and TX3). Use eight SMA female-to-female (F-F) adapters (Figure 1-6), to connect the transmit and receive cables as shown in Figure 1-7 and detailed below:

- TX0_P → SMA F-F Adapter → RX0_P
- TX0_N → SMA F-F Adapter → RX0_N
- TX1_P → SMA F-F Adapter → RX1_P
- TX1_N → SMA F-F Adapter → RX1_N
- TX2_P → SMA F-F Adapter → RX2_P
- TX2_N → SMA F-F Adapter → RX2_N
- TX3_P → SMA F-F Adapter → RX3_P
- TX3_N → SMA F-F Adapter → RX3_N
Figure 1-8 shows the KC724 board with the cable connections required for the Quad 115 GTX IBERT demonstration.

Configuring the FPGA

This section describes how to configure the FPGA using the SD card included with the board. The FPGA can also be configured through ChipScope Pro or iMPACT software using the .bit files which are available online (as collection rdf0183_<ISE version>.zip) at:

http://www.xilinx.com/kc724

To configure from the SD card:

1. Insert the SD card provided with the KC724 board into the SD card reader slot located on the bottom-side (upper-right corner) of the board.
2. Plug the 12V output from the power adapter into connector J2.
3. Connect the host computer to the KC724 board using a standard-A plug to micro-B plug USB cable. The standard-A plug connects to a USB port on the host computer and the micro-B plug connects to U8, the Digilent USB JTAG configuration port on the KC724 board.
4. Select the GTX IBERT demonstration with the System ACE SD controller SASD CFG switch, SW8. The setting on this 4-bit DIP switch (Figure 1-9) selects the file used to configure the FPGA. A switch is in the ON position if set to the far right and in the OFF position if set to the far left. For the Quad 115 GTX IBERT demonstration, set ADR2 = ON, ADR1 = ON, and ADR0 = ON. The MODE bit (switch position 4) is not used and can be set either ON or OFF.

![Figure 1-9: Configuration Address DIP Switch (SW8)](image)

There is one IBERT demonstration design for each GTX Quad on the KC724 board, for a total of four IBERT designs. Four other demonstration designs are included that show other board features (the use of these designs are described in the README file within the SD card). All eight designs are organized and stored on the SD card as shown in Table 1-1.

Table 1-1: SD Card Contents and Configuration Addresses

<table>
<thead>
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<th>ADR2</th>
<th>ADR1</th>
<th>ADR0</th>
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<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>GTX Quad 116</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
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<tr>
<td>GTX Quad 117</td>
<td>ON</td>
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<td>ON</td>
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<td>GTX Quad 118</td>
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<td>OFF</td>
</tr>
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<td>ON</td>
<td>ON</td>
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<td>DIP Switches</td>
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<td>ON</td>
<td>OFF</td>
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<tr>
<td>Push Buttons</td>
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<td>ON</td>
</tr>
<tr>
<td>USB/UART</td>
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<td>OFF</td>
<td>OFF</td>
</tr>
</tbody>
</table>

5. Place the main power switch SW1 to the ON position.

Setting Up the ChipScope Pro Software

1. Start the ChipScope Pro analyzer tools on the host computer and select **File → Open Project**.

2. When the Project window opens, navigate to the directory where the ChipScope software project files (.cpj) were extracted. Select `kc724_q115.cpj` and click **Open**.

*Note:* The .cpj file loads pre-saved project settings for the demonstration including MGT/IBERT and clock module control parameters. For more information regarding MGT/IBERT settings, refer to [UG029](https://www.xilinx.com), *ChipScope Pro Software Cores.*
3. Click the **Open Cable** button (Figure 1-10).

4. When the dialog appears asking to set up the core with the settings from the current project, click **Yes** (Figure 1-11).

**Starting the SuperClock-2 Module**

The IBERT demonstration designs use an integrated ChipScope Pro software VIO core to control the clocks on the SuperClock-2 module. The SuperClock-2 module features two clock-source components: 1) An always-on Si570 crystal oscillator and, 2) an Si5368 jitter-attenuating clock multiplier. Outputs from either device can be used to drive the transceiver reference clocks. To start the SuperClock-2 Module:
1. In the Project Panel, click **VIO Console** below **UNIT 1: SCLK2 Control (VIO)** (Figure 1-12).

![Project: kc724_q115](image)

**Figure 1-12: Project Panel - VIO Console (GTX)**

2. The clock sources on the SuperClock-2 module are controlled from the VIO Console. Click on the **Si5368 Start** button (Figure 1-13) to enable the clock output.

**Note:** The ROM address values for the Si5368 and Si570 devices (i.e., Si5368 ROM Addr and Si570 ROM Addr) are preset to 19 to produce an output frequency of 125.000 MHz. Entering a different ROM address changes the reference clock(s) frequency. The complete list of pre-programmed SuperClock-2 frequencies and their associated ROM addresses is provided in Table 1-2, page 19.

![Si5368 Address, Frequency and Start Button](image)

**Figure 1-13: Si5368 Address, Frequency and Start Button**
3. In the project panel, click **IBERT Console** (Figure 1-14) to view GTX transceiver operation.

![Figure 1-14: Project Panel - IBERT Console (GTX)](image)

**Figure 1-14:** Project Panel - IBERT Console (GTX)

### Viewing GTX Transceiver Operation

After completing step 3 in **Starting the SuperClock-2 Module**, the IBERT demonstration is configured and running. The status and test settings are displayed on the **MGT/IBERT Settings** tab in the IBERT Console shown in Figure 1-15.

Note the line rate, TX differential output swing, and RX bit error count:

- The line rate for all four GTX transceivers is 12.5 Gbps (see **MGT Link Status** in Figure 1-15).
- The GTX transmitter differential output swing is preset to 850 mV.
- Verify that there are no bit errors.
Running the GTX IBERT Demonstration

In Case of RX Bit Errors

If the RX Bit Error Count for any transceiver displays a non-zero value, or to simply reset the counter, click the respective BERT Reset button (Figure 1-16) to zero the count.

Figure 1-15: GTX IBERT Console

Figure 1-16: Click BERT Reset Button to Zero a Non-Zero RX Error Count

If the MGT Link Status shows No Link for one or more transceivers click the respective TX Reset button followed by BERT Reset (Figure 1-17).
Closing the IBERT Demonstration

To stop the IBERT demonstration:

1. Close the ChipScope application by selecting File → Exit. **Note:** Do not save changes to the project.

2. Place the main power switch SW1 in the off position.

Additional information on the ChipScope Pro software and IBERT core can be found in:

- **UG029**, ChipScope Pro Software Cores.
- **DS855**, ChipScope Integrated Bit Error Ratio Test (IBERT) for Kintex-7 GTX (v2.00.a)
SuperClock-2 Frequency Table

Table 1-2 lists the addresses for the frequencies that are programmed into the SuperClock-2 read-only-memory (ROM).

**Table 1-2: Si570 and Si5368 Frequency Table**

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<thead>
<tr>
<th>Address</th>
<th>Protocol</th>
<th>Frequency (MHz)</th>
<th>Address</th>
<th>Protocol</th>
<th>Frequency (MHz)</th>
<th>Address</th>
<th>Protocol</th>
<th>Frequency (MHz)</th>
<th>Address</th>
<th>Protocol</th>
<th>Frequency (MHz)</th>
</tr>
</thead>
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<td>161.130</td>
<td>30</td>
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<td>307.200</td>
<td>60</td>
<td>XAUI</td>
<td>156.250</td>
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<td>31</td>
<td>OBSAI</td>
<td>614.400</td>
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<td>XAUI</td>
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Creating the GTX IBERT Core

To rebuild the designs shown here, you must have an installation of ISE Design Suite.
This section provides a procedure to create a single Quad GTX IBERT core using CORE Generator software. The procedure assumes Quad 115 and 12.5 Gb/s line rate, but cores for any of the GTX Quads with any supported line rate can be created following the same series of steps.

For more details on generating IBERT cores, refer to UG029, ChipScope Pro Software Cores.

1. Start the CORE Generator tool from either the ISE Project Navigator window or a command line:
   - From the Project Navigator window, select: Tools → Core Generator...
   - From a command line, enter: coregen

2. In the Core Generator window, click the New Project icon (highlighted in Figure. Figure 1-18).
Creating the GTX IBERT Core

3. When the New Project dialog window opens (not shown), name the project and click **Save**.

4. In the Project Options window, click on **Part** and select the parameters listed here:
   - Family: **Kintex7**
   - Device: **xc7k325t**
   - Package: **ffg900**
   - Speed Grade: **-3**

   Figure 1-19 shows the correct settings.

5. Click **OK** to close the Project Options window.
6. In the IP Catalog pane of the CORE Generator window (Figure 1-20) select:
   **Debug & Verification →
   Debug →
   IBERT 7 Series GTX (ChipScope Pro - IBERT) 2.02.a**

7. Click on the **Customize and Generate** link under the **Actions** heading (Figure 1-20)

8. After a few seconds page 1 of the IP customization window will appear. For Component Name type **ibert_k7_q115** and under Board Configuration Settings select **kc724 scm2** as shown in Figure 1-21, then click **Next**.
9. Enter the information shown here and in Figure 1-22, then click Next:
   - No. of Quads: 1
   - Select Quad: QUAD 115
   - Max Rate (Gbps): 12.5
   - Refclk (MHz): 125.000
   - GT count: 4
10. Enter the information shown here and in Figure 1-23, then click **Next**:

- MGT0_115: **CUSTOM1 / 12.5 Gbps**
- MGT1_115: **CUSTOM1 / 12.5 Gbps**
- MGT2_115: **CUSTOM1 / 12.5 Gbps**
- MGT3_115: **CUSTOM1 / 12.5 Gbps**
11. Enter the information shown here and in Figure 1-24, then click **Next**:
   - MGT0_115: MGTFCLK1 115
   - MGT1_115: MGTFCLK1 115
   - MGT2_115: MGTFCLK1 115
   - MGT3_115: MGTFCLK1 115
12. Verify the information shown in Figure 1-25, then click **Generate**.
13. The generation process will take a few minutes. When complete, a *Readme* window will appear (Figure 1-26).

![Figure 1-26: CORE Generator - Readme](image-url)
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