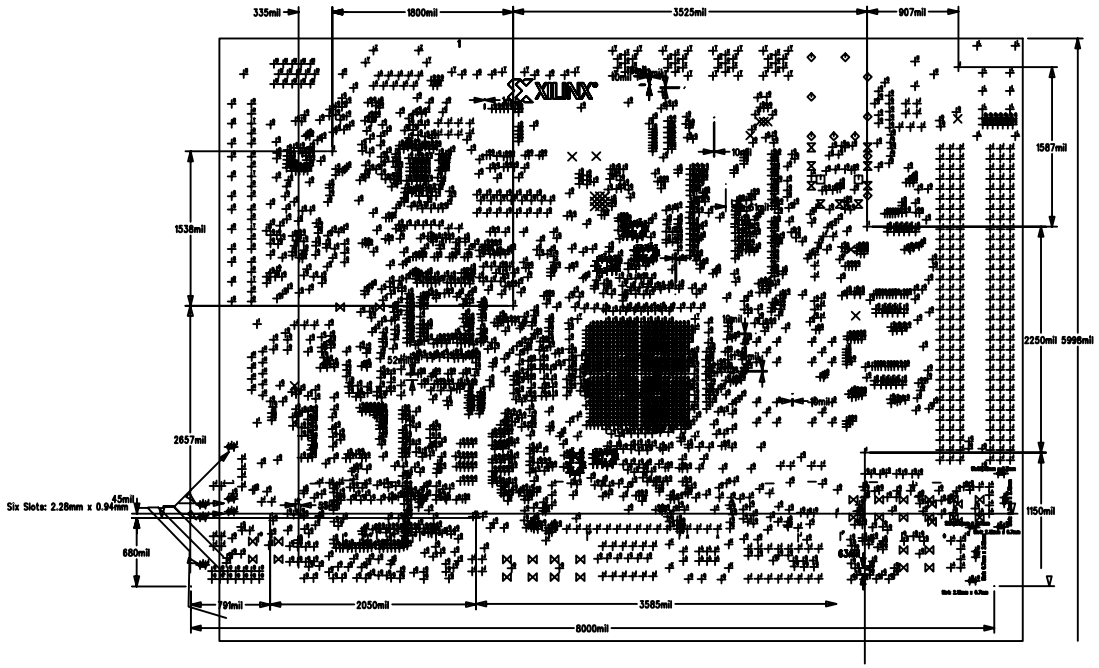
REV	REVISION DESCRIPTION	DATE	DRAWN	APPVD	DATE
	SEE MATRIXONE FOR REVISION HISTORY				
03	REVISE PER ECO-3761	12/6/07	F.PADILLA		



SIZE	QTY	SYM	PLTD
12	29	X	PLTD
61	2	□	PLTD
42	10	◇	PLTD
38	9	⧖	PLTD
40	34	⋈	PLTD
35	48	A	PLTD
27	4	B	NPLTD
27	12	C	PLTD
67	20	D	PLTD
13	32	E	PLTD
18	16	G	PLTD
45	9	H	PLTD
125	11	I	PLTD
37	314	J	PLTD
47	4	K	PLTD
65	10	L	PLTD
43	15	M	PLTD
120	2	N	PLTD
32	14	O	PLTD
157	2	P	PLTD
10	2953	Q	PLTD
51	20	R	PLTD
59	8	S	NPLTD
59	4	T	PLTD
105	2	U	PLTD
93	2	V	PLTD
62	2	W	NPLTD
15.75	134	X	PLTD
63	26	Y	PLTD
128	2	Z	PLTD
27 x 86.61	4	C	PLTD
37 x 90	6	J	PLTD
27 x 86.61	2	B	NPLTD

NOTES: UNLESS OTHERWISE SPECIFIED.

1. APPLICABLE STANDARDS/SPECIFICATIONS:
   FABRICATE BOARD PER IPC-A-600D STANDARD.
2. PRIMARY SIDE SHOWN.
3. MATERIAL: .093 THK. FR-4, NATURAL GREEN, UL94V-0 COMPLIANT,
   START 1/2 OZ COPPER &IGNAL LAYERS. ALL PLANES ARE 1 OZ COPPER.
4. ALL HOLES TO BE PLATED THRU. PLATING IN HOLES TO BE .001 MIN. THICKNESS.
   HOLE SIZES ARE AFTER PLATING. HOLE TOLERANCE +/-.003 EXCEPT VIAS.
   VIA TOLERANCE +.000/-100x OF HOLE DIAMETER.
5. PLATING: GOLD IMMERSION.
6. USE ARTMASTER # ML405
7. FINISHED THICKNESS TO BE +/-.005 OR 5%, WHICHEVER IS GREATER.
8. SILKSCREEN TOP & BOTTOM SIDE WITH WHITE NON-CONDUCTIVE EPOXY INK.
9. FABRICATE PER DIMENTIONS SHOWN. BOARD DIMENSION
   TOLERANCE'S .XX: +/-.01 .XXX: +/-.003.
10. BREAK ALL SHARP EDGES.
11. CONTROL IMPEDANCE SEE CHART BELOW. STACKUP IN EXCEL FORMAT IS PROVIDED.
12. REMOVE ALL UNUSED PADS ON INTERNAL TRACE LAYERS. LAYERS 2, 4, 6, 7, 9 & 11.
13. SIGNAL ENDED IMPEDENCE CONTROL NETS ON TOP LAYER. ADJUST IT EXACTLY 75-OHM
    NETS ARE $16N88,$16N90,& $16N93. ADJUST IT EXACTLY 75-OHM
14. FIVE LOCATIONS (TOTAL TEN COMPONENTS) COMPONENTS ARE PLACED ON COMP & SOLDER SIDE
    SO THAT THERE PTH PINS ARE EXACTLY MATCH IN X &Y LOCATION. TOTAL OF 12x5=60 DRILLS

LAYERS STACK-UP OVER ALL THICKNESS 0.093 +/- 5%%

Lyr#	Type	Gerber file name	Dielectric	Copper Weight	Trace width (INCHES)	Ohms	Trace width (INCHES)	Separation (INCHES)	Ohms	Trace width (INCHES)	Separation (INCHES)	Ohms	Comments
1	Top Side	COMPSIDE.PHO	0.003"	1/2 OZ	0.006	50+/-5	0.0045	0.0065	100+/-5	0.007	-	75+/-5	-
2	GND PLANE 1	GND2.PHO	0.005"	1 OZ							-		CORE
3	INNER TRACE 1	INTRC3.PHO	0.0044"	1/2 OZ	0.006	50+/-5	0.0045	0.0065	100+/-5		-		PRE-PREG
4	PWR PLANE 1	PWR4.PHO	0.005"	1 OZ							-		CORE
5	INNER TRACE 2	INTRC5.PHO	0.0044"	1/2 OZ	0.006	50+/-5	0.0045	0.0065	100+/-5		-		PRE-PREG
6	PWR PLANE 2	PWR6.PHO	0.054"	1 OZ							-		CORE
7	PWR PLANE 3	PWR7.PHO	0.0044"	1 OZ							-		PRE-PREG
8	INNER TRACE 3	INTRC8.PHO	0.005"	1/2 OZ	0.006	50+/-5	0.0045	0.0065	100+/-5		-		PRE-PREG
9	GND PLANE 2	GND9.PHO	0.0044"	1 OZ							-		CORE
10	INNER TRACE 4	INTRC10.PHO	0.005"	1/2 OZ	0.006	50+/-5	0.0045	0.0065	100+/-5		-		PRE-PREG
11	GND PLANE 3	GND11.PHO	0.003"	1 OZ							-		CORE
12	BOTTOM SIDE	SLDRSIDE.PHO		1/2 OZ	0.006	50+/-5	0.0045	0.0065	100+/-5		-		PRE-PREG

NOTES: FINISHED COPPER THICKNESS ON OUTER LAYERS WILL BE .0027" AFTER PLATING.

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TOLERANCES

∠ .X .XX .XXX

Unless otherwise specified, dimensions are in inches.

XILINX®

DRAWN BY	N. FARMER	DATE 8/26/05
CHECKED BY		DATE
ENG APPROVAL		DATE
MFG APPROVAL		DATE
FSCM 68994		

TITLE

PCB, ML405 EVAL PLATFORM, ROHS

PROJECT:

SIZE	DRAWING NUMBER	REV.
B	1280367	03

SCALE NTS SHEET 1 OF 1