

4	3	2	1
D			
C			
B			
A			

NOTE: PLEASE REVIEW THE ML410 BOM FOR ITEMS DESIGNATED AS "NOSTUFF".

NOSTUFF ITEMS ARE NOT POPULATED ON THE PCB.

THE ML410 BOM CONTAINS THE MOST ACCURATE INFORMATION ABOUT

NOSTUFF DISCRETES AND COMPONENTS.

XILINX PART NUMBERS

SCHEMATICS

0381203

PCB ARTWORK

0531499

PCB FABRICATION

1280372



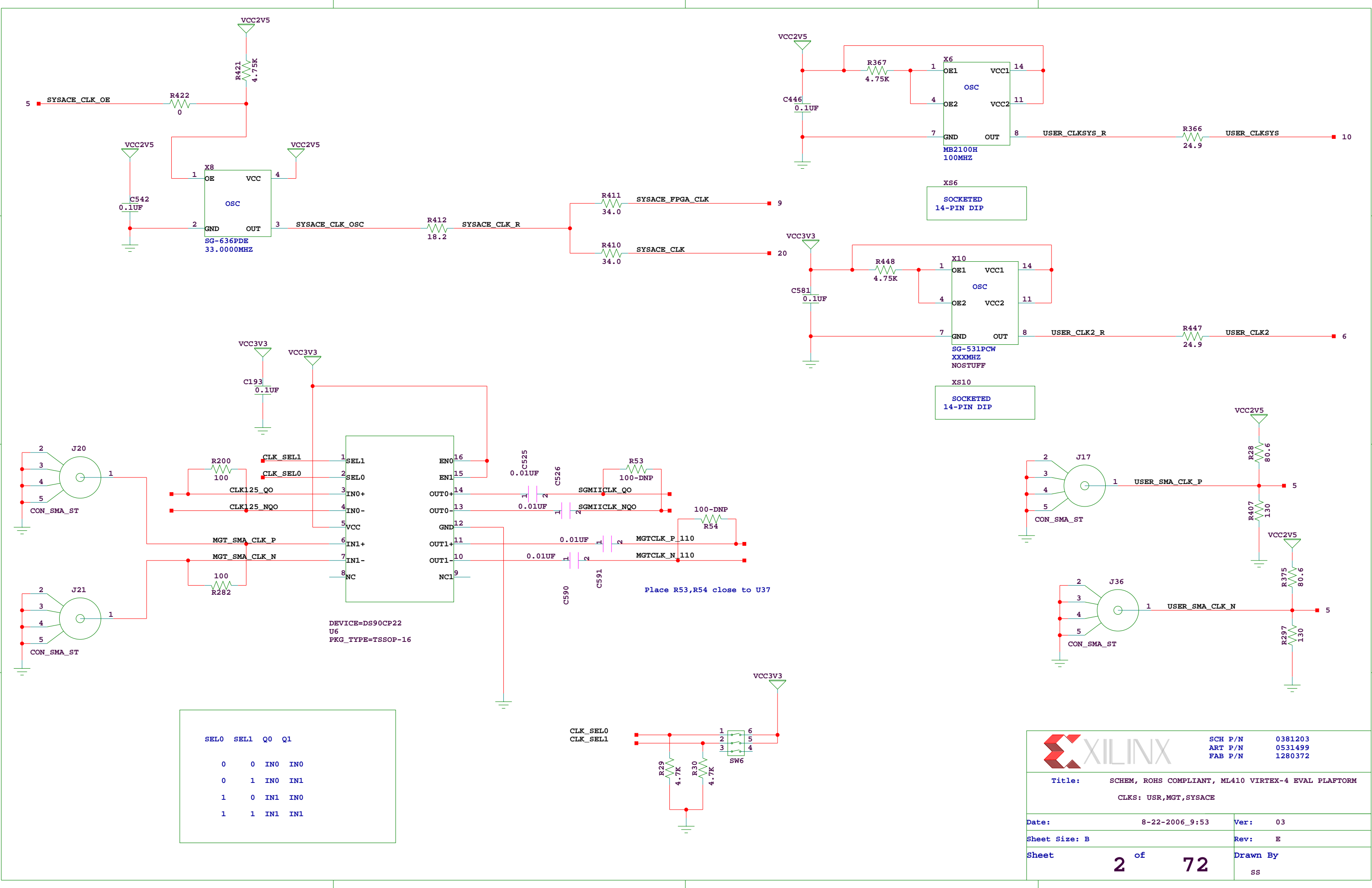
SCH P/N 0381203  
ART P/N 0531499  
FAB P/N 1280372

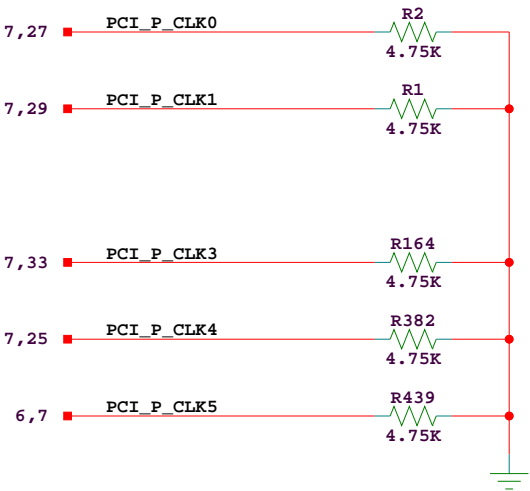
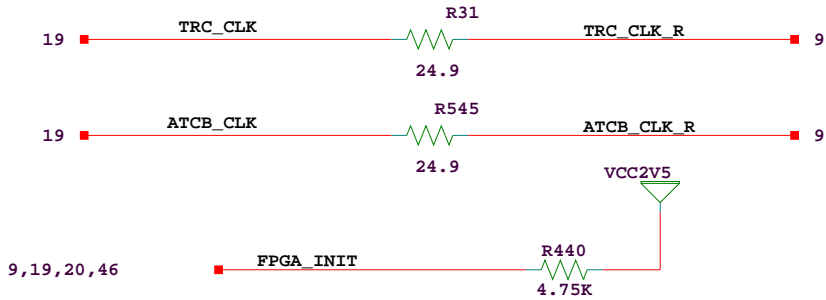
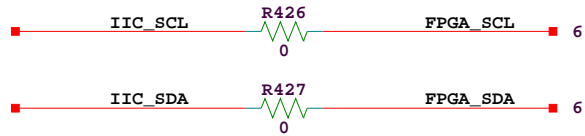
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM  
TABLE OF CONTENTS

Date: 8-22-2006\_9:53 Ver: 03

Sheet Size: B Rev: E

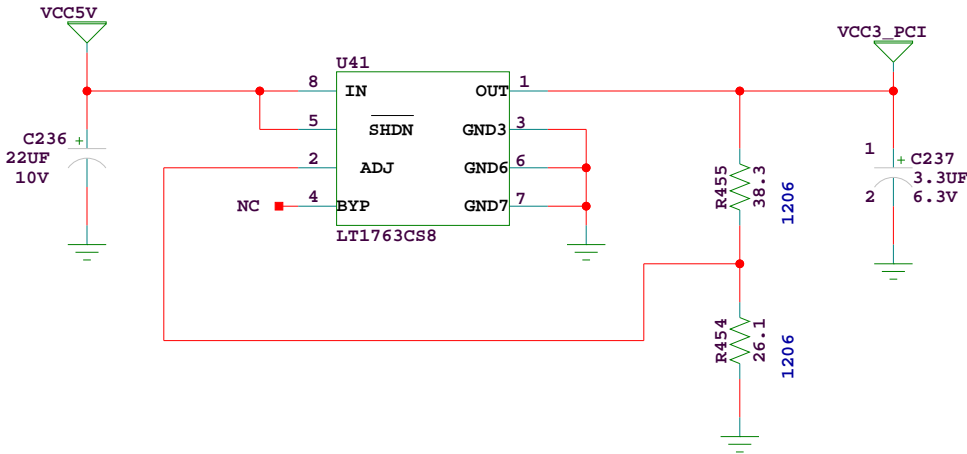
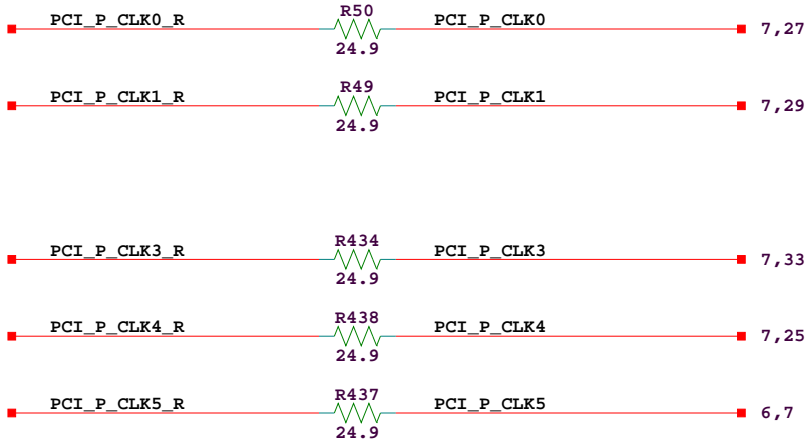
Sheet 1 of 72 Drawn By  
SS





NOTE: THE PCI SPEC RECOMMENDS THAT  
CLOCKS BE PULLED LOW WHEN THE  
BUS IS NOT ACTIVELY CLOCKED.

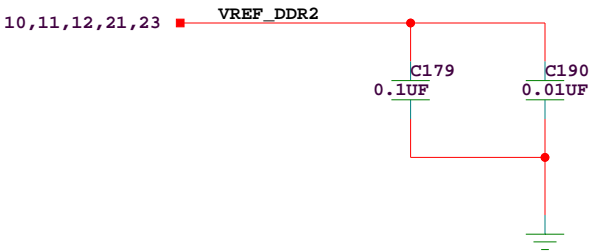
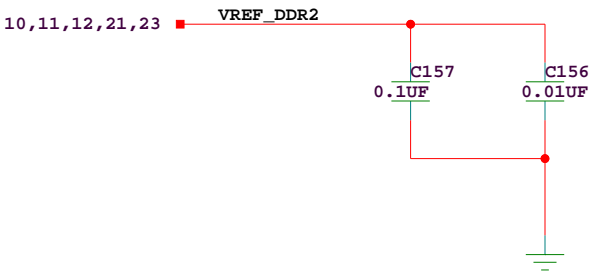
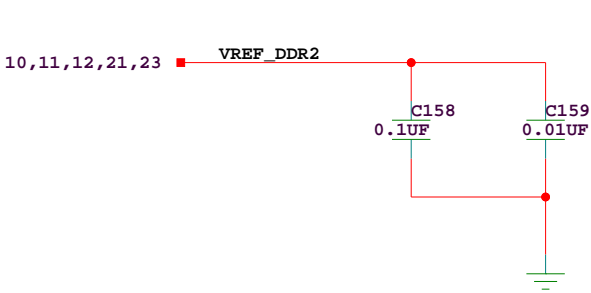
NOTE: PCI\_CLK RESISTORS ALLOW CLOCK TERMINATION  
TO BE ADJUSTED INDEPENDENTLY OF OTHER I/O.



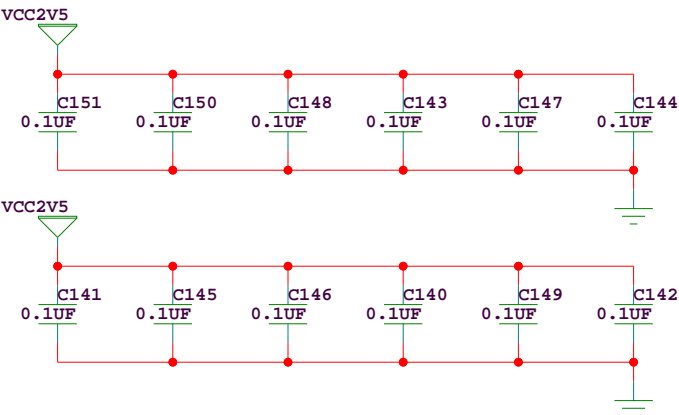
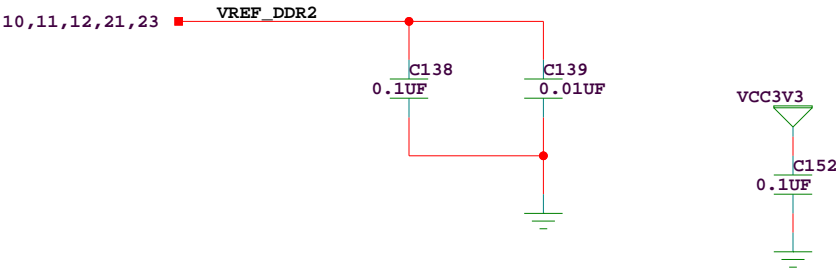
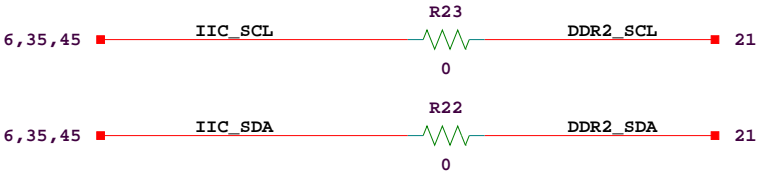
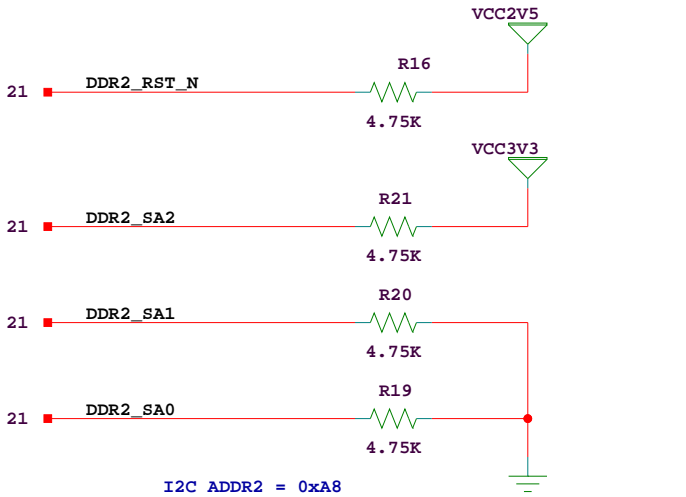
NOTE: THE COMPONENT VALUES FOR THIS REGULATOR ARE TAKEN  
FROM XAPP653. THIS DESIGN IS INTENDED TO SINK CURRENT  
THROUGH THE 1206 RESISTORS WHEN THE CLAMP DIODES ON  
THE FPGA ARE CONDUCTING DURING OVERSHOOT. THIS IS WHY  
THE VALUES ARE UNUSUAL RELATIVE TO THE LT1763 DATASHEET.



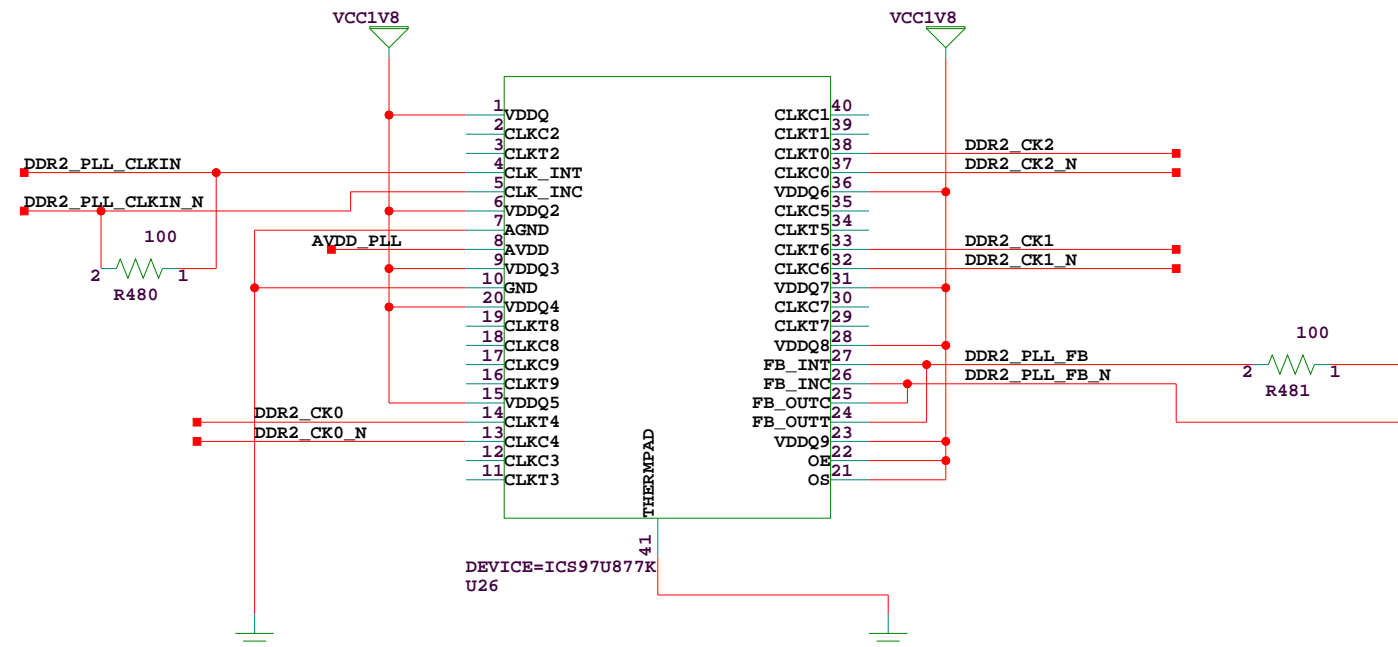
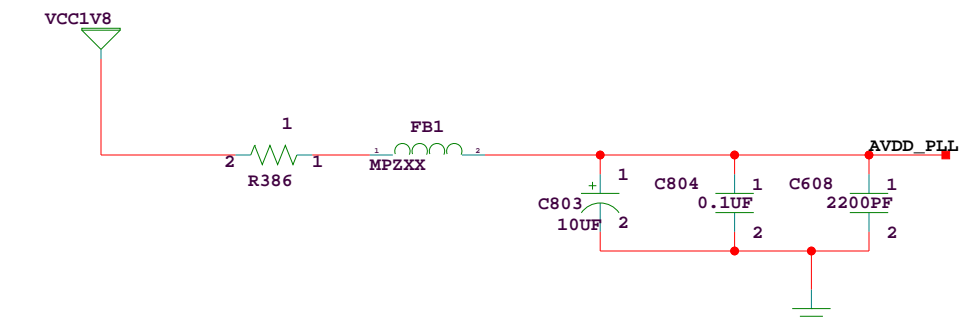
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		ART P/N	0531499
		FAB P/N	1280372
Title:		SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLATFORM PCI_SUPPLY .....	
Date:	8-22-2006_9:53	Ver:	03
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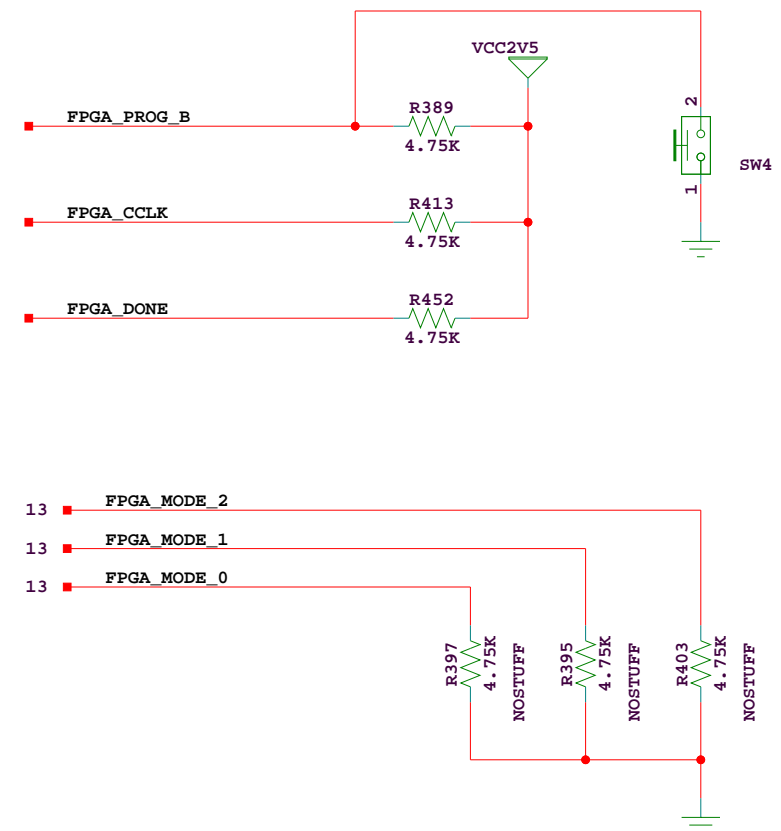
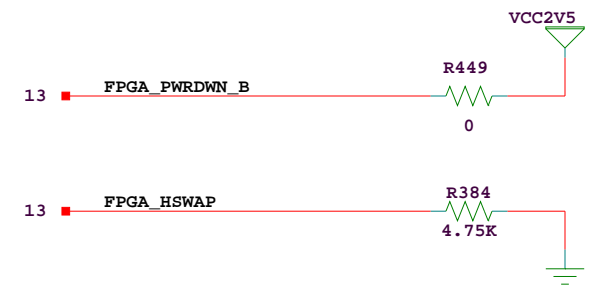
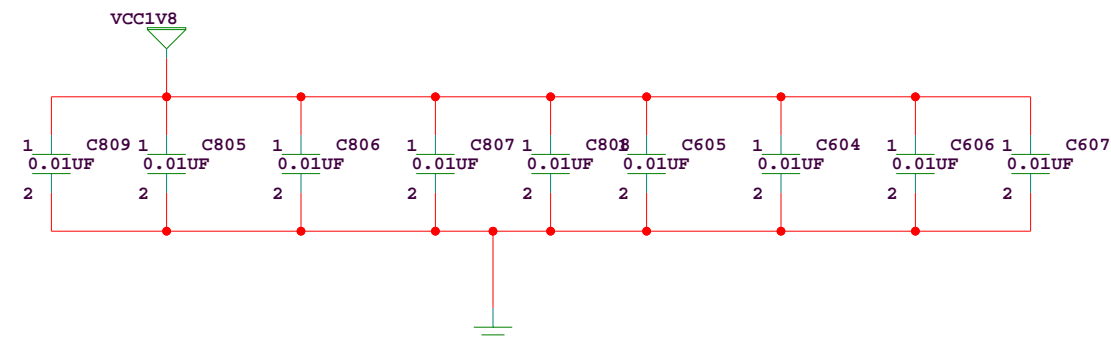
NOTE: THE PINOUT OF THE DDR2 DQ AND DQS SIGNALS IS INTENDED TO ALLOW THE USE OF LOCAL CLOCKING RESOURCES AS DESCRIBED IN XAPP609.




		SCH P/N	0381203
		ART P/N	0531499
		FAB P/N	1280372
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLATFOMR			
DDR2 DECOUPLING			
Date: 8-22-2006_9:53		Ver:	03
Sheet Size: B		Rev:	E
Sheet 4 of 72		Drawn By SS	



```
All DDR2_CK* to be length matched
DDR2_PLL_FB* to be length matched to DDR2_CK*
```

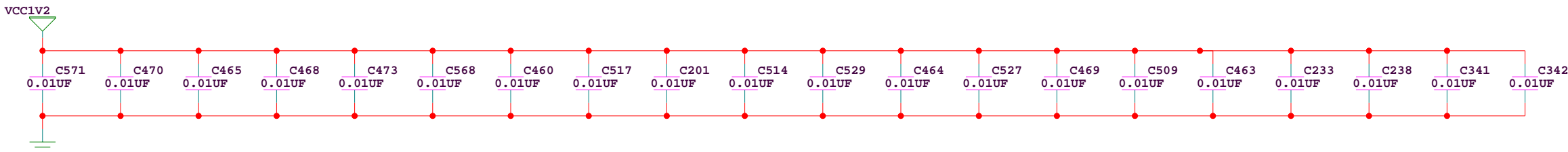
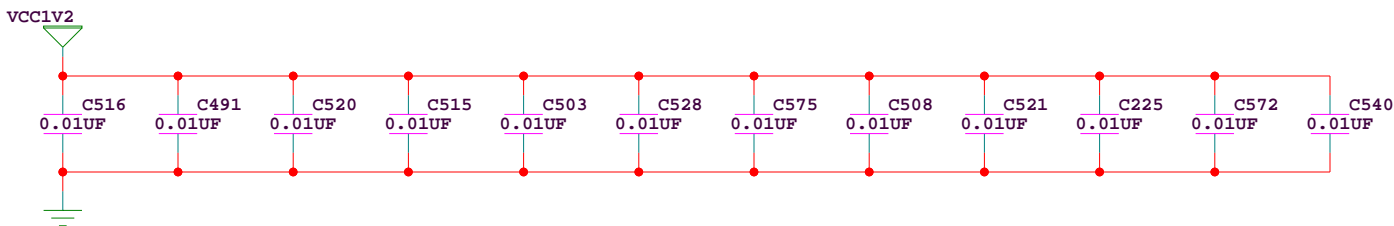
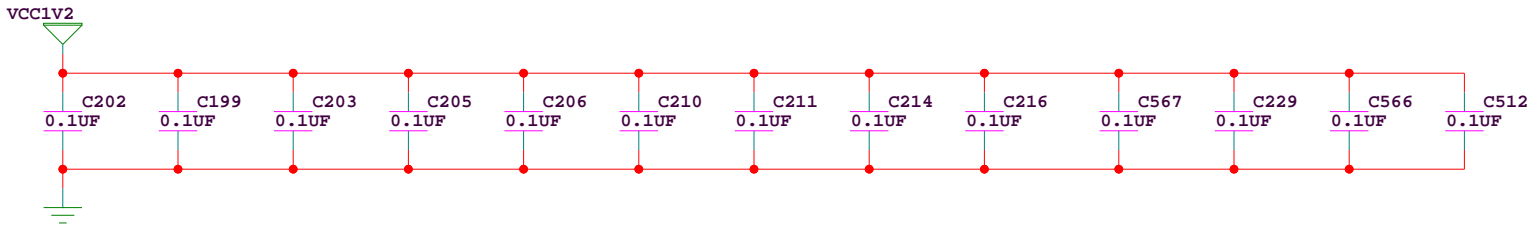
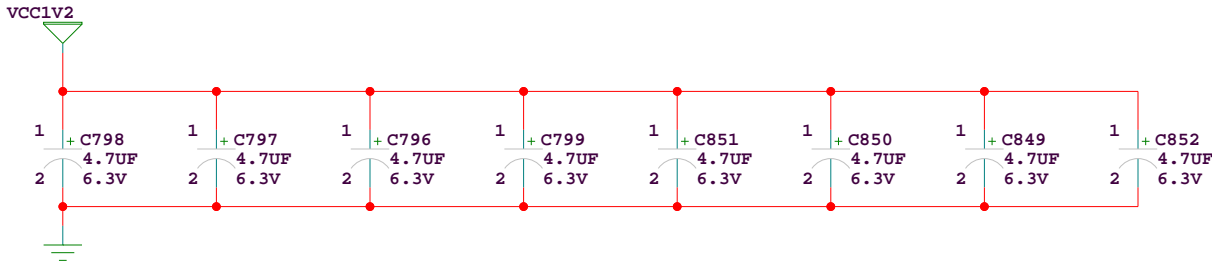


NOTE: MODE BITS HAVE INTERNAL PULLUPS AND DEFAULT  
TO SLAVE-SERIAL MODE. THERE MAY BE SOME  
CONFLCITS BETWEEN THE JTAG MODES AND ICAP  
HOWEVER SLAVE-SERIAL MODE IS KNOWN TO WORK.

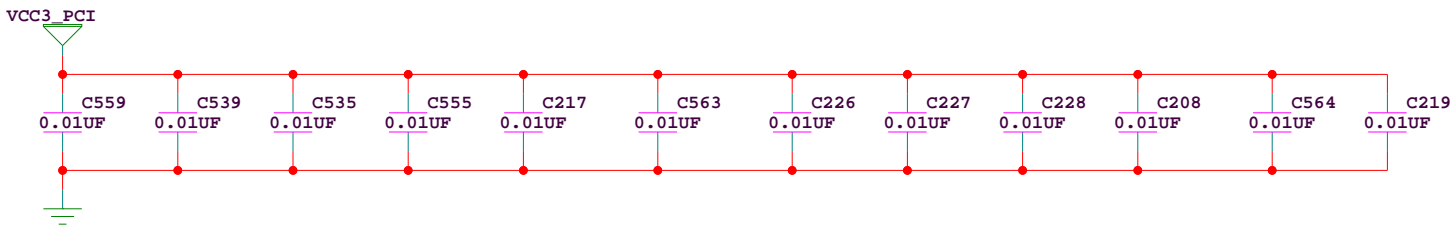
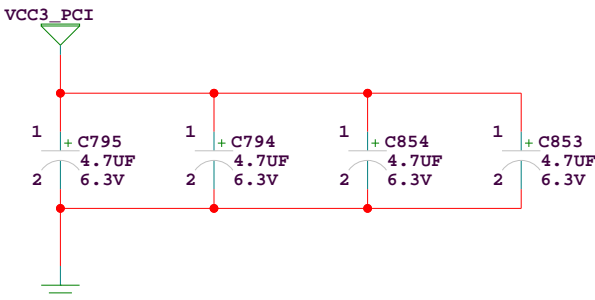
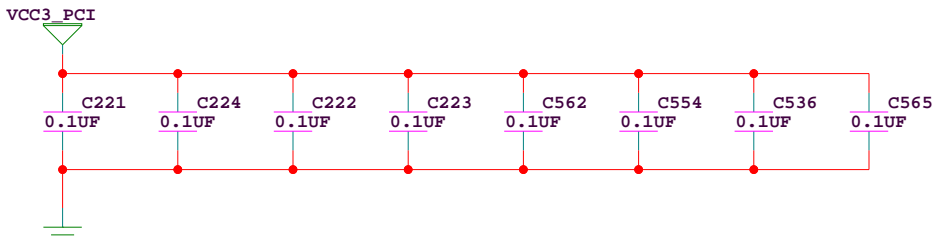
		SCH P/N 0381203 ART P/N 0531499 FAB P/N 1280372
<b>Title:</b> SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFORM FPGA CONFIG AND MISC I/O		
<b>Date:</b>	8-22-2006_9:53	<b>Ver:</b> 03
<b>Sheet Size:</b> B		<b>Rev:</b> E
<b>Sheet</b>	5 of 72	<b>Drawn By</b> SS



VCORE



BANK 6,10,12



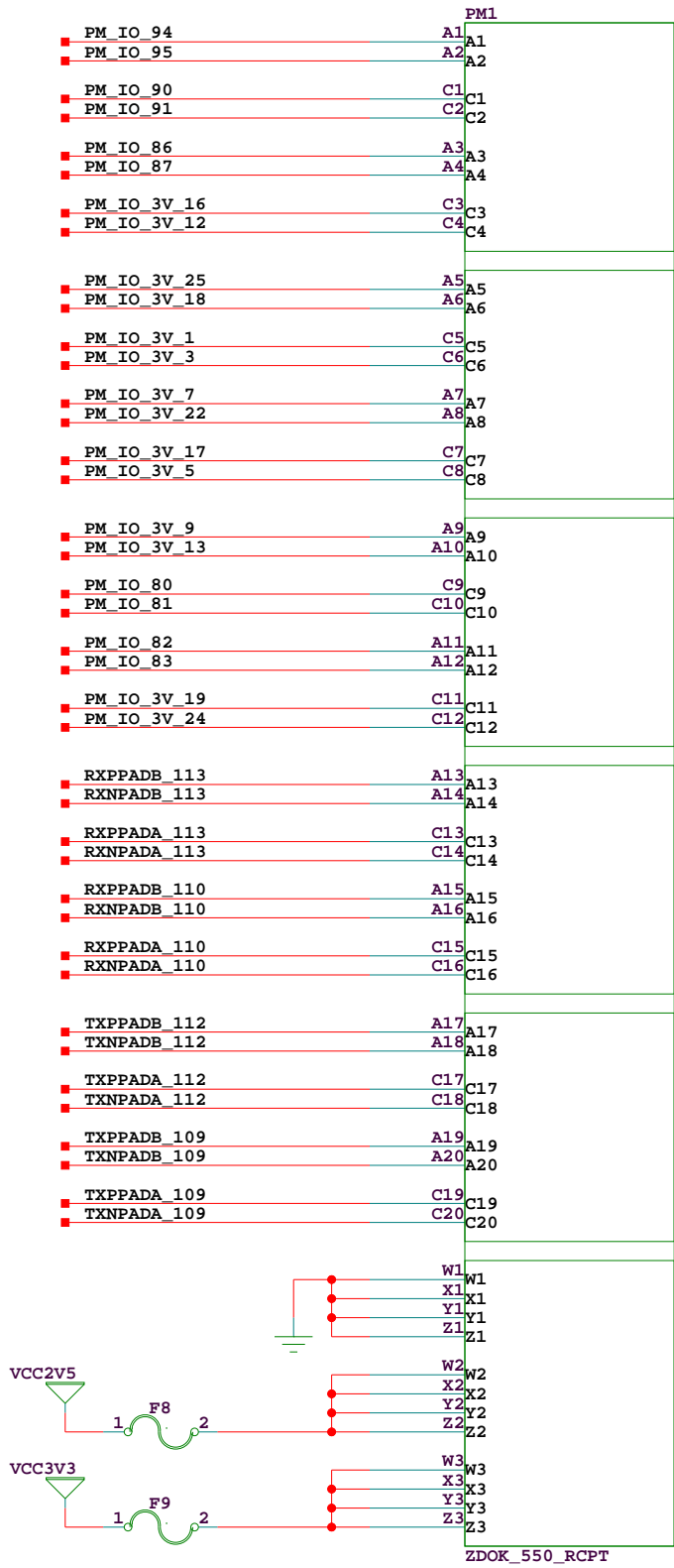
SCH P/N 0381203  
ART P/N 0531499  
FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLATFOrm  
FPGA DECOUPLING

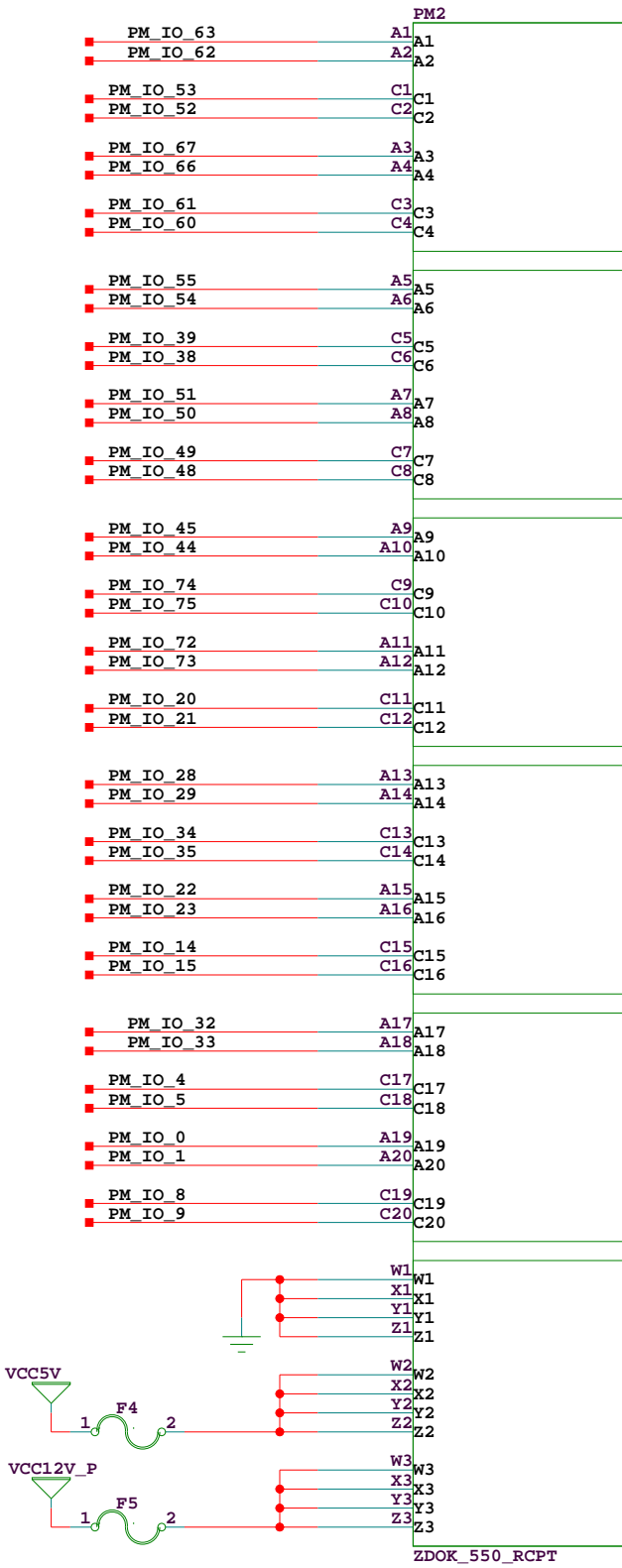
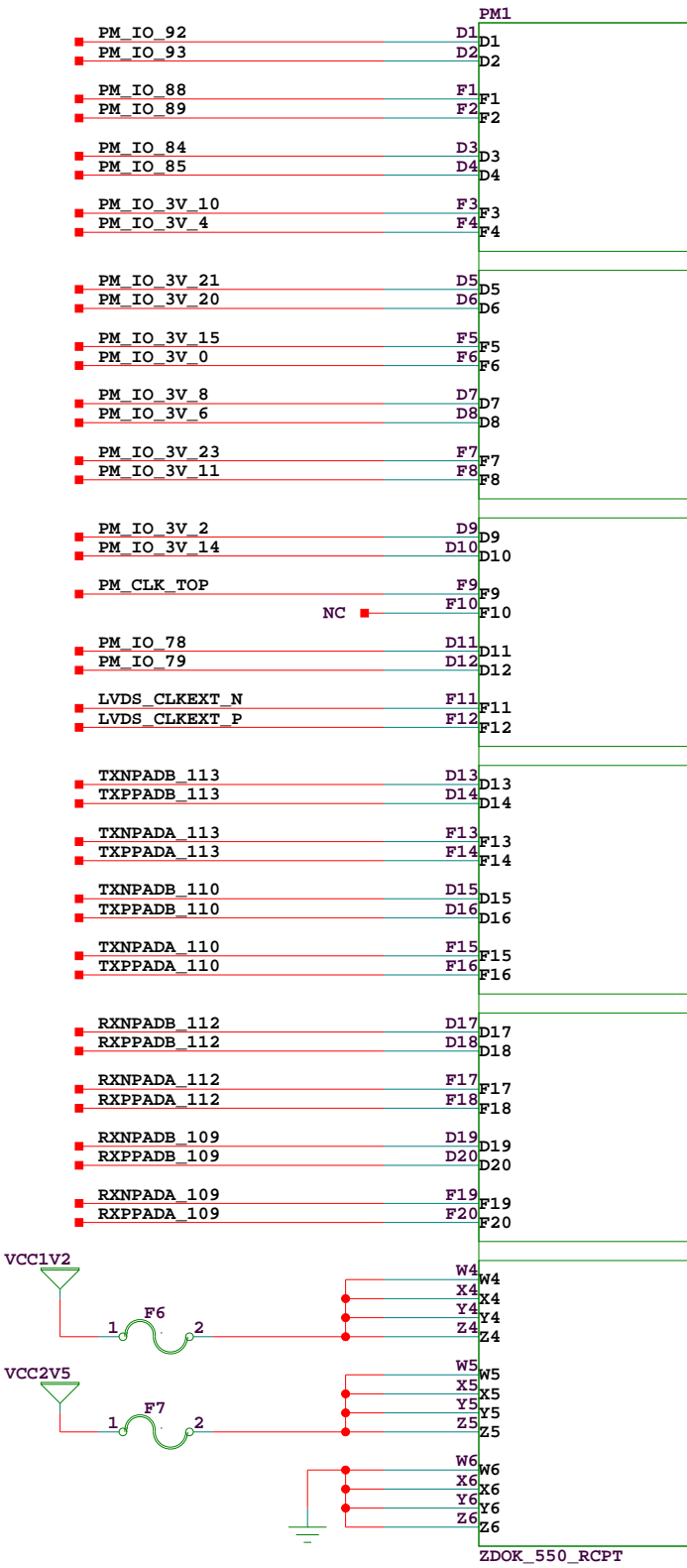
Date: 8-22-2006\_9:53 Ver: 03

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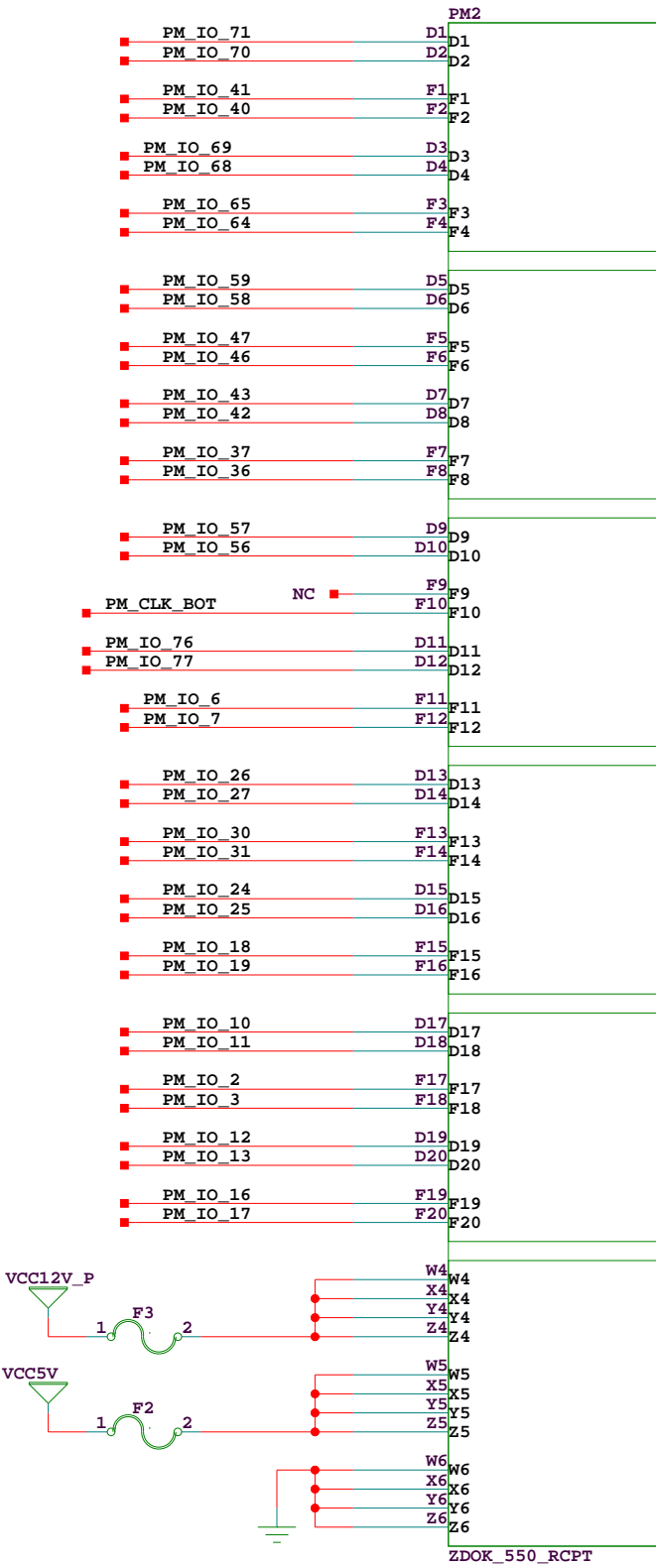
Sheet 7 of 72 Drawn By ss



GND;B1,B2,B3,B4,B5  
GND;B6,B7,B8,B9,B10  
GND;B11,B12,B13,B14,B15  
GND;B16,B17,B18,B19,B20  
GND;E1,E2,E3,E4,E5  
GND;E6,E7,E8,E9,E10  
GND;E11,E12,E13,E14,E15  
GND;E16,E17,E18,E19,E20



GND;B1,B2,B3,B4,B5  
GND;B6,B7,B8,B9,B10  
GND;B11,B12,B13,B14,B15  
GND;B16,B17,B18,B19,B20  
GND;E1,E2,E3,E4,E5  
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GND;E16,E17,E18,E19,E20



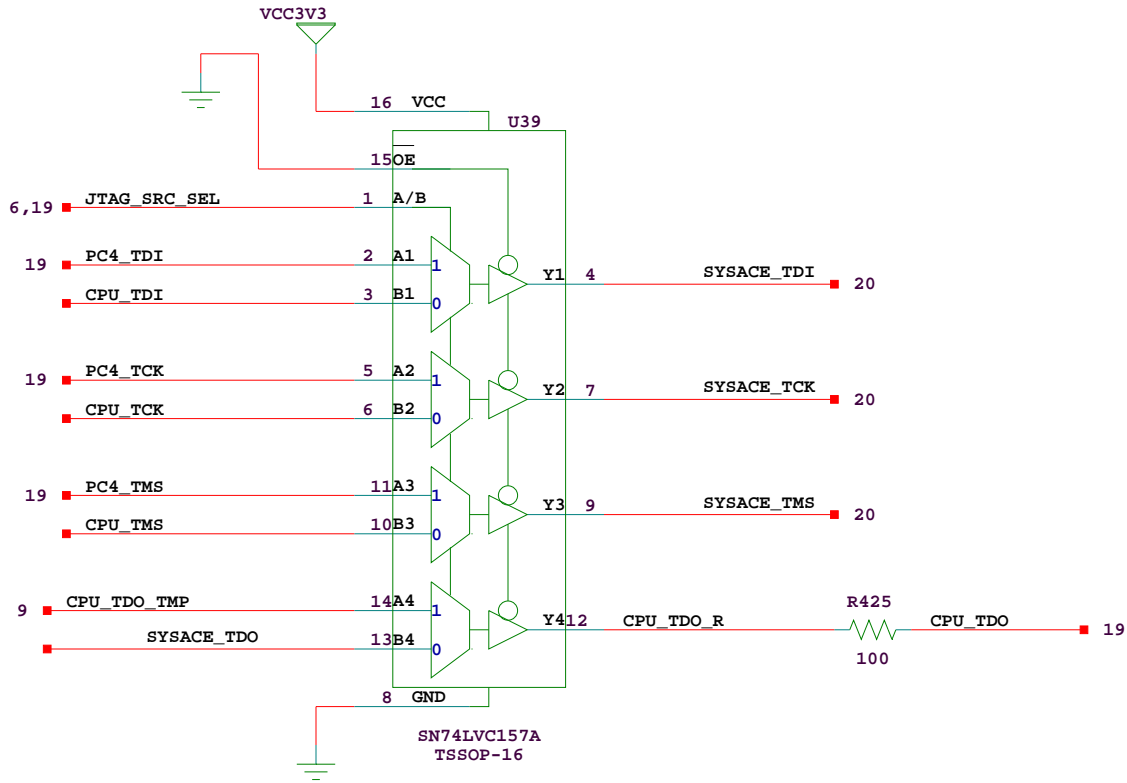
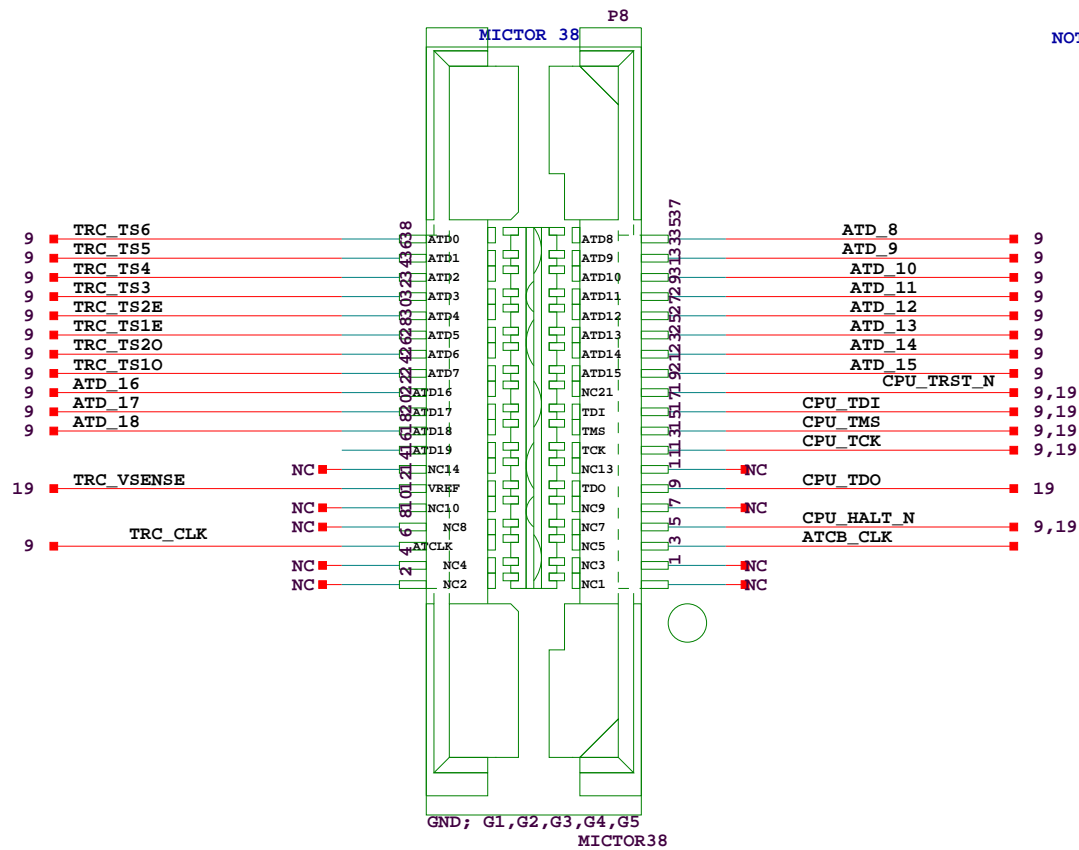
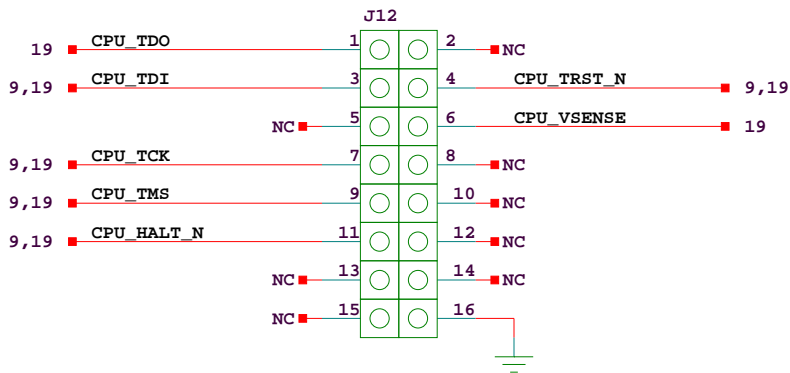
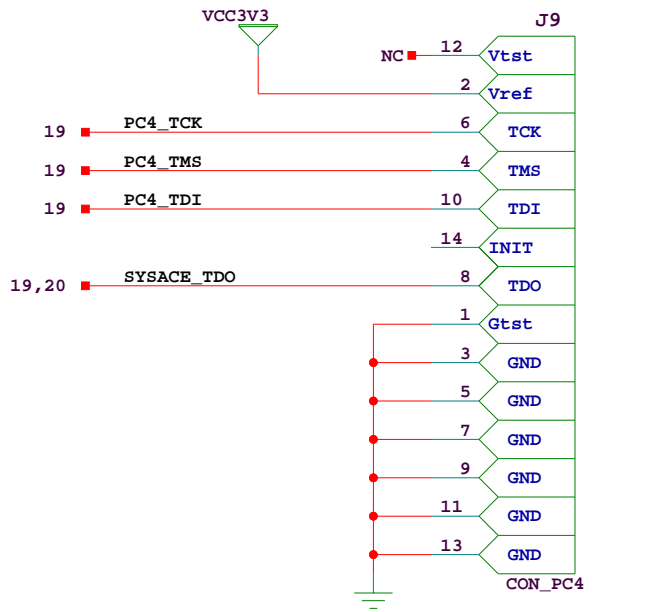
SCH P/N 0381203  
ART P/N 0531499  
FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFRTORM  
PERSONALITY MODULE CONNECTORS

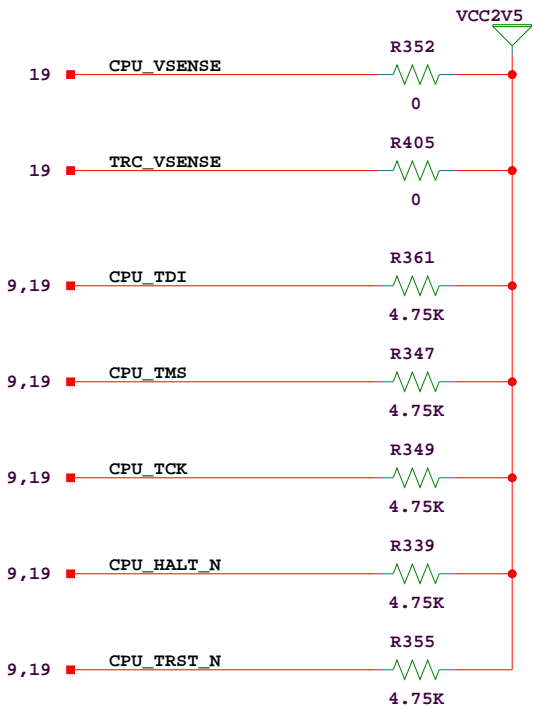
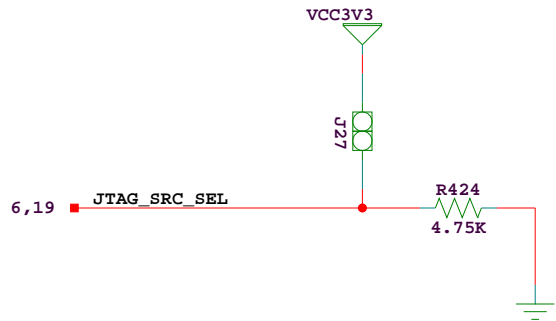
Date: 8-22-2006\_9:53 Ver: 03

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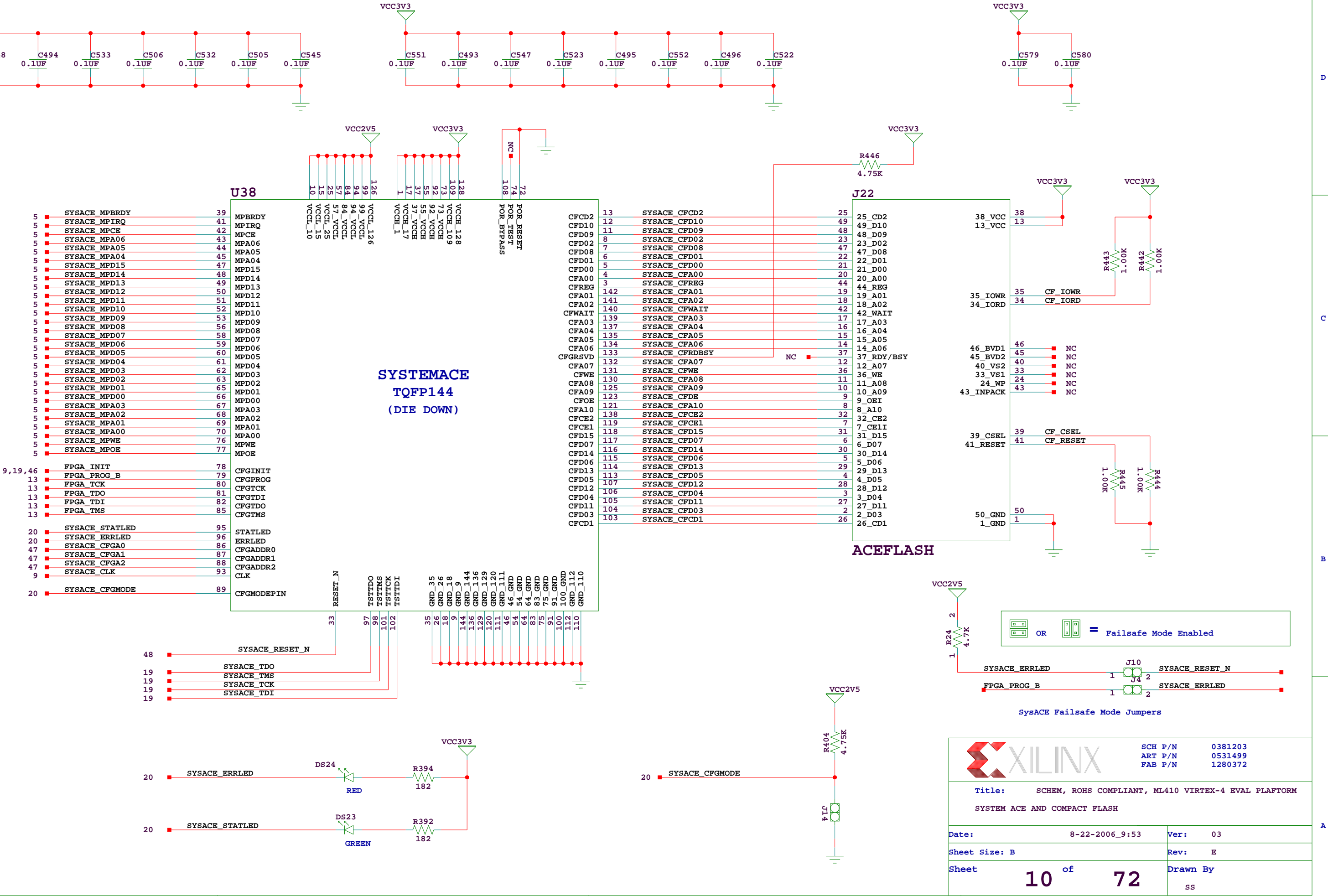
Sheet 8 of 72 Drawn By ss

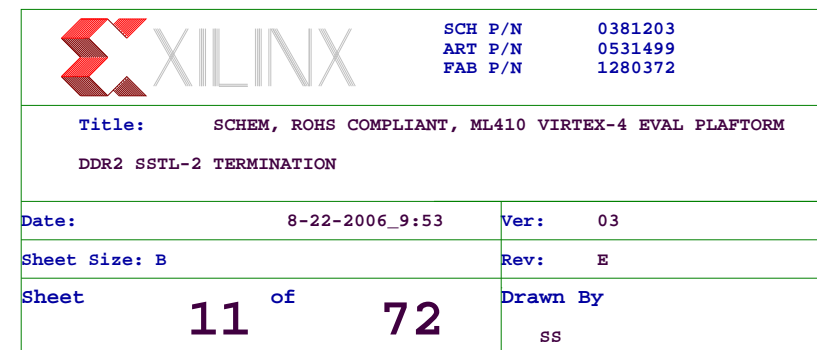
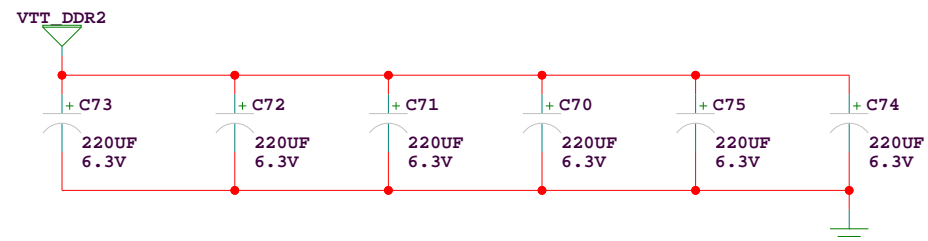
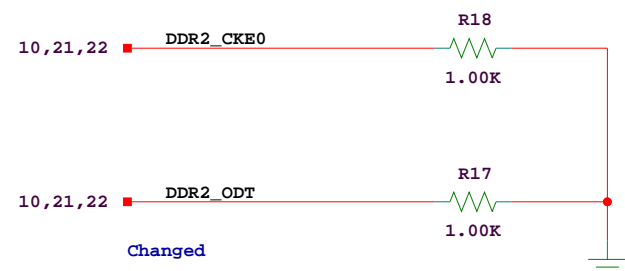
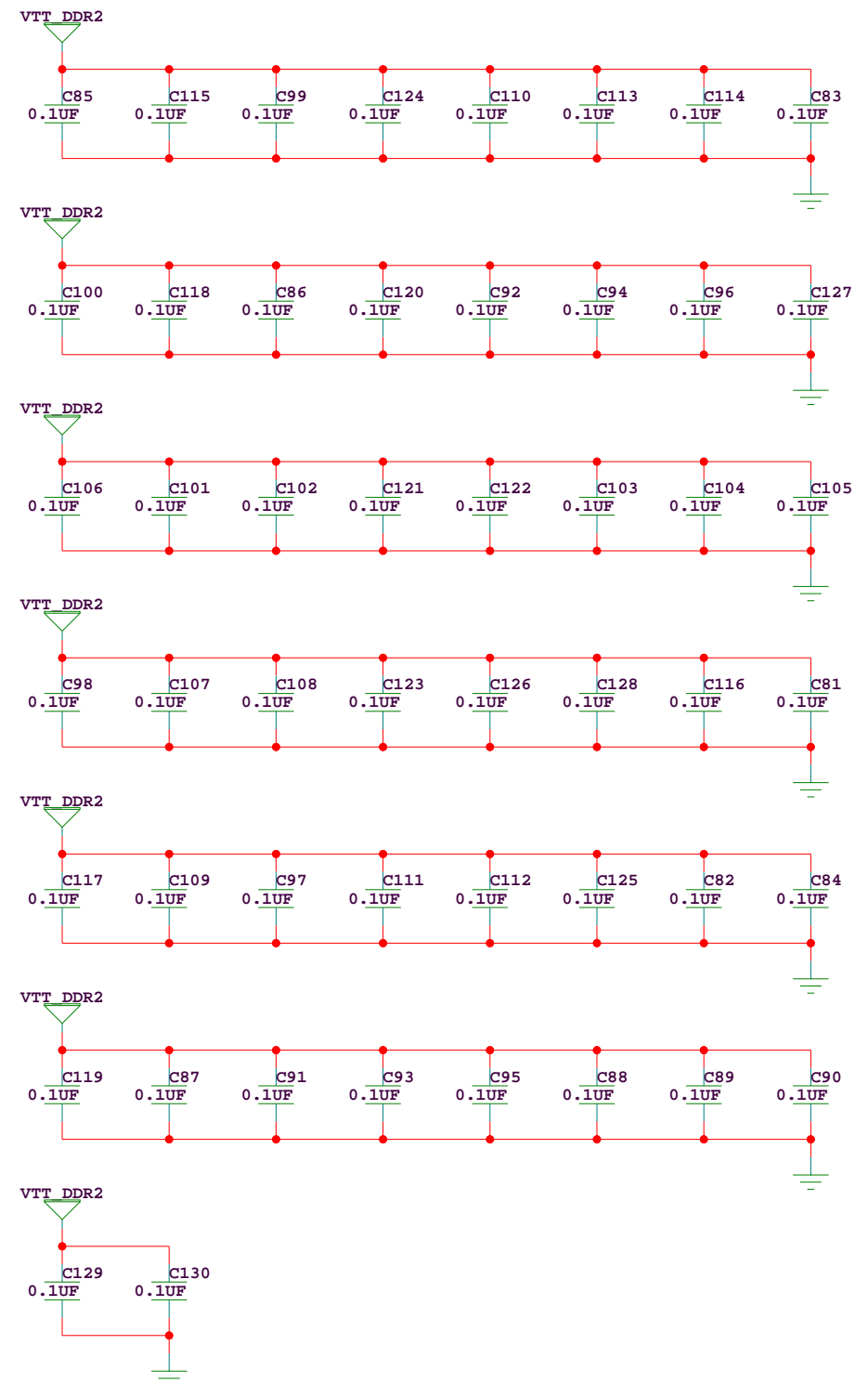
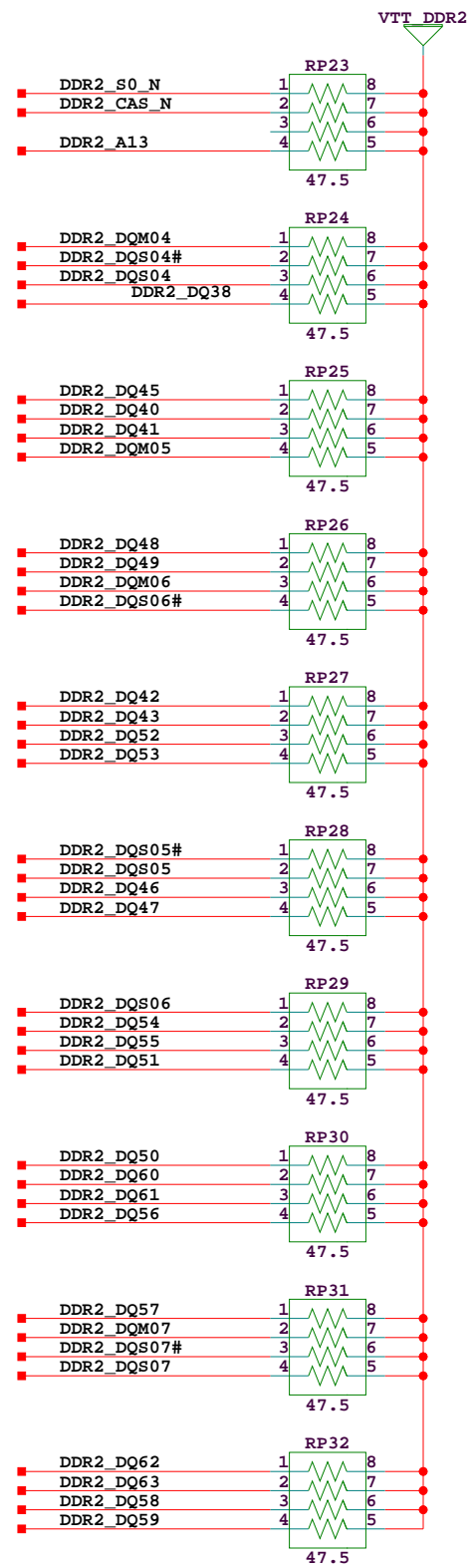
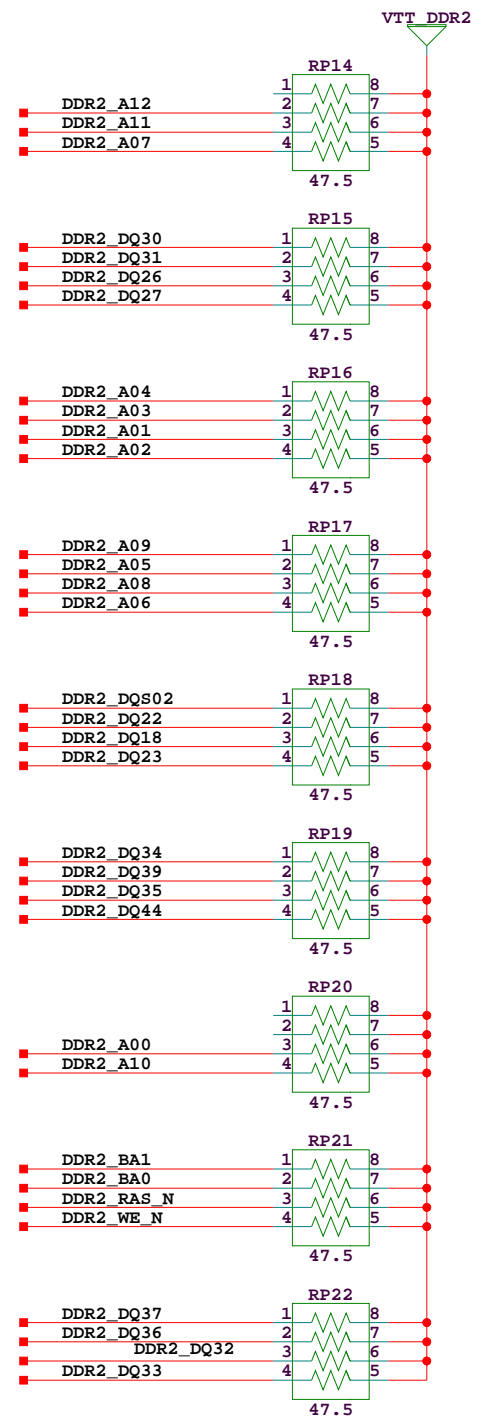
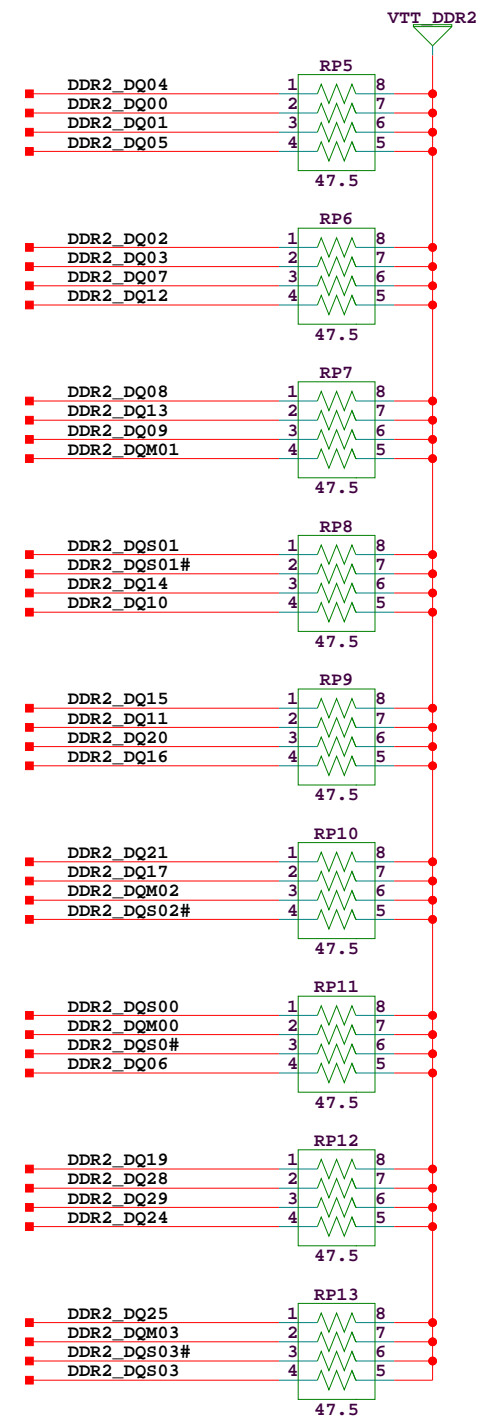


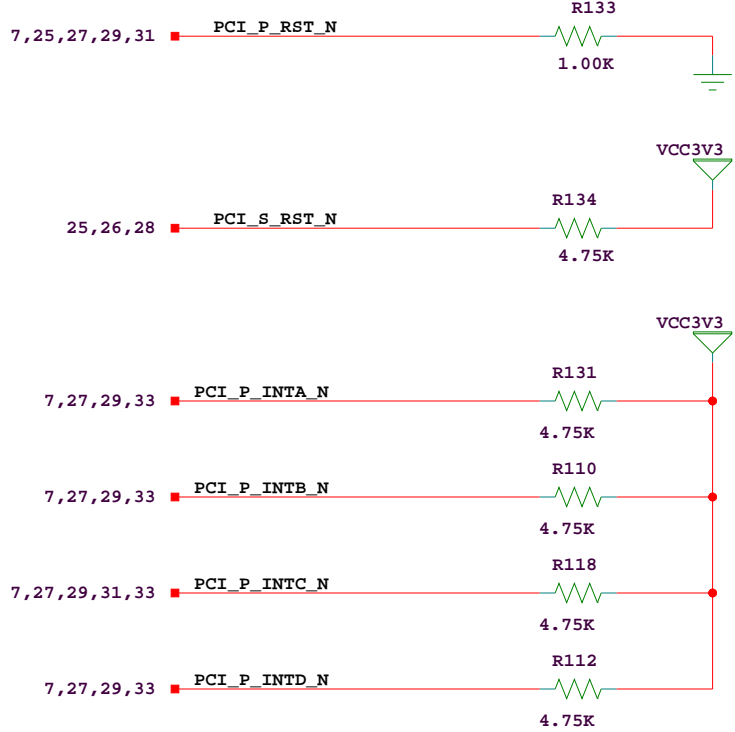
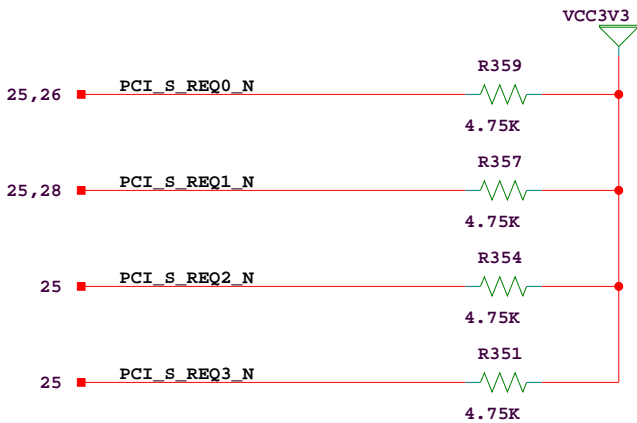
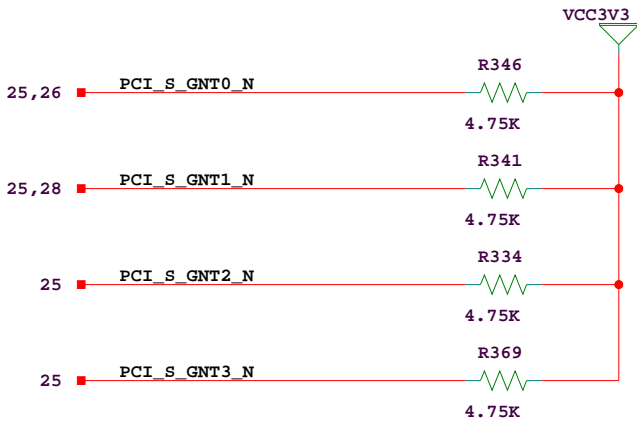
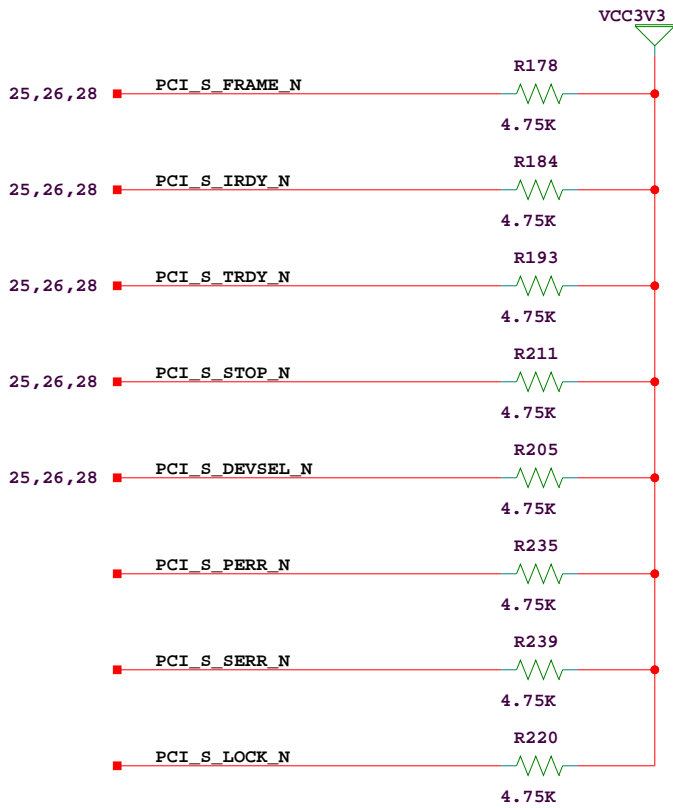
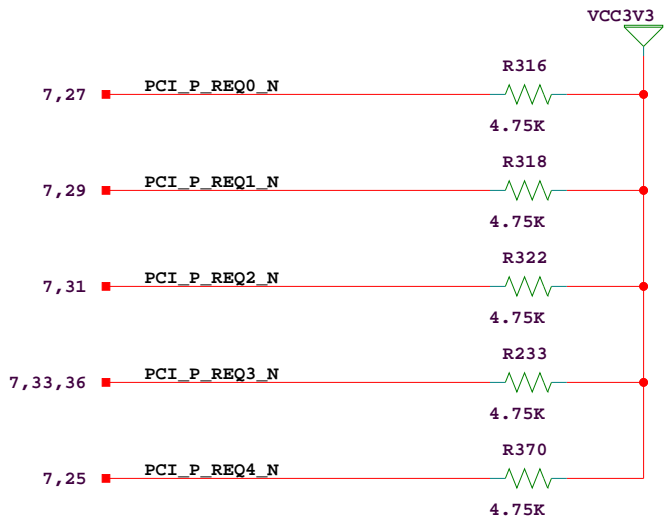
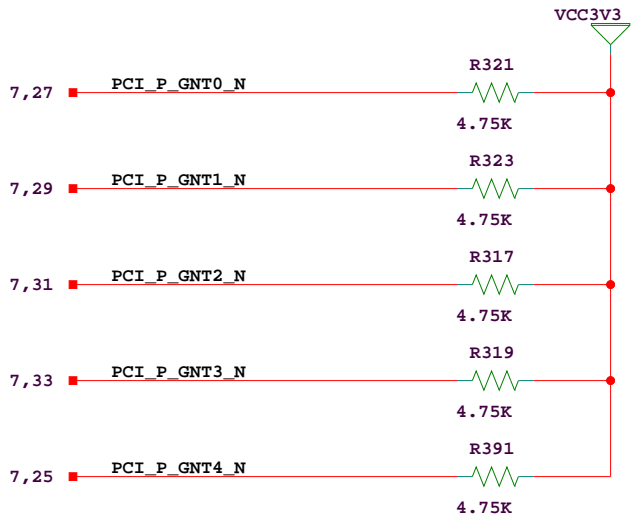
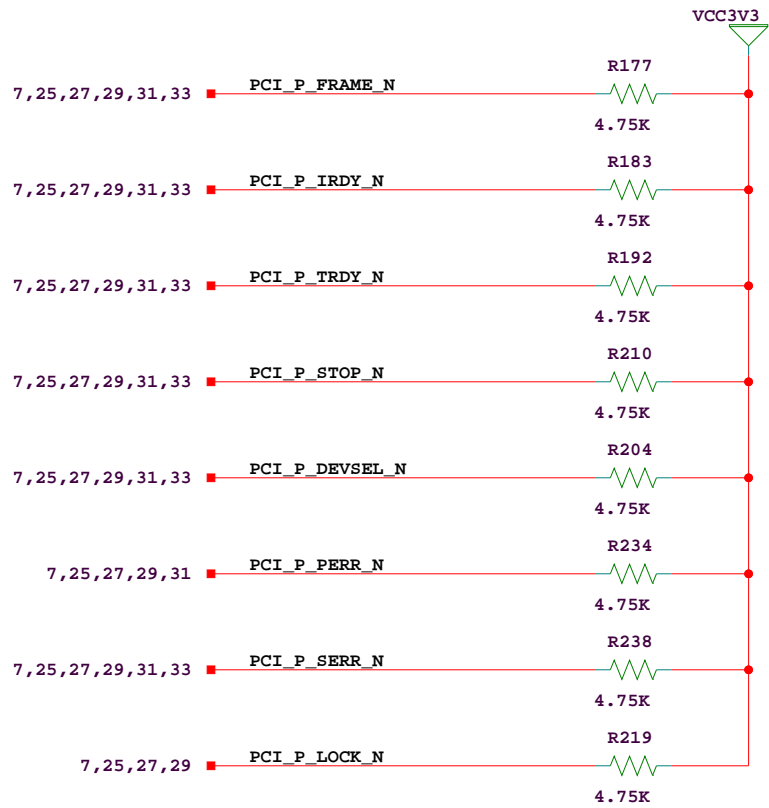
NOTE: THIS MUX INTRODUCES AN IMPLICIT 2.5V TO 3.3V LEVEL-SHIFT FOR THE CPU JTAG SIGNALS. THE SERIES RESISTOR ON CPU\_TDO IS INTENDED TO PROVIDE PROTECTION FOR A 2.5V JTAG PROBE.



		SCH P/N	0381203
		ART P/N	0531499
		FAB P/N	1280372
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLATFOrm			
JTAG, DEBUG, TRACE CONNECTORS			
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SCH P/N 0381203  
ART P/N 0531499  
FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFRTOM  
PCI BUS PULLUPS

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PCI-PCI BRIDGE  
PCI2250\_PGF

U32		
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7,27,29,31,33	PCI_P_AD02	144 P_AD2
7,27,29,31,33	PCI_P_AD03	143 P_AD3
7,27,29,31,33	PCI_P_AD04	141 P_AD4
7,27,29,31,33	PCI_P_AD05	140 P_AD5
7,27,29,31,33	PCI_P_AD06	138 P_AD6
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7,27,29,31,33	PCI_P_AD10	125 P_AD10
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7,27,29,31,33	PCI_P_AD12	123 P_AD12
7,27,29,31,33	PCI_P_AD13	121 P_AD13
7,27,29,31,33	PCI_P_AD14	120 P_AD14
7,27,29,31,33	PCI_P_AD15	119 P_AD15
7,27,29,31,33	PCI_P_AD16	103 P_AD16
7,27,29,31,33	PCI_P_AD17	102 P_AD17
7,27,29,31,33	PCI_P_AD18	101 P_AD18
7,27,29,31,33	PCI_P_AD19	99 P_AD19
7,27,29,31,33	PCI_P_AD20	98 P_AD20
7,27,29,31,33	PCI_P_AD21	97 P_AD21
7,27,29,31,33	PCI_P_AD22	95 P_AD22
7,27,29,31,33	PCI_P_AD23	94 P_AD23
7,27,29,31,33	PCI_P_AD24	86 P_AD24
7,27,29,31,33	PCI_P_AD25	84 P_AD25
7,27,29,31,33	PCI_P_AD26	83 P_AD26
7,27,29,31,33	PCI_P_AD27	82 P_AD27
7,27,29,31,33	PCI_P_AD28	80 P_AD28
7,27,29,31,33	PCI_P_AD29	79 P_AD29
7,27,29,31,33	PCI_P_AD30	78 P_AD30
7,27,29,31,33	PCI_P_AD31	76 P_AD31
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	PCI_P_CBE1_N	117 P_C/BE1_N
	PCI_P_CBE2_N	105 P_C/BE2_N
	PCI_P_CBE3_N	91 P_C/BE3_N

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7,24 PCI\_P\_REQ4\_N 75 P\_REQ\_N

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	PCI_P_FRAME_N	106 P_FRAME_N
	PCI_P_IRDY_N	107 P_IRDY_N
	PCI_P_LOCK_N	112 P_MFUNC
	PCI_P_PAR	116 P_PAR
	PCI_P_PERR_N	114 P_PERR_N
	PCI_P_RST_N	70 P_RST_N
	PCI_P_SERR_N	115 P_SERR_N
	PCI_P_STOP_N	111 P_STOP_N
	PCI_P_TRDY_N	109 P_TRDY_N
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		68 NO/HSLD
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PRIMARY

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S_AD4	154 PCI_S_AD04	26,28
S_AD5	155 PCI_S_AD05	26,28
S_AD6	156 PCI_S_AD06	26,28
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S_AD9	162 PCI_S_AD09	26,28
S_AD10	163 PCI_S_AD10	26,28
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S_AD19	20 PCI_S_AD19	26,28
S_AD20	22 PCI_S_AD20	26,28
S_AD21	23 PCI_S_AD21	26,28
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S_AD23	26 PCI_S_AD23	26,28
S_AD24	28 PCI_S_AD24	26,28
S_AD25	30 PCI_S_AD25	26,28
S_AD26	31 PCI_S_AD26	26,28
S_AD27	33 PCI_S_AD27	26,28
S_AD28	34 PCI_S_AD28	26,28
S_AD29	35 PCI_S_AD29	26,28
S_AD30	37 PCI_S_AD30	26,28
S_AD31	38 PCI_S_AD31	26,28

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S_C/BE1_N	172 PCI_S_CBE1_N	26,28
S_C/BE2_N	15 PCI_S_CBE2_N	26,28
S_C/BE3_N	27 PCI_S_CBE3_N	26,28

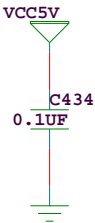
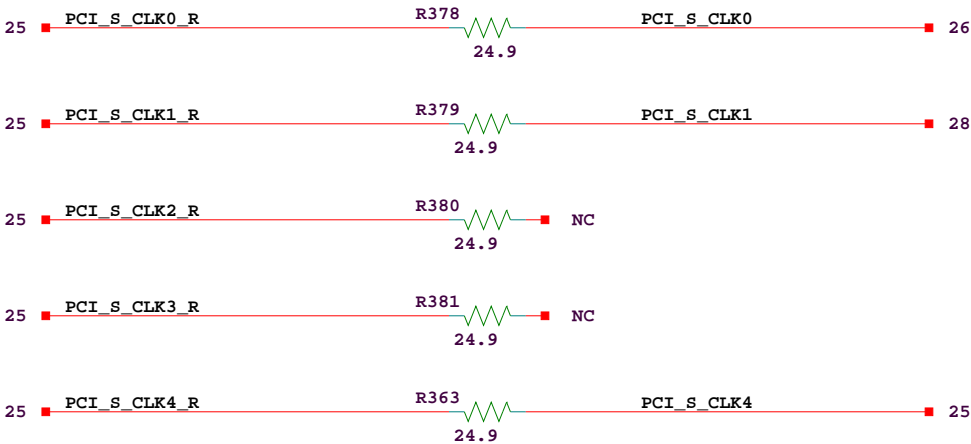
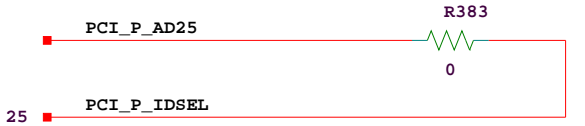
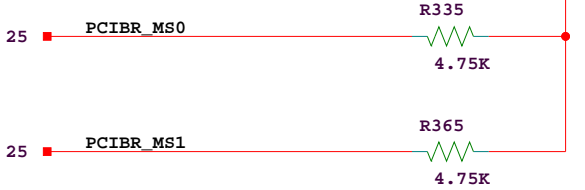
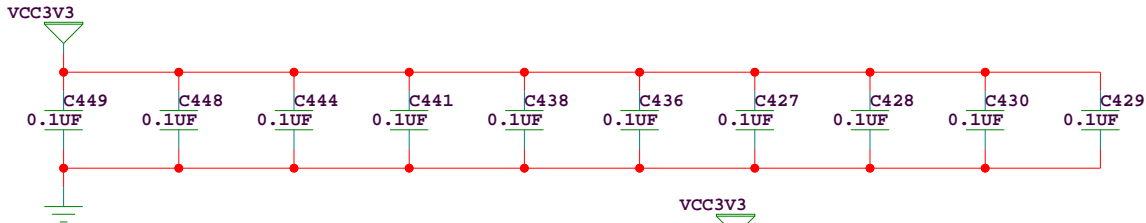
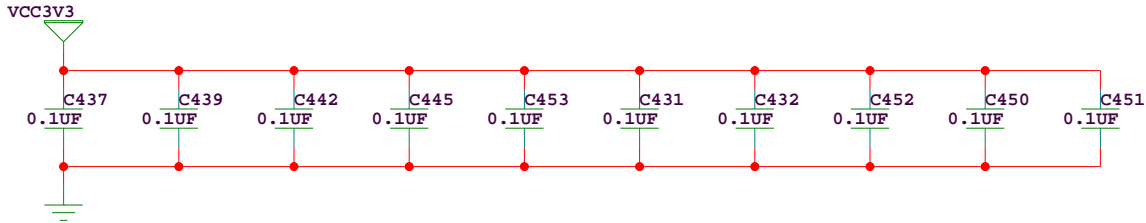
S_GNT0_N	49 PCI_S_GNT0_N	24,26
S_GNT1_N	50 PCI_S_GNT1_N	24,28
S_GNT2_N	51 PCI_S_GNT2_N	24
S_GNT3_N	53 PCI_S_GNT3_N	24

S_REQ0_N	39 PCI_S_REQ0_N	24,26
S_REQ1_N	40 PCI_S_REQ1_N	24,28
S_REQ2_N	42 PCI_S_REQ2_N	24
S_REQ3_N	47 PCI_S_REQ3_N	24

S_CLKOUT0	59 PCI_S_CLK0_R	25
S_CLKOUT1	61 PCI_S_CLK1_R	25
S_CLKOUT2	63 PCI_S_CLK2_R	25
S_CLKOUT3	65 PCI_S_CLK3_R	25
S_CLKOUT4	67 PCI_S_CLK4_R	25

S_CLK	57 PCI_S_CLK4	25
S_DEVSEL_N	9 PCI_S_DEVSEL_N	24,26,28
S_FRAME_N	13 PCI_S_FRAME_N	24,26,28
S_IRDY_N	12 PCI_S_IRDY_N	24,26,28
S_MFUNC	7 PCI_S_LOCK_N	24,26,28
S_PAR	3 PCI_S_PAR	26,28
S_PERR_N	6 PCI_S_PERR_N	24,26,28
S_RST_N	54 PCI_S_RST_N	24,26,28
S_SERR_N	5 PCI_S_SERR_N	24,26,28
S_STOP_N	8 PCI_S_STOP_N	24,26,28
S_TRDY_N	11 PCI_S_TRDY_N	24,26,28

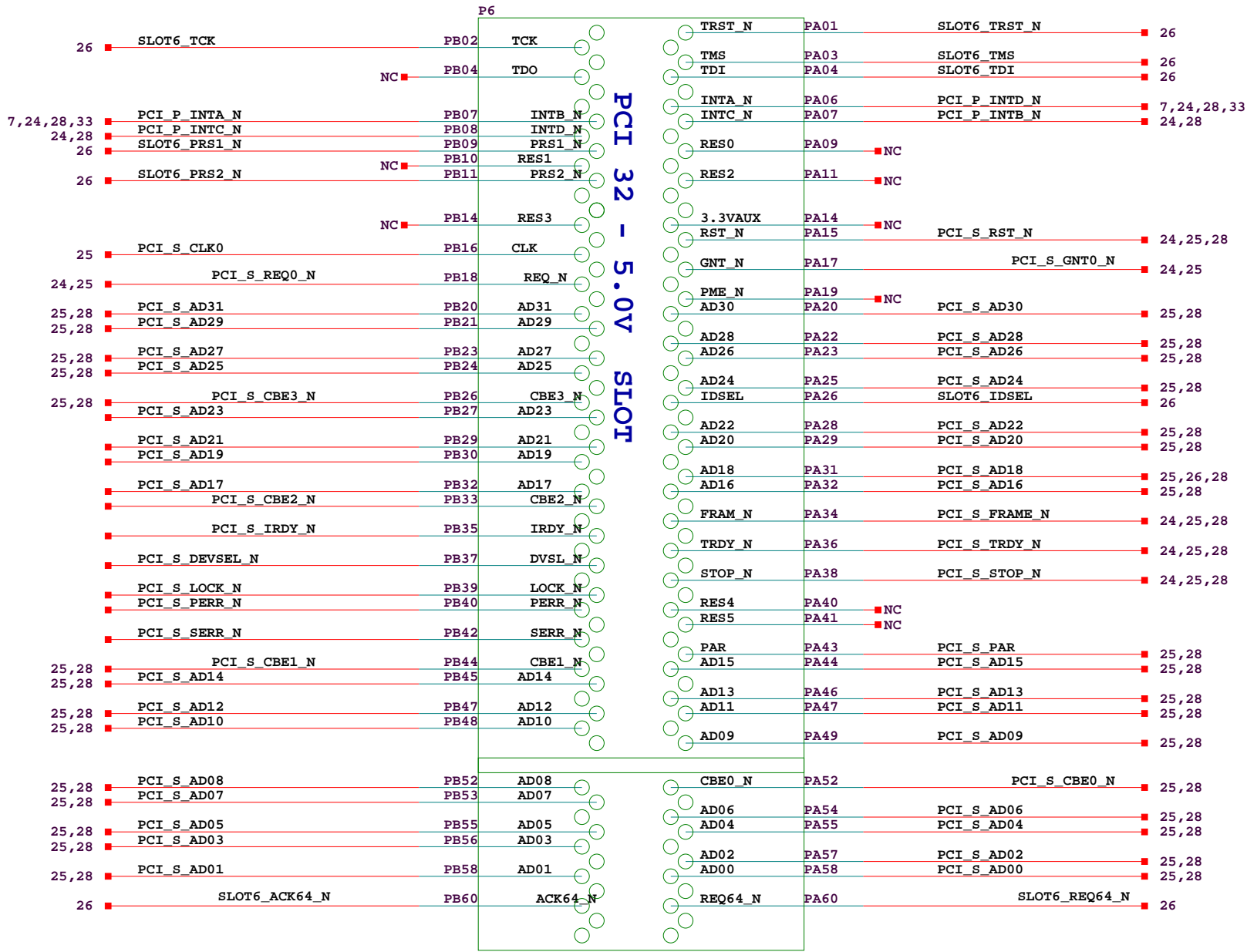
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S_C/CFN_N	55 PCIBR_CFN_N	25



SCH P/N 0381203  
ART P/N 0531499  
FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFRTORM  
PCI-PCI BRIDGE

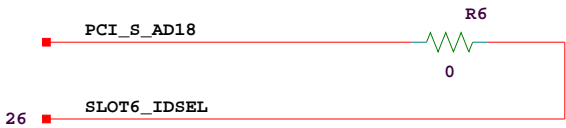
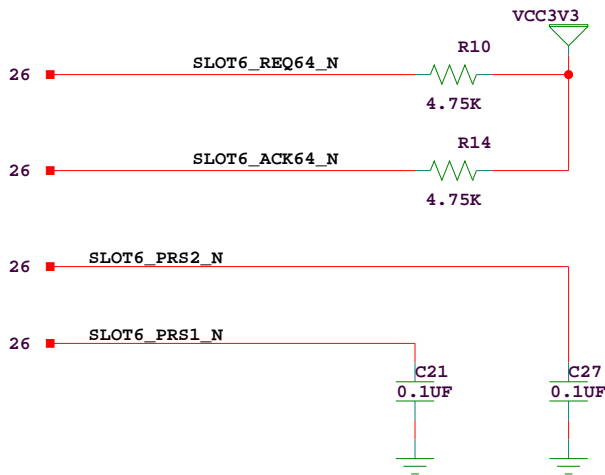
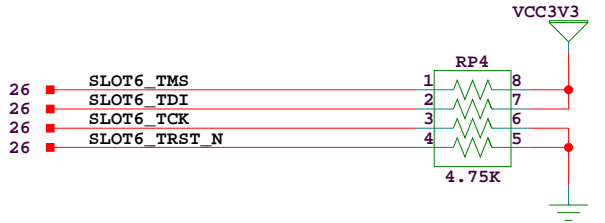
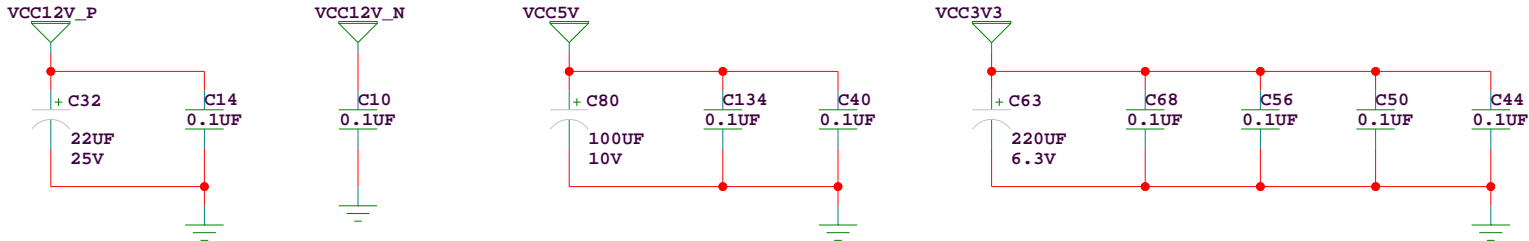
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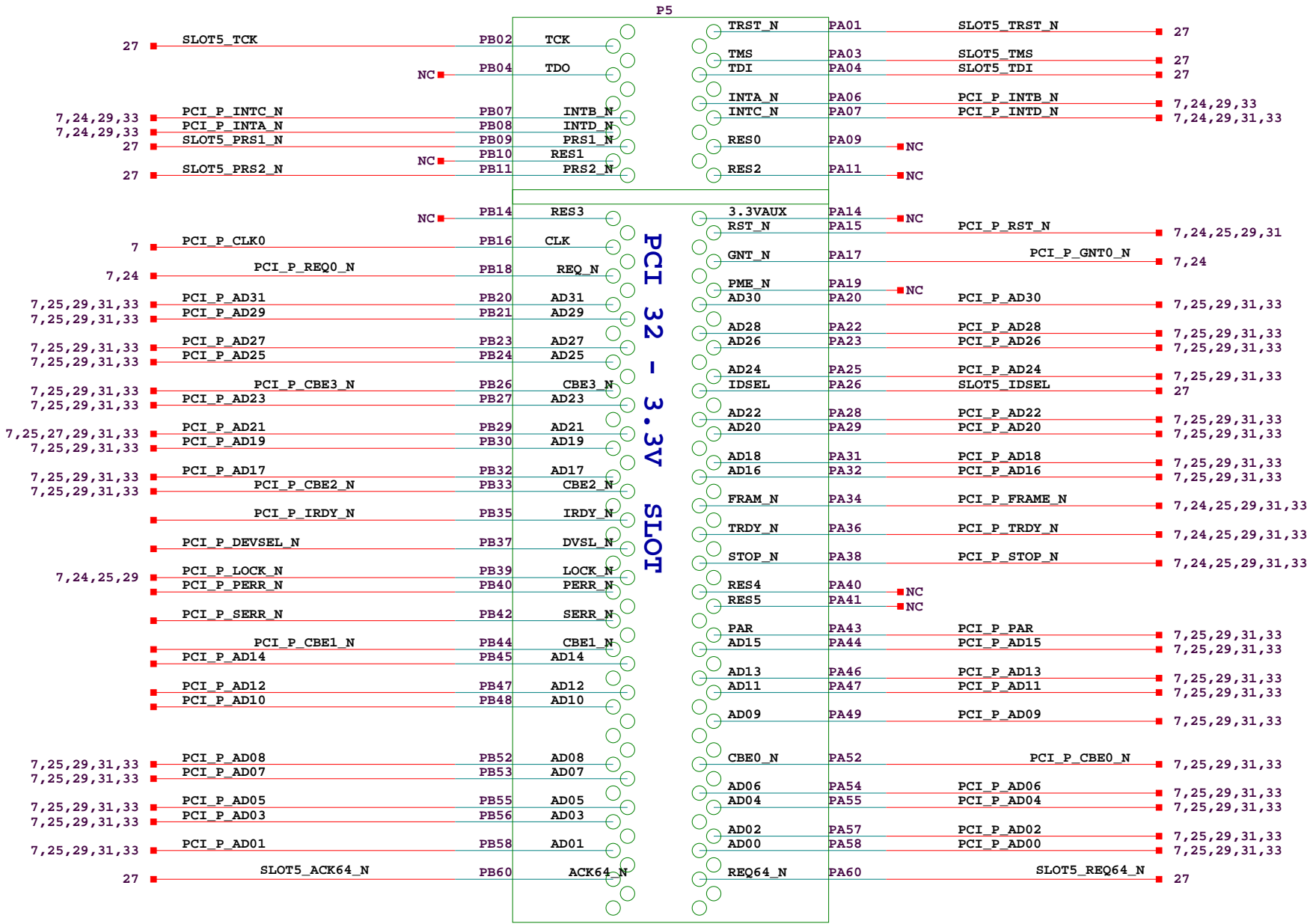
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VCC12V\_N;PB01  
VCC5V;PA05,PB05,PB06,PA08  
VCC5V;PA61,PB61,PA62,PB62  
VCC3V3;PA21,PB25,PA27,PB31,PA33,PB36  
VCC3V3;PA39,PB41,PB43,PA45,PA53,PB54

VCCIO VCC5V;PA10,PA16,PB19,PB59,PA59

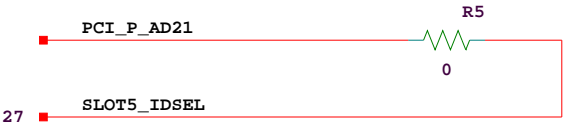
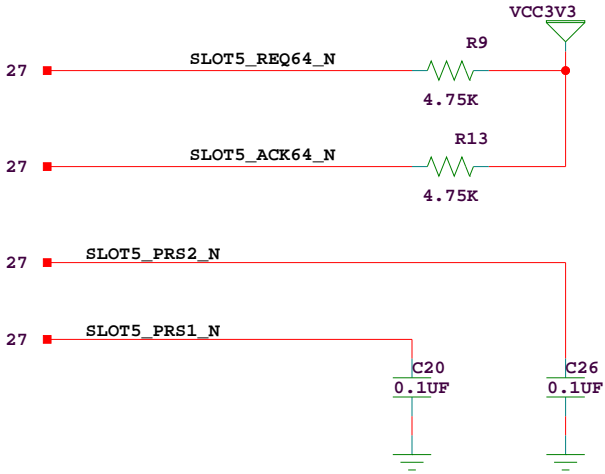
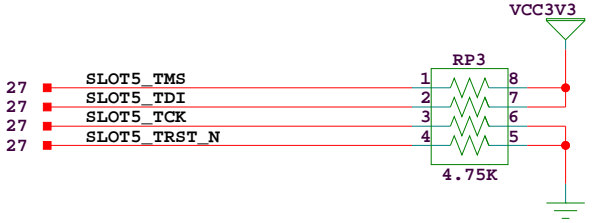
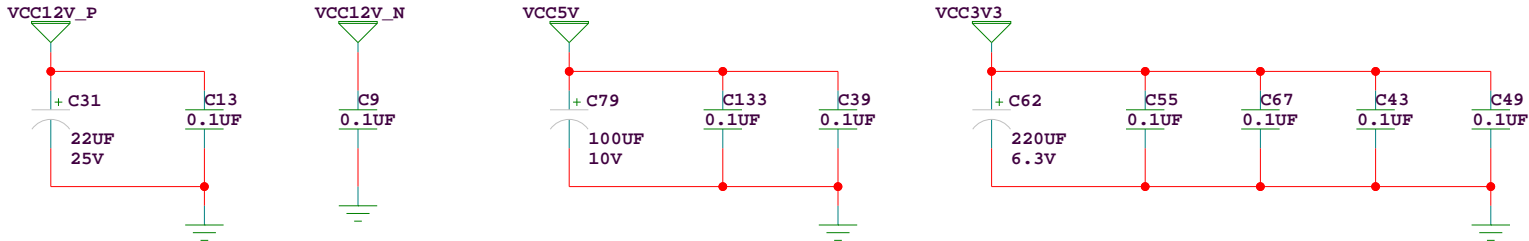
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GND;PB28,PA30,PB34,PA35,PA37,PB38  
GND;PA42,PB46,PA48,PB49,PA56,PB57  
GND;PB12,PA12,PB13,PA13



		SCH P/N	0381203
		ART P/N	0531499
		FAB P/N	1280372
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLATFOrm			
PCI SLOT 6, 5.0V, SECONDARY BUS			
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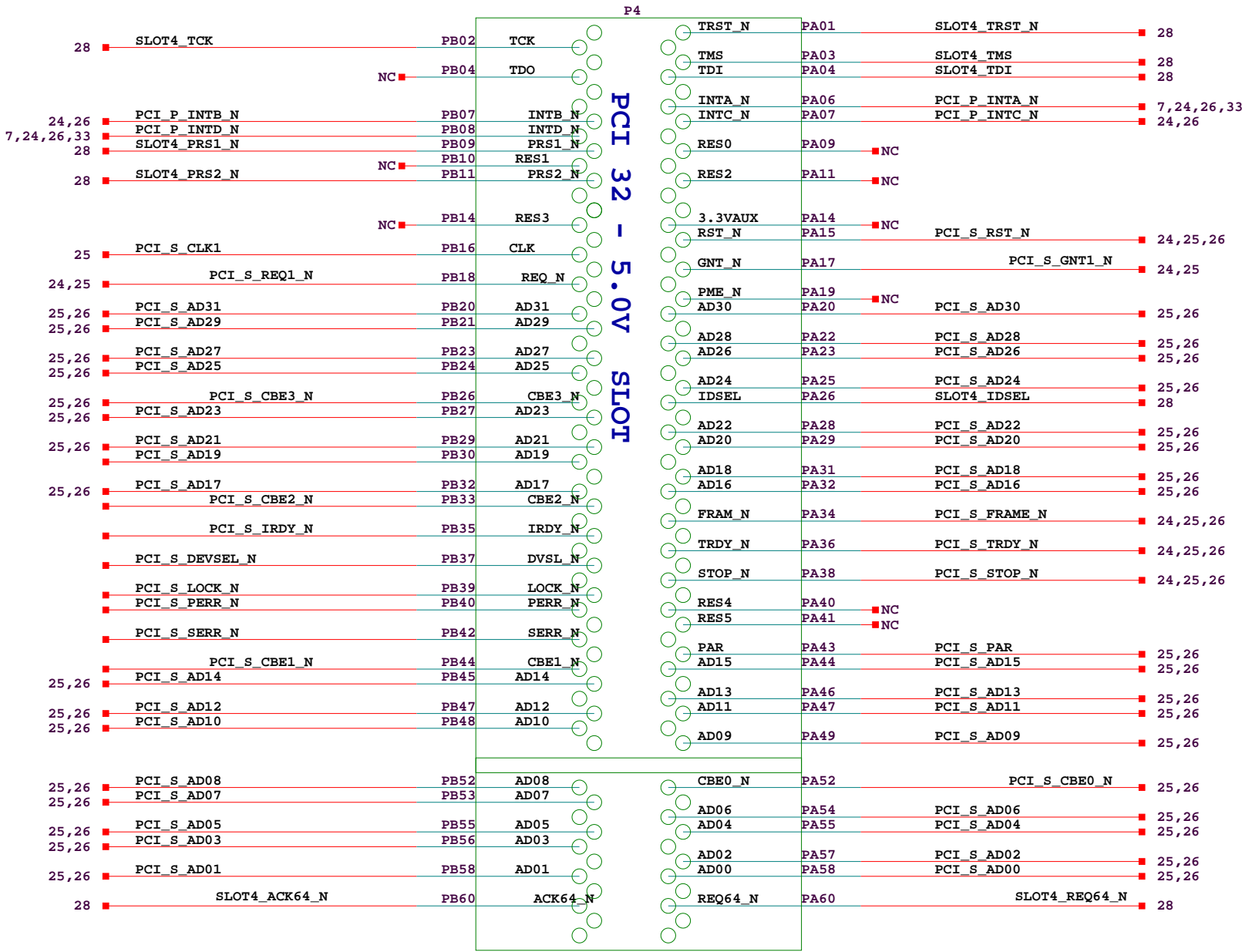
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VCC12V\_N;PB01  
VCC5V;PA05,PB05,PB06,PA08  
VCC5V;PA61,PB61,PA62,PB62  
VCC3V3;PA21,PB25,PA27,PB31,PA33,PB36  
VCC3V3;PA39,PB41,PB43,PA45,PA53,PB54  
  
VCCIO VCC3V3;PA10,PA16,PB19,PB59,PA59  
  
GND;PB03,PB15,PB17,PA18,PB22,PA24  
GND;PB28,PA30,PB34,PA35,PA37,PB38  
GND;PA42,PB46,PA48,PB49,PA56,PB57  
GND;PB50,PA50,PB51,PA51



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FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFORM  
PCI SLOT 5, 3.3V, PRIMARY BUS

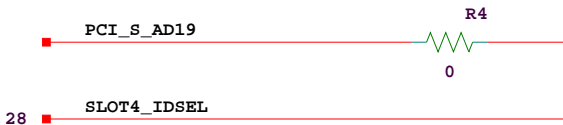
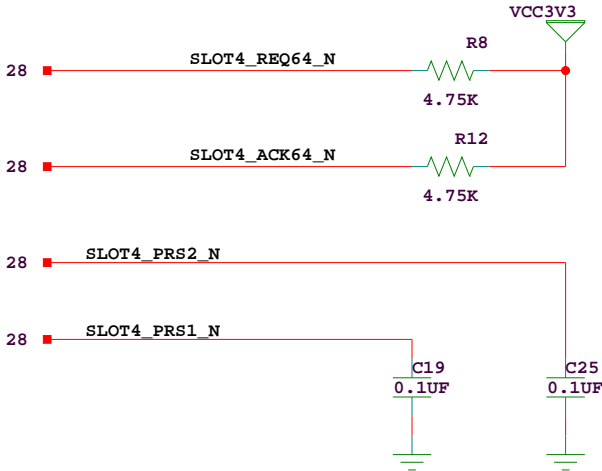
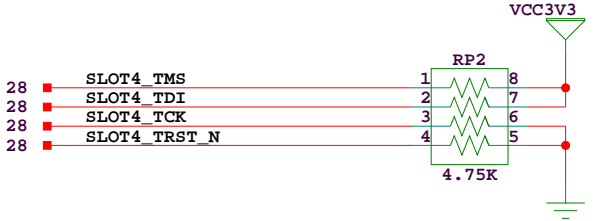
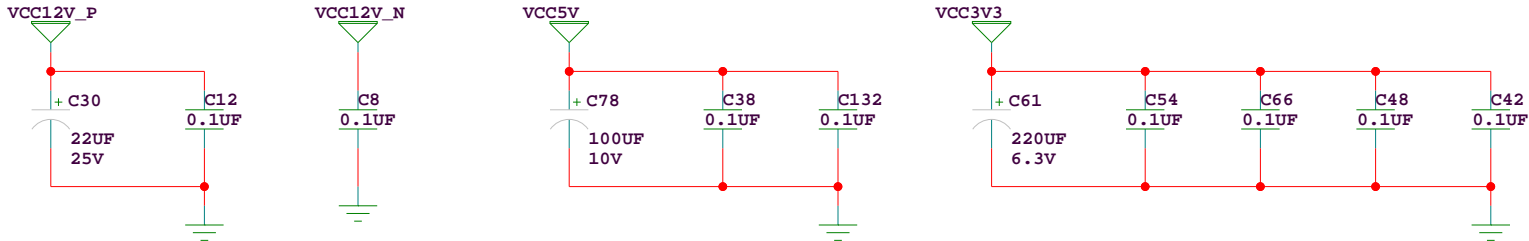
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VCC12V\_P;PA02  
VCC12V\_N;PB01  
VCC5V;PA05,PB05,PB06,PA08  
VCC5V;PA61,PB61,PA62,PB62  
VCC3V3;PA21,PB25,PA27,PB31,PA33,PB36  
VCC3V3;PA39,PB41,PB43,PA45,PA53,PB54

VCCIO VCC5V;PA10,PA16,PB19,PB59,PA59

GND;PB03,PB15,PB17,PA18,PB22,PA24  
GND;PB28,PA30,PB34,PA35,PA37,PB38  
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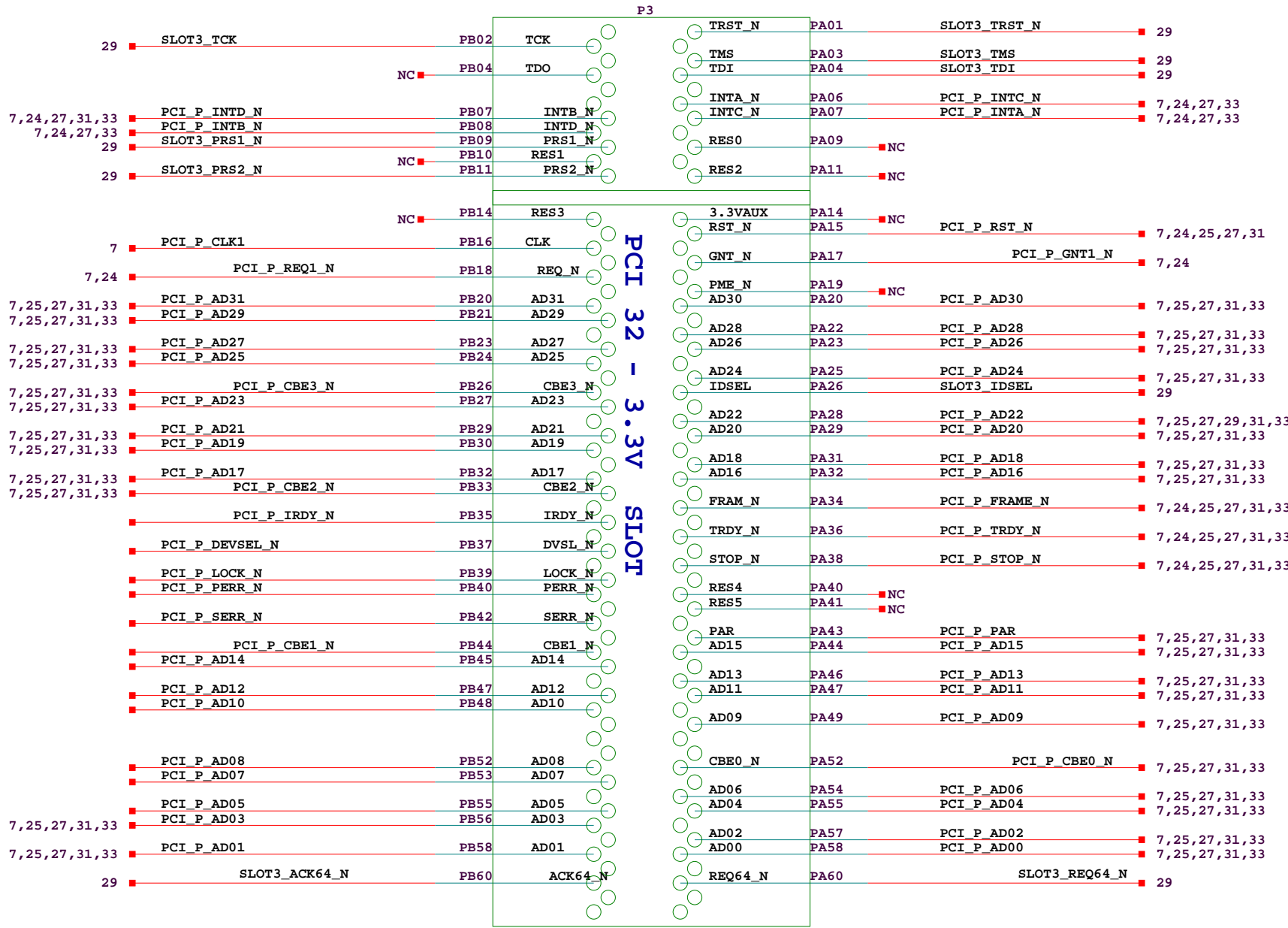
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ART P/N 0531499  
FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFORM  
PCI SLOT 4, 5.0V, SECONDARY BUS

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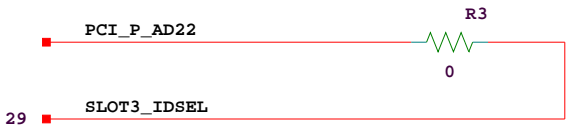
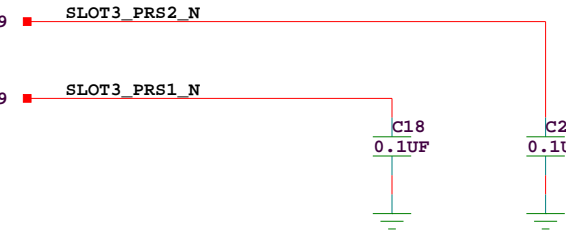
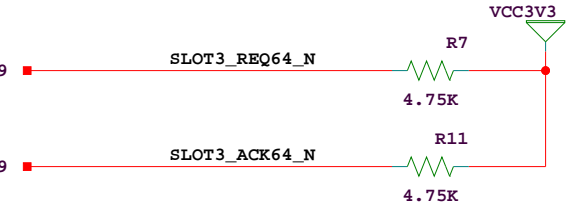
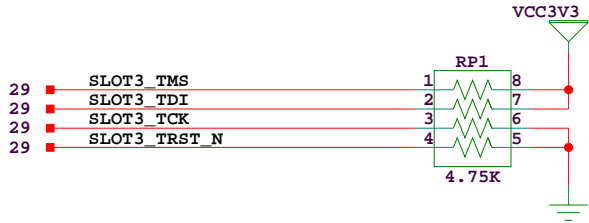
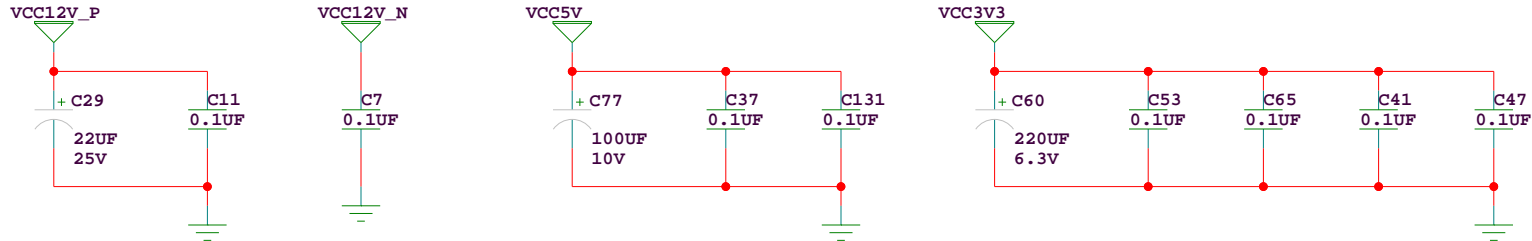
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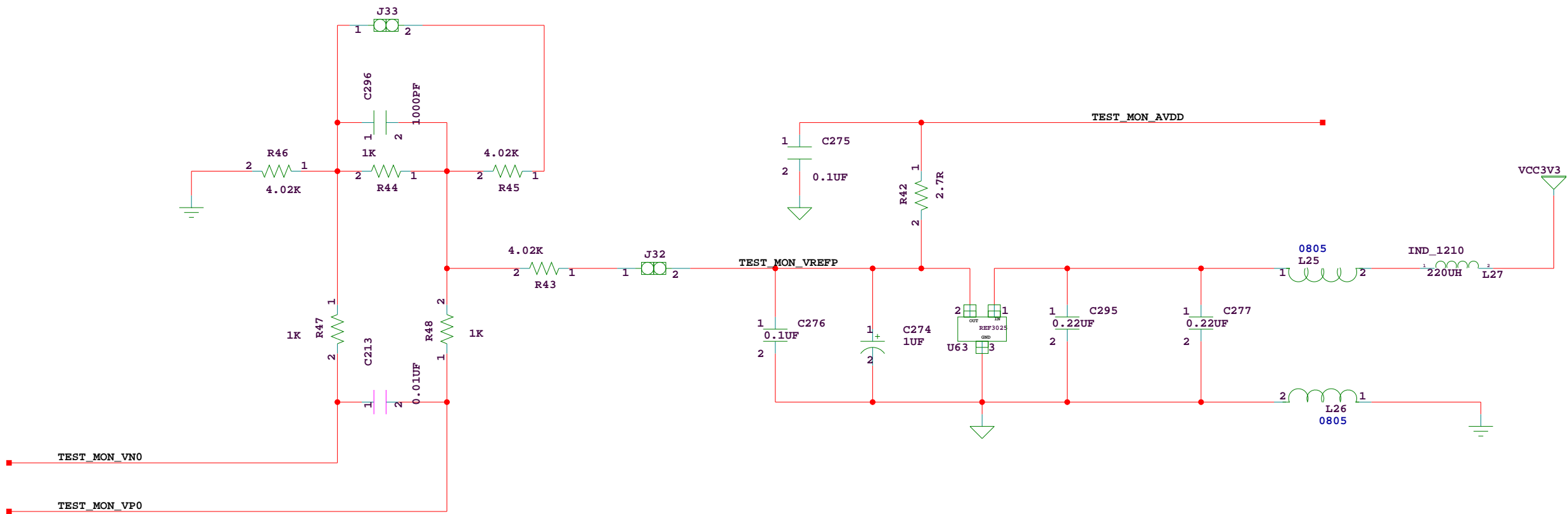
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VCC12V\_N;PB01  
VCC5V;PA05,PB05,PB06,PA08  
VCC5V;PA61,PB61,PA62,PB62  
VCC3V3;PA21,PB25,PA27,PB31,PA33,PB36  
VCC3V3;PA39,PB41,PB43,PA45,PA53,PB54

VCCIO VCC3V3;PA10,PA16,PB19,PB59,PA59

GND;PB03,PB15,PB17,PA18,PB22,PA24  
GND;PB28,PA30,PB34,PA35,PA37,PB38  
GND;PA42,PB46,PA48,PB49,PA56,PB57  
GND;PB50,PA50,PB51,PA51

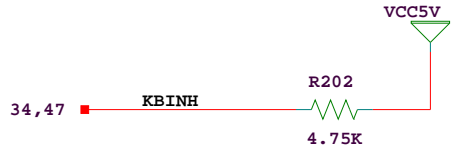
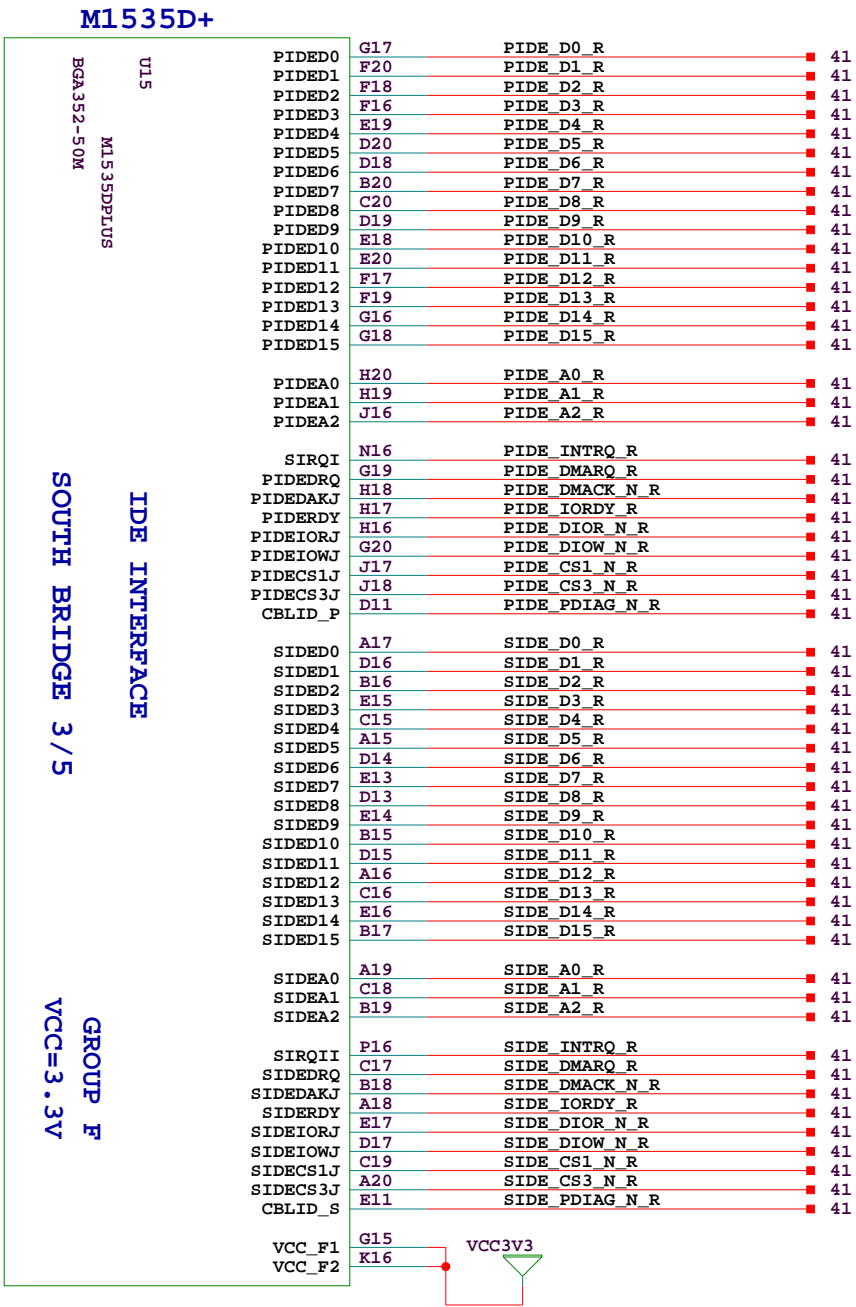
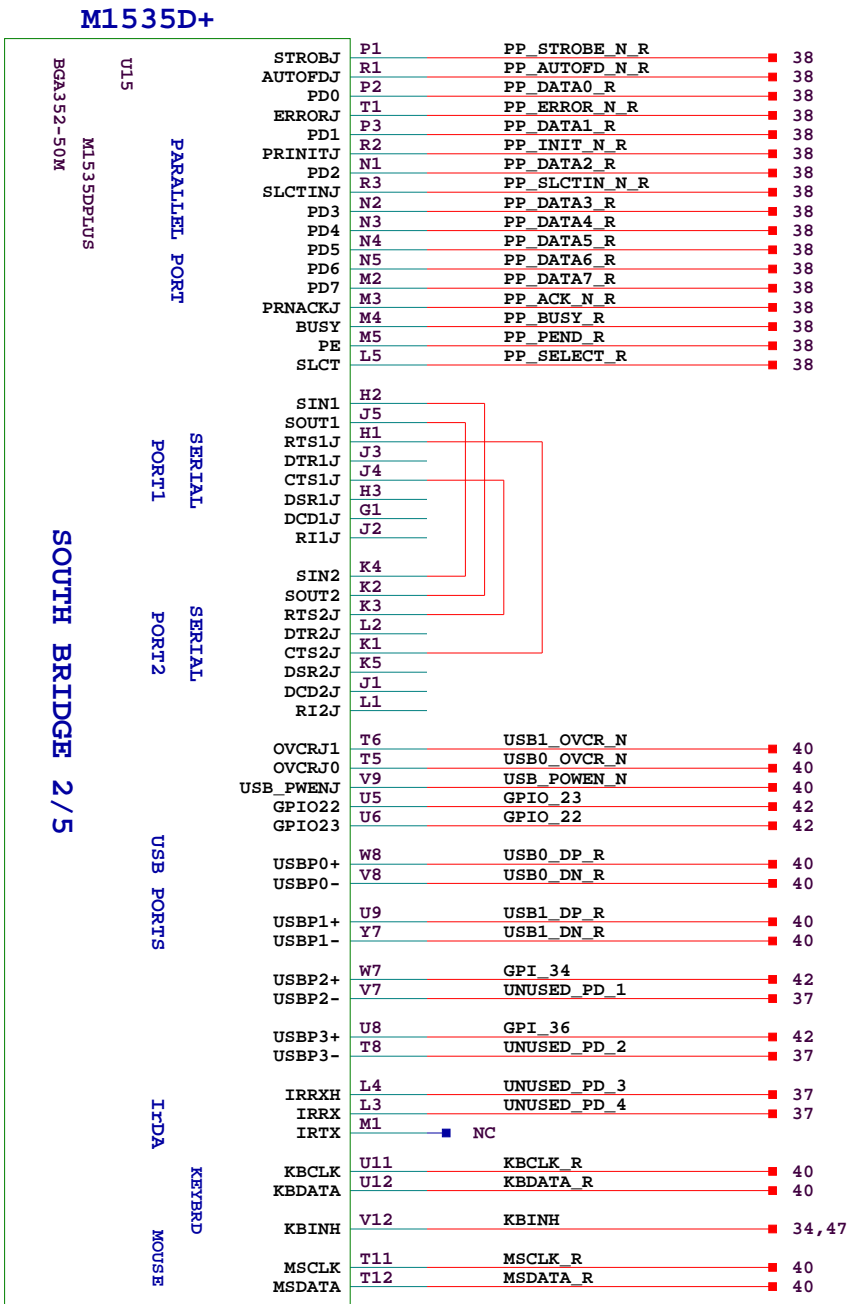


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		ART P/N	0531499
		FAB P/N	1280372
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFORM			
PCI SLOT 3, 3.3V, PRIMARY BUS			
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		ART P/N	0531499
		FAB P/N	1280372
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFRTOM TEST INTERFACE			
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FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLATFORM  
PCI SOUTH BRIDGE, PART 2-3

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M1535D+

BGA352-SOM  
M1535DPLUS  
U15

POWER MANAGEMENT UNIT1

POWER MANAGEMENT UNIT2

SOUTH BRIDGE 4/5

AC97 INTERFACE

SOUND CNTRL

RSM_RSTJ	W10	RSM_RSTJ	
SUSPENDJ	W13	NC	
PWRBTNJ	Y15	UNUSED_PU33V_5	
SLPBTNJ	V10	UNUSED_PU33V_6	
OFF_PWR0	V14	NC	
OFF_PWR1	W14	NC	
OFF_PWR2	Y14	NC	
SPLED	Y13	SPLED	
RSM_ENT0	W11	RSM_ENT0	
RSM_ENT1	Y11	UNUSED_PU5V_3	
RSM_ENT8	Y10	UNUSED_PD_5	
PMEJ	W12	UNUSED_PU33V_7	
RI	V11	UNUSED_PD_6	
IRQ8J	Y12	UNUSED_PU5V_4	
RSM_ENT3	T9	UNUSED_PD_7	
SMIJ	A13	NC	
STPCLKJ	B14	NC	
SLEEPJ	D12	NC	
ZZ	E12	UNUSED_PU5V_5	37
NUINP1	A11	UNUSED_PD_8	37
CPU_STPJ	C10	NC	
THRMJ	T18	IIC_THERM_N	6,45
SQWO	V6	SQWO	36
SMBCLK	T7	SMB_SCL	35
SMBDATA	U7	SMB_SDA	35
SMBALERTJ	T2	IIC_ALERT_N	6,45
GPI25	E9	GPI_25	42
GPO34	P18	GPO_34	36,42
GPO35	P19	GPO_35	36,42
ACRESETJ	Y9	AC_RESET_N	43
ACSDATA_IN0	W9	AC_SDATA_IN0	43
ACSDATA_IN1	Y8	UNUSED_PD_9	37
ACSDATA_OUT	U1	AC_SDATA_OUT	43
ACSYNC	P4	AC_SYNC	43
ACBIT_CLK	P5	AC_BIT_CLK	43
ACMIDI_TXD	R4	NC	
ACMIDI_RXD	T4	UNUSED_PD_10	37
ACGAME0	V1	NC	
ACGAME1	V2	NC	
ACGAME2	V3	NC	
ACGAME3	W1	NC	
ACGAME4	W2	NC	
ACGAME5	W3	NC	
ACGAME6	Y1	NC	
ACGAME7	Y2	NC	
ACGP_UPJ	U3	UNUSED_PU5V_7	37
ACGP_MUTEJ	U2	UNUSED_PU5V_8	37
ACGP_DOWNJ	R5	UNUSED_PU5V_9	37
FANOUT1	W5	NC	
FANOUT2	V5	NC	
FANIN2	Y5	UNUSED_PU5V_6	37
SPDIF_OUT	D9	NC	
SPDIF_IN	U4	UNUSED_PU5V_10	37

M1535D+

BGA352-SOM  
M1535DPLUS  
U15

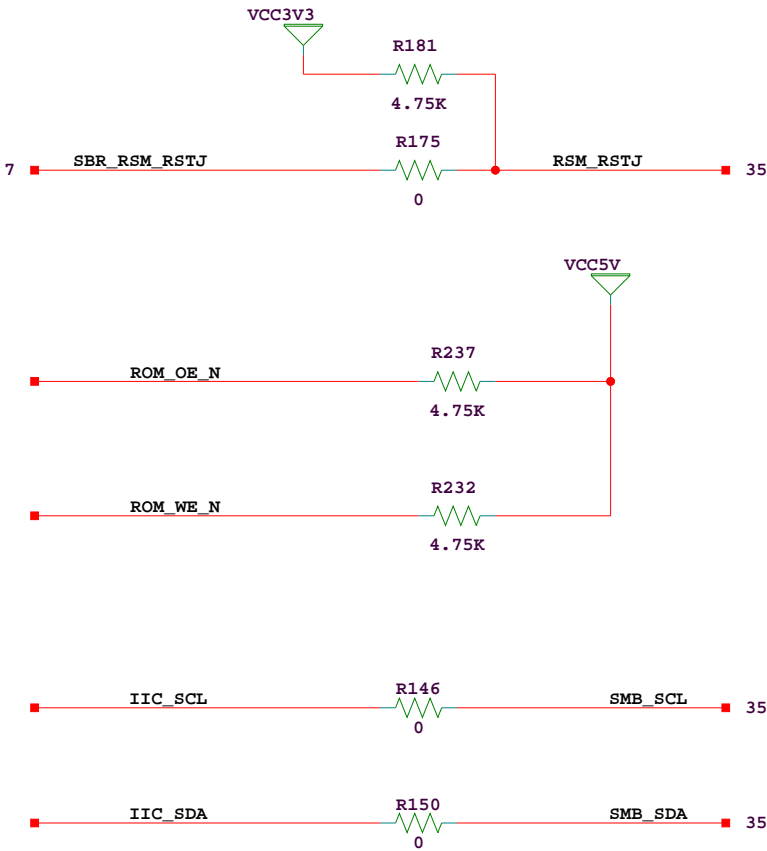
XD(ISA) BUS

SOUTH BRIDGE 5/5

FLOPPY DISK

MISCELLANEOUS LOGIC

XD0	U20	ROM_D0	42
XD1	U19	ROM_D1	42
XD2	U18	ROM_D2	42
XD3	Y20	ROM_D3	42
XD4	W20	ROM_D4	42
XD5	V20	ROM_D5	42
XD6	Y19	ROM_D6	42
XD7	W19	ROM_D7	42
SA0	V19	ROM_A0	42
SA1	Y18	ROM_A1	42
SA2	W18	ROM_A2	42
SA3	V18	ROM_A3	42
SA4	Y17	ROM_A4	42
SA5	W17	ROM_A5	42
SA6	V17	ROM_A6	42
SA7	U17	ROM_A7	42
SA8	T17	ROM_A8	42
SA9	R17	ROM_A9	42
SA10	Y16	ROM_A10	42
SA11	W16	ROM_A11	42
SA12	V16	ROM_A12	42
SA13	U16	ROM_A13	42
SA14	T16	ROM_A14	42
SA15	W15	ROM_A15	42
BIOSA16	V15	ROM_A16	42
BIOSA17	U15	ROM_A17	42
BIOSA18	T15	ROM_A18	42
MEMRJ	T14	ROM_OE_N	35,42
MEMWJ	U14	ROM_WE_N	35,42
IORJ	T13	NC	
IOWJ	U13	NC	
RDATAJ	M18	UNUSED_PU5V_11	37
WGATEJ	L19	NC	
WDATAJ	L18	NC	
HDSELJ	M19	NC	
FD_DIRJ	L16	NC	
STEPJ	L17	NC	
DSKCHGJ	M20	UNUSED_PU5V_12	37
DRV0J	K19	NC	
DRV1J	K20	NC	
MOT0J	K17	NC	
MOT1J	K18	NC	
WPROTJ	M16	UNUSED_PU5V_13	37
TRK0J	L20	UNUSED_PU5V_14	37
INDEXJ	J20	UNUSED_PU5V_15	37
DENSEL	J19	NC	
SPKR	T19	SPKR	43,47
RTCAS	R20	NC	
RTCRW	R19	NC	
RTCDS	R18	NC	
ROMKBCSJ	T20	ROMKBCSJ	36,42
IRQSER	N19	UNUSED_PU5V_16	37
GPI24	M17	GPI_24	42
GPO29	N17	GPO_29	36,42
GPO30	N18	GPO_30	36,42
PCS0J	P20	PCS0J	36
PCS1J	R16	PCS1J	36
RUN_ENT0	Y3	GPIO_0	42
RUN_ENT1	V4	GPIO_1	42
RUN_ENT2	W4	GPIO_2	42
RUN_ENT3	Y4	GPIO_3	42
GPO10	T3	GPO_10	42
LFRAMEJ	N20	UNUSED_PU5V_17	37
LDRQJ	P17	UNUSED_PU5V_18	37



SCH P/N 0381203  
ART P/N 0531499  
FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLATFOrm  
PCI SOUTH BRIDGE, PART 4-5

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D

C

B

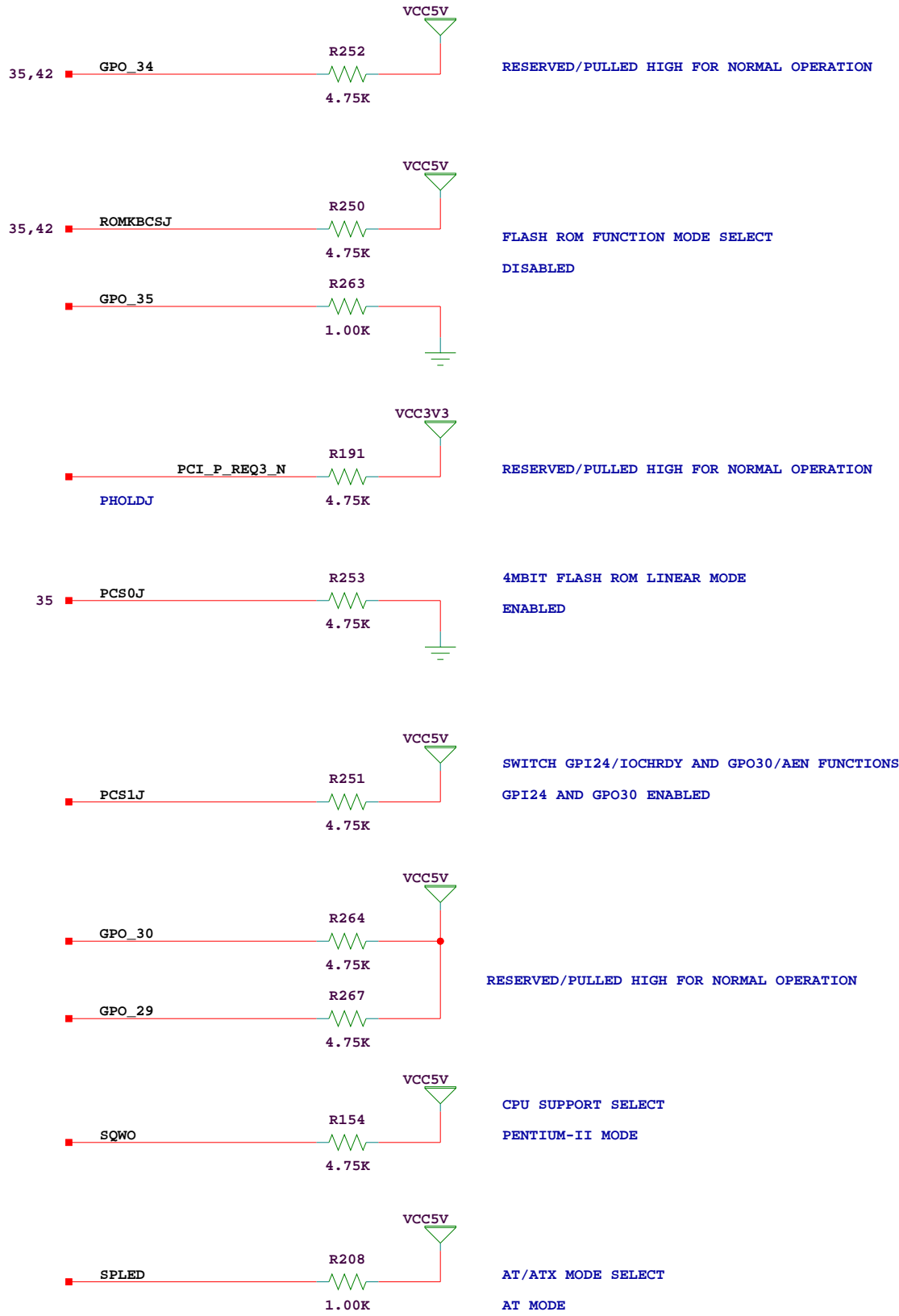
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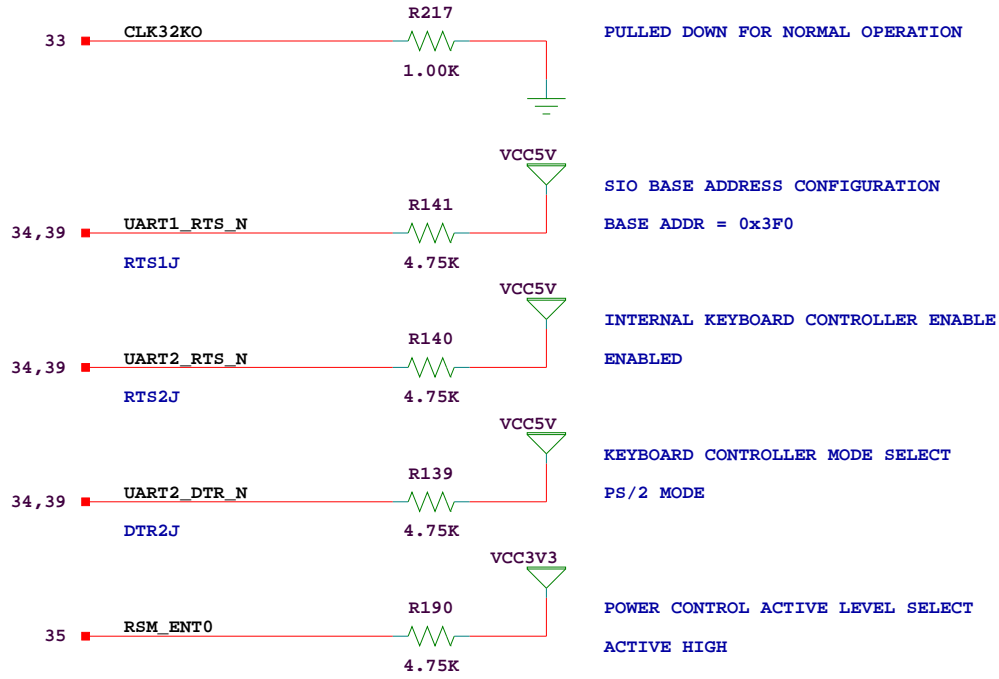
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A

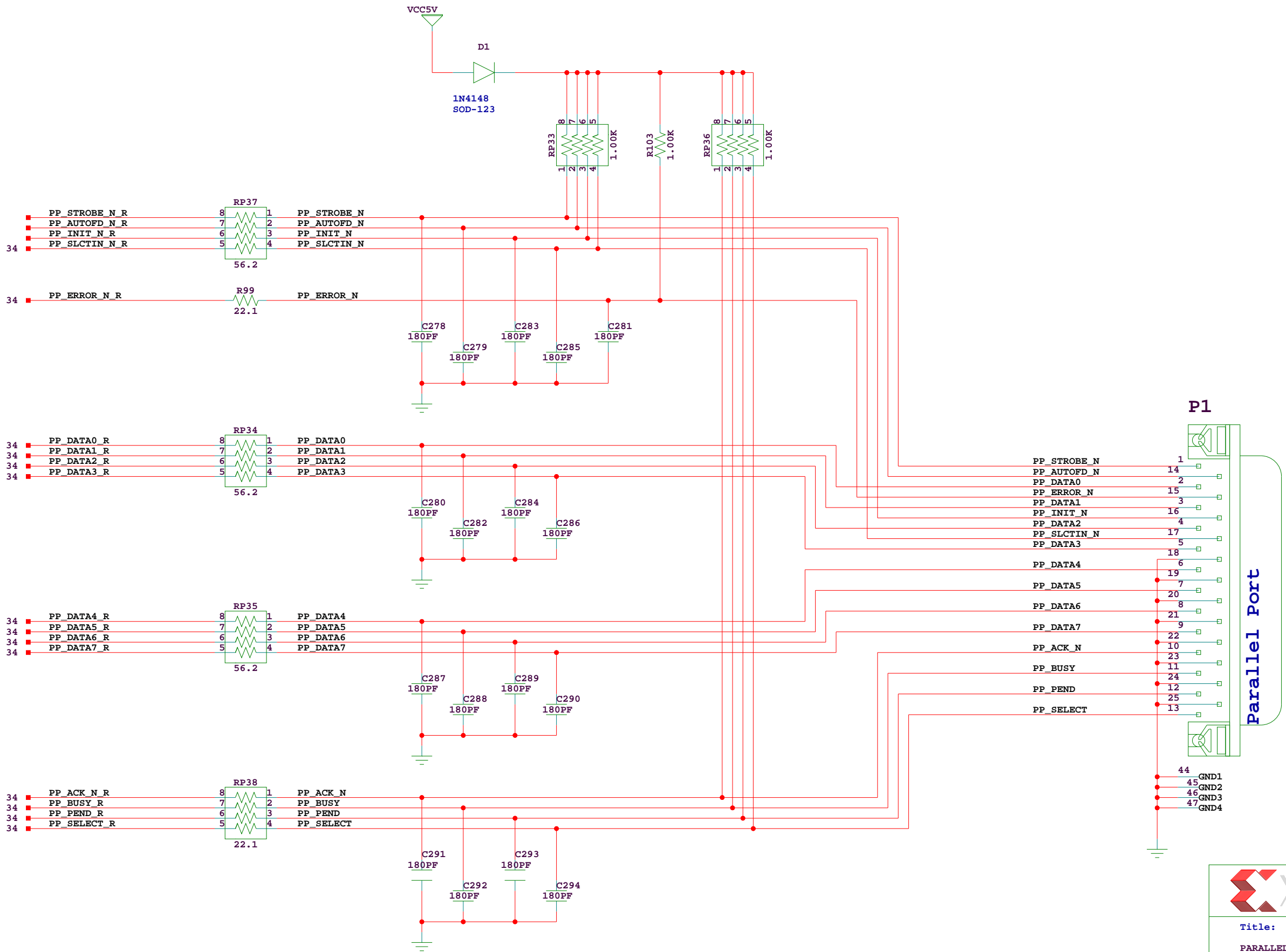



NOTE: AT MODE IS USED HERE TO DISABLE THE SOFT-POWER  
FUNCTIONALITY OF THE SOUTH BRIDGE



		SCH P/N	0381203
		ART P/N	0531499
		FAB P/N	1280372
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFORM PCI SOUTH BRIDGE, CONFIG RESISTORS			
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SCH P/N0381203

ART P/N0531499

FAB P/N1280372

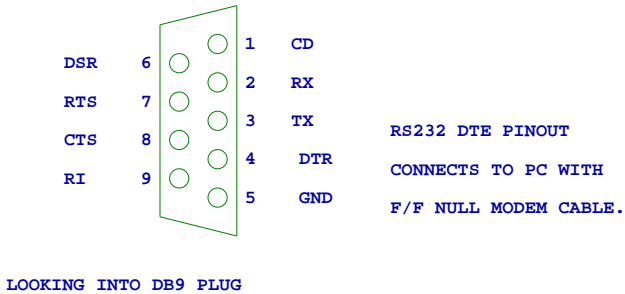
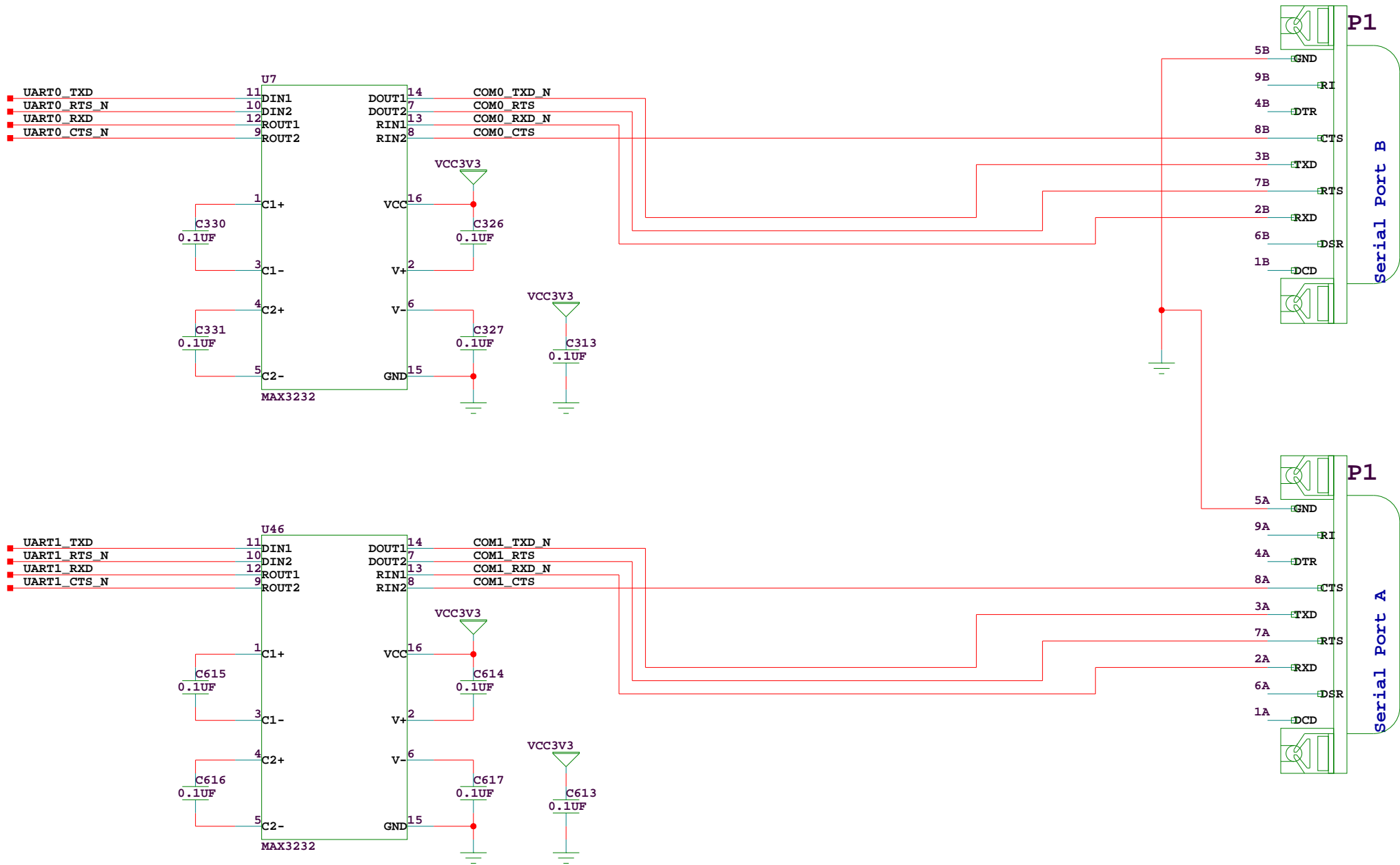
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SCH, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTRM

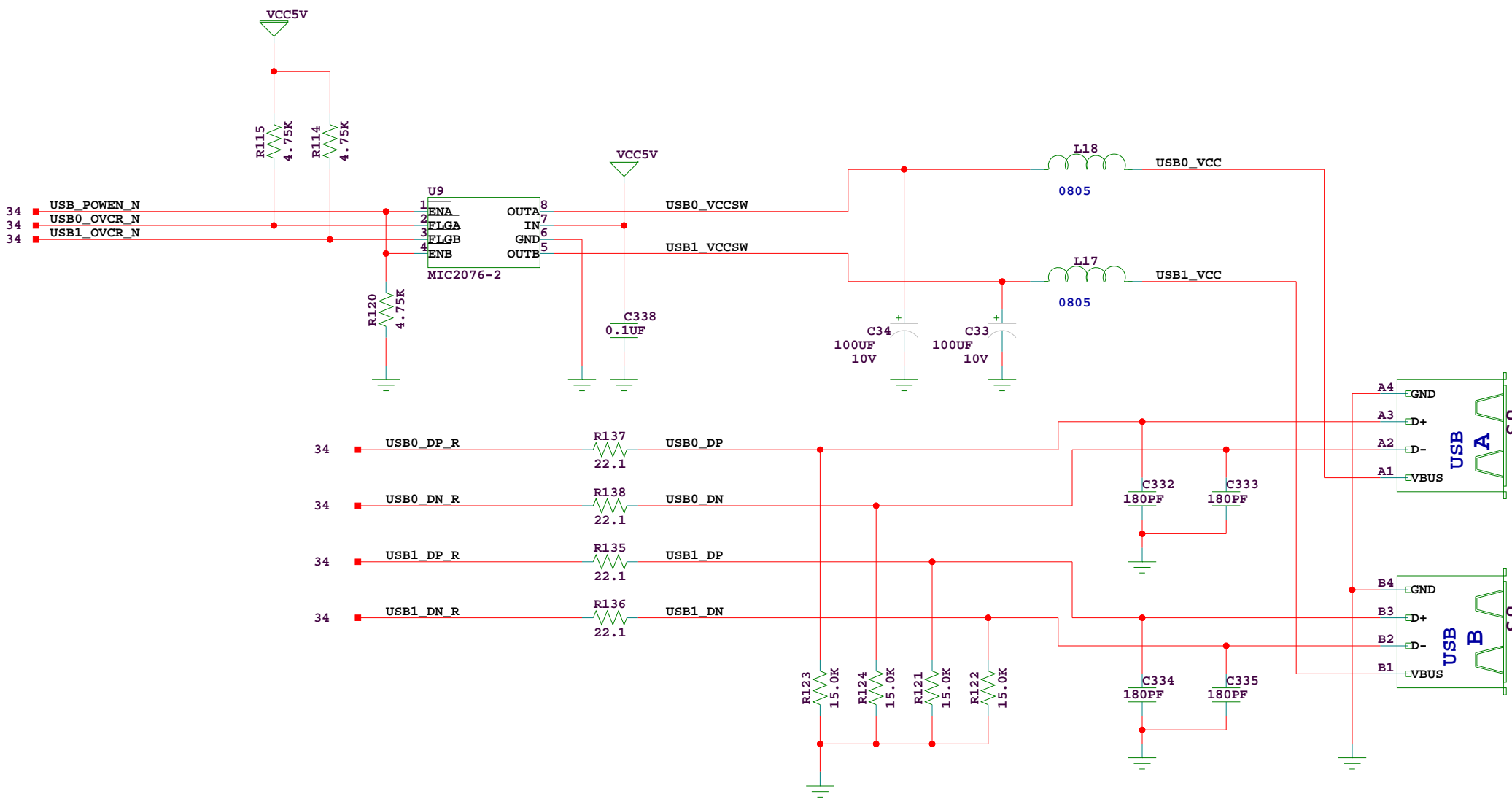
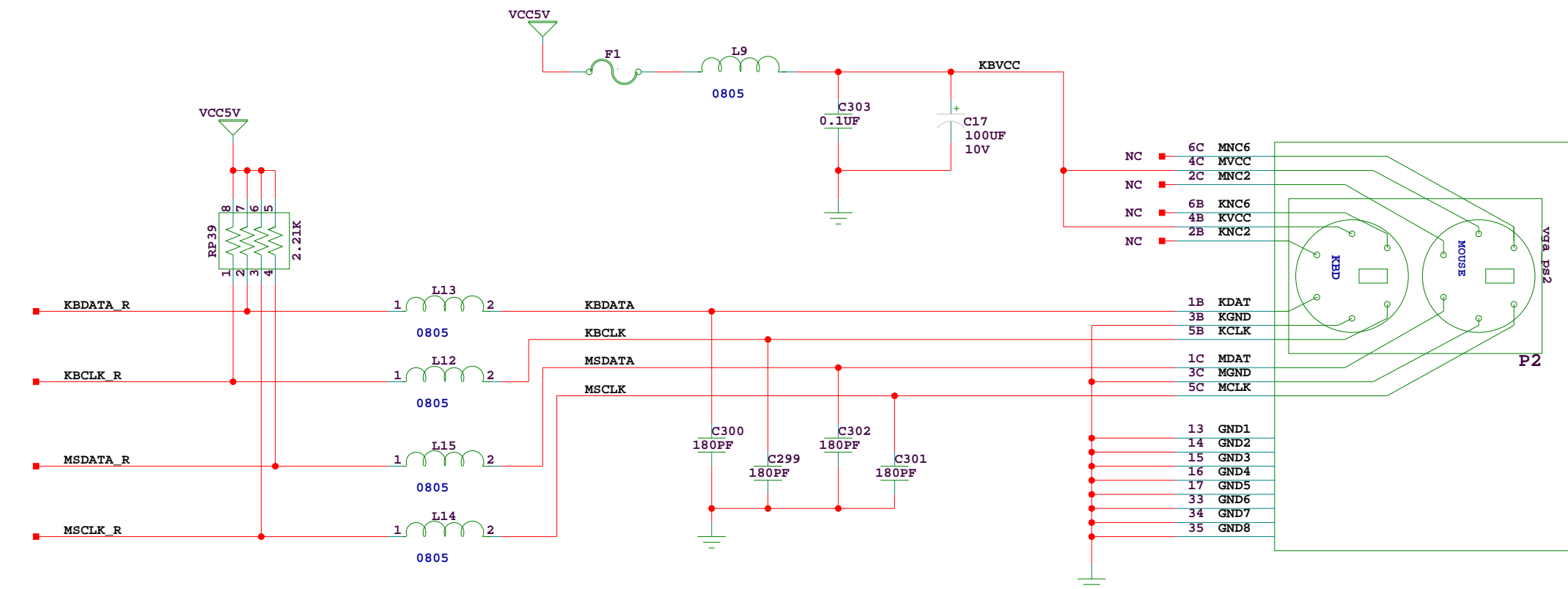
PARALLEL PORT INTERFACE

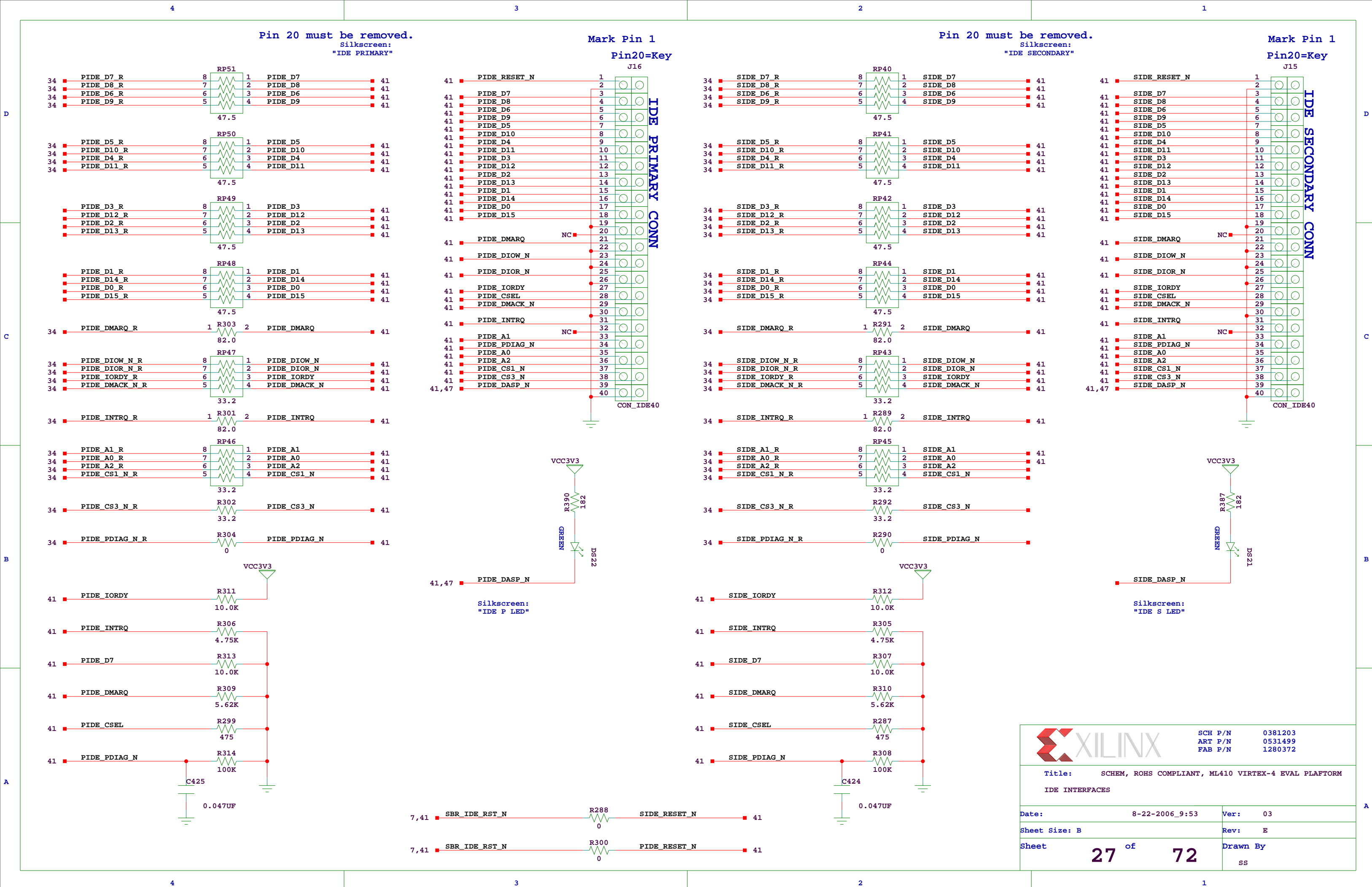
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Parallel Port

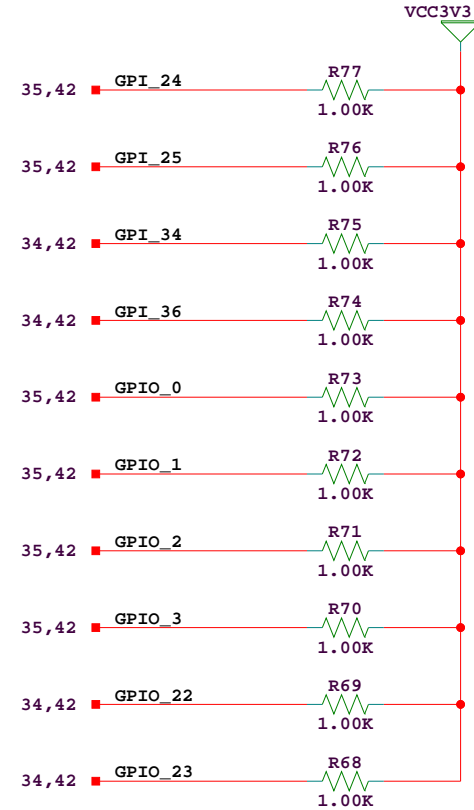
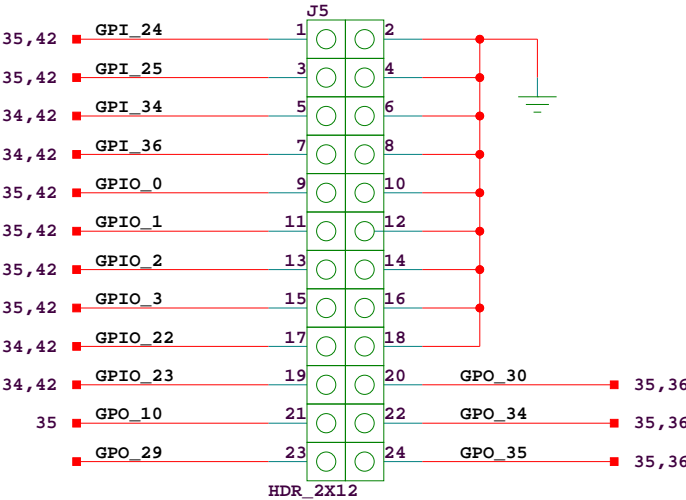
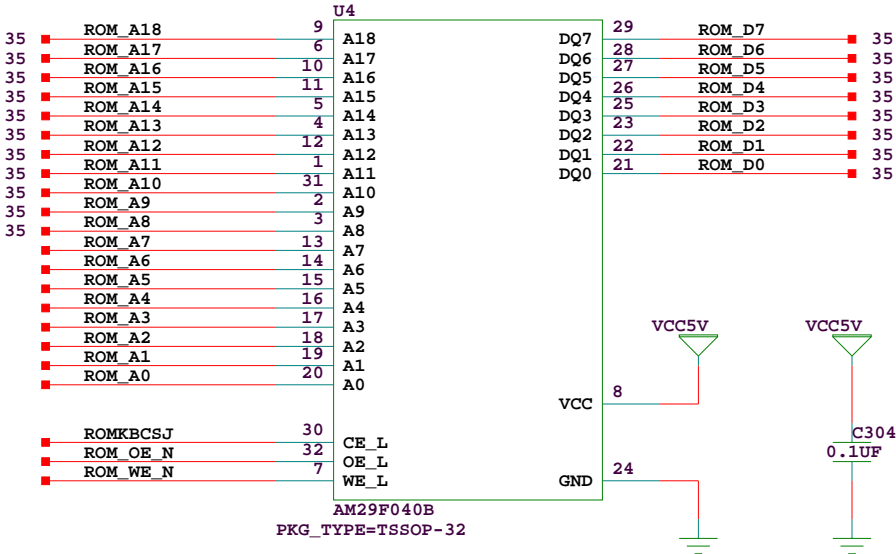


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		ART P/N	0531499
		FAB P/N	1280372
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFORM RS232 SERIAL PORT INTERFACE			
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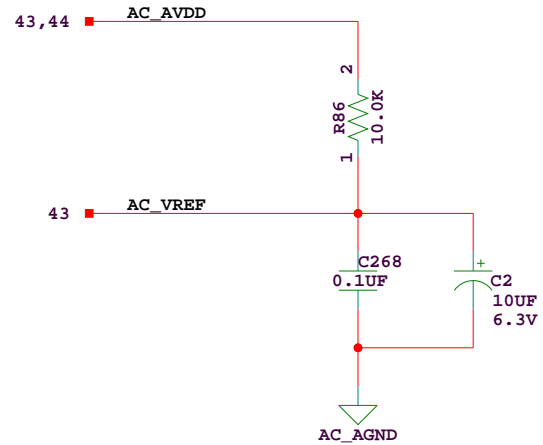
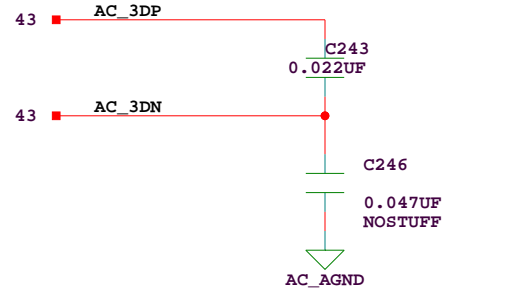
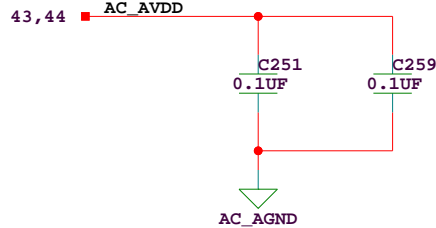
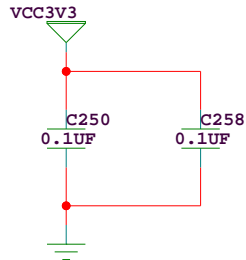
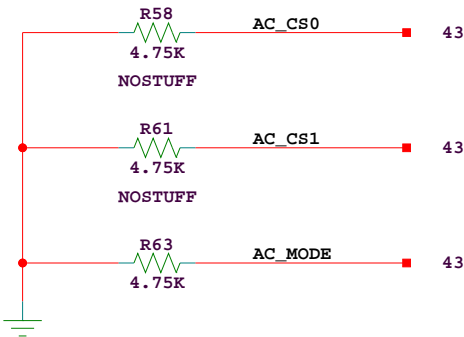
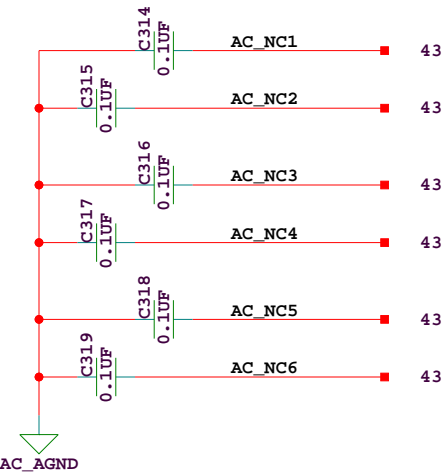
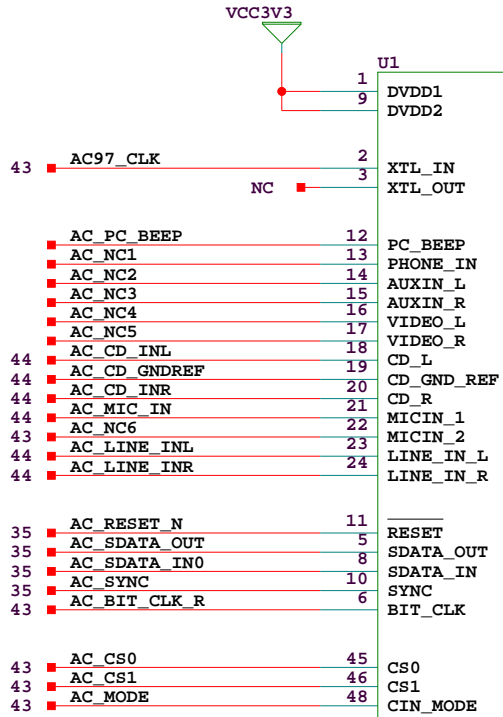
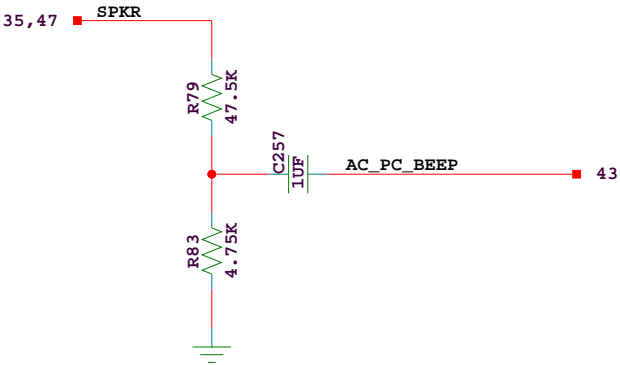
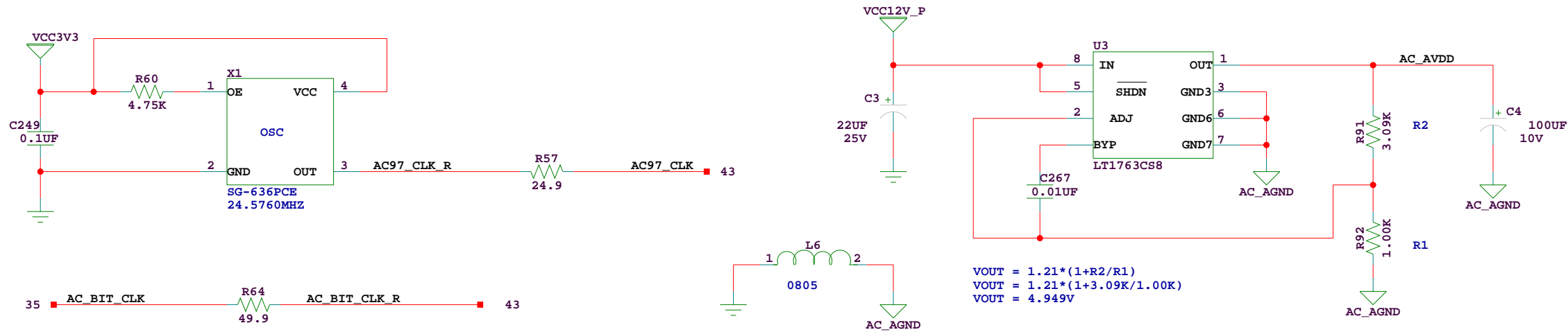
SOUTH BRIDGE  
GPIO HEADER



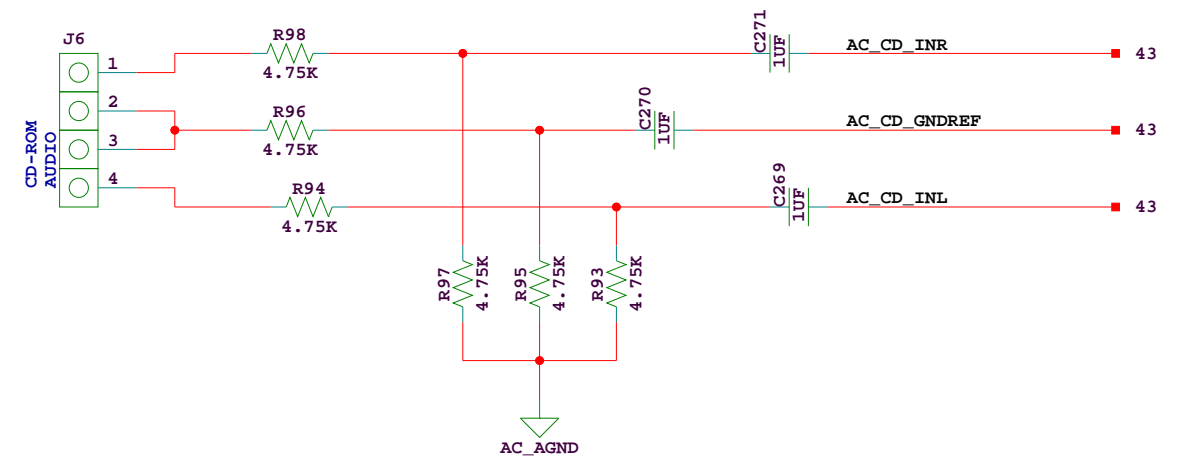
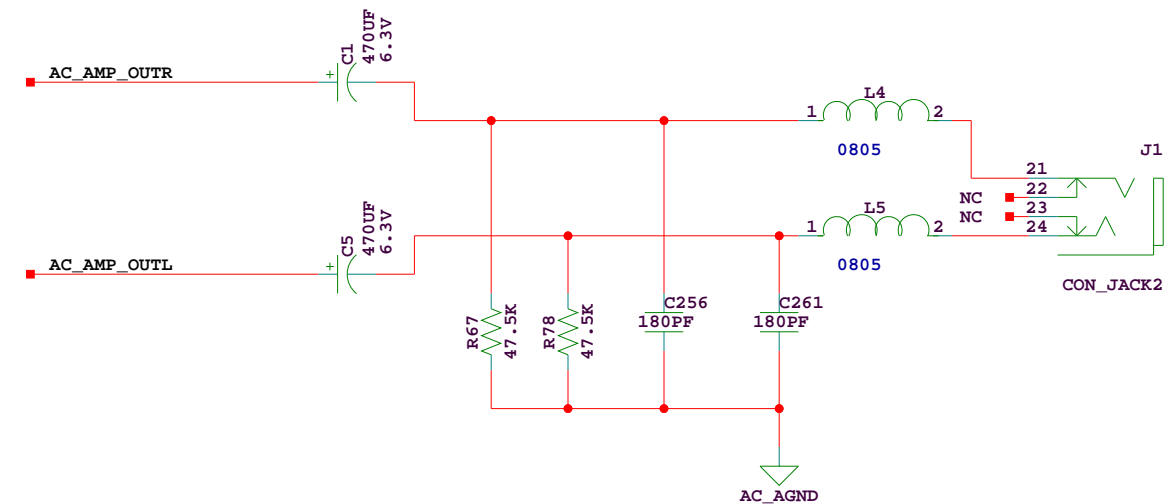
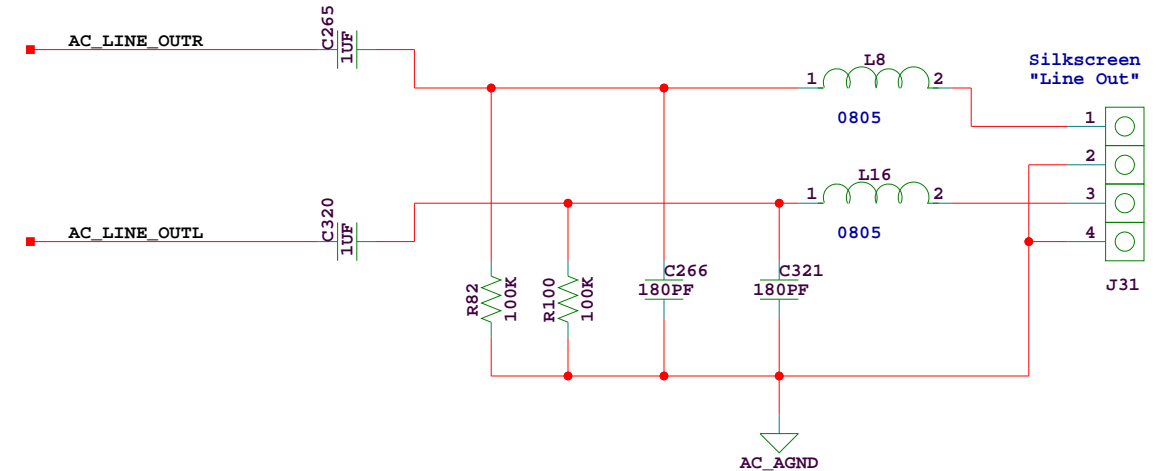
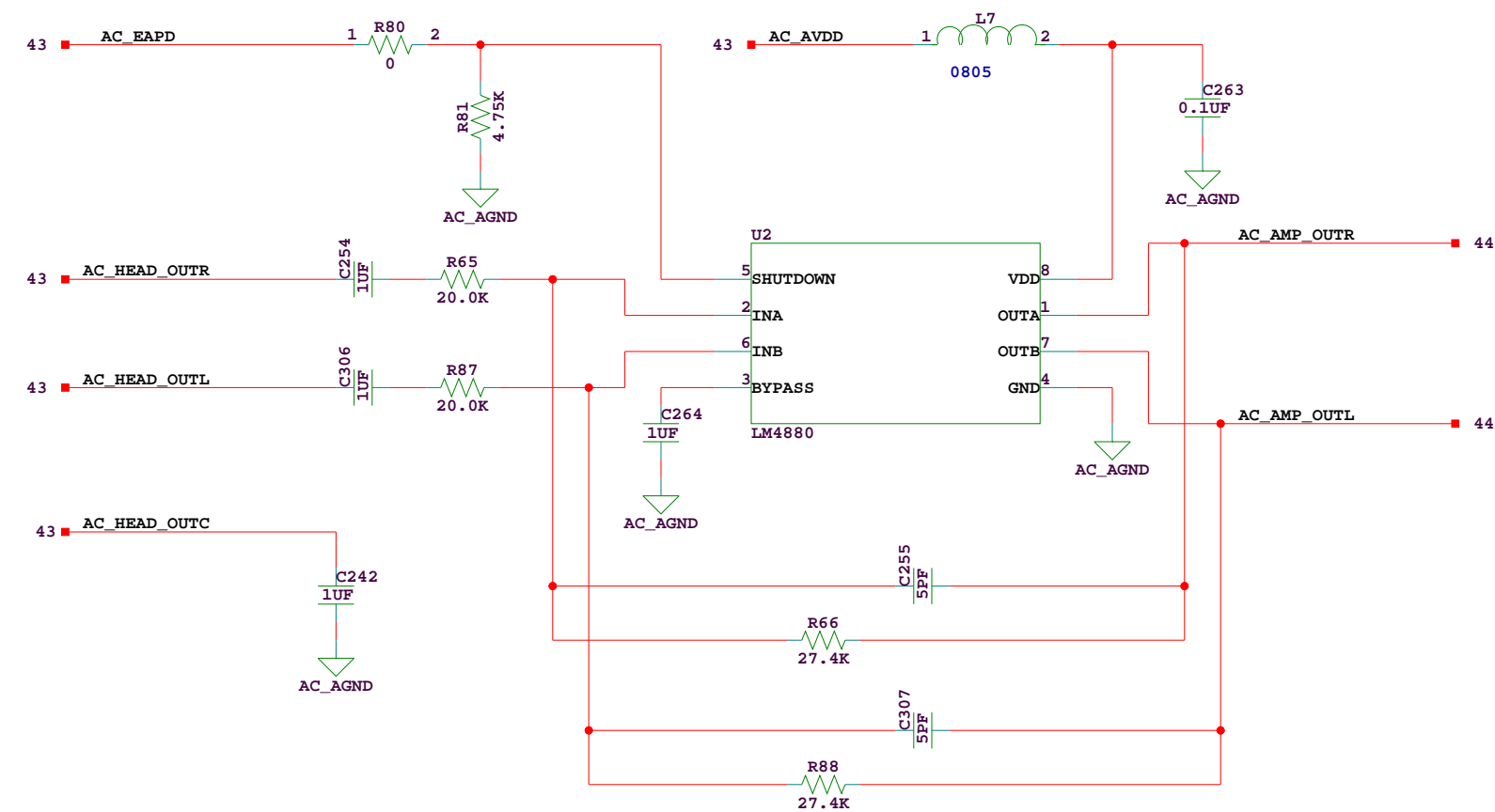
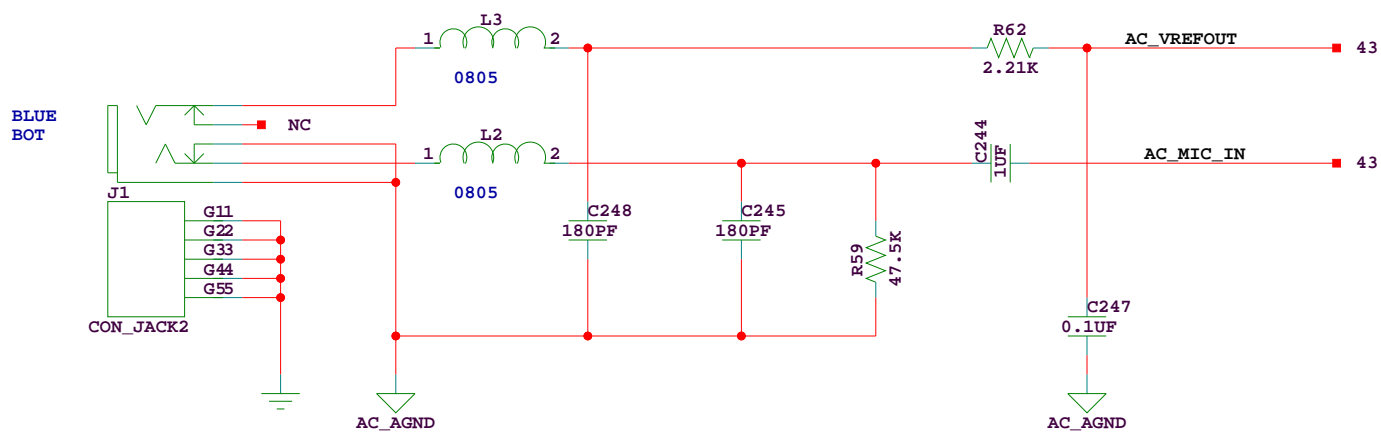
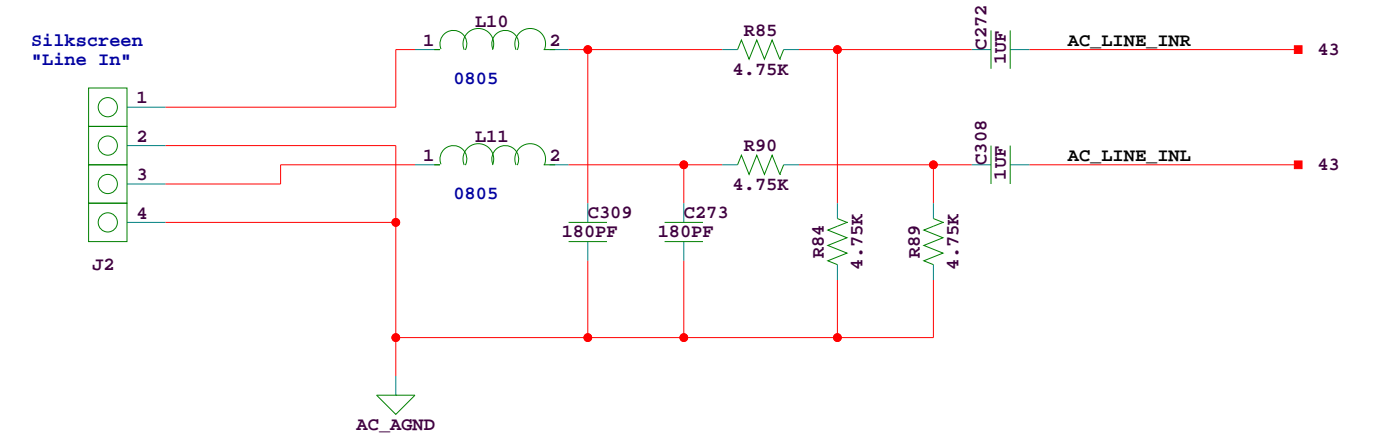
SCH P/N 0381203  
ART P/N 0531499  
FAB P/N 1280372


Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFORM  
SOUTH BRIDGE ROM AND GPIO

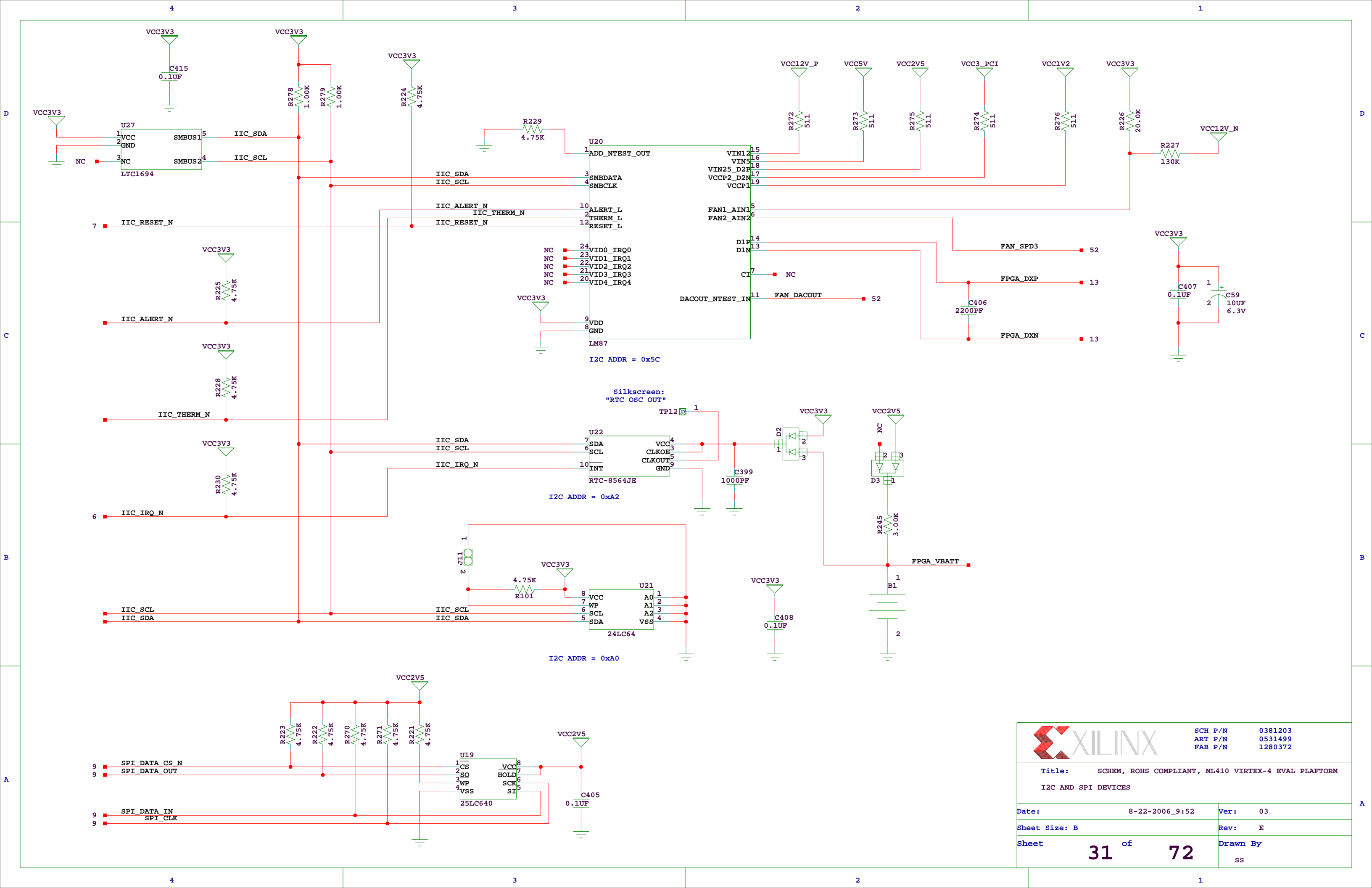
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		ART P/N	0531499
		FAB P/N	1280372
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFORM AC97 CODEC			
Date:	8-22-2006_9:52	Ver:	03
Sheet Size:	B	Rev:	E
Sheet	29 of 72	Drawn By	ss



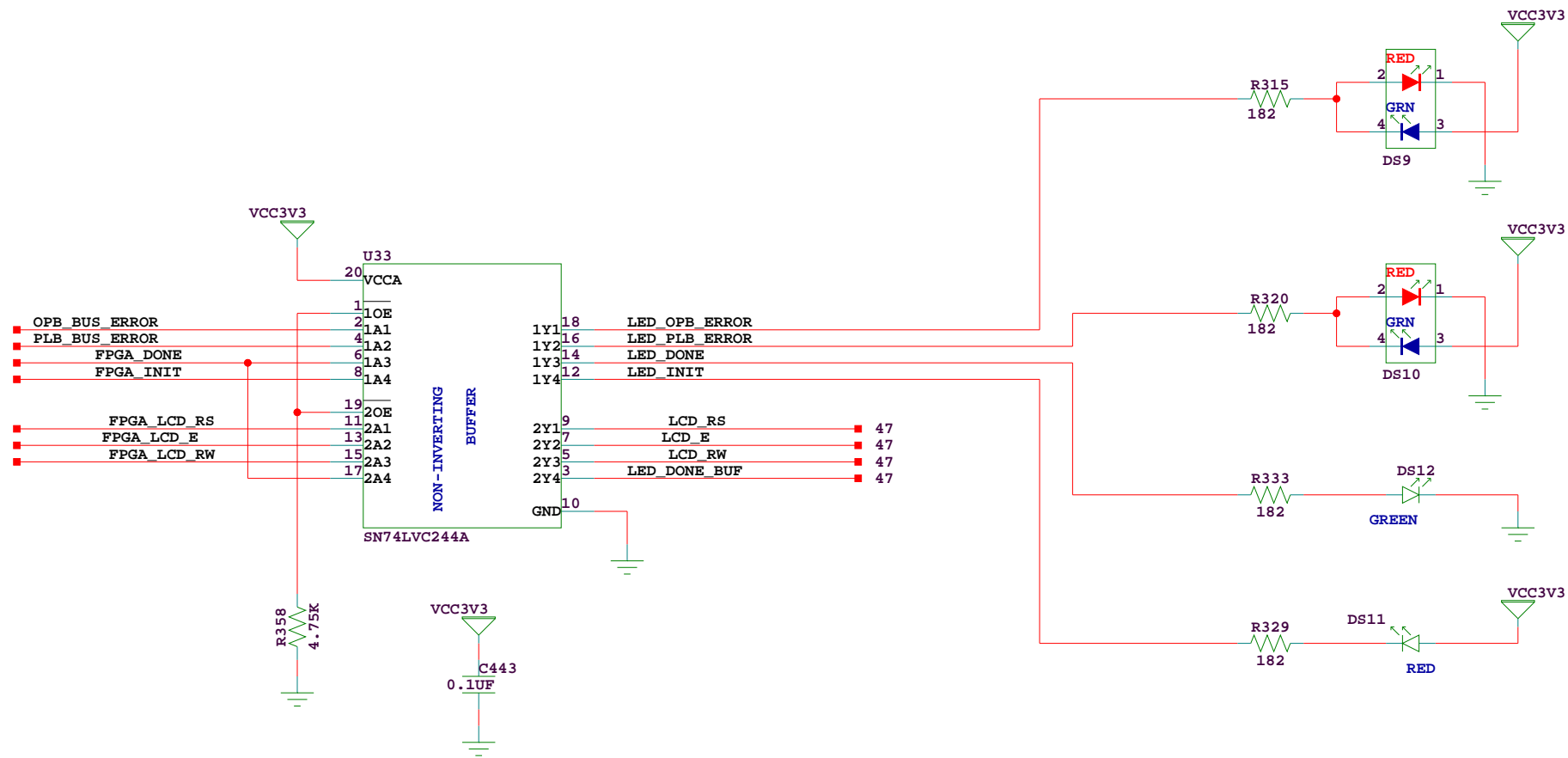
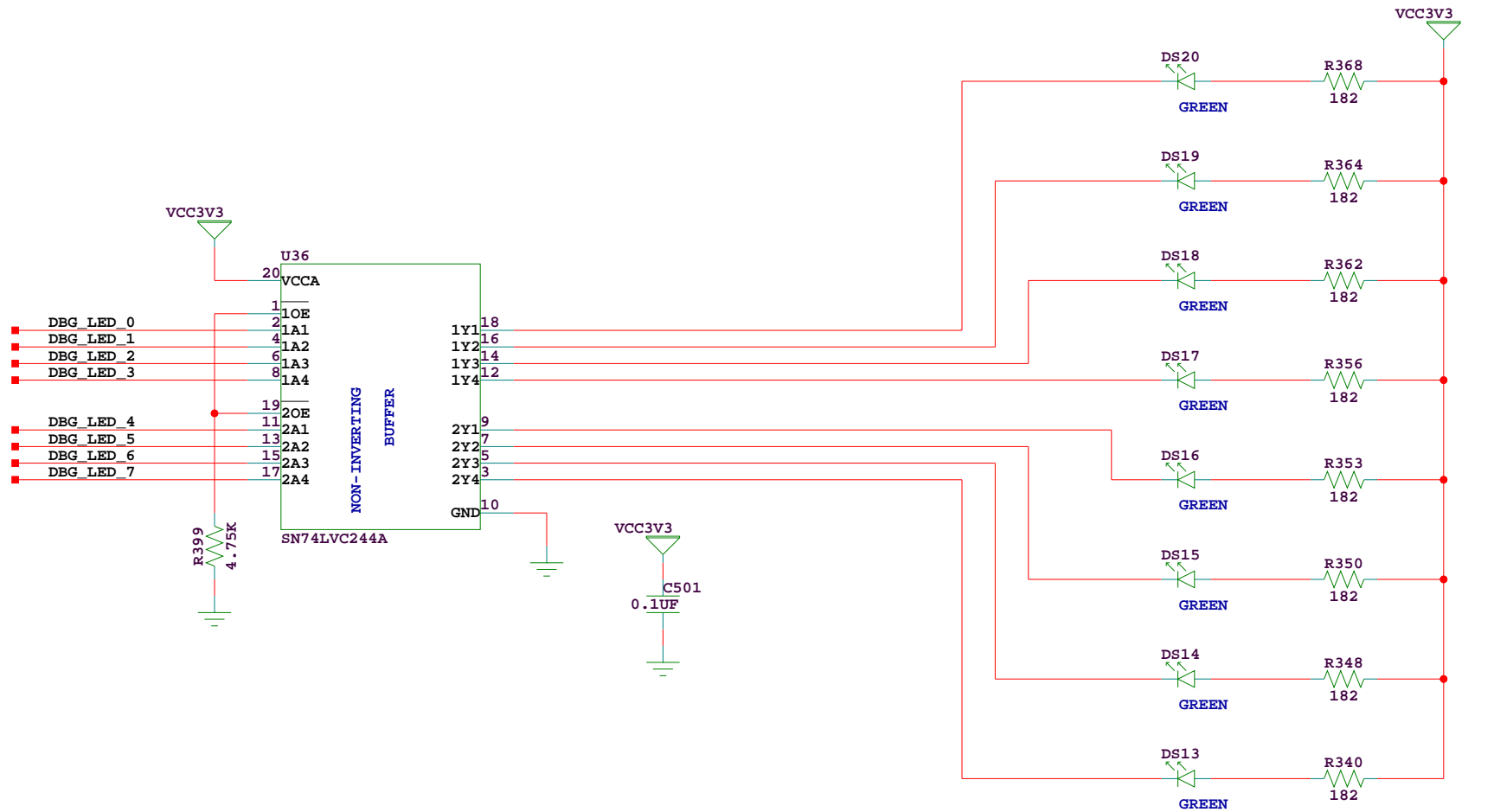
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<b>Title:</b> SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM AC97 CONNECTORS		
<b>Date:</b> 8-22-2006_9:52	<b>Ver:</b> 03	
<b>Sheet Size:</b> B	<b>Rev:</b> E	
<b>Sheet</b> 30 <b>of</b> 72	<b>Drawn By</b> SS	

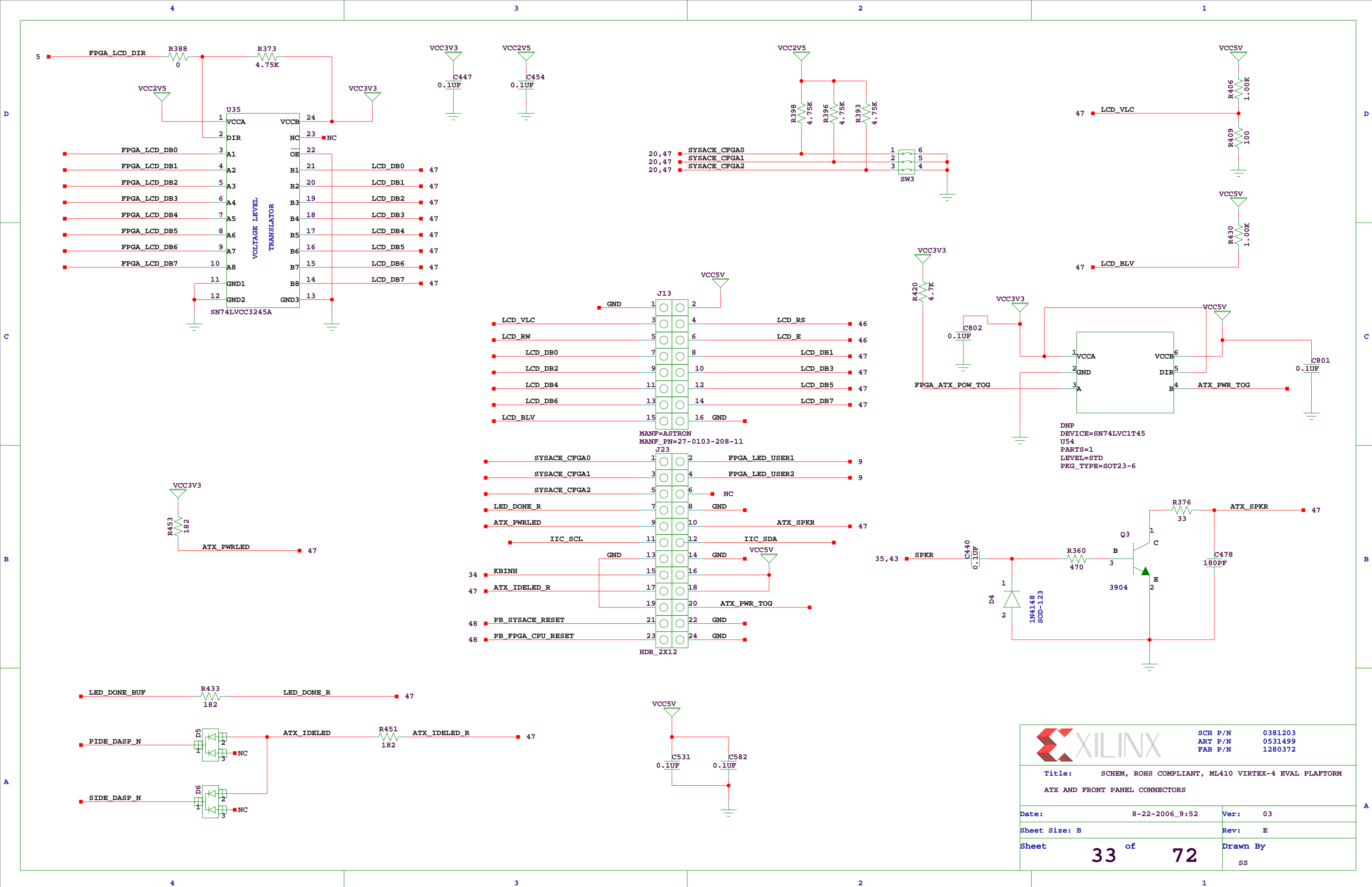


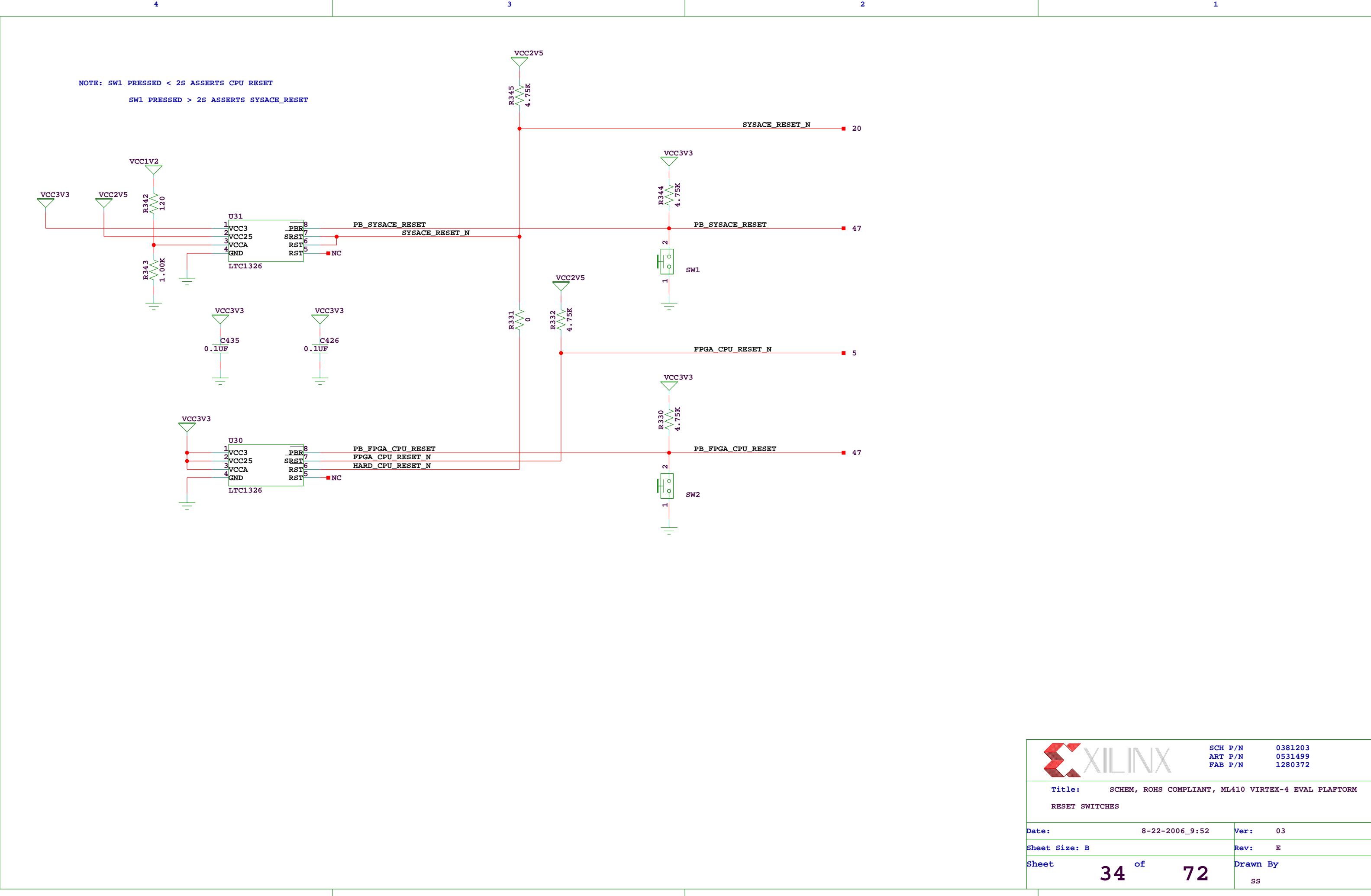
SCH P/N 0381203  
ART P/N 0531499  
FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFORM  
I2C AND SPI DEVICES

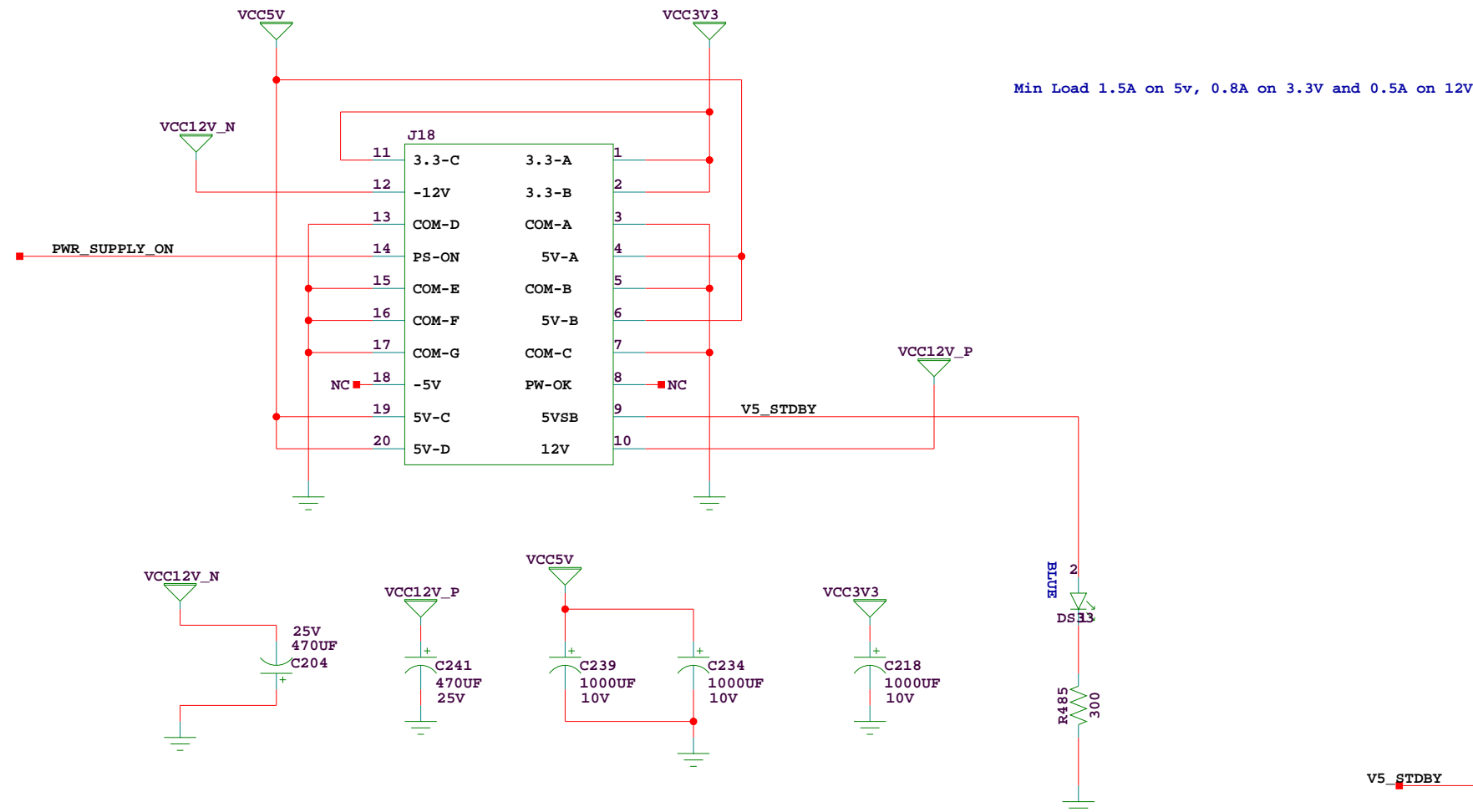
Date:	8-22-2006_9:52	Ver:	03
Sheet Size:	B	Rev:	E
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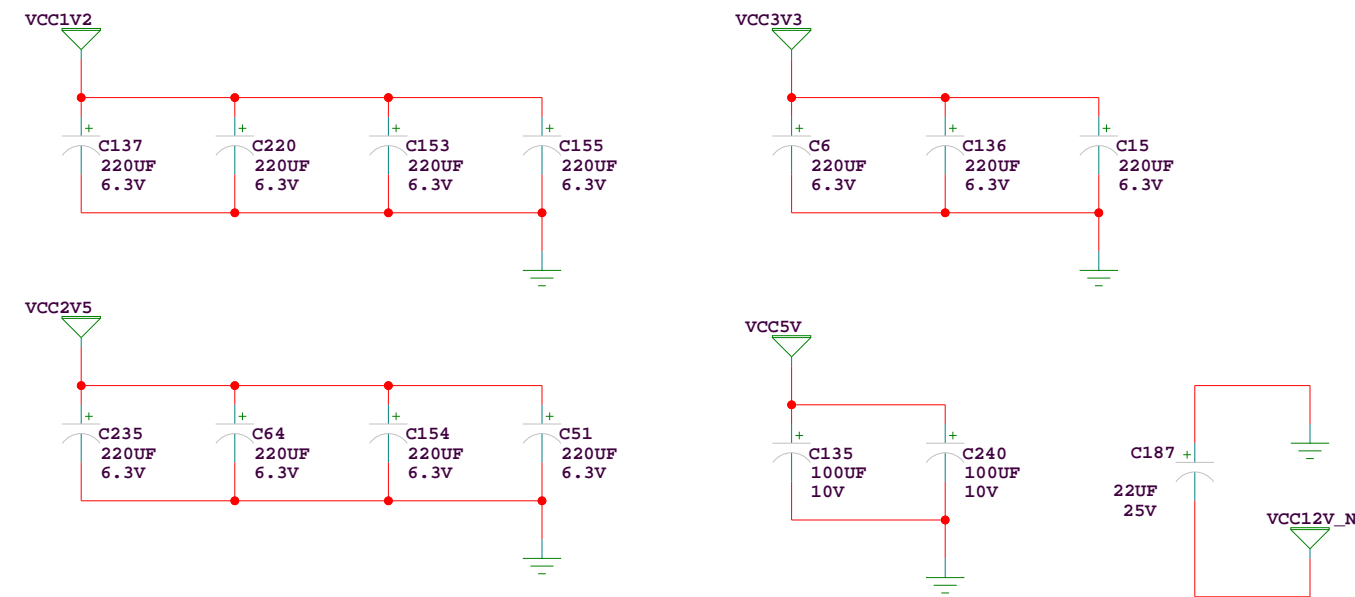




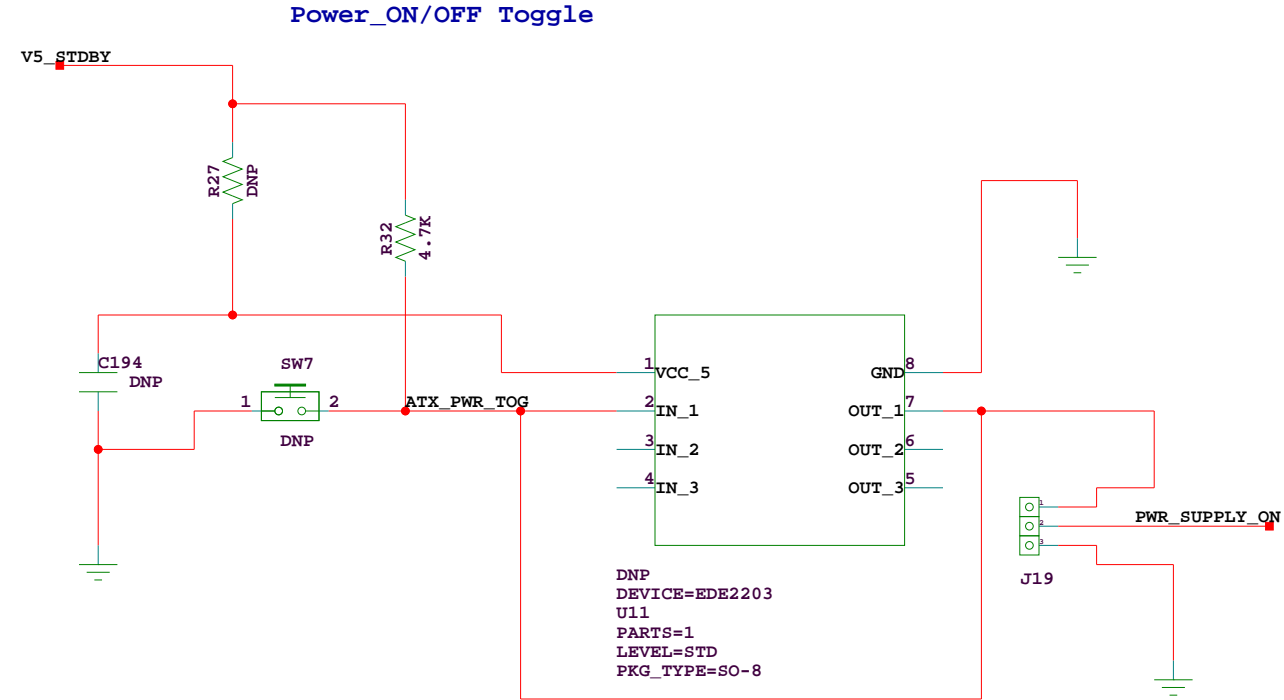
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		ART P/N	0531499
		FAB P/N	1280372
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFORM RESET SWITCHES			
Date: 8-22-2006_9:52		Ver:	03
Sheet Size: B		Rev:	E
Sheet 34 of 72		Drawn By SS	



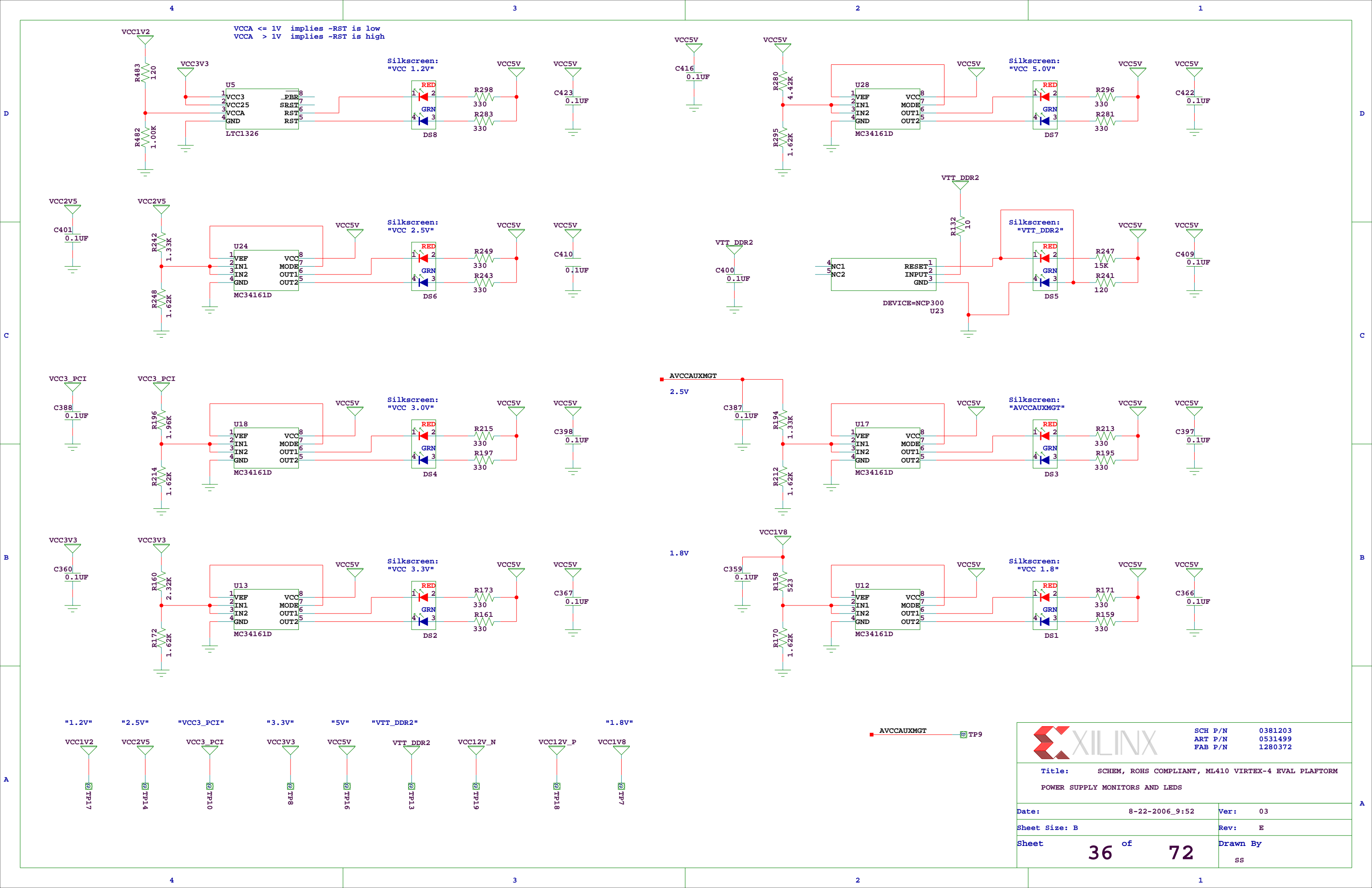
ATX Power Connector



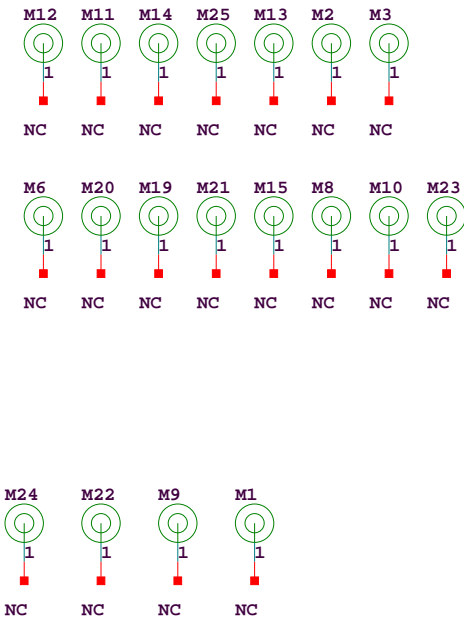
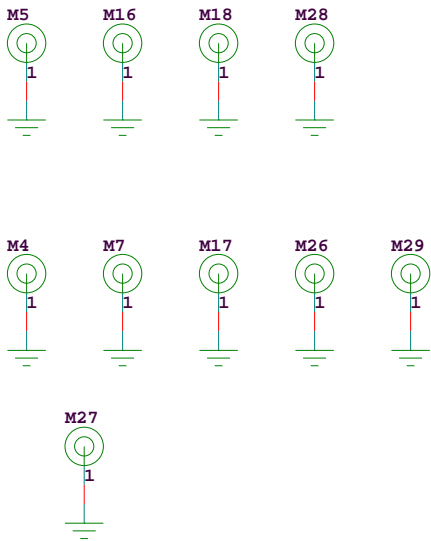
BULK CAPS DISTRIBUTED AROUND BOARD.



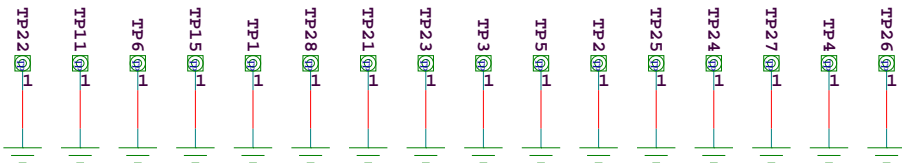
		SCH P/N	0381203
		ART P/N	0531499
		FAB P/N	1280372
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFORM ATX CONNECTOR, PWR TOGGLE AND HEADER			
Date:	8-22-2006_9:52	Ver:	03
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Mounting holes for ATX Form Factor

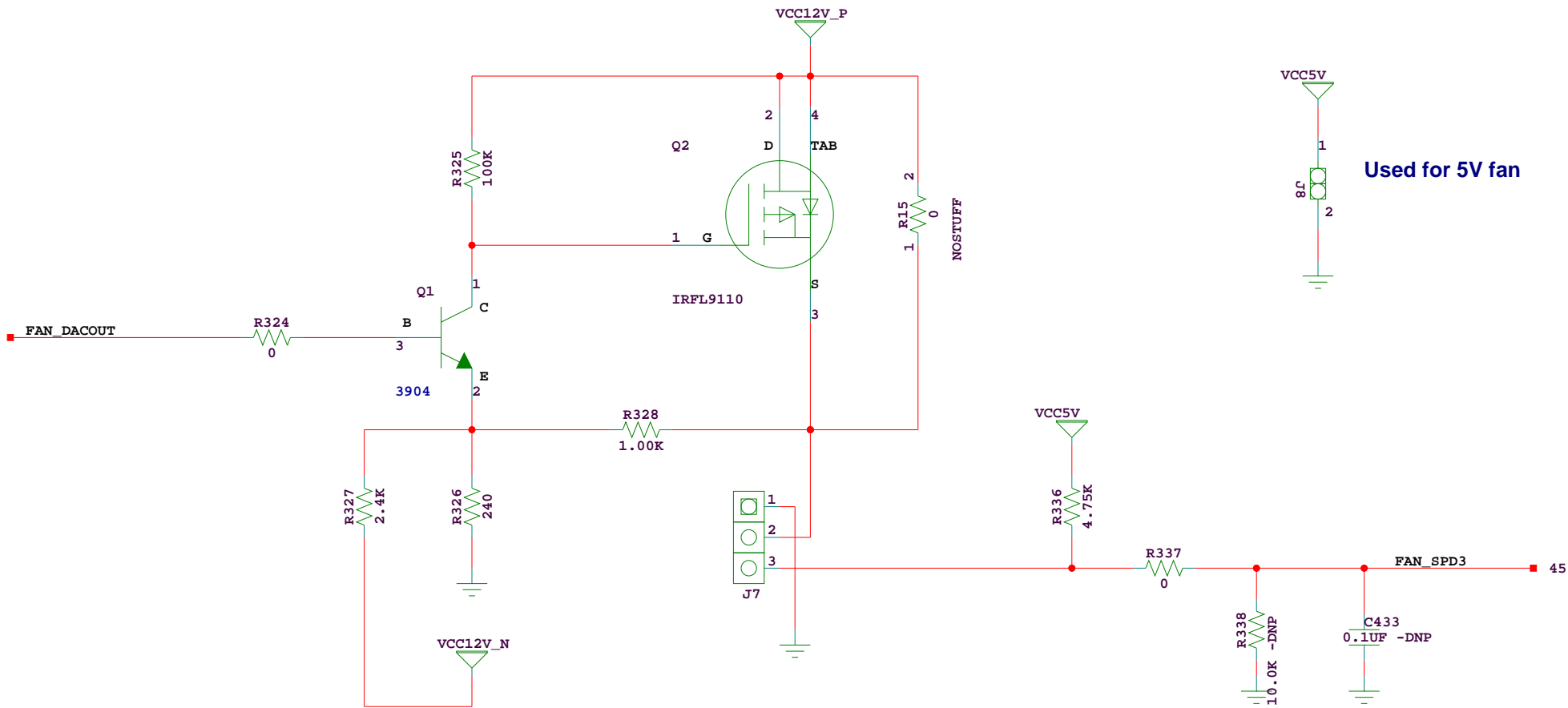


Spread out on the board.



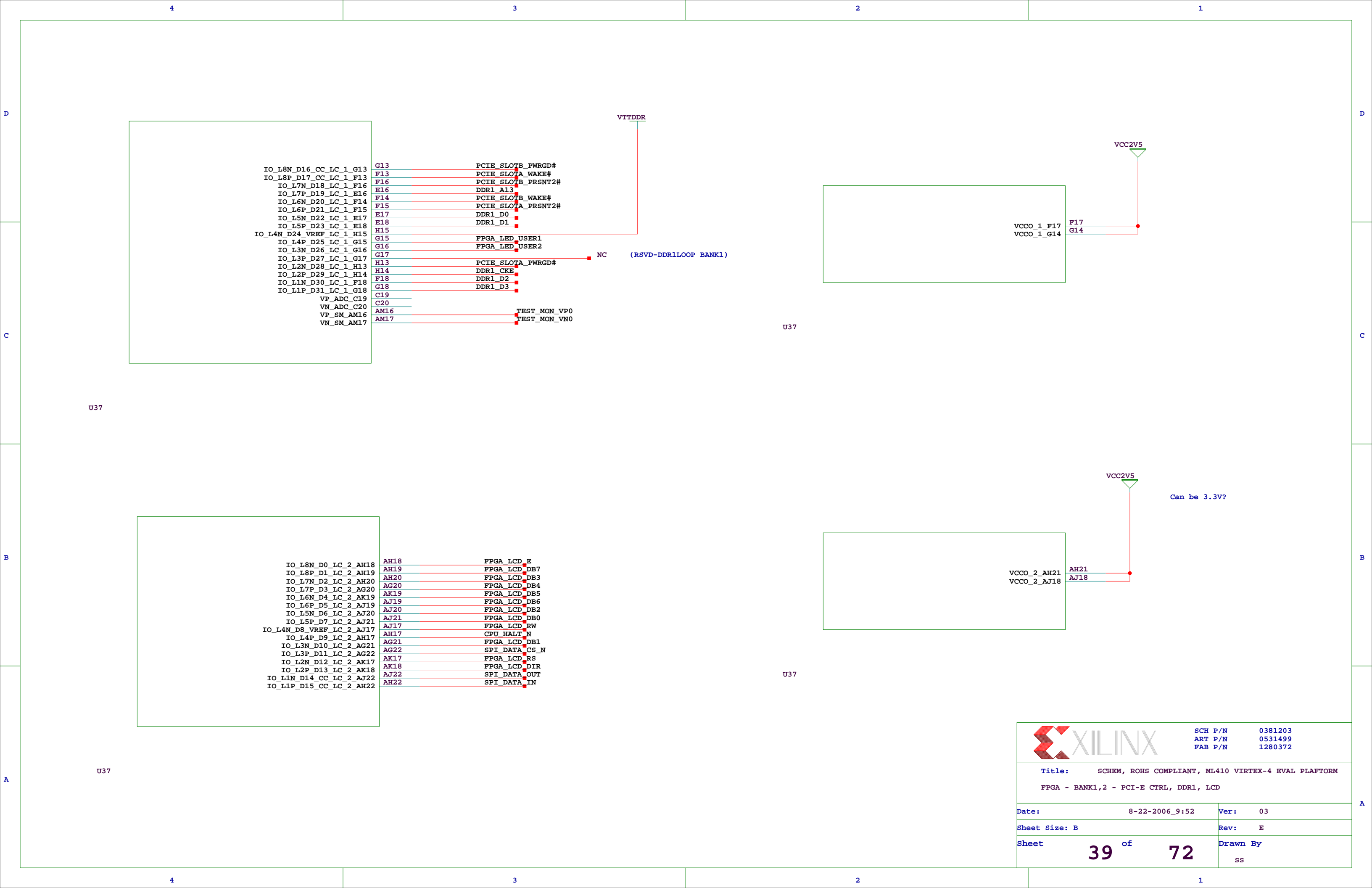
Silkscreen:  
"GND"

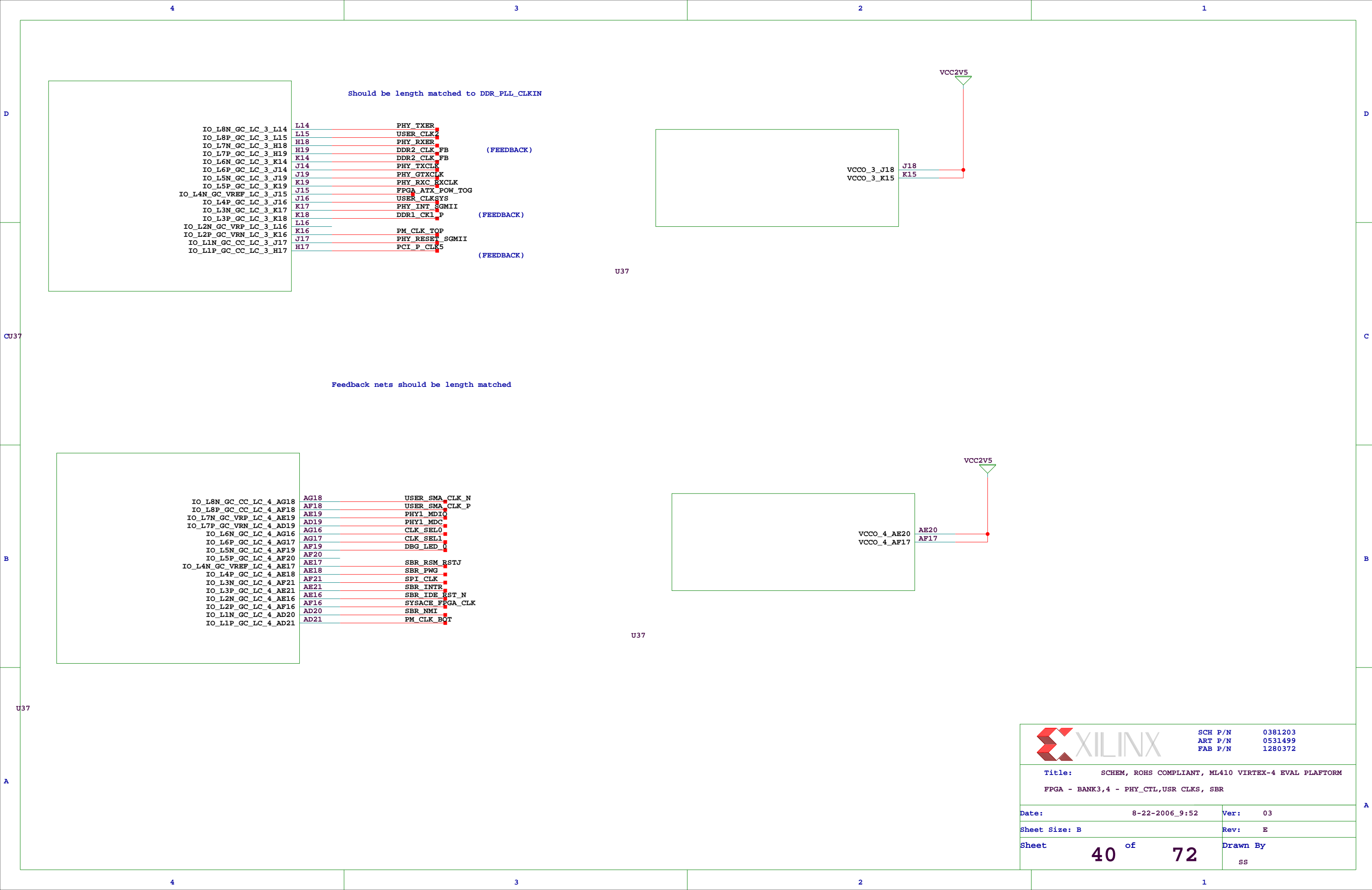
		SCH P/N	0381203
		ART P/N	0531499
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Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFORM ATX MOUNTING HOLES AND TEST POINTS			
Date:	8-22-2006_9:52	Ver:	03
Sheet Size:	B	Rev:	E
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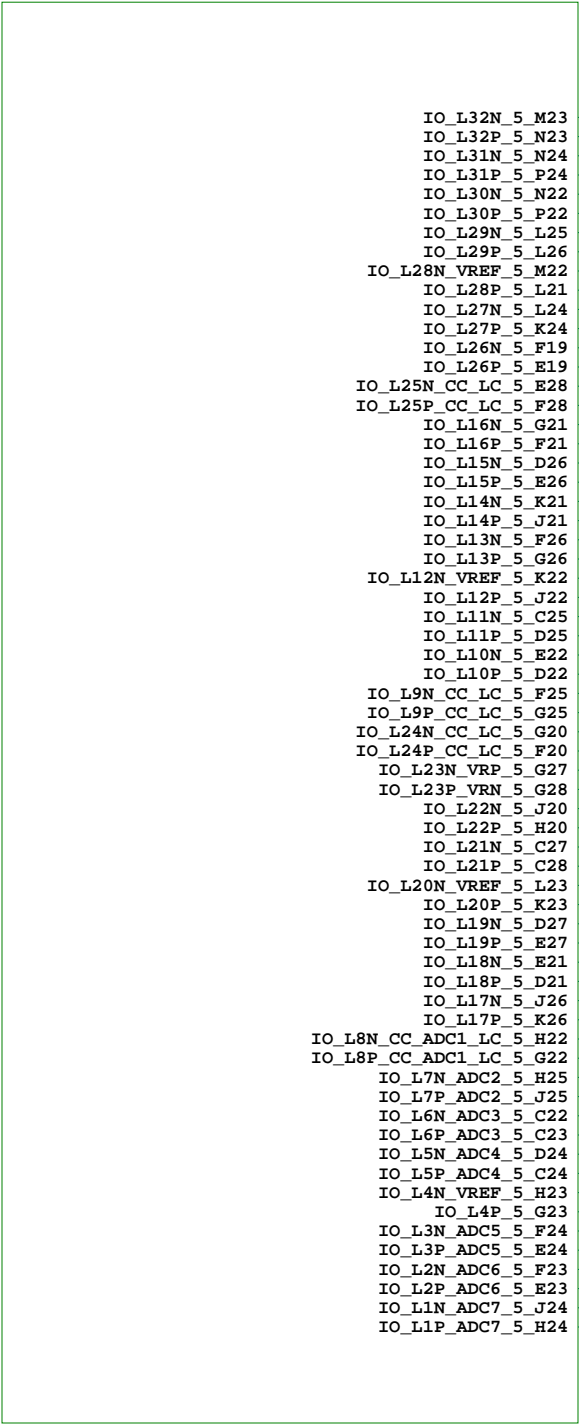


Used for 5V fan

		SCH P/N	0381203
		ART P/N	0531499
		FAB P/N	1280372
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFORM FPGA FAN SWITCH AND TACH			
Date: 8-22-2006_9:52		Ver:	03
Sheet Size: B		Rev:	E
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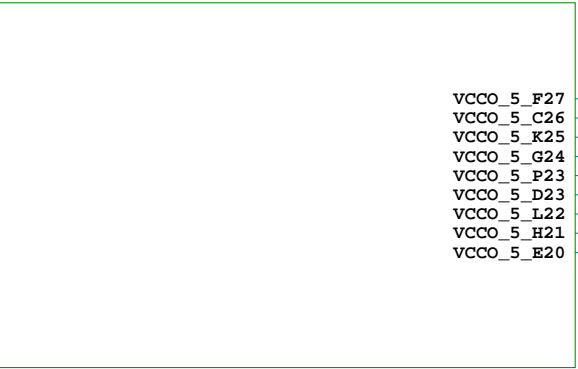


M23	DDR1_A5
N23	DDR1_A3
N24	DDR1_A4
P24	DDR1_A0
N22	DDR1_A2
P22	DDR1_A1
L25	DDR1_A7
L26	DDR1_A8
M22	
L21	DDR1_D13
L24	DDR1_A6
K24	DDR1_A10
F19	DDR1_D4
E19	DDR1_D5
E28	DDR1_CK1_N
F28	DDR1_CK1_P
G21	DDR1_D8
F21	DDR1_DM0
D26	DDR1_CAS_N
E26	
K21	DDR1_D12
J21	DDR1_D11
F26	DDR1_D26
G26	DDR1_D27
K22	
J22	DDR1_D14
C25	DDR1_D19
D25	DDR1_D22
E22	DDR1_D31
D22	DDR1_D20
F25	DDR1_DQS3
G25	DDR1_DQS2
G20	DDR1_DQS1
F20	DDR1_DQS0
G27	VRP_BANK5
G28	VRN_BANK5
J20	DDR1_D10
H20	DDR1_D9
C27	DDR1_CS_N
C28	DDR1_D23
L23	
K23	DDR1_A9
D27	DDR1_RAS_N
E27	DDR1_WE_N
E21	DDR1_D7
D21	DDR1_D6
J26	DDR1_BA1
K26	DDR1_A11
H22	DDR1_D15
G22	DDR1_DM1
H25	DDR1_D28
J25	DDR1_BA0
C22	DDR1_D16
C23	DDR1_D17
D24	DDR1_D21
C24	DDR1_D18
H23	
G23	DDR1_DM3
F24	DDR1_D25
E24	DDR1_D30
F23	DDR1_D24
E23	DDR1_DM2
J24	DDR1_A12
H24	DDR1_D29

VTDDR

NC (RSVD-DDR1LOOP BANK5)

U37



VCC2V5

VCCO_5_F27	F27
VCCO_5_C26	C26
VCCO_5_K25	K25
VCCO_5_G24	G24
VCCO_5_P23	P23
VCCO_5_D23	D23
VCCO_5_L22	L22
VCCO_5_H21	H21
VCCO_5_E20	E20

VCC2V5

VRN\_BANK5

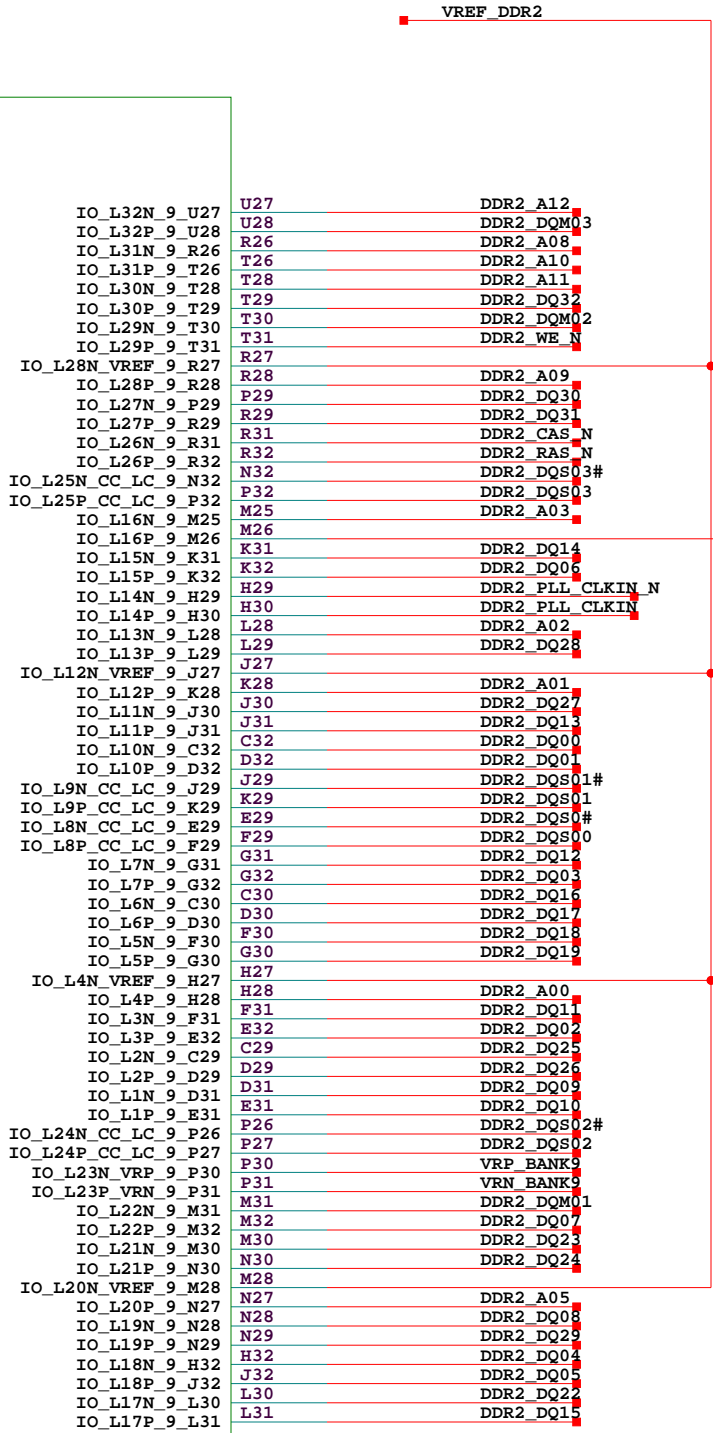
VRP\_BANK5



SCH P/N 0381203  
ART P/N 0531499  
FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFORM  
FPGA - BANK5 - DDR1

Date:	8-22-2006_9:52	Ver:	03
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VREF\_DDR2

NC

(RSVD-DDR2 LOOP BANK9)

VCCO\_9\_L32  
VCCO\_9\_H31  
VCCO\_9\_R30  
VCCO\_9\_E30  
VCCO\_9\_M29  
VCCO\_9\_J28  
VCCO\_9\_T27  
VCCO\_9\_N26

L32  
H31  
R30  
E30  
M29  
J28  
T27  
N26

VCC1V8

VCC1V8

R144

49.9

VRN\_BANK9

R147

49.9

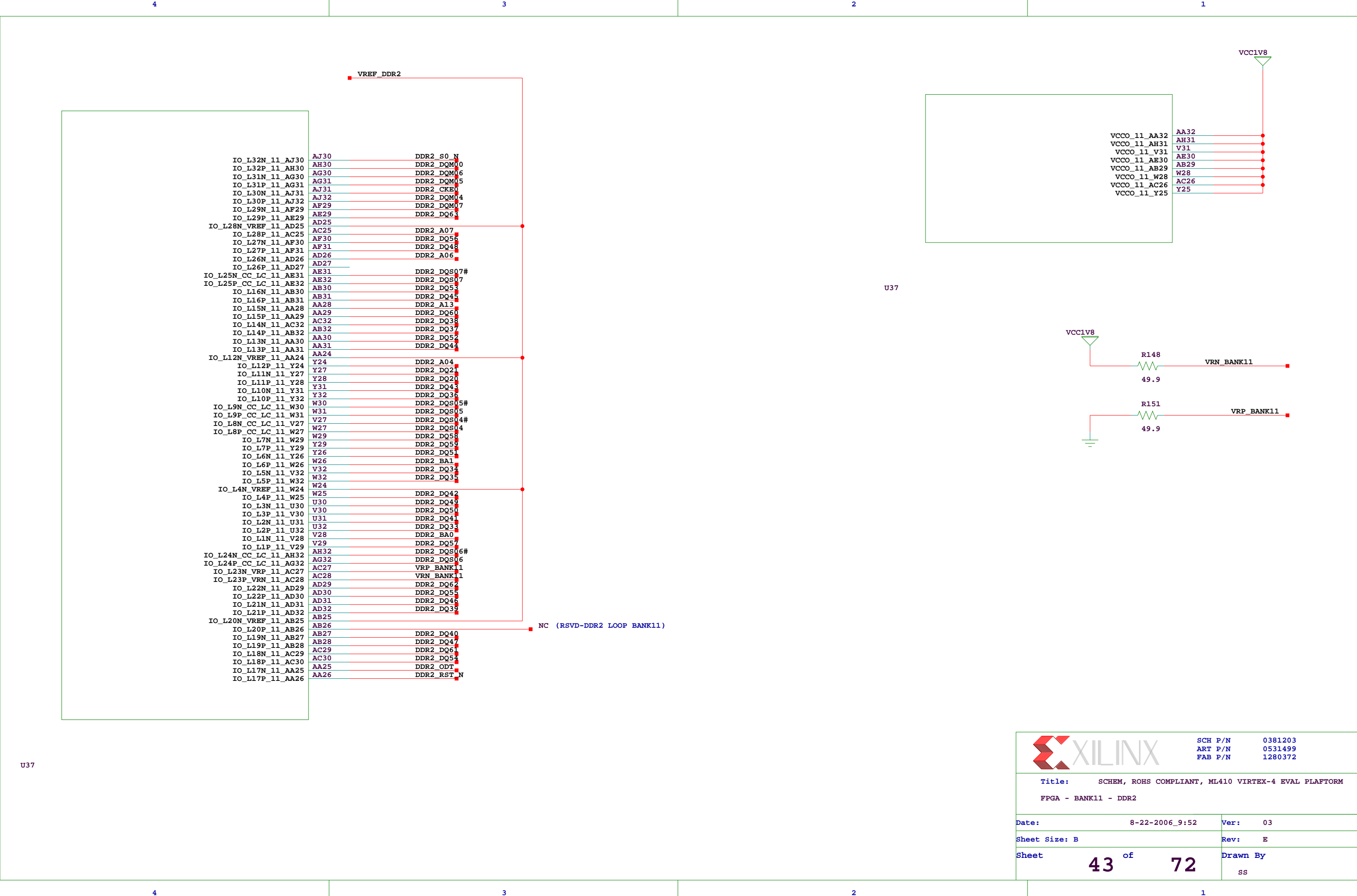
VRP\_BANK9



SCH P/N 0381203  
ART P/N 0531499  
FAB P/N 1280372

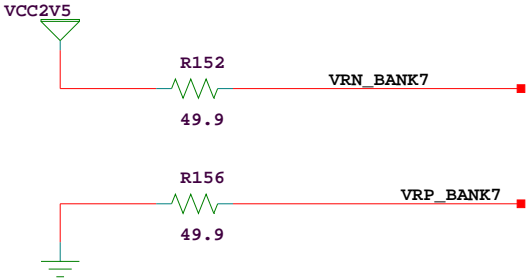
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FPGA - BANK9 - DDR2

Date:	8-22-2006_9:52	Ver:	03
Sheet Size:	B	Rev:	E
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IO_L16N_7_AK22	AK22	PM_IO_49
IO_L16P_7_AK23	AK23	PM_IO_48
IO_L15N_7_AL28	AL28	PM_IO_31
IO_L15P_7_AK28	AK28	PM_IO_30
IO_L14N_7_AL23	AL23	PM_IO_51
IO_L14P_7_AM23	AM23	PM_IO_50
IO_L13N_7_AM27	AM27	PM_IO_33
IO_L13P_7_AM28	AM28	PM_IO_32
IO_L12N_VREF_7_AD22	AD22	PM_IO_21
IO_L12P_7_AE22	AE22	PM_IO_20
IO_L11N_7_AH28	AH28	PM_IO_9
IO_L11P_7_AH29	AH29	PM_IO_8
IO_L10N_7_AM21	AM21	PM_IO_53
IO_L10P_7_AM22	AM22	PM_IO_52
IO_L9N_CC_LC_7_AK29	AK29	CPU_TDI
IO_L9P_CC_LC_7_AJ29	AJ29	ATD_10
IO_L8N_CC_LC_7_AK21	AK21	ATD_15
IO_L8P_CC_LC_7_AL21	AL21	ATD_12
IO_L7N_7_AL29	AL29	PM_IO_5
IO_L7P_7_AM30	AM30	PM_IO_4
IO_L6N_7_AL20	AL20	PM_IO_57
IO_L6P_7_AM20	AM20	PM_IO_56
IO_L5N_7_AL30	AL30	PM_IO_3
IO_L5P_7_AL31	AL31	PM_IO_2
IO_L4N_VREF_7_AC22	AC22	PM_IO_19
IO_L4P_7_AC23	AC23	PM_IO_18
IO_L3N_7_AM31	AM31	PM_IO_1
IO_L3P_7_AM32	AM32	PM_IO_0
IO_L2N_7_AL18	AL18	PM_IO_59
IO_L2P_7_AL19	AL19	PM_IO_58
IO_L1N_7_AK31	AK31	PM_IO_75
IO_L1P_7_AK32	AK32	PM_IO_74
IO_L24N_CC_LC_7_AH24	AH24	ATD_14
IO_L24P_CC_LC_7_AJ24	AJ24	ATD_11
IO_L23N_VRP_7_AK26	AK26	VRP_BANK7
IO_L23P_VRN_7_AK27	AK27	VRN_BANK7
IO_L22N_7_AK24	AK24	PM_IO_47
IO_L22P_7_AL24	AL24	PM_IO_46
IO_L21N_7_AE26	AE26	PM_IO_15
IO_L21P_7_AE27	AE27	PM_IO_14
IO_L20N_VREF_7_AE23	AE23	PM_IO_23
IO_L20P_7_AF23	AF23	PM_IO_22
IO_L19N_7_AF28	AF28	PM_IO_13
IO_L19P_7_AE28	AE28	PM_IO_12
IO_L18N_7_AG23	AG23	PM_IO_43
IO_L18P_7_AH23	AH23	PM_IO_42
IO_L17N_7_AG27	AG27	PM_IO_11
IO_L17P_7_AG28	AG28	PM_IO_10
IO_L32N_SM1_7_AJ25	AJ25	PM_IO_39
IO_L32P_SM1_7_AJ26	AJ26	PM_IO_38
IO_L31N_SM2_7_AF24	AF24	PM_IO_25
IO_L31P_SM2_7_AF25	AF25	PM_IO_24
IO_L30N_SM3_7_AM26	AM26	PM_IO_35
IO_L30P_SM3_7_AL26	AL26	PM_IO_34
IO_L29N_SM4_7_AH25	AH25	PM_IO_41
IO_L29P_SM4_7_AG25	AG25	PM_IO_40
IO_L28N_VREF_7_AE24	AE24	PM_IO_17
IO_L28P_7_AD24	AD24	PM_IO_16
IO_L27N_SM5_7_AG26	AG26	PM_IO_27
IO_L27P_SM5_7_AF26	AF26	PM_IO_26
IO_L26N_SM6_7_AM25	AM25	PM_IO_37
IO_L26P_SM6_7_AL25	AL25	PM_IO_36
IO_L25N_CC_SM7_LC_7_AJ27	AJ27	CPU_TCK
IO_L25P_CC_SM7_LC_7_AH27	AH27	CPU_TRST_N

VCCO_7_AL32	AL32
VCCO_7_AM29	AM29
VCCO_7_AJ28	AJ28
VCCO_7_AF27	AF27
VCCO_7_AK25	AK25
VCCO_7_AG24	AG24
VCCO_7_AD23	AD23
VCCO_7_AL22	AL22
VCCO_7_AM19	AM19



SCH P/N 0381203  
ART P/N 0531499  
FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFORM  
FPGA - BANK7- PM\_IO\_\*

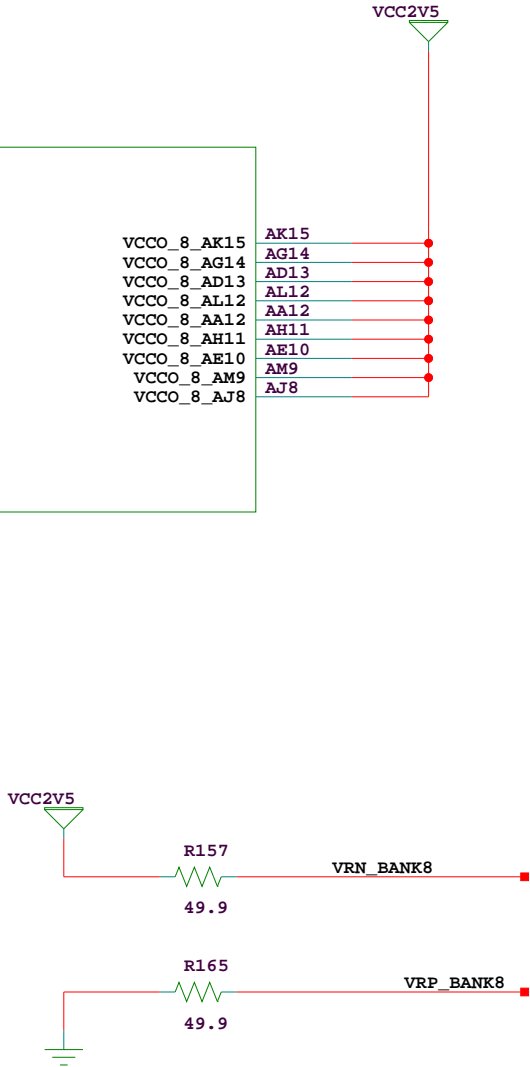
Date: 8-22-2006\_9:52 Ver: 03


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IO_L16N_8_AM10	AM10	PM_IO_7
IO_L16P_8_AL10	AL10	PM_IO_6
IO_L15N_8_AF13	AF13	PM_IO_61
IO_L15P_8_AE13	AE13	PM_IO_60
IO_L14N_8_AH9	AH9	PM_IO_55
IO_L14P_8_AJ9	AJ9	PM_IO_54
IO_L13N_8_AF14	AF14	PM_IO_85
IO_L13P_8_AE14	AE14	PM_IO_84
IO_L12N_VREF_8_AD9	AD9	PLB_BUS_ERROR
IO_L12P_8_AD10	AD10	OPB_BUS_ERROR
IO_L11N_8_AE11	AE11	PM_IO_73
IO_L11P_8_AD11	AD11	PM_IO_72
IO_L10N_8_AK9	AK9	PM_IO_95
IO_L10P_8_AL9	AL9	PM_IO_94
IO_L9N_CC_LC_8_AE12	AE12	TRC_TS6
IO_L9P_CC_LC_8_AD12	AD12	TRC_TS5
IO_L8N_CC_LC_8_AK8	AK8	TRC_CLK_8
IO_L8P_CC_LC_8_AL8	AL8	ATCB_CLK_R
IO_L7N_8_AC13	AC13	PM_IO_87
IO_L7P_8_AD14	AD14	PM_IO_86
IO_L6N_8_AM7	AM7	CPU_TMS
IO_L6P_8_AM8	AM8	CPU_TDO_TMP
IO_L5N_8_AB12	AB12	PM_IO_93
IO_L5P_8_AC12	AC12	PM_IO_92
IO_L4N_VREF_8_AH7	AH7	TRC_TS10
IO_L4P_8_AH8	AH8	TRC_TS1E
IO_L3N_8_AA13	AA13	PM_IO_89
IO_L3P_8_AB13	AB13	PM_IO_88
IO_L2N_8_AJ7	AJ7	ATD_8
IO_L2P_8_AK7	AK7	ATD_16
IO_L1N_8_AA11	AA11	PM_IO_91
IO_L1P_8_AB11	AB11	PM_IO_90
IO_L24N_CC_LC_8_AK11	AK11	ATD_13
IO_L24P_CC_LC_8_AJ11	AJ11	ATD_17
IO_L23N_VRP_8_AJ14	AJ14	VRP_BANK8
IO_L23P_VRN_8_AH14	AH14	VRN_BANK8
IO_L22N_8_AM11	AM11	PM_IO_45
IO_L22P_8_AL11	AL11	PM_IO_44
IO_L21N_8_AJ15	AJ15	PM_IO_79
IO_L21P_8_AH15	AH15	PM_IO_78
IO_L20N_VREF_8_AG10	AG10	TRC_TS20
IO_L20P_8_AF10	AF10	TRC_TS4
IO_L19N_8_AK16	AK16	PM_IO_77
IO_L19P_8_AJ16	AJ16	PM_IO_76
IO_L18N_8_AJ10	AJ10	PM_IO_63
IO_L18P_8_AH10	AH10	PM_IO_62
IO_L17N_8_AG15	AG15	PM_IO_81
IO_L17P_8_AF15	AF15	PM_IO_80
IO_L32N_8_AL13	AL13	PM_IO_65
IO_L32P_8_AK13	AK13	PM_IO_64
IO_L31N_8_AL14	AL14	PM_IO_83
IO_L31P_8_AK14	AK14	PM_IO_82
IO_L30N_8_AM12	AM12	PM_IO_67
IO_L30P_8_AM13	AM13	PM_IO_66
IO_L29N_8_AH12	AH12	PM_IO_71
IO_L29P_8_AG12	AG12	PM_IO_70
IO_L28N_VREF_8_AE9	AE9	PM_IO_29
IO_L28P_8_AF9	AF9	PM_IO_28
IO_L27N_8_AG11	AG11	TRC_TS2E
IO_L27P_8_AF11	AF11	TRC_TS3
IO_L26N_8_AK12	AK12	PM_IO_69
IO_L26P_8_AJ12	AJ12	PM_IO_68
IO_L25N_CC_LC_8_AH13	AH13	ATD_18
IO_L25P_CC_LC_8_AG13	AG13	ATD_9

U37





SCH P/N

ART P/N

FAB P/N

0381203

0531499

1280372

Title:

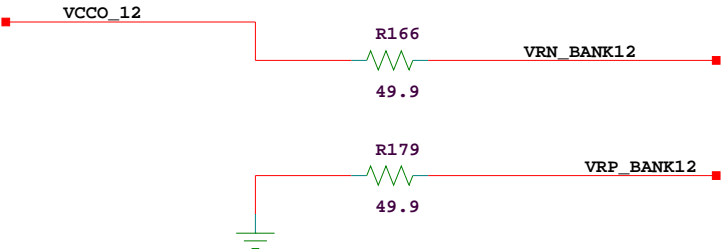
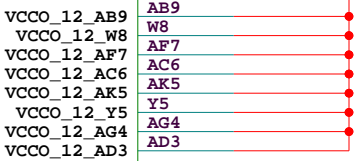
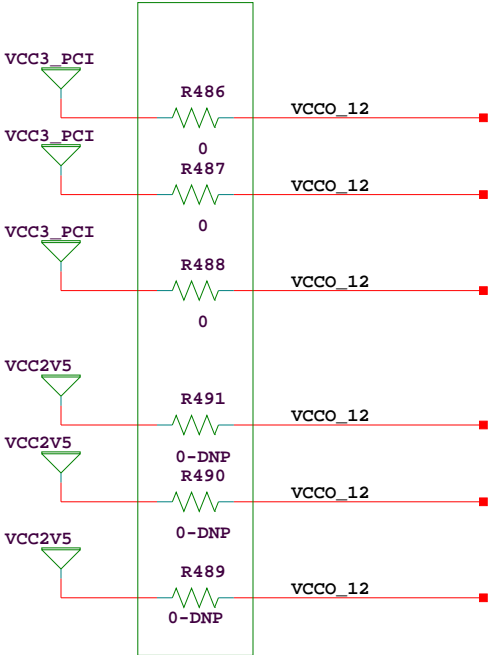
SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFORM

FPGA - BANK8 - PM\_IO,MICTOR, CPU\_DEBUG

Date:	8-22-2006_9:52	Ver:	03
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IO_L32N_12_AH5	AH5	SYSACE_MPD03
IO_L32P_12_AJ5	AJ5	SYSACE_MPD07
IO_L31N_12_AC9	AC9	DBG_LED_6
IO_L31P_12_AC10	AC10	DBG_LED_7
IO_L30N_12_AG5	AG5	SYSACE_MPD01
IO_L30P_12_AG6	AG6	SYSACE_MPD00
IO_L29N_12_AL6	AL6	SYSACE_MPD12
IO_L29P_12_AM6	AM6	SYSACE_MPD1RQ
IO_L28N_VREF_12_AD6	AD6	DBG_LED_2
IO_L28P_12_AD7	AD7	DBG_LED_3
IO_L27N_12_AG7	AG7	PM_IO_3V_17
IO_L27P_12_AG8	AG8	PM_IO_3V_5
IO_L26N_12_AL3	AL3	PM_IO_3V_9
IO_L26P_12_AM3	AM3	PM_IO_3V_13
IO_L25N_CC_LC_12_AJ6	AJ6	SYSACE_MPD06
IO_L25P_CC_LC_12_AK6	AK6	SYSACE_MPD09
IO_L16N_12_AD4	AD4	SYSACE_CLK_OE
IO_L16P_12_AD5	AD5	DBG_LED_1
IO_L15N_12_AE6	AE6	SYSACE_MPA00
IO_L15P_12_AF6	AF6	SYSACE_MPA03
IO_L14N_12_AC3	AC3	PM_IO_3V_16
IO_L14P_12_AC4	AC4	PM_IO_3V_12
IO_L13N_12_AA8	AA8	PM_IO_3V_25
IO_L13P_12_AA9	AA9	PM_IO_3V_18
IO_L12N_VREF_12_Y9	Y9	PM_IO_3V_1
IO_L12P_12_W9	W9	PM_IO_3V_3
IO_L11N_12_AF3	AF3	SYSACE_MPA06
IO_L11P_12_AG3	AG3	SYSACE_MPD02
IO_L10N_12_Y6	Y6	PM_IO_3V_7
IO_L10P_12_AA6	AA6	PM_IO_3V_22
IO_L9N_CC_LC_12_AB6	AB6	SYSACE_MPCE
IO_L9P_CC_LC_12_AB7	AB7	SYSACE_MPBRDY
IO_L8N_CC_LC_12_AA3	AA3	SYSACE_MPD15
IO_L8P_CC_LC_12_AB3	AB3	SYSACE_MPWE
IO_L7N_12_AB5	AB5	PM_IO_3V_19
IO_L7P_12_AC5	AC5	PM_IO_3V_24
IO_L6N_12_Y3	Y3	PM_IO_3V_10
IO_L6P_12_Y4	Y4	PM_IO_3V_4
IO_L5N_12_Y7	Y7	PM_IO_3V_21
IO_L5P_12_Y8	Y8	PM_IO_3V_20
IO_L4N_VREF_12_W6	W6	PM_IO_3V_15
IO_L4P_12_W7	W7	PM_IO_3V_0
IO_L3N_12_AA4	AA4	PM_IO_3V_8
IO_L3P_12_AA5	AA5	PM_IO_3V_6
IO_L2N_12_V7	V7	PM_IO_3V_23
IO_L2P_12_V8	V8	PM_IO_3V_11
IO_L1N_12_W4	W4	PM_IO_3V_2
IO_L1P_12_W5	W5	PM_IO_3V_14
IO_L24N_CC_LC_12_AH3	AH3	SYSACE_MPD05
IO_L24P_CC_LC_12_AH4	AH4	SYSACE_MPD04
IO_L23N_VRP_12_AE7	AE7	VRP_BANK12
IO_L23P_VRN_12_AF8	AF8	VRN_BANK12
IO_L22N_12_AF4	AF4	SYSACE_MPA05
IO_L22P_12_AF5	AF5	SYSACE_MPA04
IO_L21N_12_AK4	AK4	SYSACE_MPD10
IO_L21P_12_AL4	AL4	SYSACE_MPD14
IO_L20N_VREF_12_AB8	AB8	DBG_LED_4
IO_L20P_12_AC7	AC7	DBG_LED_5
IO_L19N_12_AL5	AL5	SYSACE_MPD13
IO_L19P_12_AM5	AM5	SYSACE_MPOE
IO_L18N_12_AE3	AE3	SYSACE_MPA02
IO_L18P_12_AE4	AE4	SYSACE_MPA01
IO_L17N_12_AK3	AK3	SYSACE_MPD11
IO_L17P_12_AJ4	AJ4	SYSACE_MPD08

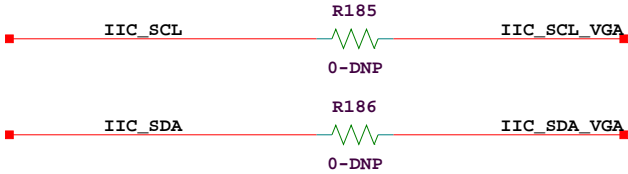
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	SCH P/N	0381203
	ART P/N	0531499
	FAB P/N	1280372
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FPGA - BANK12 - SYSACE, PM_IO_3,DBG_LED		
Date:	8-22-2006_9:52	Ver: 03
Sheet Size: B		Rev: E
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IO_L32N_10_U6	U6	
IO_L32P_10_U7	U7	PCI_P_CLK3_R
IO_L31N_10_T10	T10	IIC_SDA_VGA
IO_L31P_10_T11	T11	PCI_P_CLK1_R
IO_L30N_10_V3	V3	PCI_P_GNT3_N
IO_L30P_10_V4	V4	PCI_P_INTD_N
IO_L29N_10_R9	R9	PCI_P_REQ4_N
IO_L29P_10_T9	T9	PCI_P_REQ3_N
IO_L28N_VREF_10_R7	R7	PCI_P_REQ1_N
IO_L28P_10_R8	R8	PCI_P_INTB_N
IO_L27N_10_T8	T8	PCI_P_REQ2_N
IO_L27P_10_U8	U8	PCI_P_GNT2_N
IO_L26N_10_T3	T3	PCI_P_REQ0_N
IO_L26P_10_U3	U3	PCI_P_CLK4_R
IO_L25N_CC_LC_10_U5	U5	PCI_P_CLK5_R
IO_L25P_CC_LC_10_V5	V5	PCI_P_CLK0_R
IO_L16N_10_N3	N3	PCI_P_AD06
IO_L16P_10_M3	M3	PCI_P_TRDY_N
IO_L15N_10_M5	M5	PCI_P_CBE0_N
IO_L15P_10_M6	M6	PCI_P_PERR_N
IO_L14N_10_L3	L3	PCI_P_AD27
IO_L14P_10_L4	L4	PCI_P_AD00
IO_L13N_10_L5	L5	PCI_P_AD01
IO_L13P_10_L6	L6	PCI_P_CBE1_N
IO_L12N_VREF_10_N7	N7	PCI_FPGA_IDSEL
IO_L12P_10_N8	N8	PCI_P_FRAME_N
IO_L11N_10_N9	N9	PCI_P_AD18
IO_L11P_10_N10	N10	PCI_P_AD19
IO_L10N_10_K3	K3	PCI_P_AD20
IO_L10P_10_K4	K4	PCI_P_AD21
IO_L9N_CC_LC_10_K6	K6	PCI_P_AD28
IO_L9P_CC_LC_10_J6	J6	PCI_P_AD22
IO_L8N_CC_LC_10_J4	J4	PCI_P_AD14
IO_L8P_CC_LC_10_J5	J5	PCI_P_AD15
IO_L7N_10_F3	F3	PCI_P_AD09
IO_L7P_10_F4	F4	PCI_P_AD03
IO_L6N_10_H3	H3	PCI_P_AD02
IO_L6P_10_G3	G3	PCI_P_AD11
IO_L5N_10_G5	G5	PCI_P_AD08
IO_L5P_10_F5	F5	PCI_P_AD10
IO_L4N_VREF_10_M7	M7	PCI_P_SERR_N
IO_L4P_10_M8	M8	PCI_P_AD24
IO_L3N_10_M10	M10	PCI_P_AD25
IO_L3P_10_L10	L10	PCI_P_AD13
IO_L2N_10_H4	H4	PCI_P_AD16
IO_L2P_10_H5	H5	PCI_P_AD17
IO_L1N_10_L8	L8	PCI_P_PAR
IO_L1P_10_L9	L9	PCI_P_AD12
IO_L24N_CC_LC_10_R6	R6	PCI_P_CBE3_N
IO_L24P_CC_LC_10_T6	T6	PCI_P_GNT4_N
IO_L23N_VRP_10_R11	R11	PCI_P_RST_N
IO_L23P_VRN_10_P11	P11	PCI_P_STOP_N
IO_L22N_10_P6	P6	PCI_P_AD30
IO_L22P_10_P7	P7	PCI_P_AD31
IO_L21N_10_T4	T4	PCI_P_GNT0_N
IO_L21P_10_T5	T5	PCI_P_GNT1_N
IO_L20N_VREF_10_R3	R3	PCI_P_DEVSEL_N
IO_L20P_10_R4	R4	PCI_P_CBE2_N
IO_L19N_10_P9	P9	PCI_P_INTC_N
IO_L19P_10_P10	P10	IIC_SCL_VGA
IO_L18N_10_P4	P4	PCI_P_LOCK_N
IO_L18P_10_P5	P5	PCI_P_INTA_N
IO_L17N_10_N4	N4	PCI_P_AD07
IO_L17P_10_N5	N5	PCI_P_IRDY_N

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VCCO_10_R10	R10
VCCO_10_M9	M9
VCCO_10_T7	T7
VCCO_10_N6	N6
VCCO_10_K5	K5
VCCO_10_U4	U4
VCCO_10_G4	G4
VCCO_10_P3	P3

VCC3\_PCI



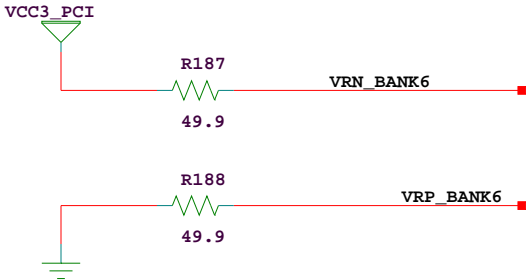
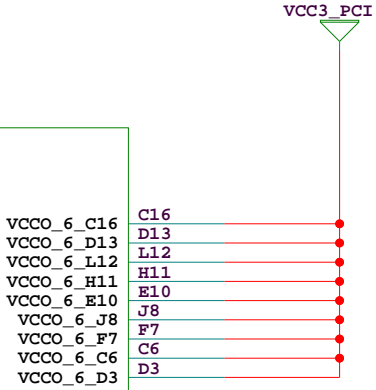
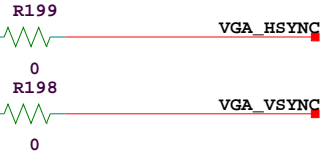
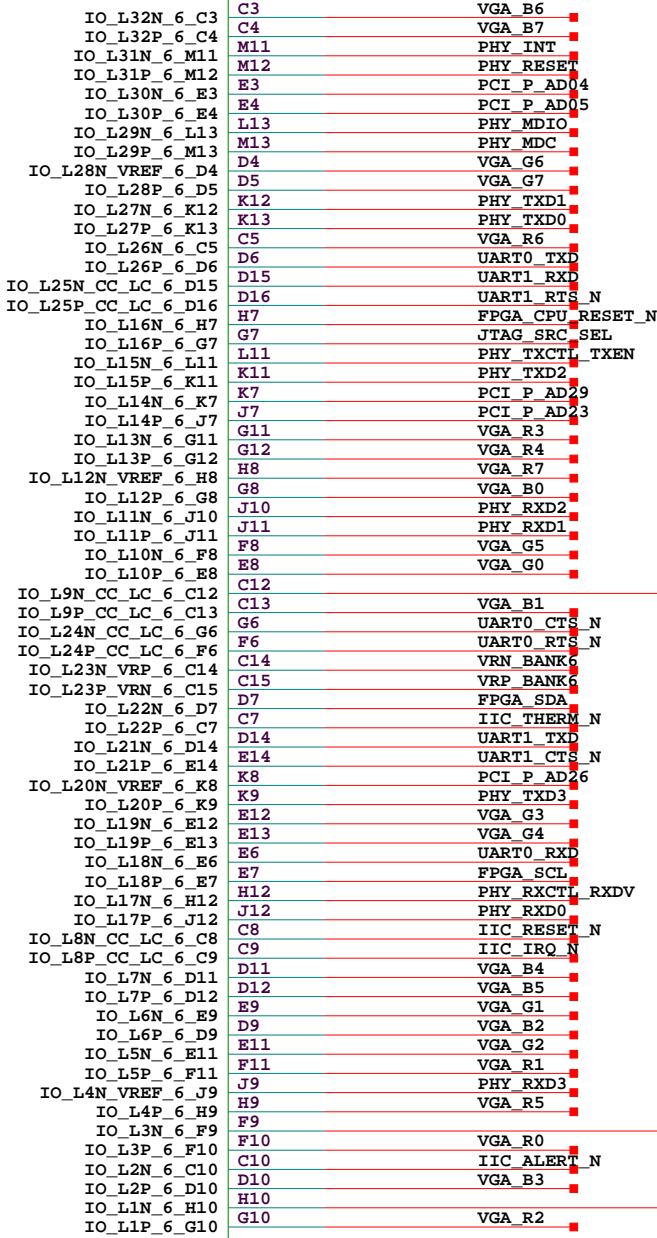
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ART P/N 0531499  
FAB P/N 1280372

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FPGA - BANK10 - PCI

Date: 8-22-2006\_9:52 Ver: 03

Sheet Size: B Rev: E

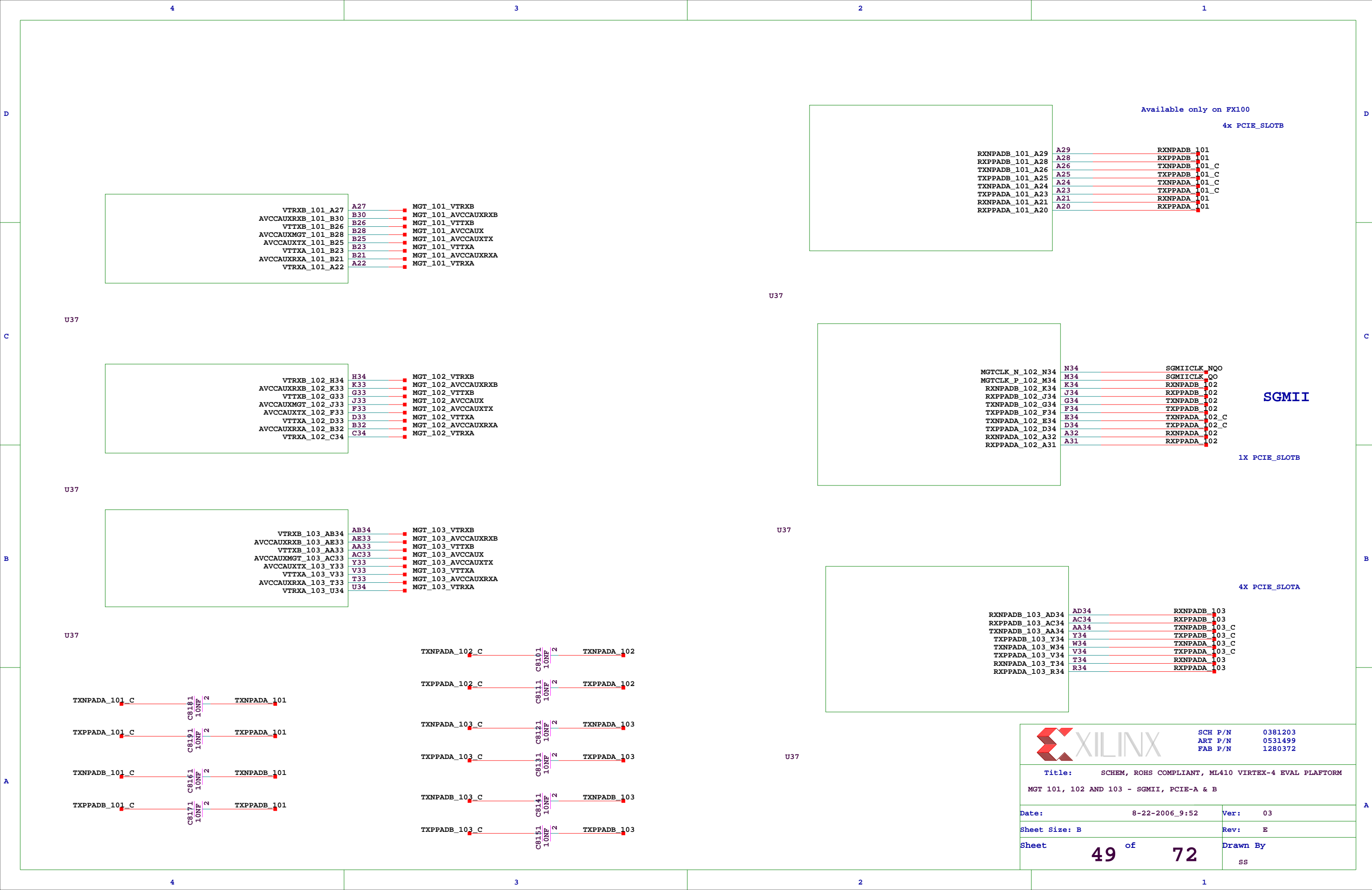
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SCH P/N 0381203  
ART P/N 0531499  
FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFORM  
FPGA-BANK6, VGA, UART, PHY

Date:	8-22-2006_9:52	Ver:	03
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MGTVREF\_105\_AN27  
RTERM\_105\_AN29

AN27  
AN29

MGTVREF\_105  
MGT\_RTERM\_105

VTRXB\_105\_AN33  
AVCCAUXRXB\_105\_AN31  
VTTXB\_105\_AM33  
AVCCAUXMGT\_105\_AN32  
AVCCAUXTX\_105\_AL33  
VTTXA\_105\_AJ33  
AVCCAUXRXA\_105\_AG33  
VTRXA\_105\_AH34

AN33  
AN31  
AM33  
AN32  
AL33  
AJ33  
AG33  
AH34

MGT\_105\_VTRXB  
MGT\_105\_AVCCAUXRXB  
MGT\_105\_VTTXB  
MGT\_105\_AVCCAUX  
MGT\_105\_AVCCAUXTX  
MGT\_105\_VTTXA  
MGT\_105\_AVCCAUXRXA  
MGT\_105\_VTRXA

VTRXB\_106\_AP19  
AVCCAUXRXB\_106\_AN17  
VTTXB\_106\_AN20  
AVCCAUXMGT\_106\_AN18  
AVCCAUXTX\_106\_AN22  
VTTXA\_106\_AN23  
AVCCAUXRXA\_106\_AN25  
VTRXA\_106\_AP24

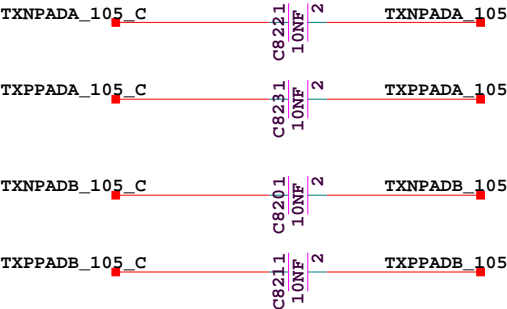
AP19  
AN17  
AN20  
AN18  
AN22  
AN23  
AN25  
AP24

MGT\_106\_VTRXB  
MGT\_106\_AVCCAUXRXB  
MGT\_106\_VTTXB  
MGT\_106\_AVCCAUX  
MGT\_106\_AVCCAUXTX  
MGT\_106\_VTTXA  
MGT\_106\_AVCCAUXRXA  
MGT\_106\_VTRXA

VTRXB\_109\_AP13  
AVCCAUXRXB\_109\_AN15  
VTTXB\_109\_AN12  
AVCCAUXMGT\_109\_AN14  
AVCCAUXTX\_109\_AN10  
VTTXA\_109\_AN9  
AVCCAUXRXA\_109\_AN7  
VTRXA\_109\_AP8

AP13  
AN15  
AN12  
AN14  
AN10  
AN9  
AN7  
AP8

MGT\_109\_VTRXB  
MGT\_109\_AVCCAUXRXB  
MGT\_109\_VTTXB  
MGT\_109\_AVCCAUX  
MGT\_109\_AVCCAUXTX  
MGT\_109\_VTTXA  
MGT\_109\_AVCCAUXRXA  
MGT\_109\_VTRXA



MGTCLK\_N\_105\_AP28  
MGTCLK\_P\_105\_AP29  
RXNPADB\_105\_AP31  
RXPPADB\_105\_AP32  
TXNPADB\_105\_AM34  
TXPPADB\_105\_AL34  
TXNPADA\_105\_AK34  
TXPPADA\_105\_AJ34  
RXNPADA\_105\_AG34  
RXPPADA\_105\_AF34

AP28  
AP29  
AP31  
AP32  
AM34  
AL34  
AK34  
AJ34  
AG34  
AF34

SATACLK\_N00  
SATACLK\_P00  
RXNPADB\_105  
RXPPADB\_105  
TXNPADB\_105\_C  
TXPPADB\_105\_C  
TXNPADA\_105\_C  
TXPPADA\_105\_C  
RXNPADA\_105  
RXPPADA\_105

## SATA Clock

4X PCIE\_SLOTA

RXNPADB\_106\_AP17  
RXPPADB\_106\_AP18  
TXNPADB\_106\_AP20  
TXPPADB\_106\_AP21  
TXNPADA\_106\_AP22  
TXPPADA\_106\_AP23  
RXNPADA\_106\_AP25  
RXPPADA\_106\_AP26

AP17  
AP18  
AP20  
AP21  
AP22  
AP23  
AP25  
AP26

RXNPADB\_106  
RXPPADB\_106  
TXNPADB\_106  
TXPPADB\_106  
TXNPADA\_106  
TXPPADA\_106  
RXNPADA\_106  
RXPPADA\_106

## SATA

RXNPADB\_109\_AP15  
RXPPADB\_109\_AP14  
TXNPADB\_109\_AP12  
TXPPADB\_109\_AP11  
TXNPADA\_109\_AP10  
TXPPADA\_109\_AP9  
RXNPADA\_109\_AP7  
RXPPADA\_109\_AP6

AP15  
AP14  
AP12  
AP11  
AP10  
AP9  
AP7  
AP6

RXNPADB\_109  
RXPPADB\_109  
TXNPADB\_109  
TXPPADB\_109  
TXNPADA\_109  
TXPPADA\_109  
RXNPADA\_109  
RXPPADA\_109

## PM



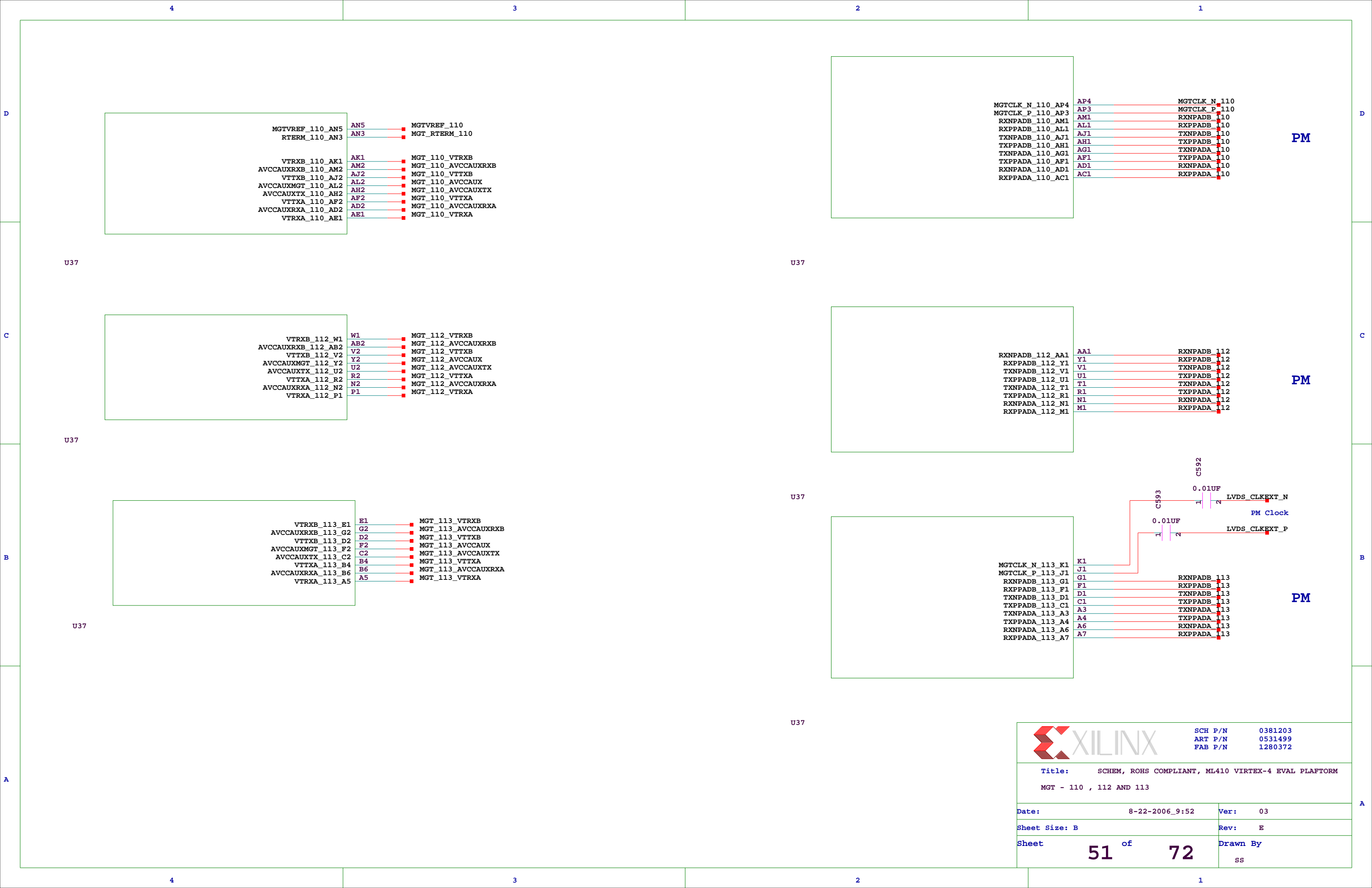
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ART P/N 0531499  
FAB P/N 1280372

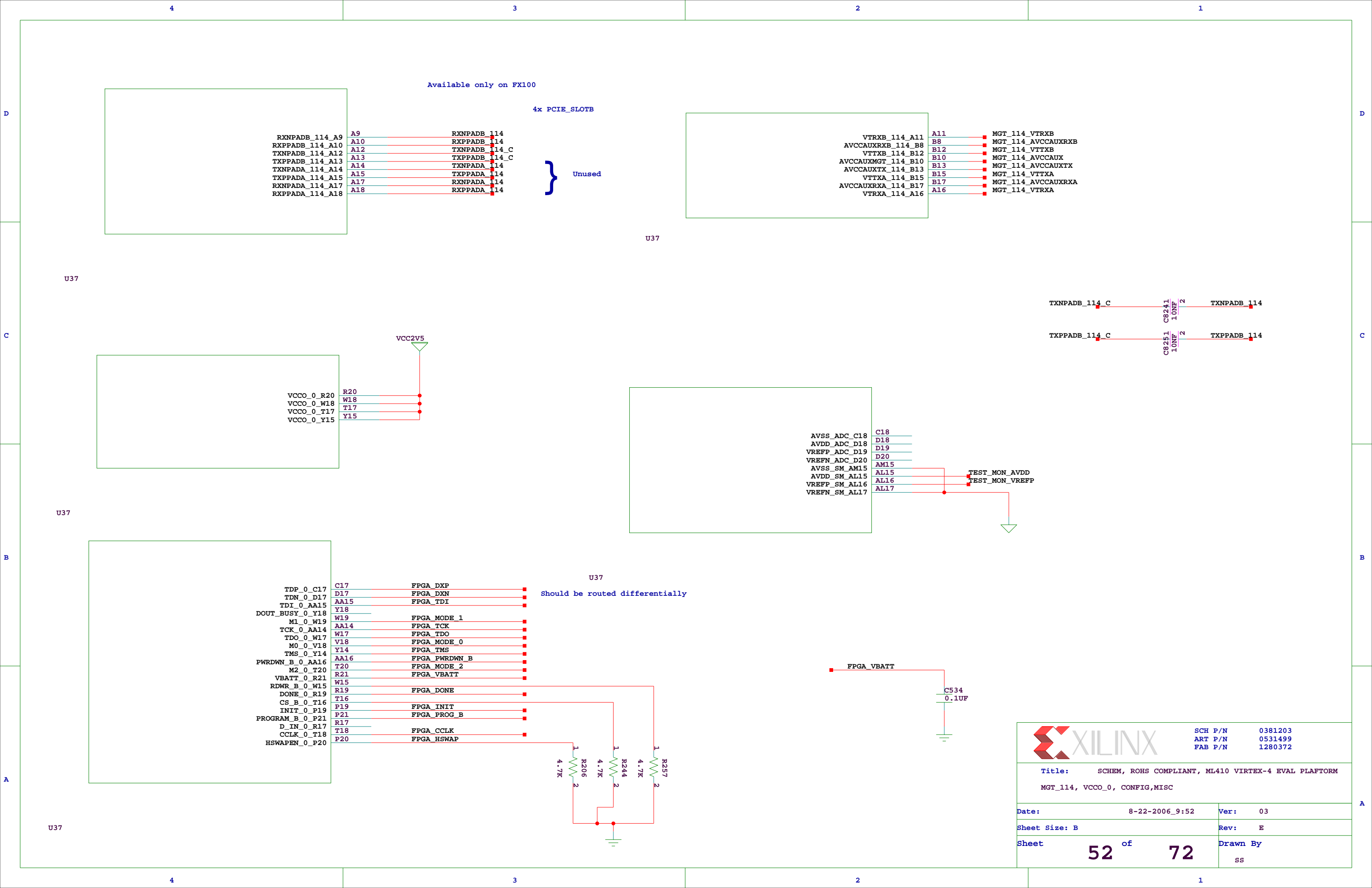
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MGT 105, 106 AND 109 - PM, SATA+CLK, PCIE

Date: 8-22-2006\_9:52 Ver: 03

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Available only on FX100

4x PCIE\_SLOTB

Unused

U37

U37

VCC2V5

U37

Should be routed differentially

FPGA\_VBATT

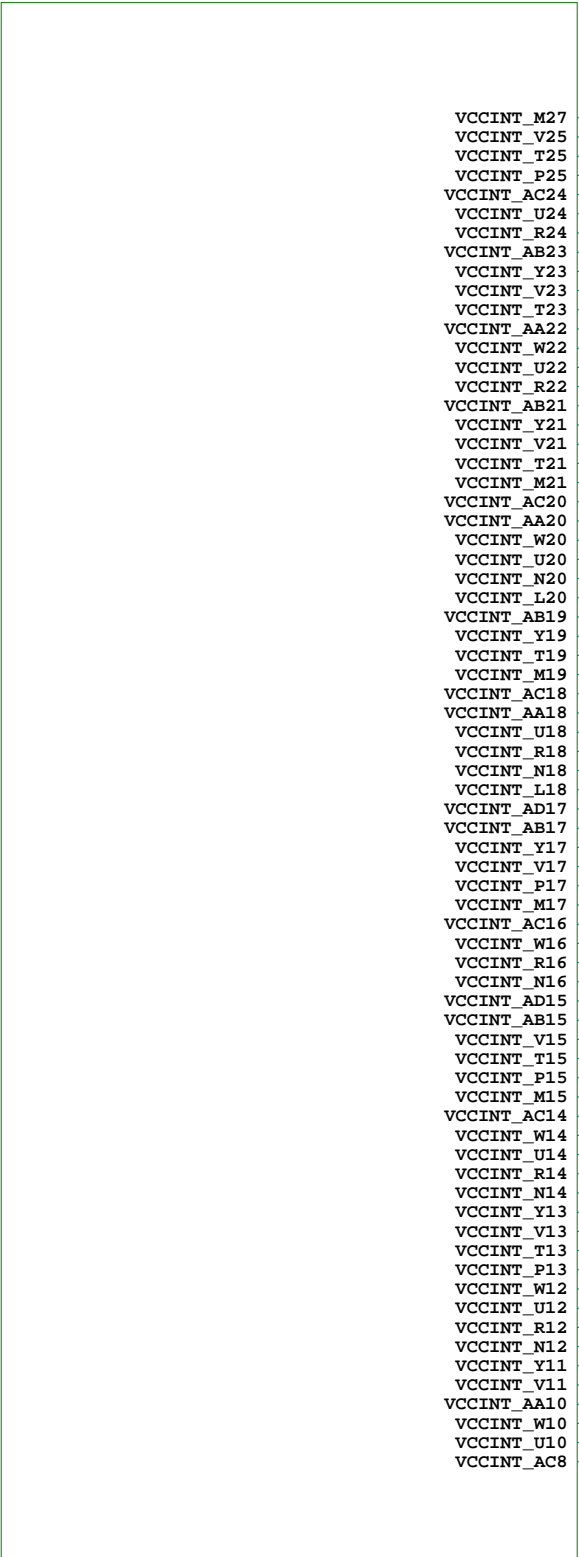
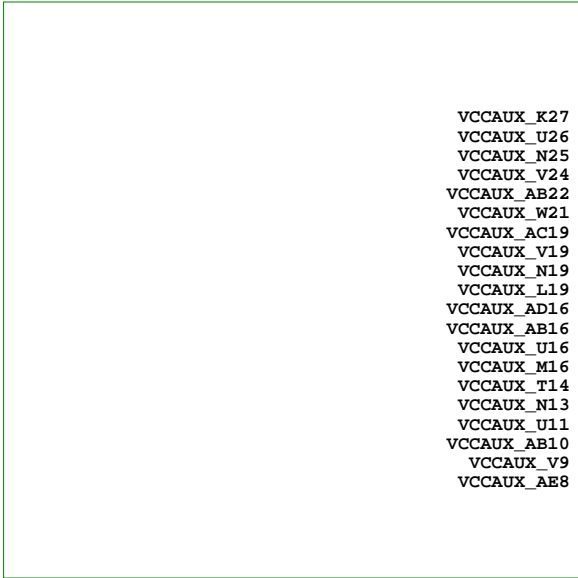
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SCH P/N 0381203  
ART P/N 0531499  
FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLATFOrm  
MGT\_114, VCCO\_0, CONFIG,MISC

Date:	8-22-2006_9:52	Ver:	03
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ART P/N 0531499  
FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLATFORM  
FPGA CORE AND VCCAUX PINS

Date:	8-22-2006_9:52	Ver:	03
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GND_AC15	AC15
GND_U15	U15
GND_R15	R15
GND_N15	N15
GND_E15	E15
GND_AM14	AM14
GND_AB14	AB14
GND_V14	V14
GND_P14	P14
GND_M14	M14
GND_AJ13	AJ13
GND_W13	W13
GND_U13	U13
GND_R13	R13
GND_J13	J13
GND_AF12	AF12
GND_Y12	Y12
GND_V12	V12
GND_T12	T12
GND_P12	P12
GND_F12	F12
GND_AC11	AC11
GND_W11	W11
GND_N11	N11
GND_C11	C11
GND_AK10	AK10
GND_Y10	Y10
GND_V10	V10
GND_K10	K10
GND_AG9	AG9
GND_U9	U9
GND_G9	G9
GND_AD8	AD8
GND_P8	P8
GND_D8	D8
GND_AL7	AL7
GND_AA7	AA7
GND_L7	L7
GND_AH6	AH6
GND_V6	V6
GND_H6	H6
GND_AE5	AE5
GND_R5	R5
GND_E5	E5
GND_AM4	AM4
GND_AB4	AB4
GND_M4	M4
GND_AJ3	AJ3
GND_W3	W3
GND_J3	J3



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GND_AE25	AE25
GND_U25	U25
GND_R25	R25
GND_E25	E25
GND_AM24	AM24
GND_AB24	AB24
GND_T24	T24
GND_M24	M24
GND_AJ23	AJ23
GND_AA23	AA23
GND_W23	W23
GND_U23	U23
GND_R23	R23
GND_J23	J23
GND_AF22	AF22
GND_Y22	Y22
GND_V22	V22
GND_T22	T22
GND_F22	F22
GND_AC21	AC21
GND_AA21	AA21
GND_U21	U21
GND_N21	N21
GND_C21	C21
GND_AK20	AK20
GND_AB20	AB20
GND_Y20	Y20
GND_V20	V20
GND_M20	M20
GND_K20	K20
GND_AG19	AG19
GND_AA19	AA19
GND_U19	U19
GND_G19	G19
GND_AM18	AM18
GND_AD18	AD18
GND_AB18	AB18
GND_P18	P18
GND_M18	M18
GND_AC17	AC17
GND_AA17	AA17
GND_U17	U17
GND_N17	N17
GND_L17	L17
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GND_H16	H16
GND_AE15	AE15



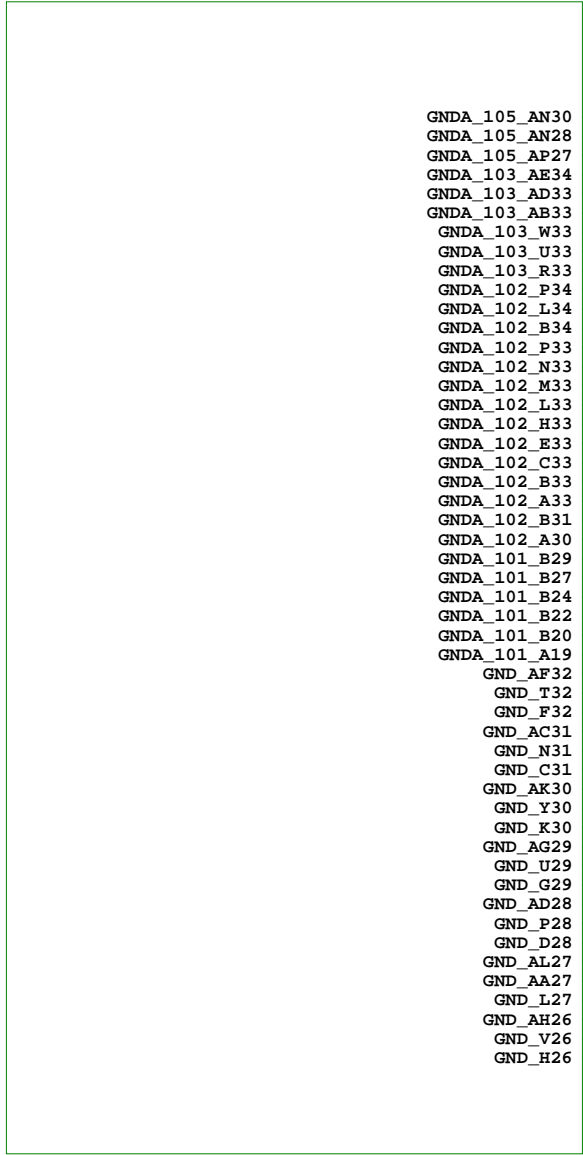
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FAB P/N	1280372

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FPGA GROUND PINS

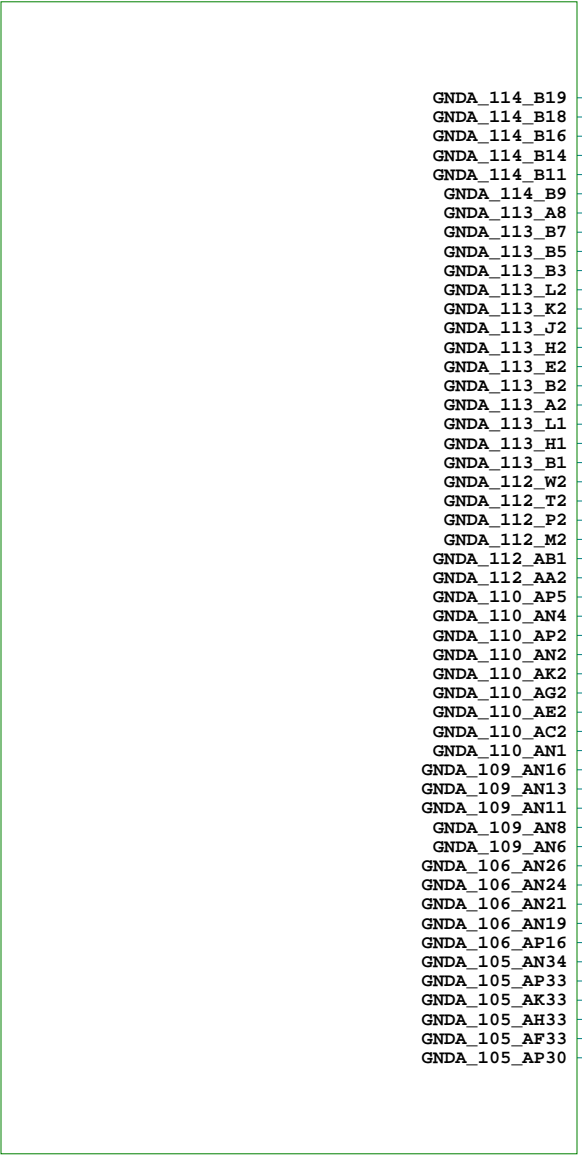
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- AN30
- AN28
- AP27
- AE34
- AD33
- AB33
- W33
- U33
- R33
- P34
- L34
- B34
- P33
- N33
- M33
- L33
- H33
- E33
- C33
- B33
- A33
- B31
- A30
- B29
- B27
- B24
- B22
- B20
- A19
- AF32
- T32
- F32
- AC31
- N31
- C31
- AK30
- Y30
- K30
- AG29
- U29
- G29
- AD28
- P28
- D28
- AL27
- AA27
- L27
- AH26
- V26
- H26



- B19
- B18
- B16
- B14
- B11
- B9
- A8
- B7
- B5
- B3
- L2
- K2
- J2
- H2
- E2
- B2
- A2
- L1
- H1
- B1
- W2
- T2
- P2
- M2
- AB1
- AA2
- AP5
- AN4
- AP2
- AN2
- AK2
- AG2
- AE2
- AC2
- AN1
- AN16
- AN13
- AN11
- AN8
- AN6
- AN26
- AN24
- AN21
- AN19
- AP16
- AN34
- AP33
- AK33
- AH33
- AF33
- AP30



SCH P/N0381203

ART P/N0531499

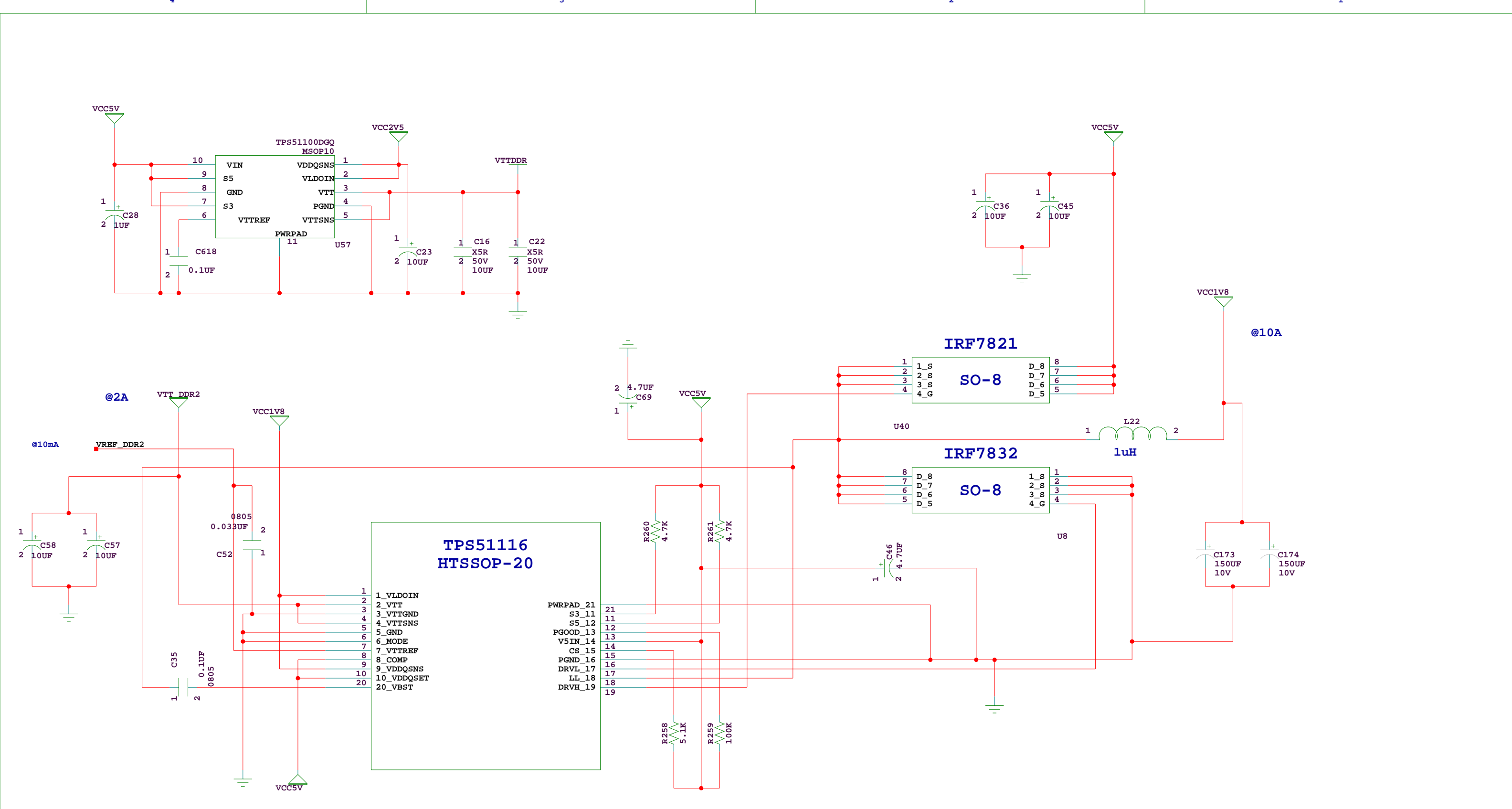
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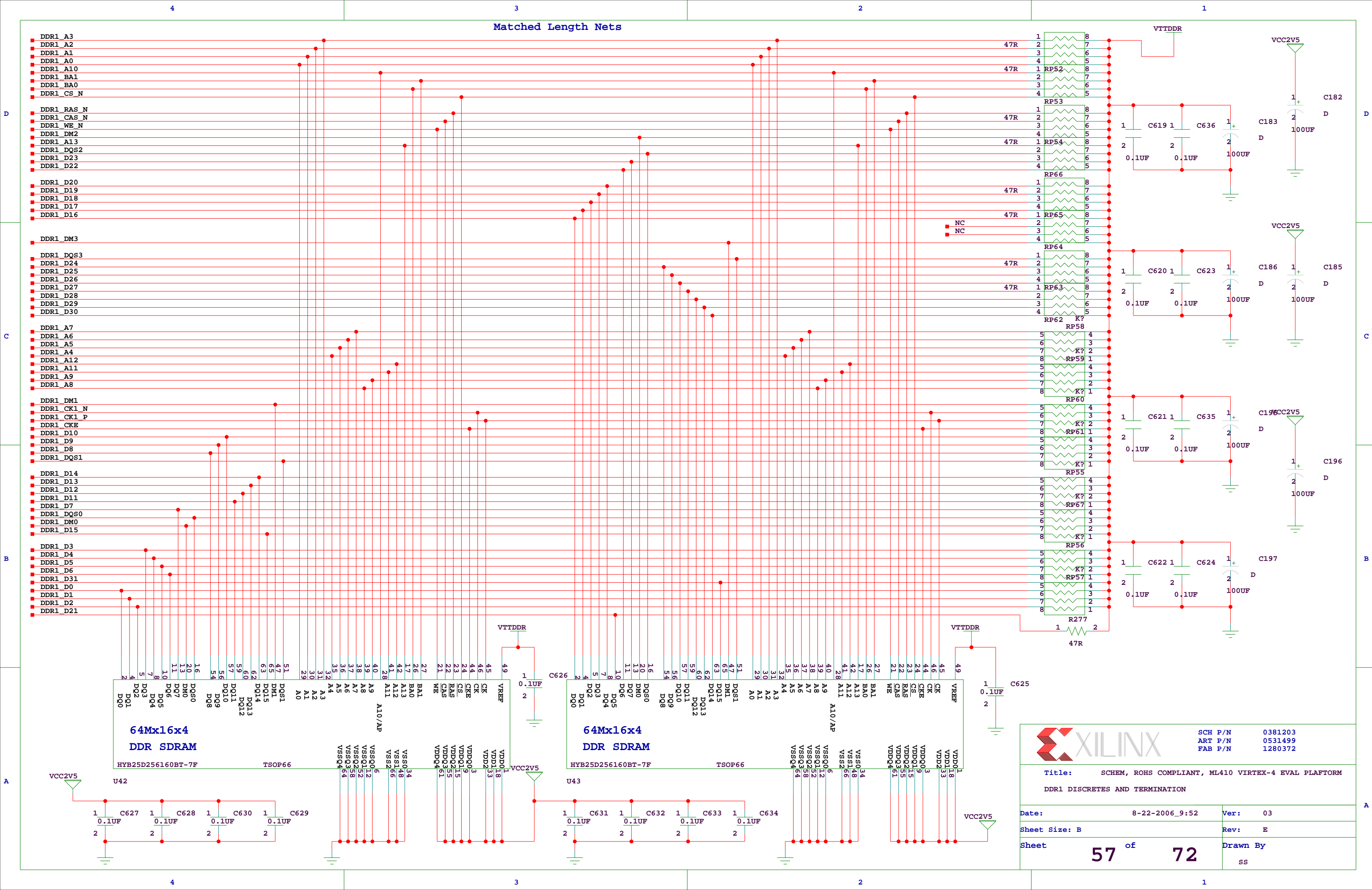
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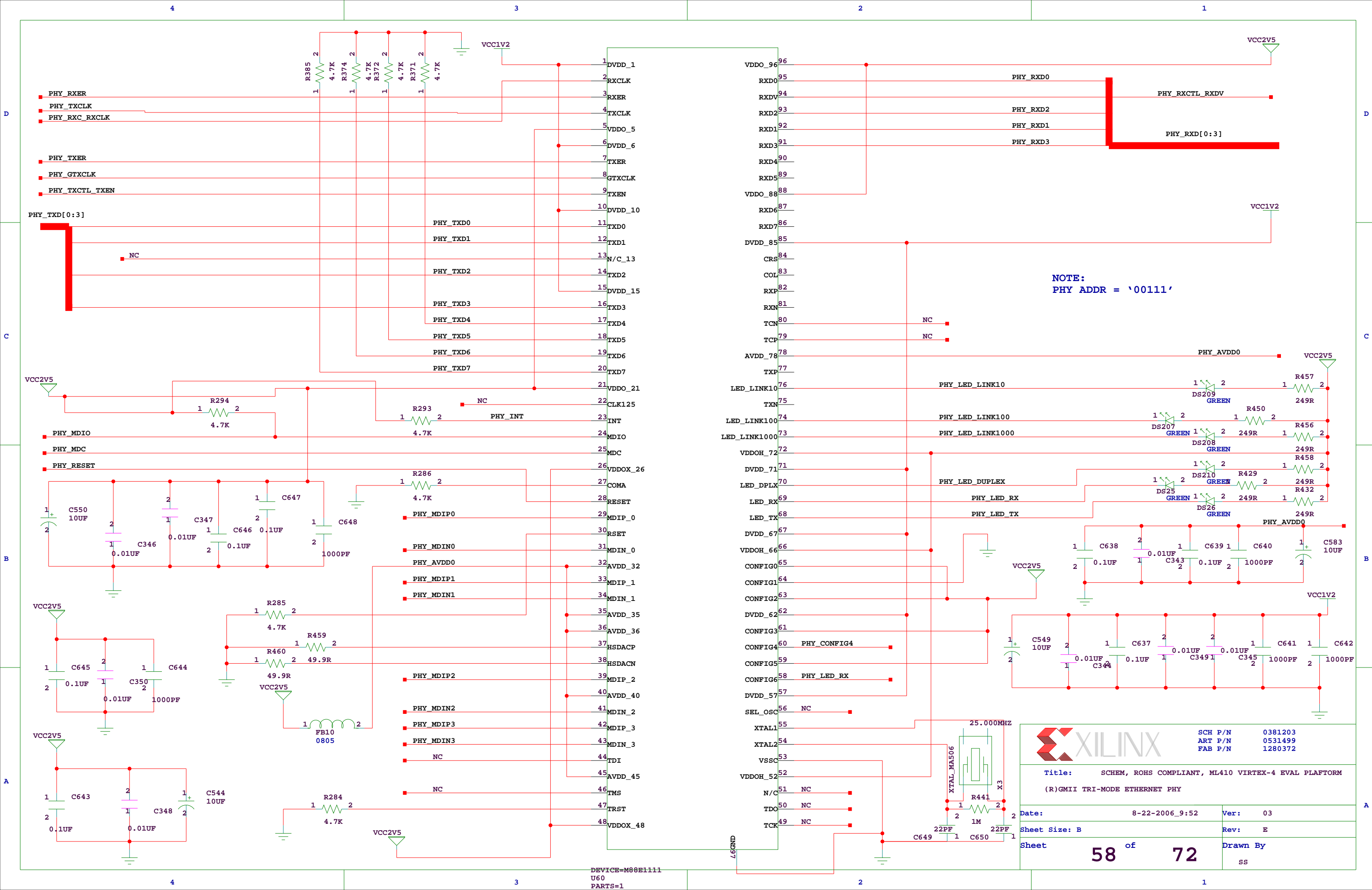
SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFORM

FPGA GROUND PINS

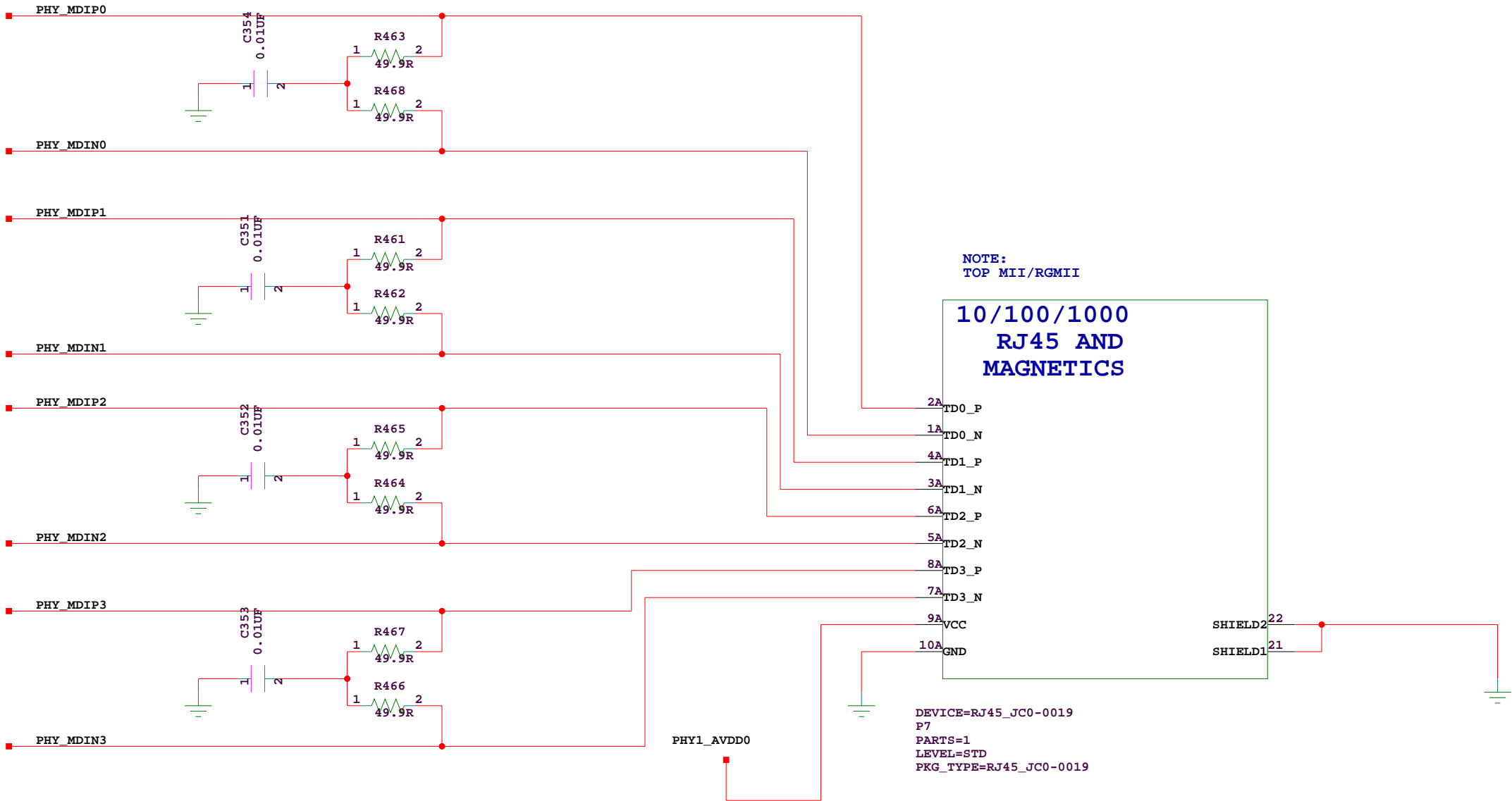
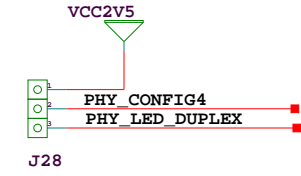
Date:	8-22-2006_9:52	Ver:	03
Sheet Size:	B	Rev:	E
Sheet	55 of 72	Drawn By	SS







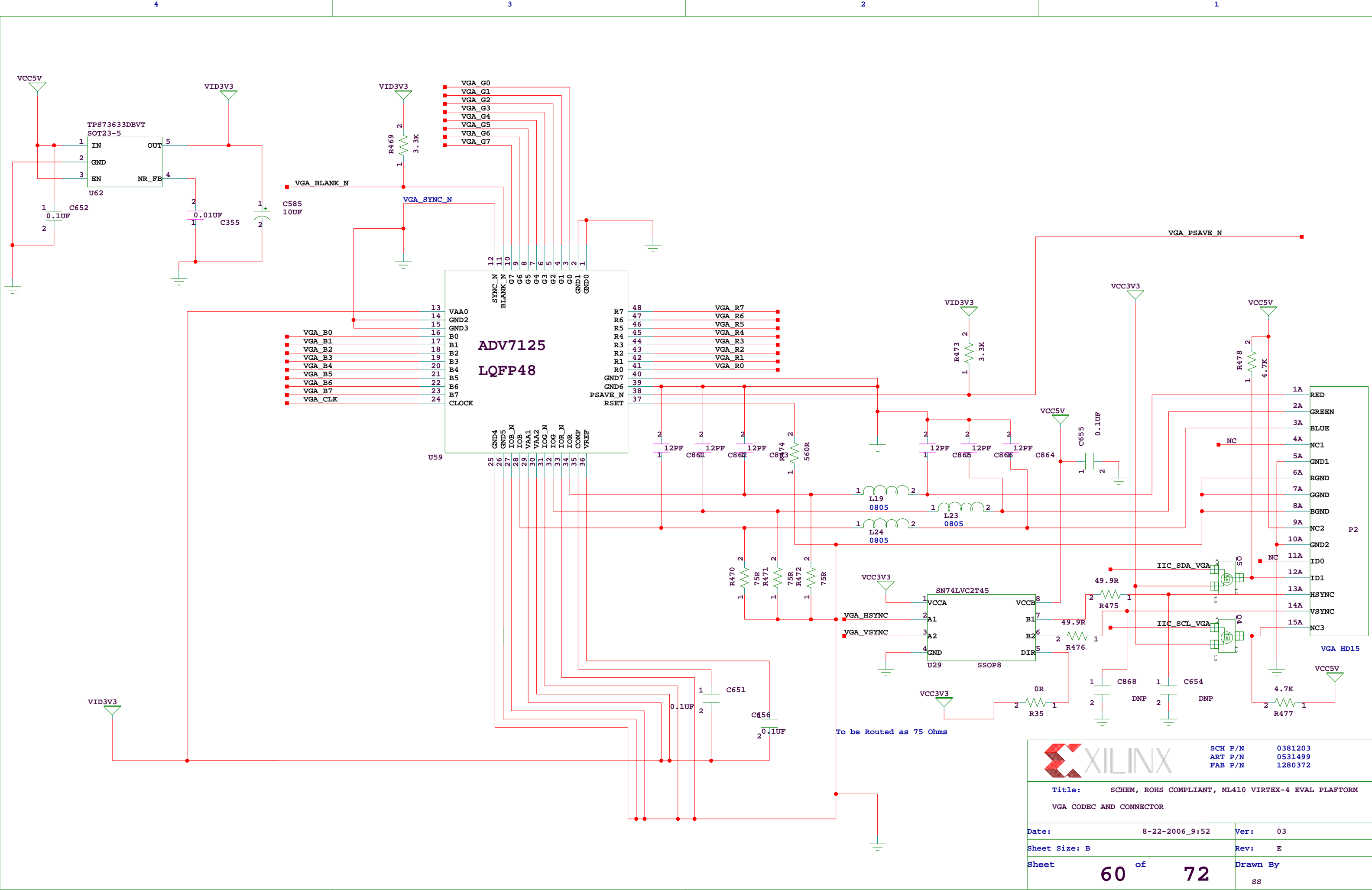
1-2: MII to Cu  
2-3: RGMII to Cu



SCH P/N 0381203  
ART P/N 0531499  
FAB P/N 1280372

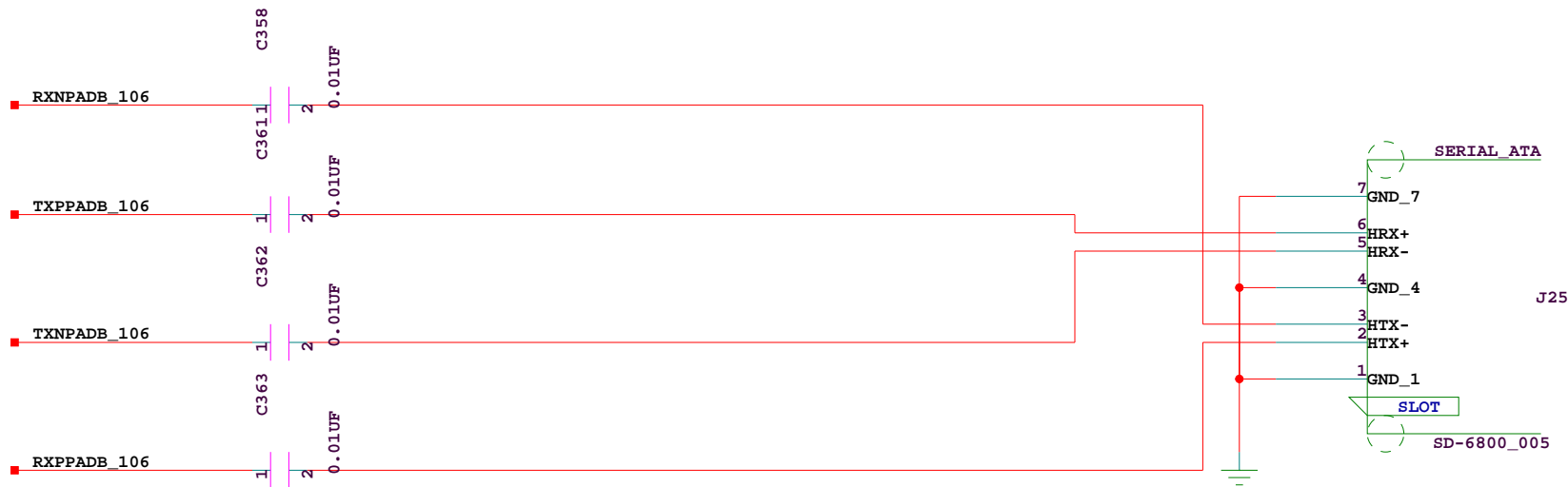
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFORM  
(R)GMII RJ-45

Date:	8-22-2006_9:52	Ver:	03
Sheet Size:	B	Rev:	E
Sheet	59 of 72	Drawn By	SS



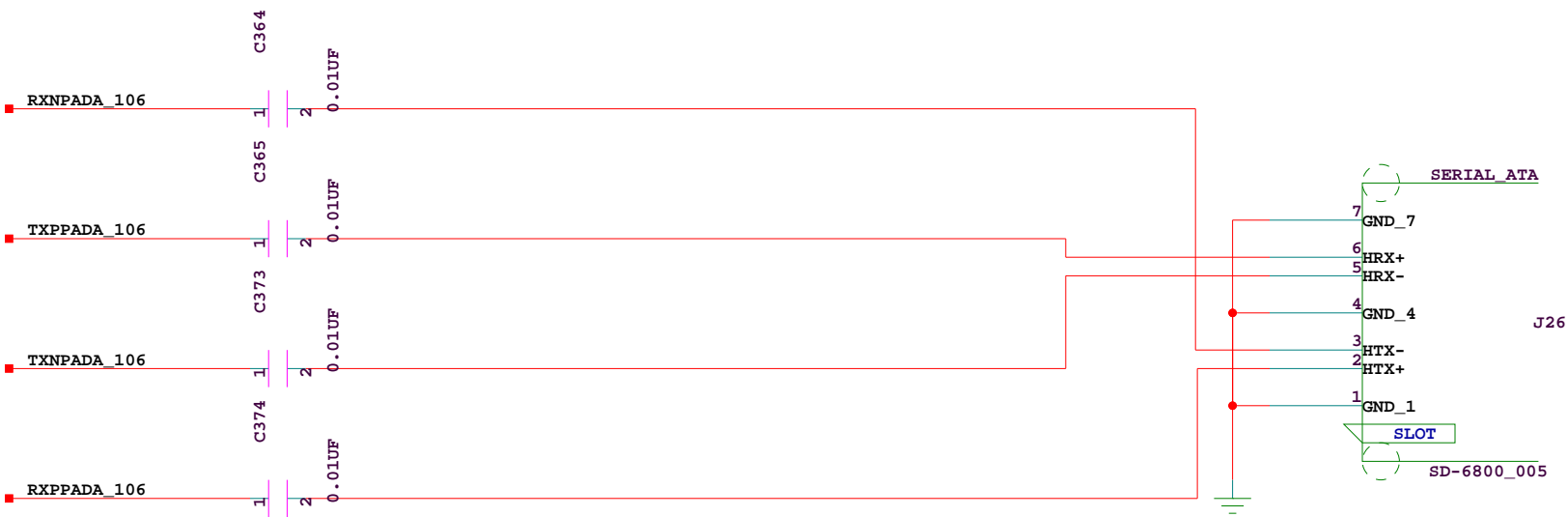
SATA Host 1


MGT 106B

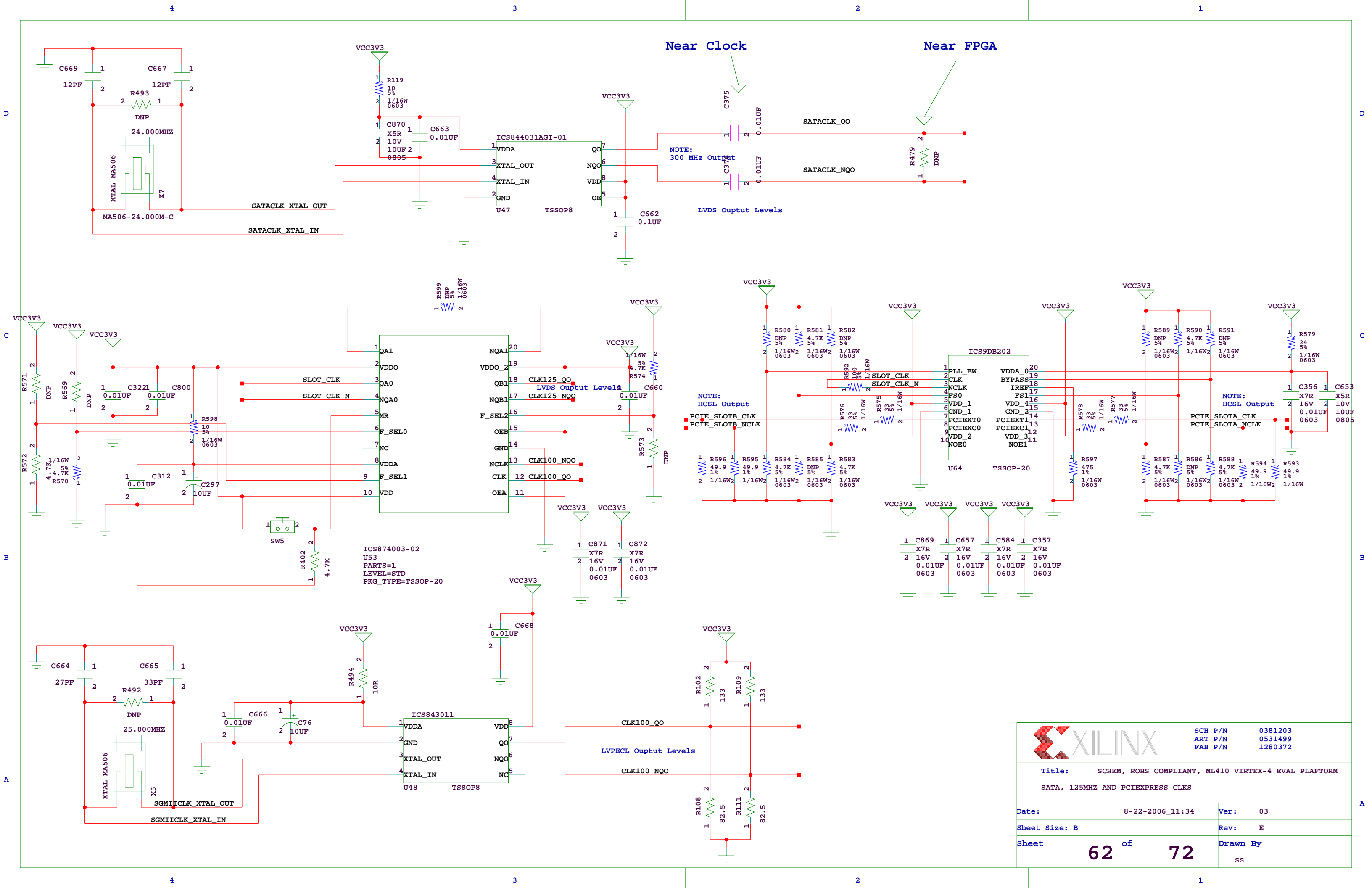


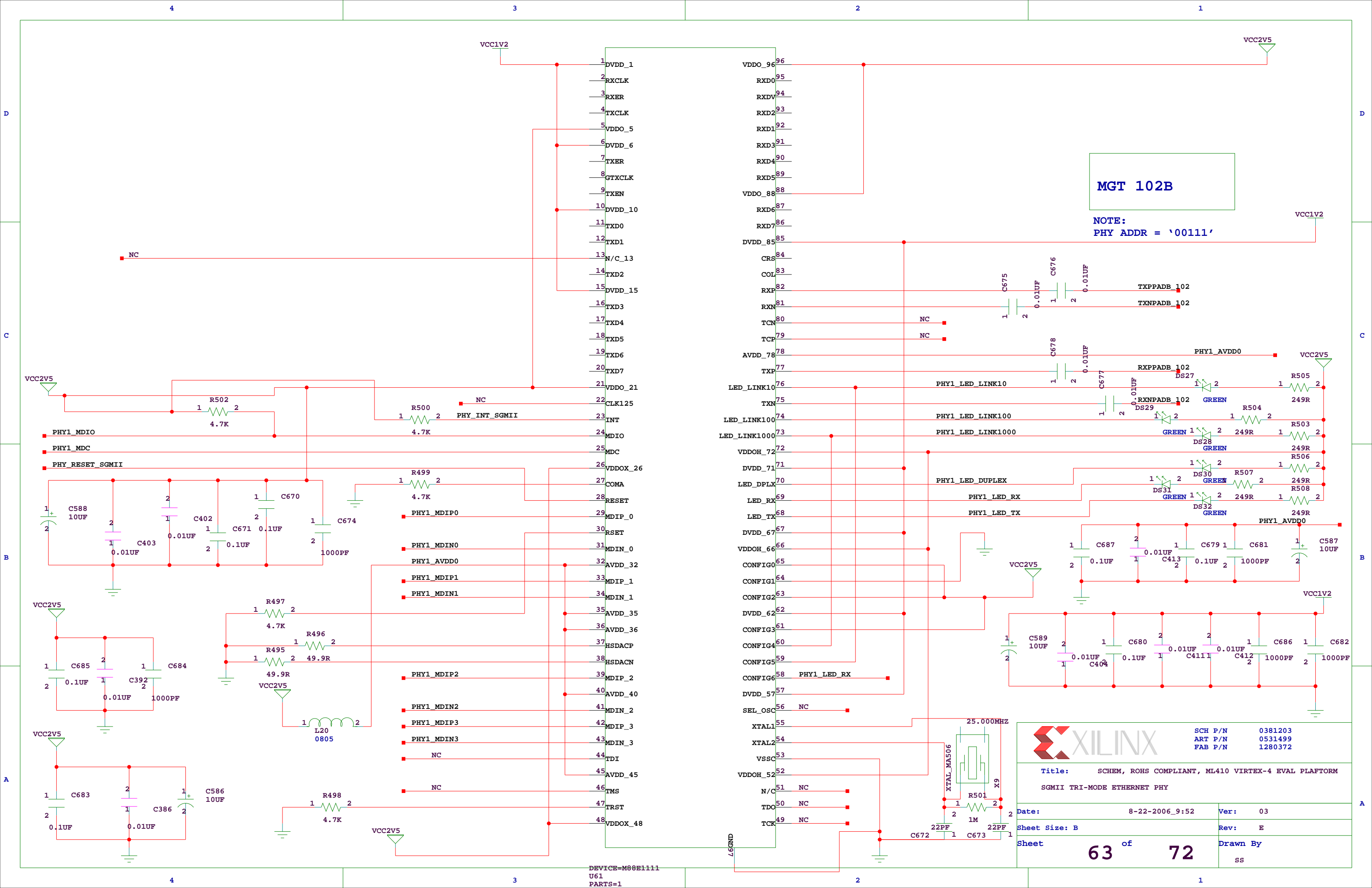
SATA Host 2

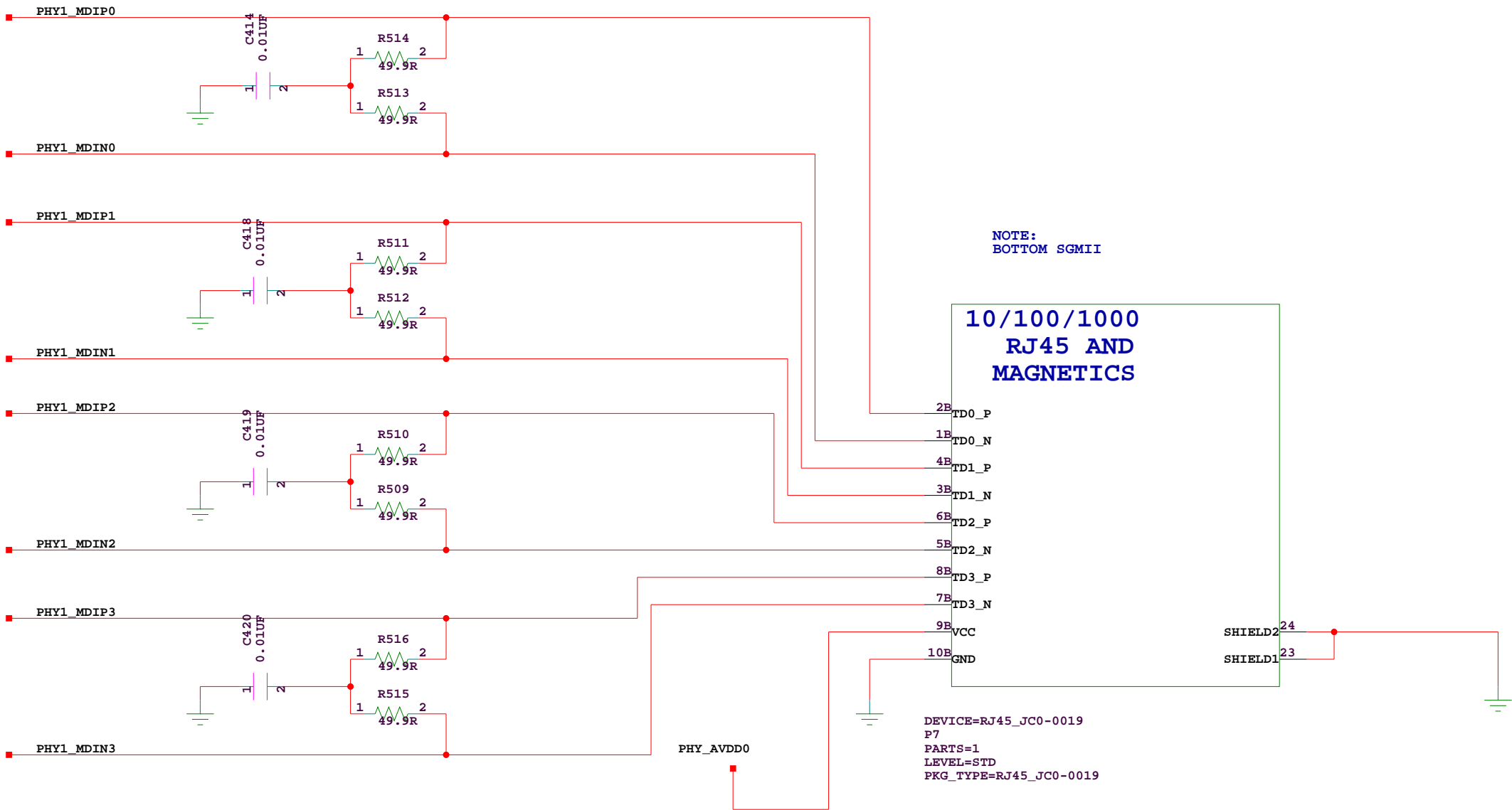
MGT 106A



		SCH P/N	0381203
		ART P/N	0531499
		FAB P/N	1280372
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLATFORM SATA INTERFACE			
Date: 8-22-2006_9:52		Ver:	03
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NOTE:  
BOTTOM SGMII

10/100/1000  
RJ45 AND  
MAGNETICS

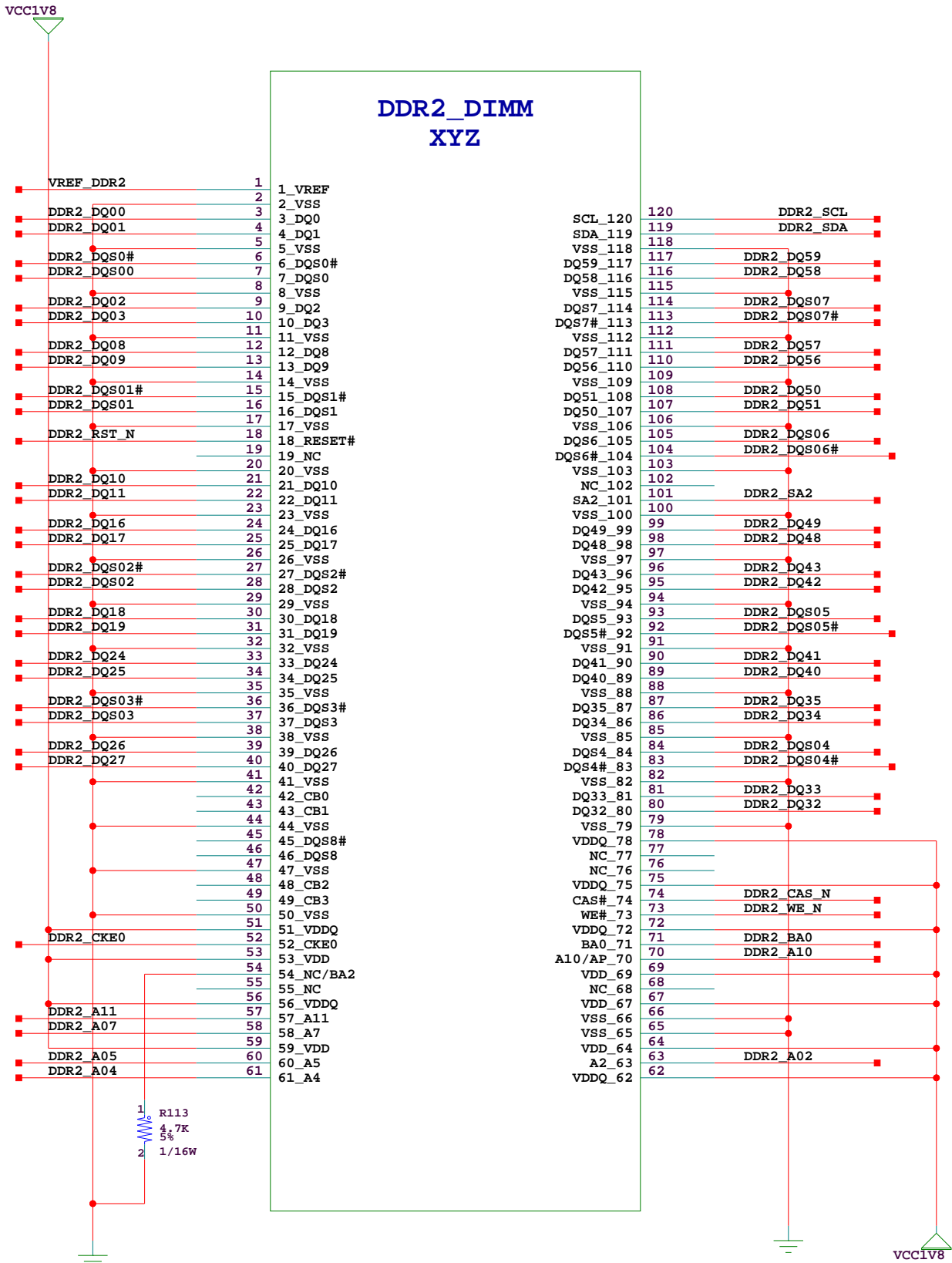
DEVICE=RJ45\_JC0-0019  
P7  
PARTS=1  
LEVEL=STD  
PKG\_TYPE=RJ45\_JC0-0019



SCH P/N 0381203  
ART P/N 0531499  
FAB P/N 1280372

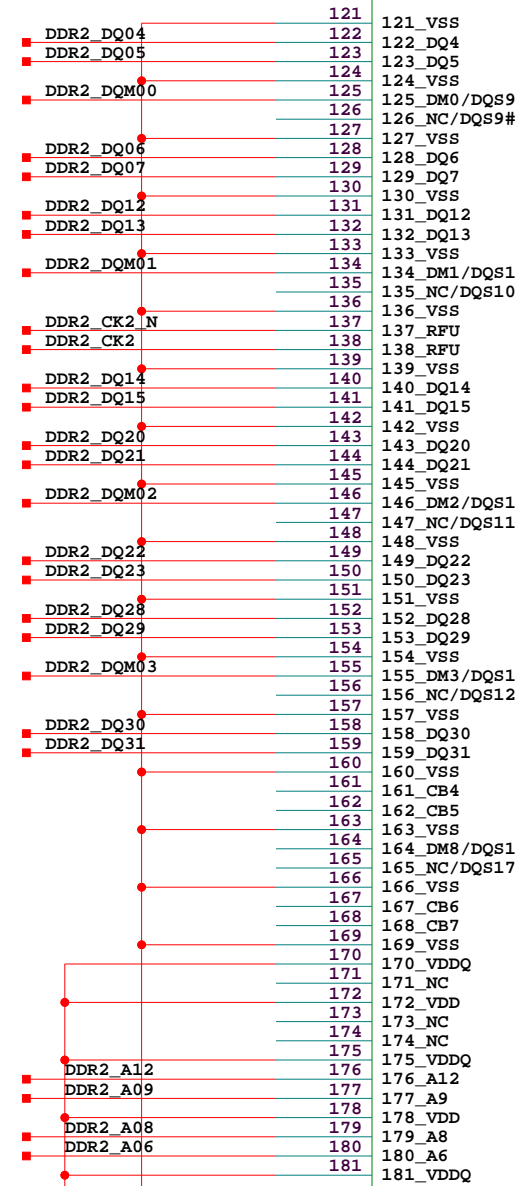
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SGMII RJ-45

Date:	8-22-2006_9:52	Ver:	03
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P48

DEVICE=DDR2\_DIMM  
PKG\_TYPE=CON-240-DDRAM  
PARTS=1  
LEVEL=STD



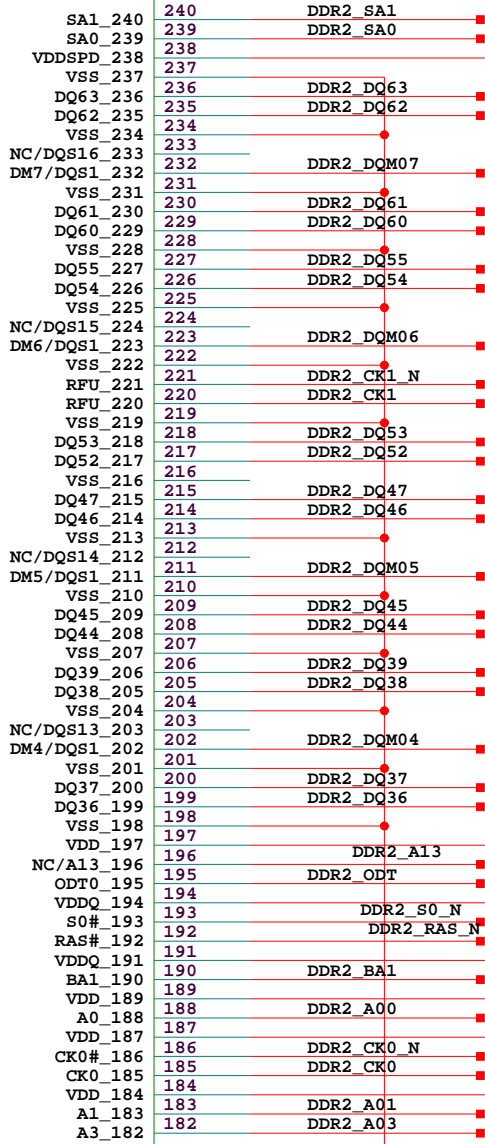
P48

DEVICE=DDR2\_DIMM  
PKG\_TYPE=CON-240-DDRAM  
PARTS=1  
LEVEL=STD

I2C ADDR = 0x68

I2C ADDR = 0xA8

## DDR2\_DIMM XYZ



SCH P/N 0381203  
ART P/N 0531499  
FAB P/N 1280372

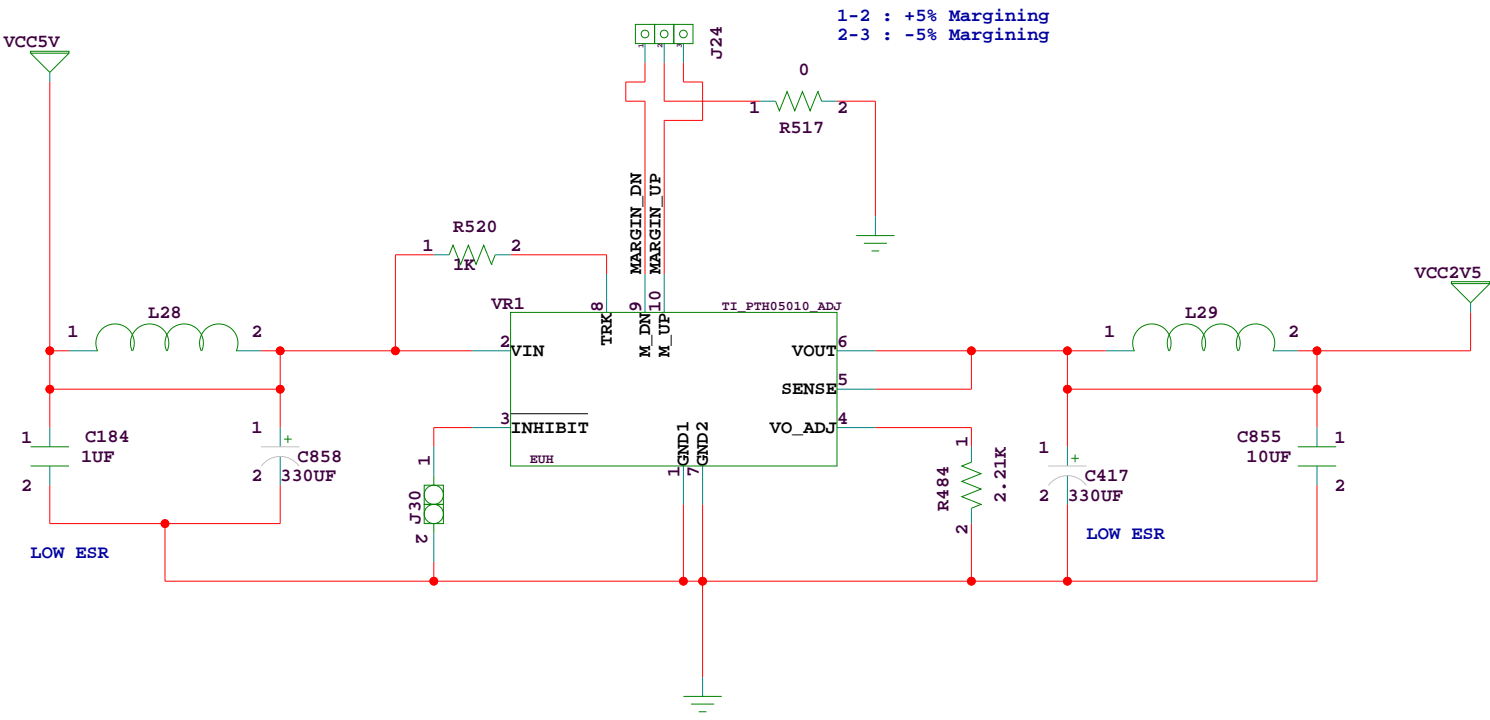
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DDR2 DIMM CONNECTOR

Date: 8-22-2006\_9:52 Ver: 03

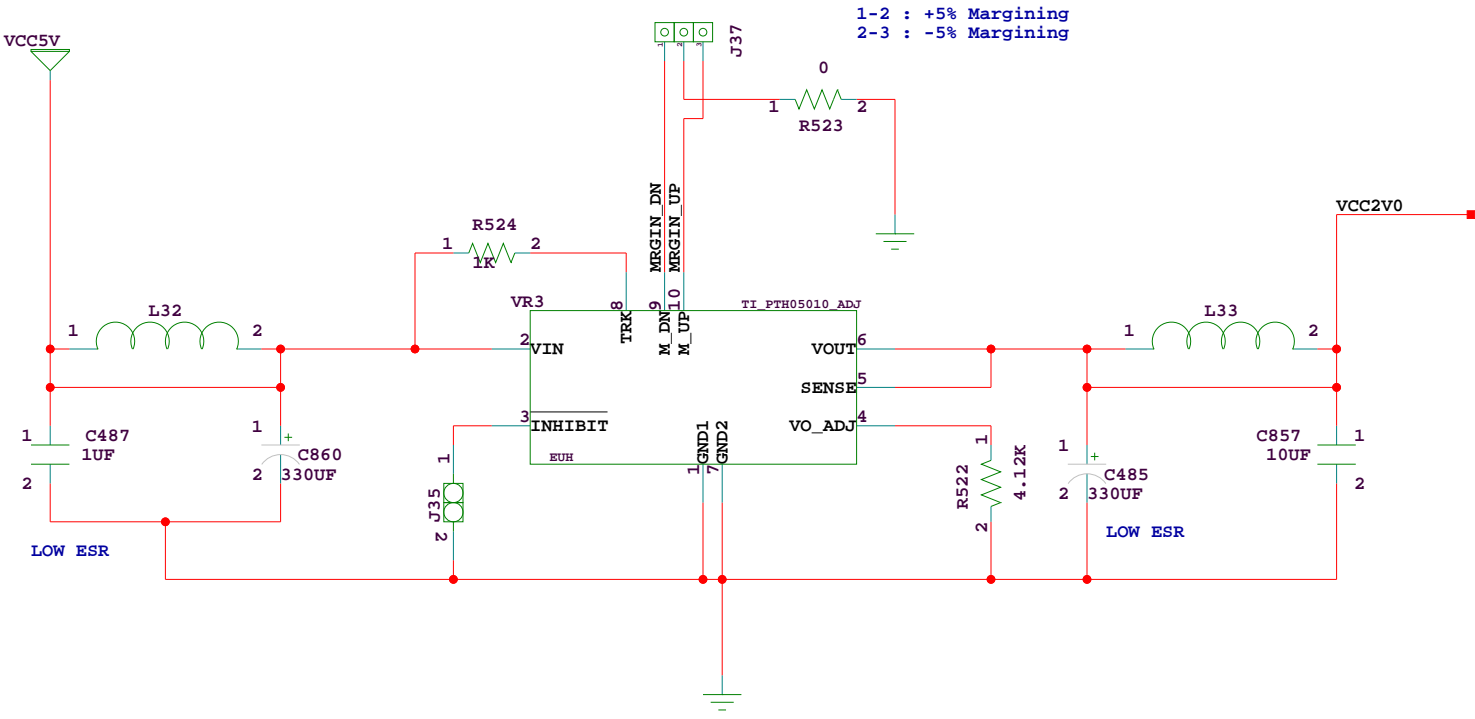
Sheet Size: B Rev: E

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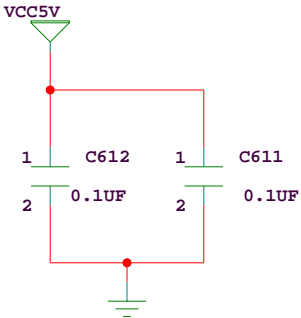
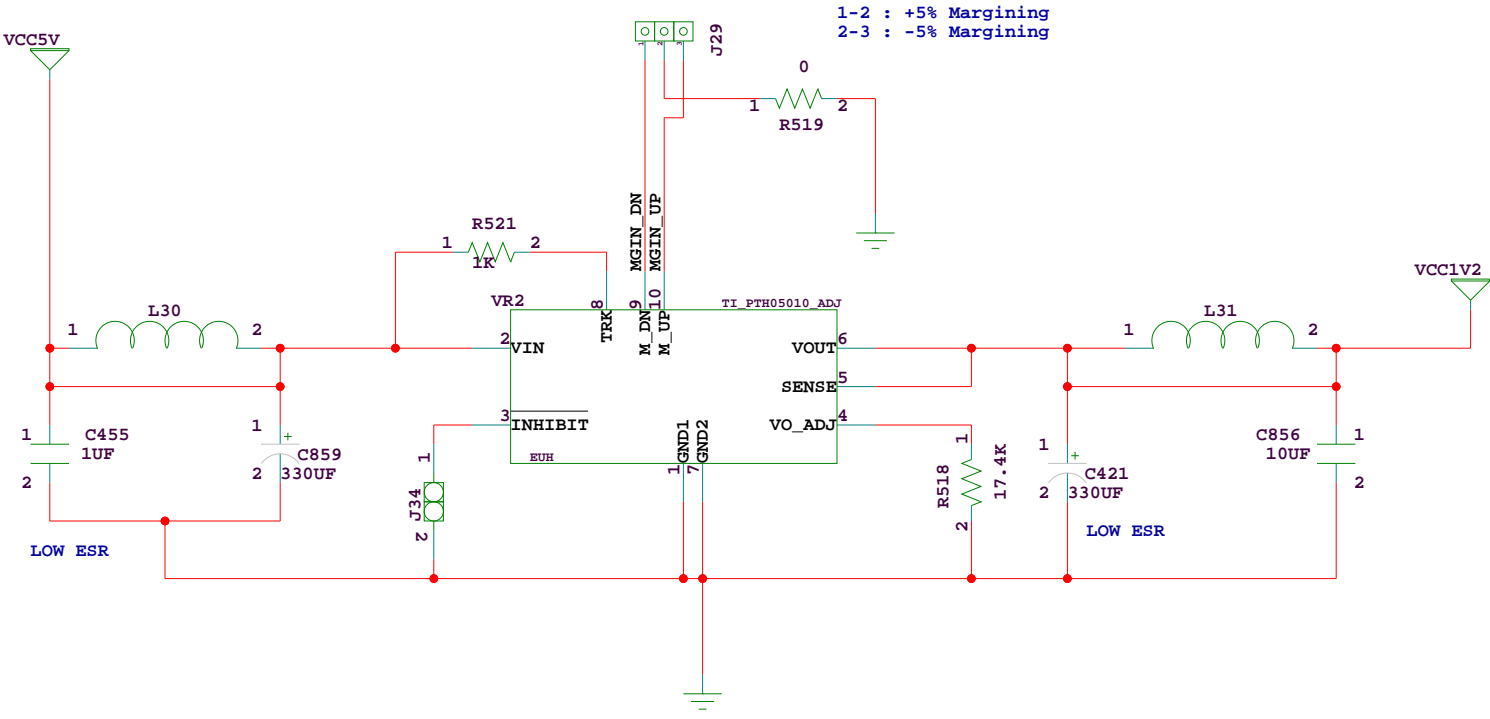
2.5V Supply @15A



2.0V Supply @15A



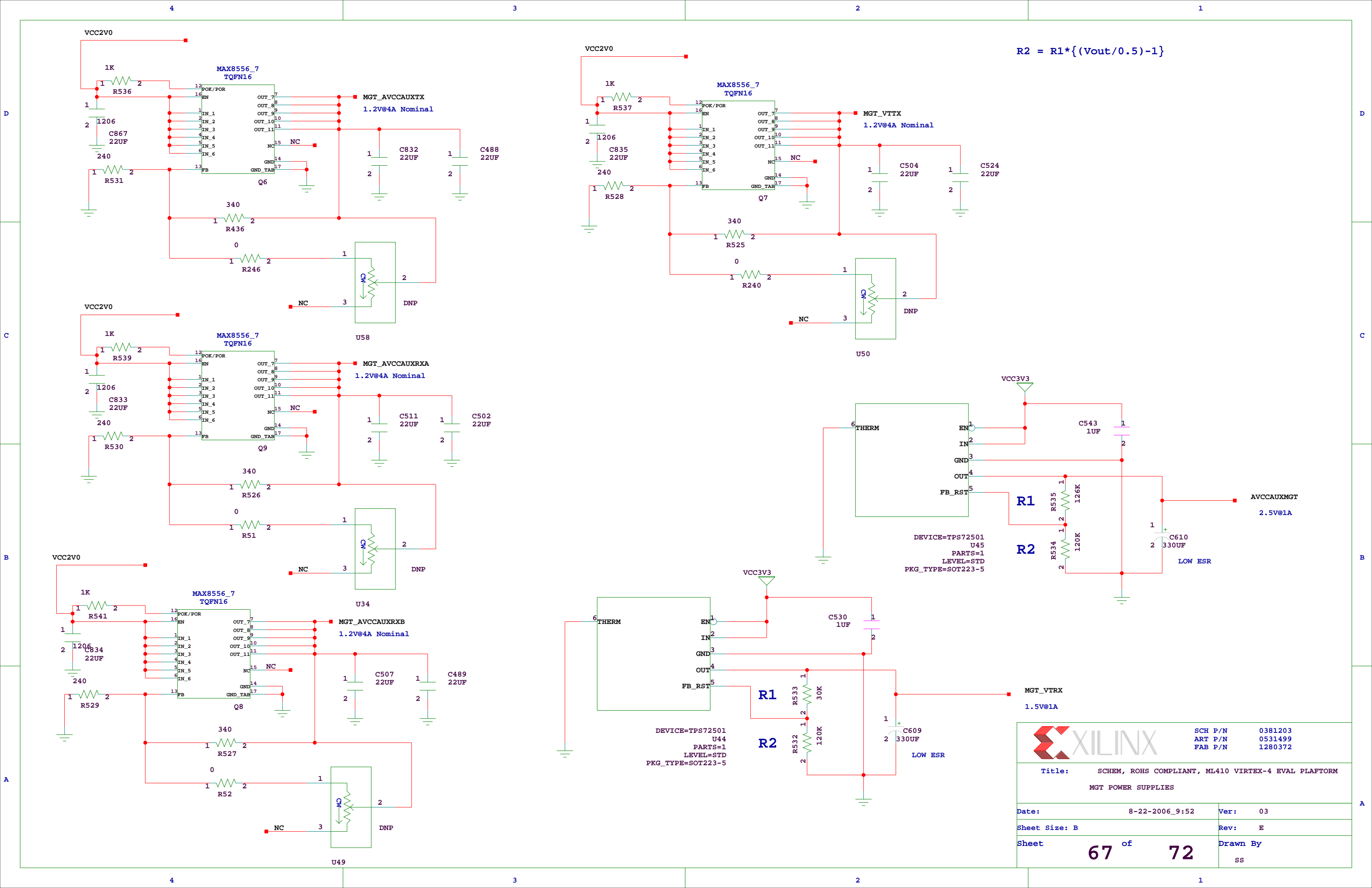
1.2V Supply @15A

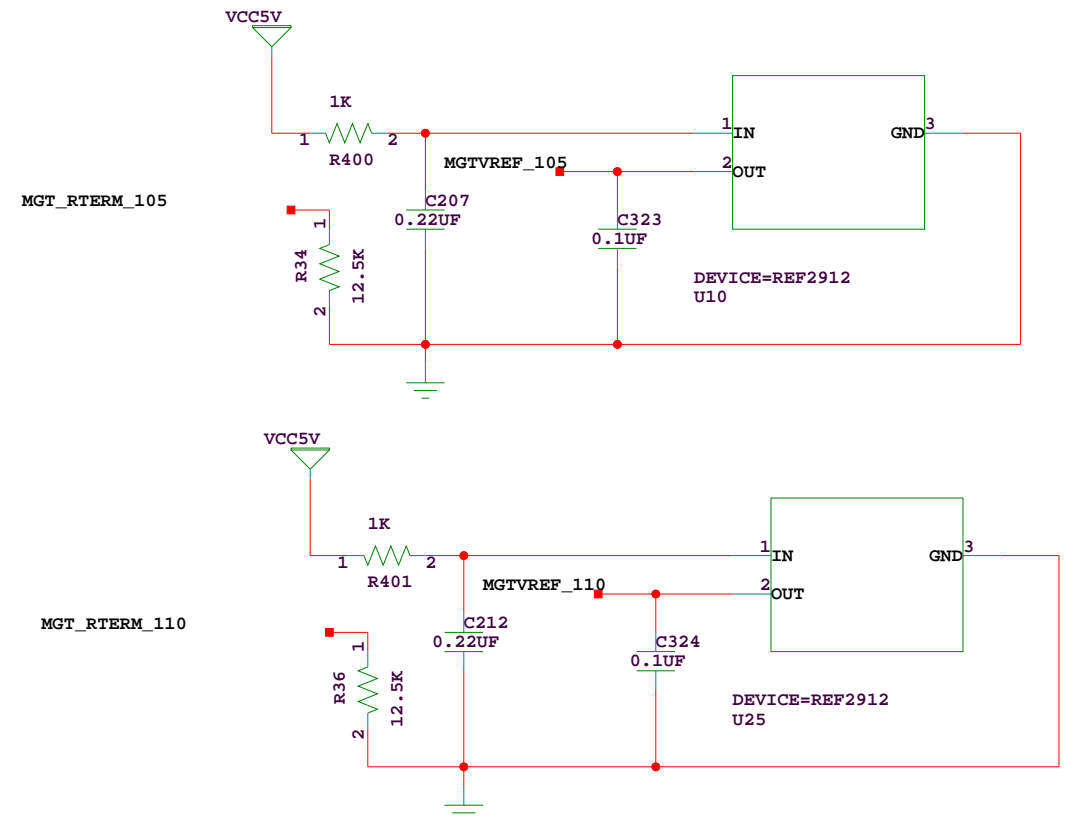
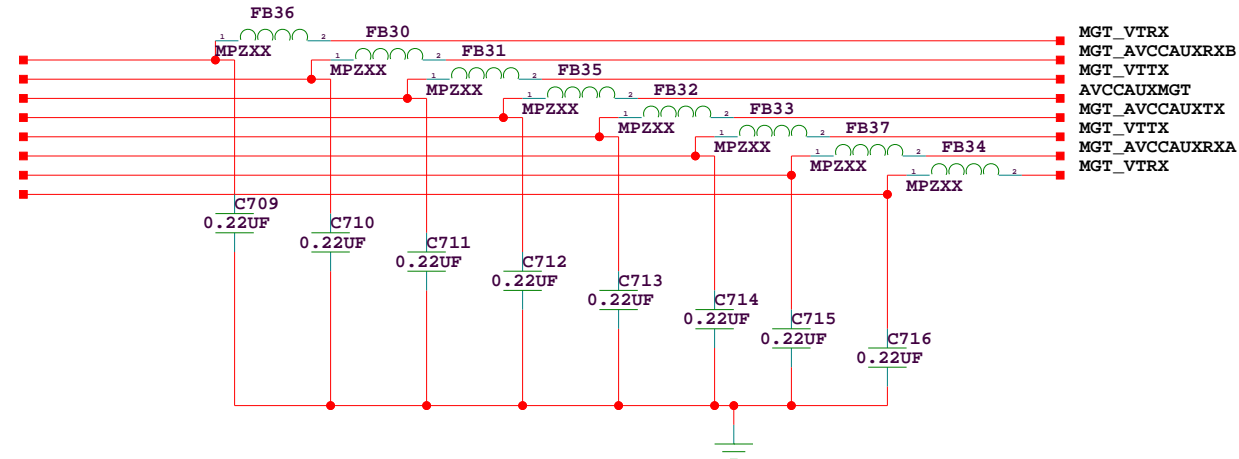
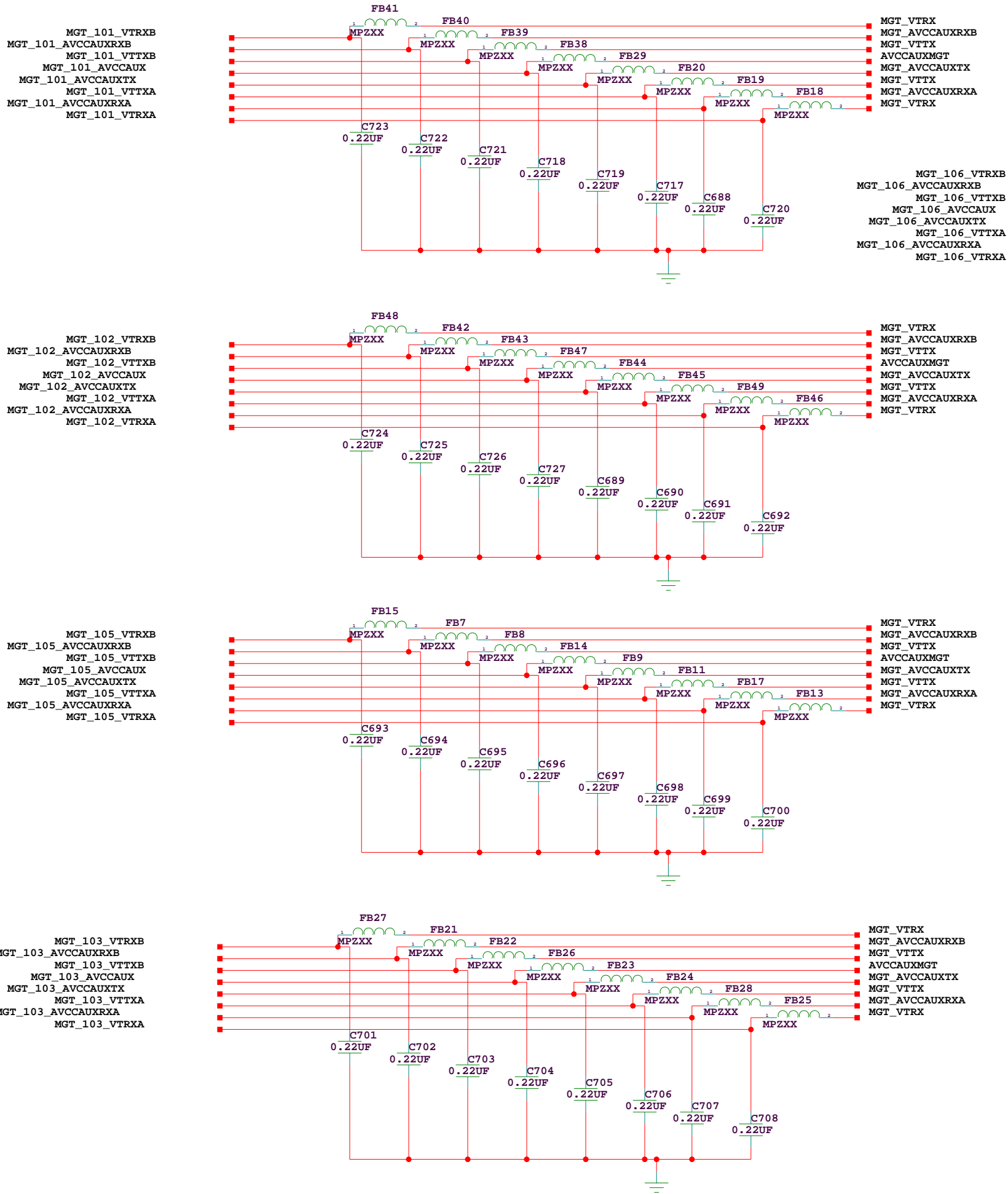


$$RSET = 10K * (0.8V / (VOUT - 0.8V) - 2.49K)$$
$$Vout = (8K / (RSET + 2.49K)) * 0.8V$$

For 2.0V, R29 = 4.176K

	SCH P/N	0381203
	ART P/N	0531499
	FAB P/N	1280372
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLATFORM FPGA CORE AND IO VOLTAGE		
Date:	8-22-2006_9:52	Ver: 03
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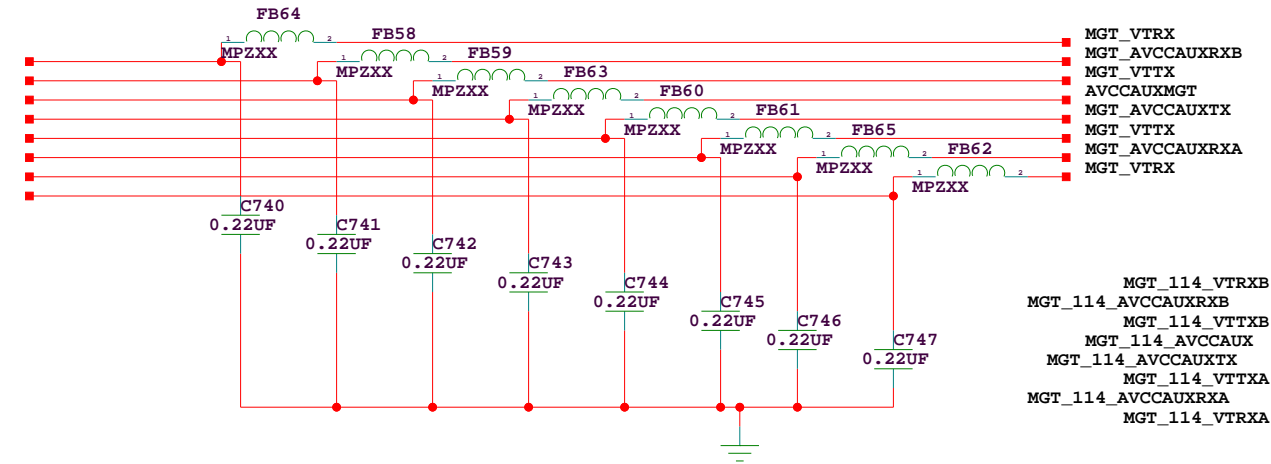
	SCH P/N	0381203
	ART P/N	0531499
	FAB P/N	1280372
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLATFOM		
MGT POWER FILTER-1, VTERM AND RTERM		
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MGT\_109\_VTRXB  
MGT\_109\_AVCCAUXRXB  
MGT\_109\_VTTXB  
MGT\_109\_AVCCAUX  
MGT\_109\_AVCCAUTX  
MGT\_109\_VTTXA  
MGT\_109\_AVCCAUXRXA  
MGT\_109\_VTRXA

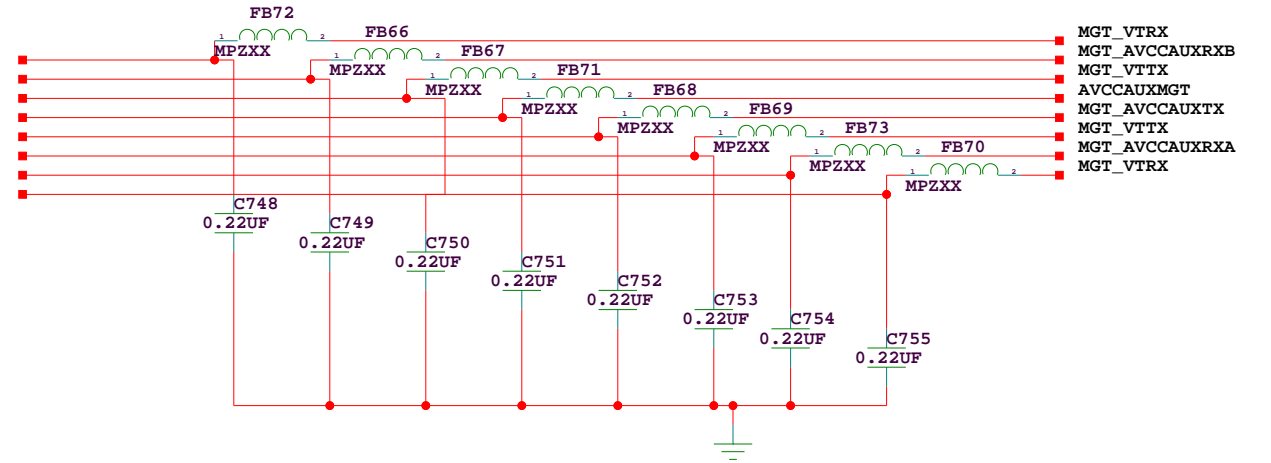
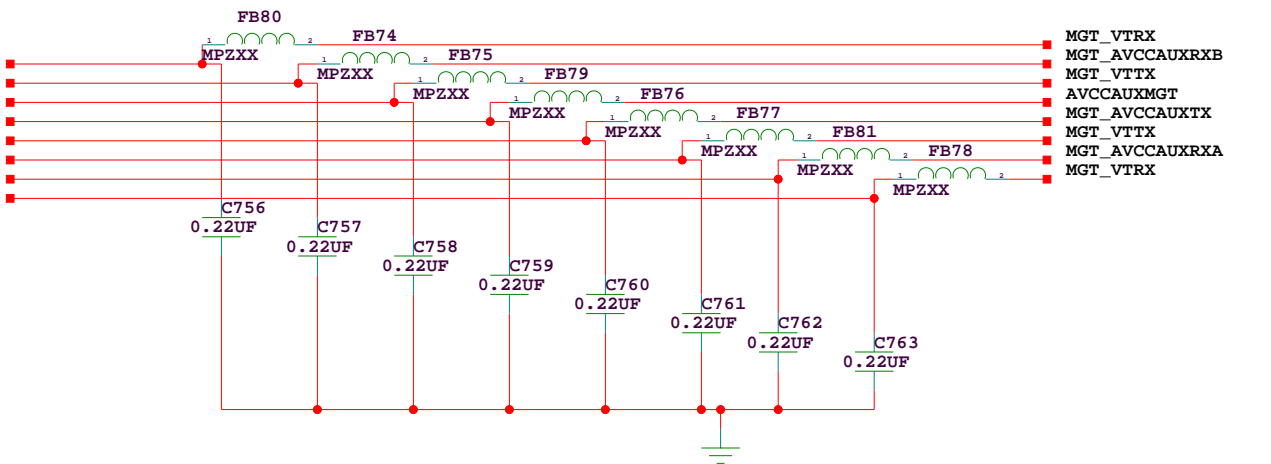
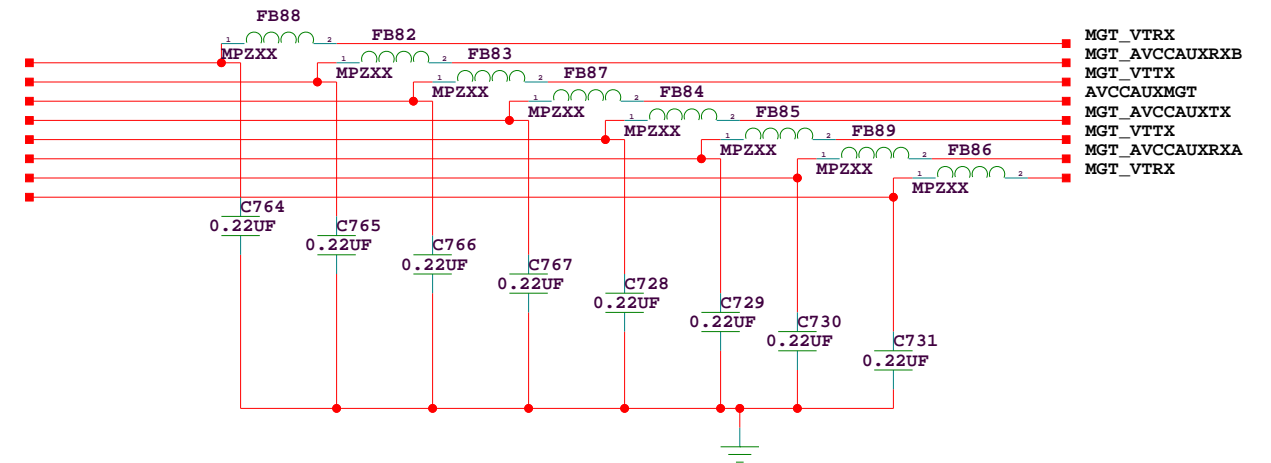
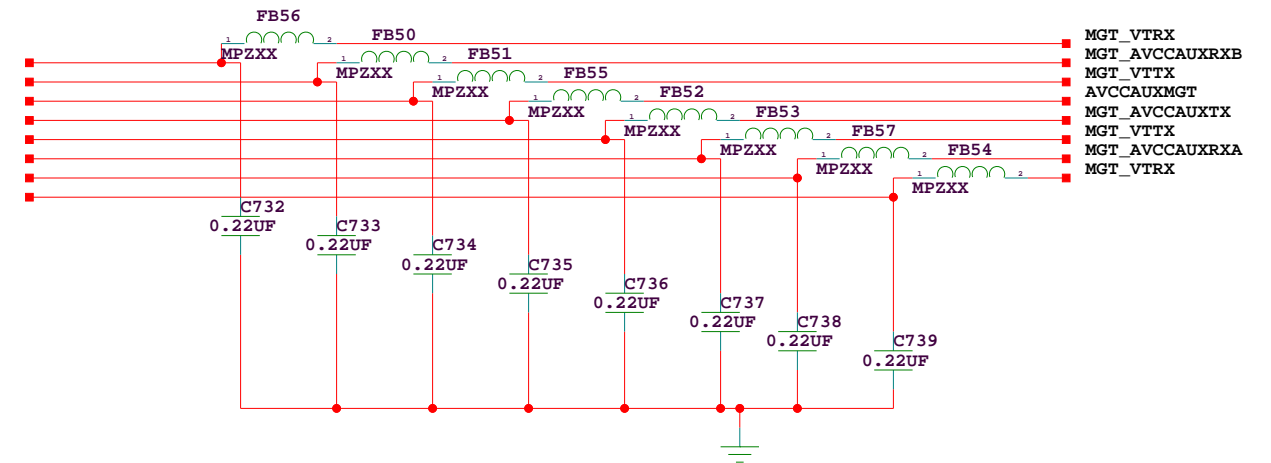
MGT\_112\_VTRXB  
MGT\_112\_AVCCAUXRXB  
MGT\_112\_VTTXB  
MGT\_112\_AVCCAUX  
MGT\_112\_AVCCAUTX  
MGT\_112\_VTTXA  
MGT\_112\_AVCCAUXRXA  
MGT\_112\_VTRXA

MGT\_110\_VTRXB  
MGT\_110\_AVCCAUXRXB  
MGT\_110\_VTTXB  
MGT\_110\_AVCCAUX  
MGT\_110\_AVCCAUTX  
MGT\_110\_VTTXA  
MGT\_110\_AVCCAUXRXA  
MGT\_110\_VTRXA

MGT\_113\_VTRXB  
MGT\_113\_AVCCAUXRXB  
MGT\_113\_VTTXB  
MGT\_113\_AVCCAUX  
MGT\_113\_AVCCAUTX  
MGT\_113\_VTTXA  
MGT\_113\_AVCCAUXRXA  
MGT\_113\_VTRXA



MGT\_114\_VTRXB  
MGT\_114\_AVCCAUXRXB  
MGT\_114\_VTTXB  
MGT\_114\_AVCCAUX  
MGT\_114\_AVCCAUTX  
MGT\_114\_VTTXA  
MGT\_114\_AVCCAUXRXA  
MGT\_114\_VTRXA



SCH P/N 0381203  
ART P/N 0531499  
FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLATFOrm  
MGT POWER FILTER-2

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