ZONE	REV	REVISION DESCRIPTION	DATE	DRAWN
	01	INITIAL RELEASE PER DCN 0101983	01/31/05	CHUMPHREY
	02	REV SKIPPED PER DCN 0102258	04/15/05	CSH
	03	REV TO CURRENT PER DCN 0102258	04/15/05	CSH

SPECIFICATIONS:

PCB P/N: **1280334**
ML450 V4 SOURCE SYNC PCB

NOTE: Note that the following pages may not be printed on standard Xilinx format, or have standard Xilinx part numbering. This is due to Engineering, and software constraints. All of these pages are required in order to test and build the PCB.

XILINX®

TITLE
SCHEM, ML450 V4 SOURCE SYNC PCB

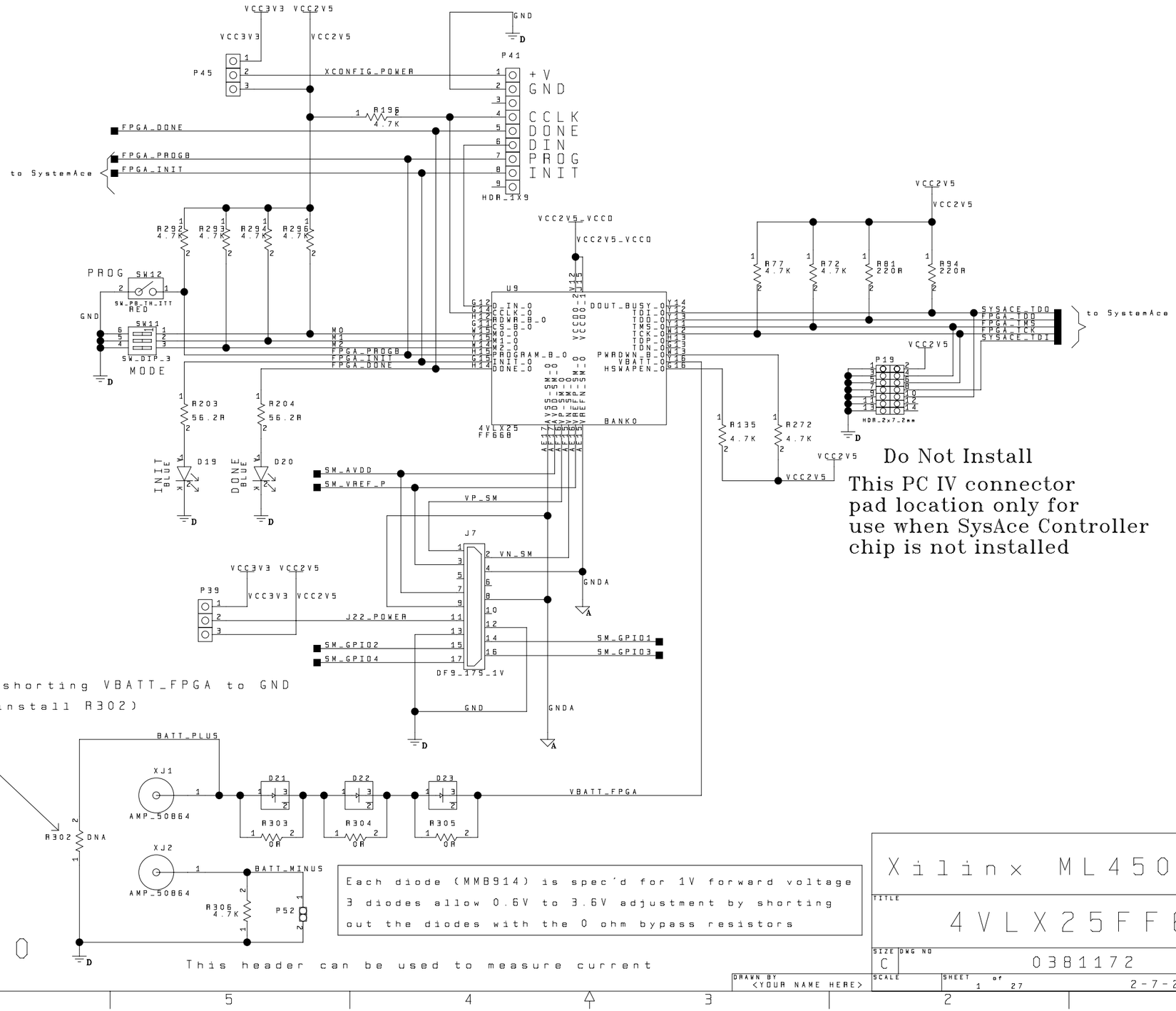
DRAWN BY *CHumphrey*	DATE *01/31/05*	
CHECKED BY	DATE	
ENG APPROVAL	DATE	
MFG APPROVAL	DATE	

TOLERANCES
.X .XX .XXX

Unless otherwise specified dimensions are in inches.

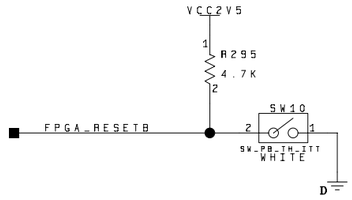
SIZE	DRAWING NUMBER	REV.
A	0381172	03
SCALE	SHEET 0 OF 27	

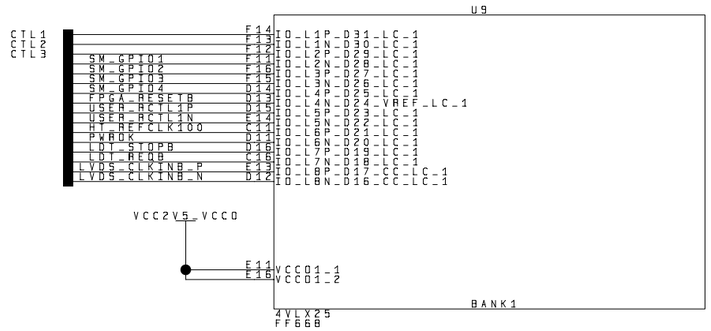
XCONFIG



Xilinx ML450 Rev3	
TITLE	4VLX25FF668
SIZE C / DWG NO	0381172 / REV 0
DRAWN BY <YOUR NAME HERE> / SCALE / SHEET 1 of 27	2-7-2005_13:35

XILINX®



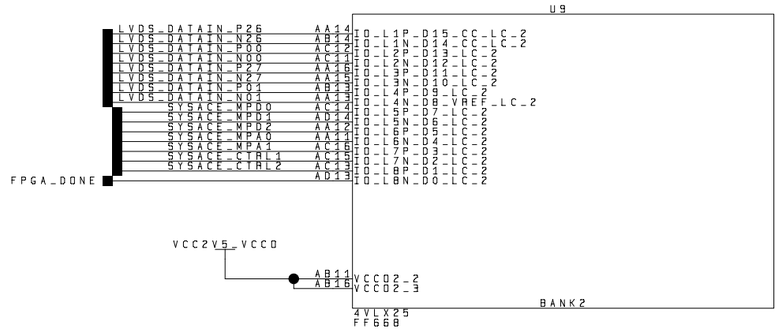


Bank 1 Mixed: HyperTransport, GPIO

Xilinx ML450 Rev3			
TITLE: 4VLX25FF668			
SIZE: C	DWG NO: 0381172	REV: 0	
DRAWN BY: <YOUR NAME HERE>	SCALE:	SHEET: 2 of 27	2-7-2005_13:35

XILINX®

LVDS Receive, SystemAce I/F



Bank 2

DRAWN BY <YOUR NAME HERE>			
SCALE	SHEET 3 of 27	2-7-2005_13:35	

Xilinx ML450 Rev3

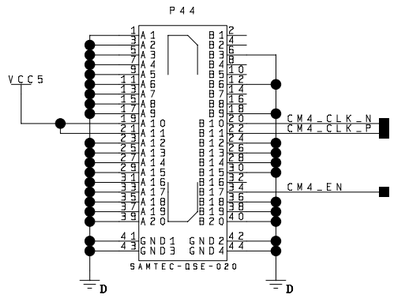
TITLE

4VLX25FF668

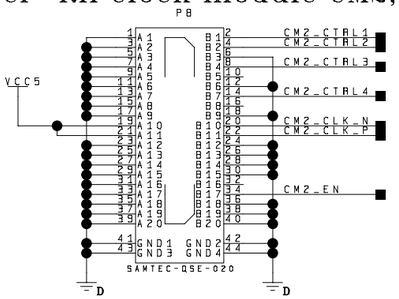
SIZE	DWG NO	REV
C	0381172	0

XILINX®

"Lower" RH clock module CM4, 3-pin

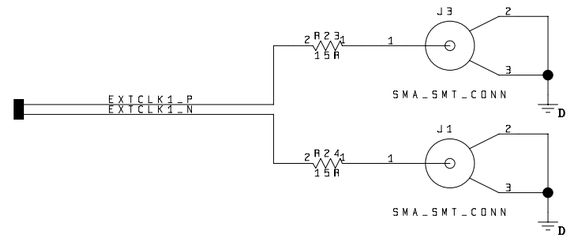


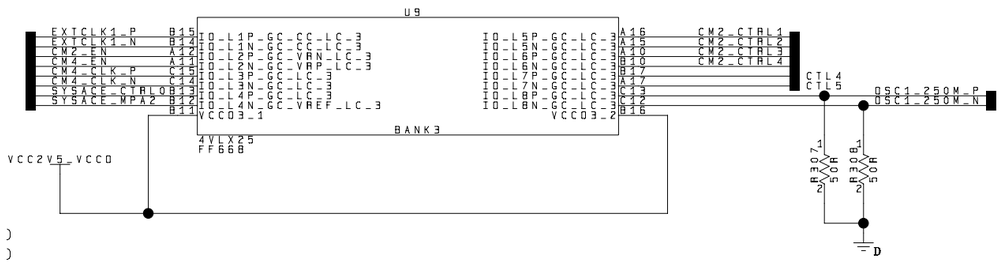
"Upper" RH clock module CM2, 7-pin



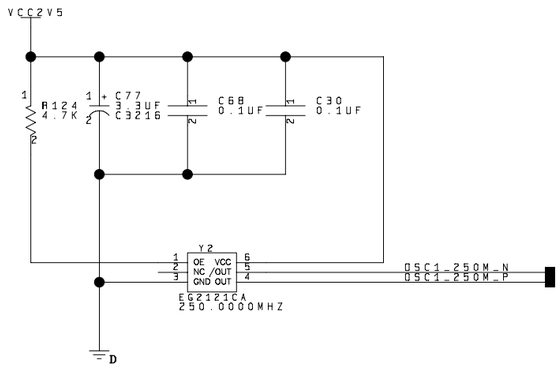
CM2_CLK_P goes to Bank9 pin M19 (Sheet10)
CM2_CLK_N goes to Bank9 pin N19 (Sheet10)

Input pair #1 within center column "GC" Global Clock inputs





250.0000MHz Epson EG2121CA-250.0000M-PHPAB

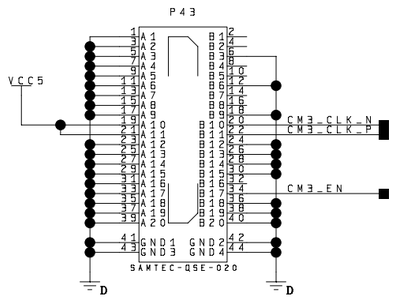


Bank3 Clock Interface

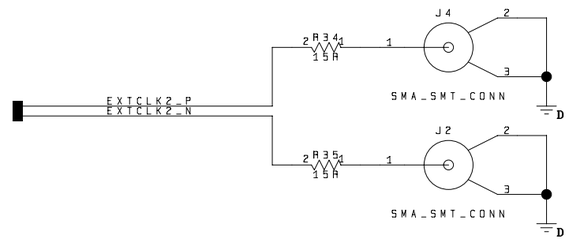
Xilinx ML450 Rev3			
TITLE: 4VLX25FF668			
SIZE: C	DWG NO: 0381172		REV: 0
DRAWN BY: <YOUR NAME HERE>	SCALE:	SHEET 4 of 27	2-7-2005_13:35

XILINX®

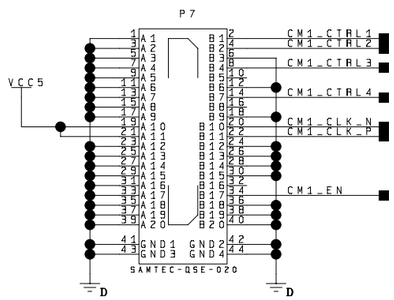
"Lower" LH clock module CM3, 3-pin



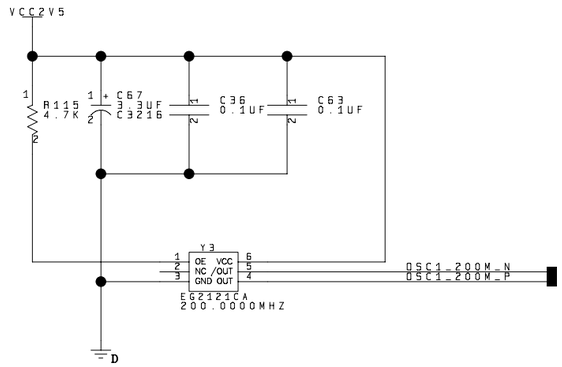
Input pair #2 within center column "GC" Global Clock inputs



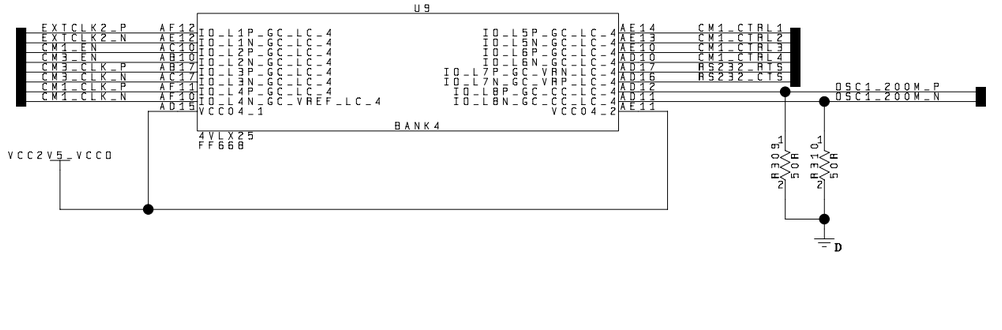
"Upper" LH clock module CM1, 7-pin



200.0000MHz Epson EG2121CA-200.0000M-PHPAB



Bank 4 Clock Interface

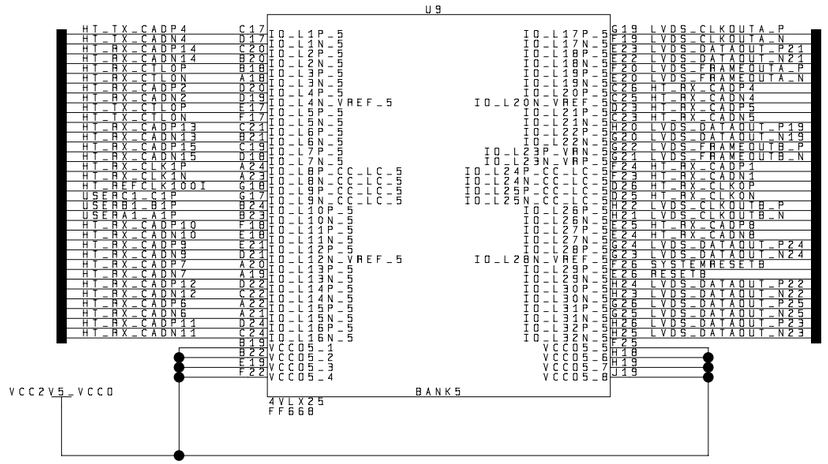


Xilinx ML450 Rev3			
TITLE: 4VLX25FF668			
SIZE: C	DWG NO: 0381172		REV: 0
DRAWN BY: <YOUR NAME HERE>	SCALE:	SHEET: 5 of 27	2-7-2005_13:35

XILINX®

HyperTransport RX I/F

Part of Transmit LVDS I/F

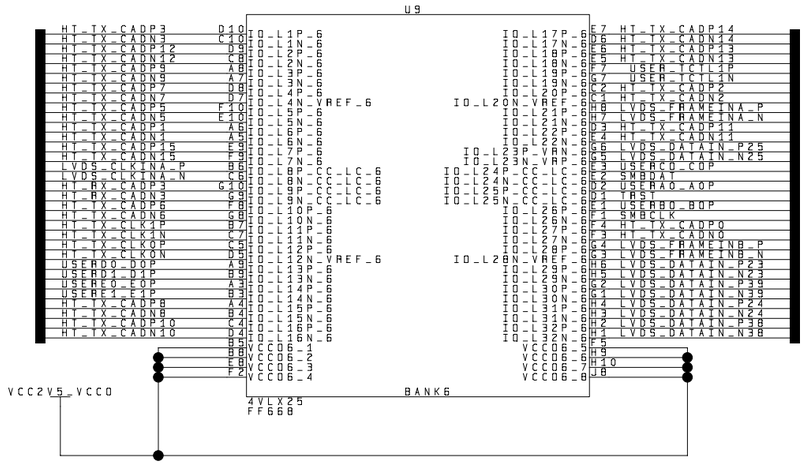


Bank 5

Xilinx ML450 Rev3			
TITLE: 4VLX25FF668			
SIZE: C	DWG NO: 0381172		REV: 0
DRAWN BY: <YOUR NAME HERE>	SCALE	SHEET 6 of 27	2-7-2005_13:35

XILINX®

HyperTransport TX I/F
Part of Receive LVDS I/F



Bank 6

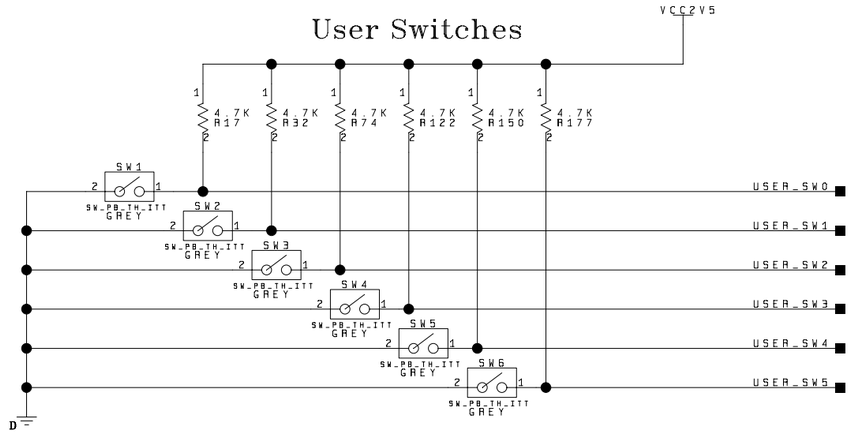
DRAWN BY <YOUR NAME HERE>			
SIZE C	DWG NO 0381172		REV 0
SCALE	SHEET 7 of 27	2-7-2005_13:35	

TITLE: 4VLX25FF668

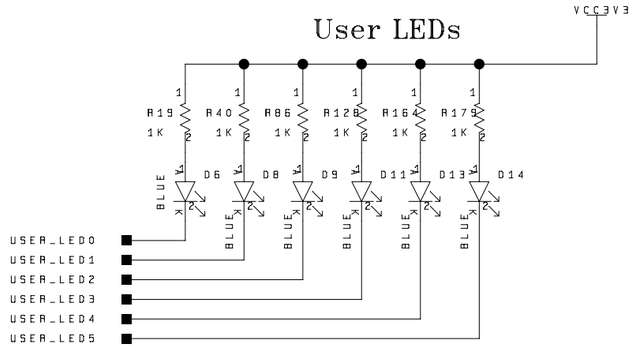
Xilinx ML450 Rev3

XILINX®

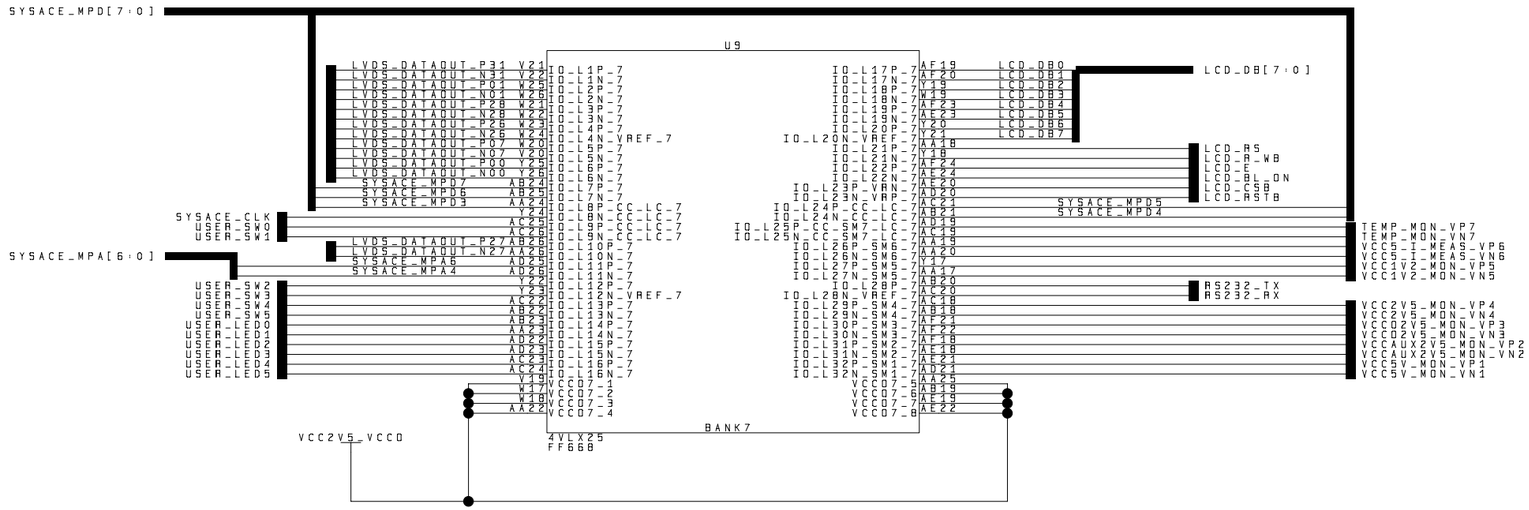
User Switches



User LEDs



U9 (Bank7)



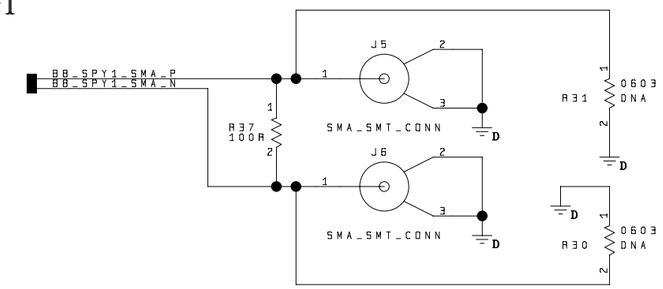
SystemAce, LCD, User Switch/LED, RS232 Tx and Rx

Bank 7

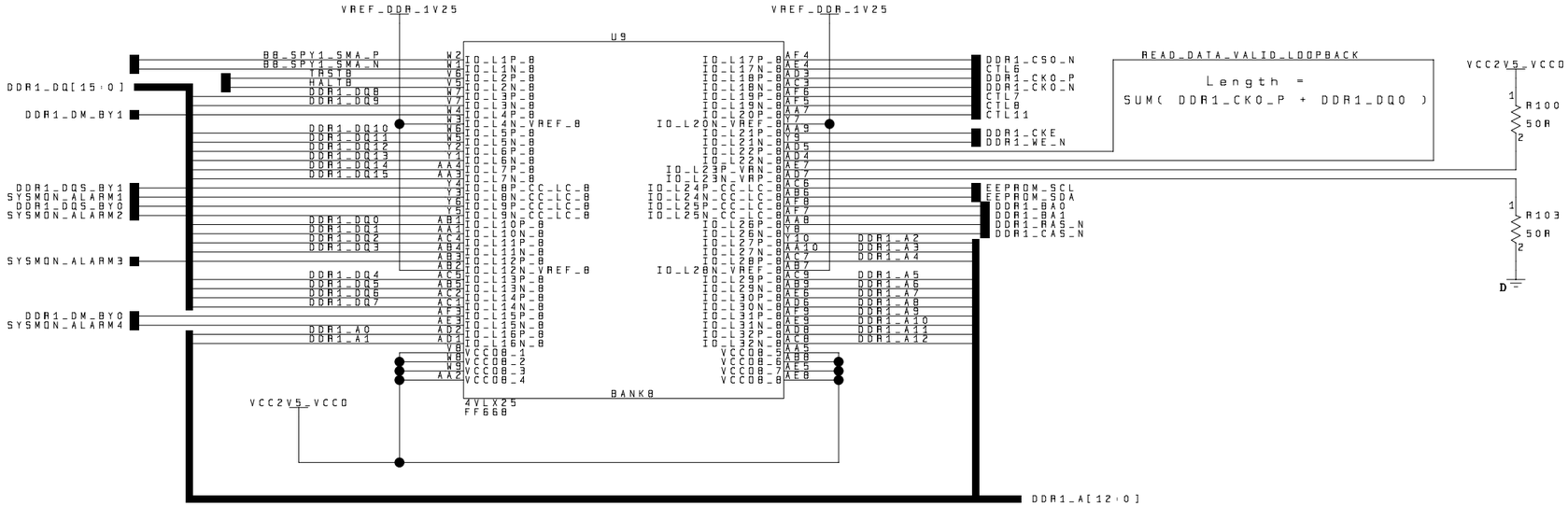
Xilinx ML450 Rev3			
TITLE: 4VLX25FF668			
SIZE: C	DWG NO: 0381172	REV: 0	
DRAWN BY: <YOUR NAME HERE>	SCALE	SHEET: 8 of 27	2-7-2005_13:35

Power Measurement "spy hole" pair #1

Output pair within Memory I/F Data



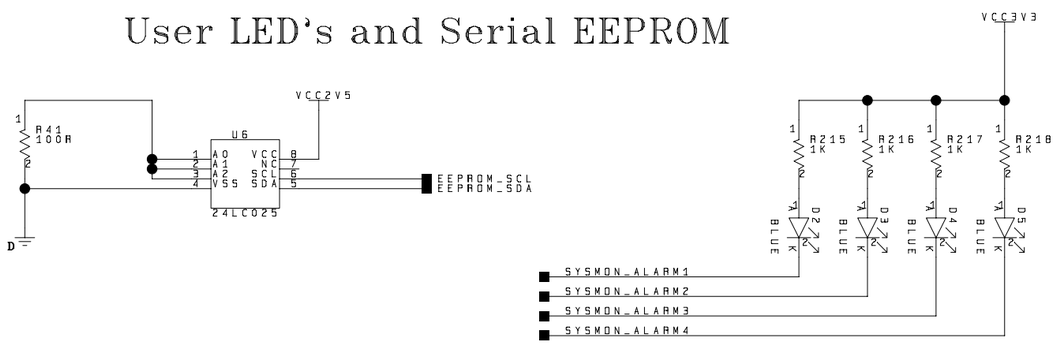
MEASURE – 1



to U3 single device Micron MT46V32M16FN–5B 8Meg x 16 DDR–1

DDR–I Memory Interface

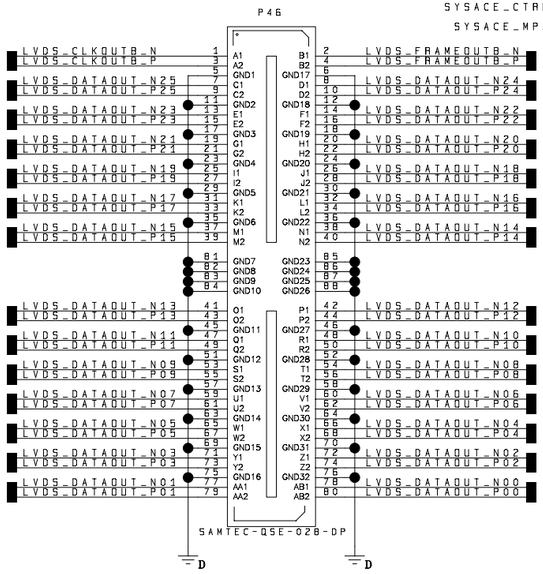
User LED's and Serial EEPROM



User LEDs

Bank 8

Xilinx ML450 Rev3			
TITLE: 4VLX25FF668			
SIZE: C	DWG NO: 0381172		REV: 0
DRAWN BY: <YOUR NAME HERE>	SCALE	SHEET 9 of 27	2-7-2005_13:35

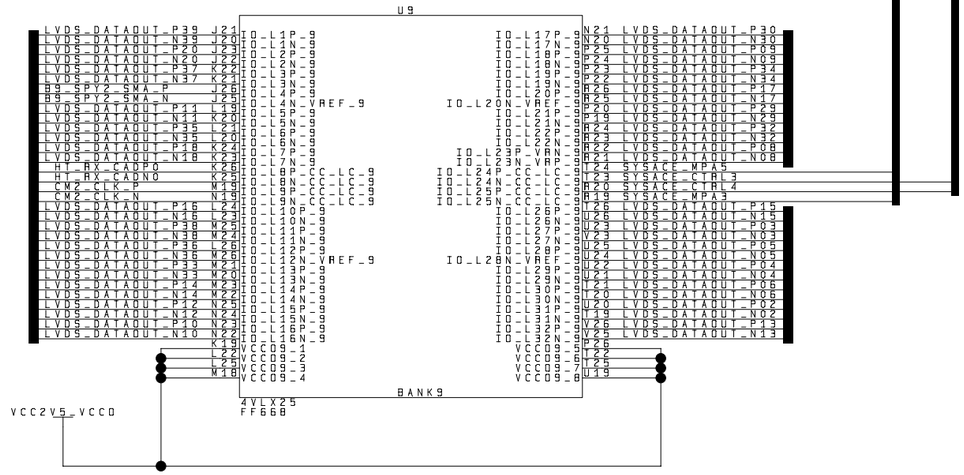


QSE-TX#1

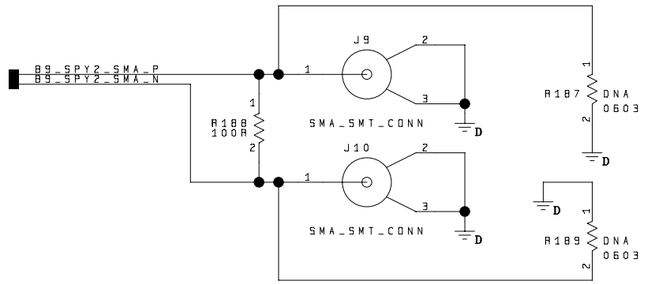
SYSACE_CTRL[4:0]

SYSACE_MPA[6:0]

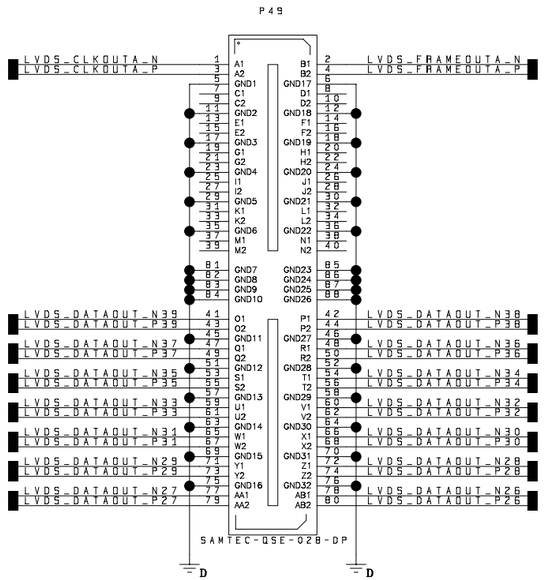
LVDS Transmit



Power Measurement "spy hole" pair #2



MEASURE - 2



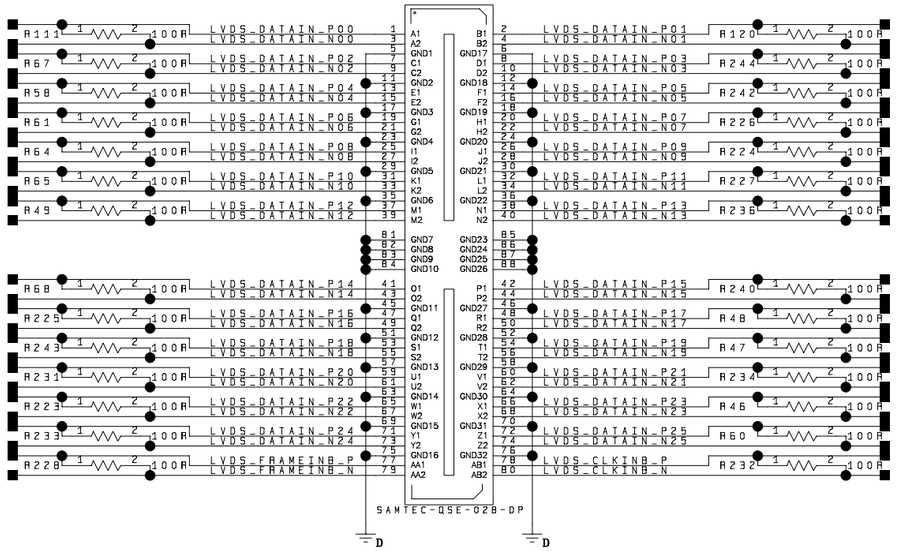
QSE-TX#2

Bank 9

40 Differential LVDS Transmit Pairs

Xilinx ML450 Rev3			
TITLE: 4VLX25FF668			
SIZE: C	DWG NO: 0381172		REV: 0
DRAWN BY: <YOUR NAME HERE>	SCALE:	SHEET: 10 of 27	2-7-2005_13:35

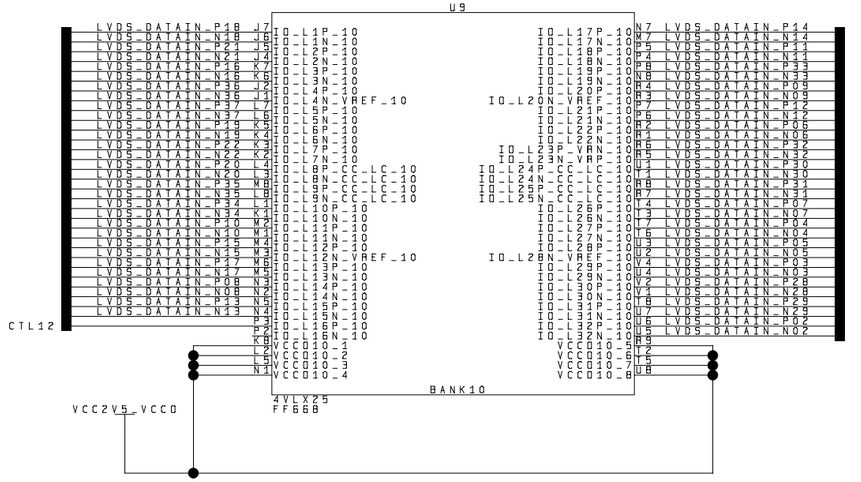
XILINX®



QSE−RX#1

Term R's are DNA (not installed)

QSE−RX#2



Bank10 40 Differential LVDS Receive Pairs

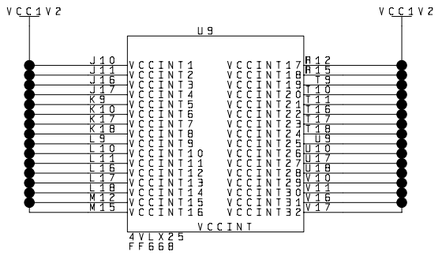
Xilinx ML450 Rev3

TITLE: 4VLX25FF668

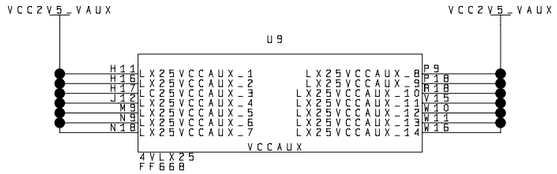
SIZE: C | DWG NO: 0381172 | REV: 0

DRAWN BY: <YOUR NAME HERE> | SCALE: | SHEET 11 of 27 | 2-7-2005_13:35

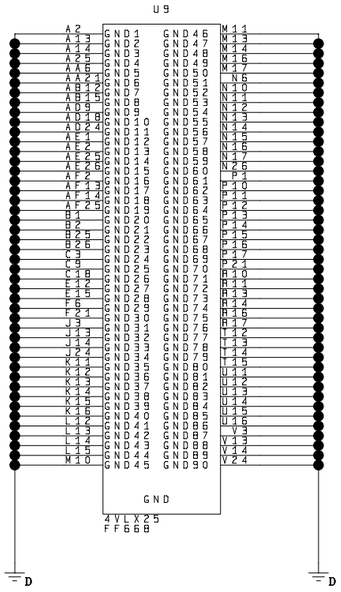
XILINX®



Bank VCCINT



Bank VCCAUX



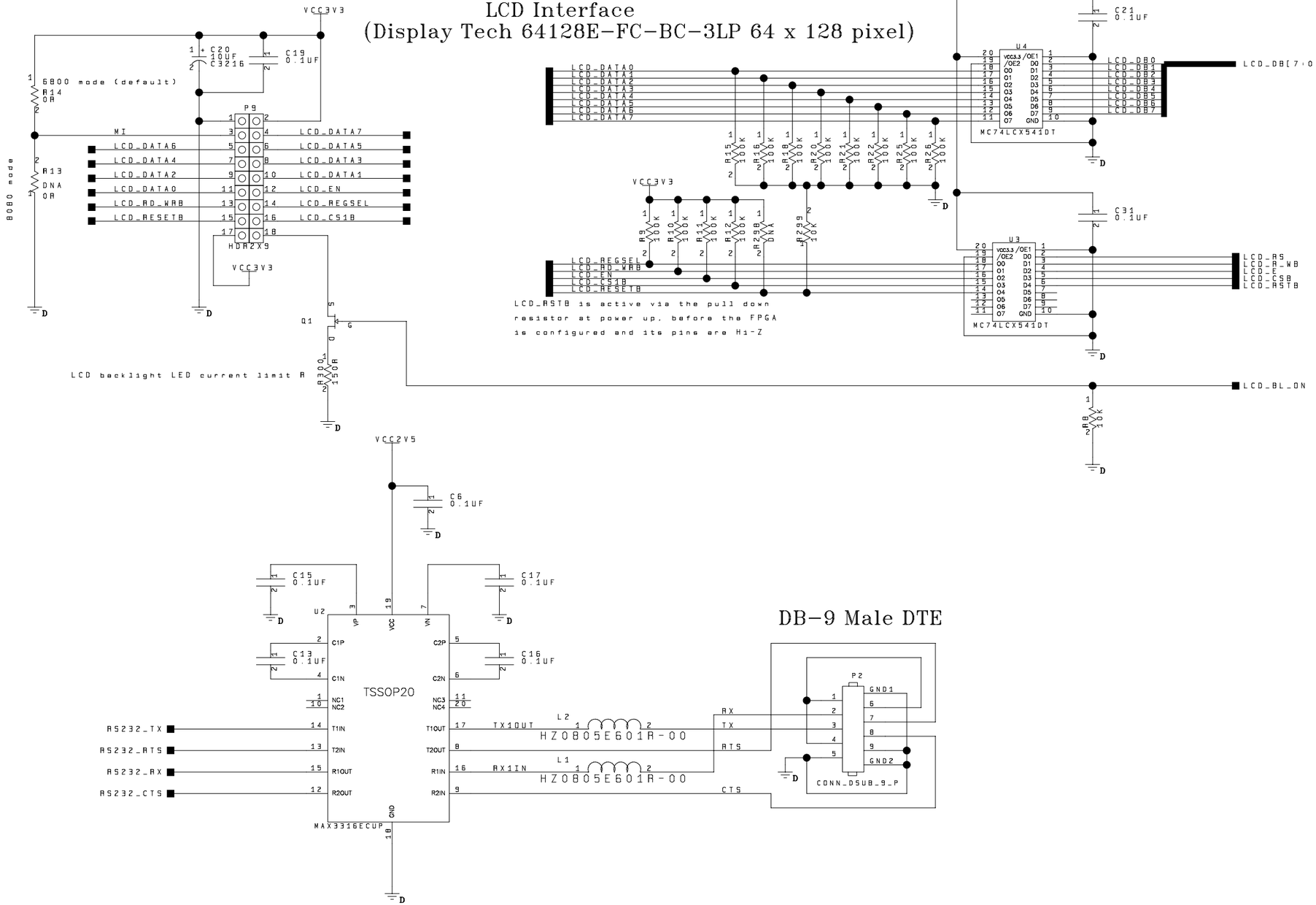
Bank GND

LX25 Power connections:

Vccaux=2.5V, Vccint=1.2V

Xilinx ML450 Rev3			
TITLE: 4VLX25FF668			
SIZE: C	DWG NO: 0381172		REV: 0
DRAWN BY: <YOUR NAME HERE>	SCALE:	SHEET: 12 of 27	2-7-2005_13:35

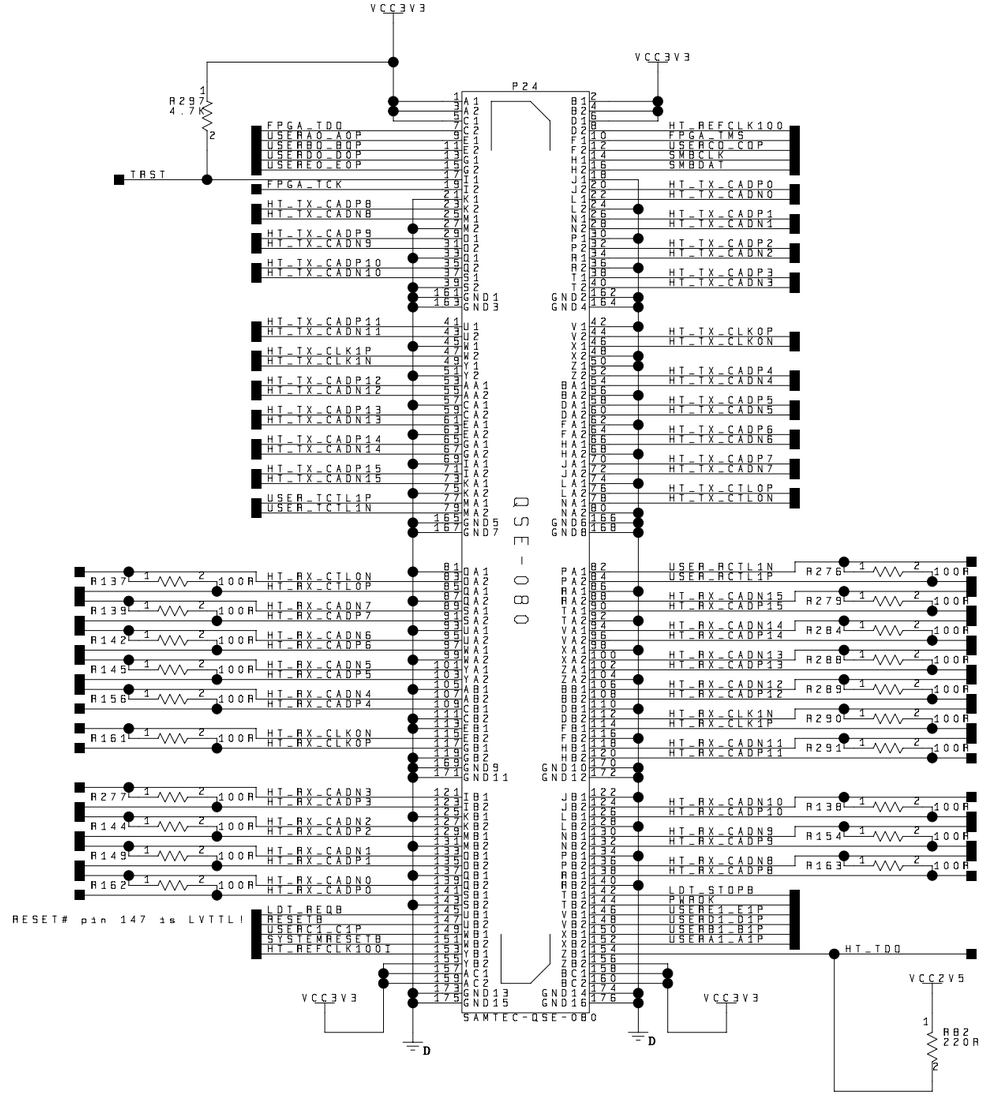
LCD Interface
(Display Tech 64128E-FC-BC-3LP 64 x 128 pixel)



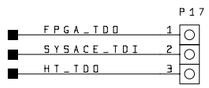
RS-232 Transceiver

Xilinx ML450 Rev3			
TITLE: 4VLX25FF668			
SIZE: C	DWG NO: 0381172		REV: 0
DRAWN BY: <YOUR NAME HERE>	SCALE:	SHEET 13 of 27	2-7-2005_13:35

HyperTransport Connector



JTAG Chain Jumper



1 – 2 => HyperTransport Conn. P23 Bypassed (not in chain)

3 – 2 => HyperTransport Conn. P23 In Chain

Xilinx ML450 Rev3		
TITLE: 4VLX25FF668		
SIZE: C	DWG NO: 0381172	REV: 0
DRAWN BY: <YOUR NAME HERE>	SCALE	SHEET 14 of 27
		2-7-2005_13:35

XILINX®

SYSACE_CTRL[4:0]

4 : MPBRDY OUT
3 : MPIRQ OUT
2 : MPCE IN
1 : MPWE IN
0 : MPOE IN

SYSTEMACE
TQFP144
(DIE DOWN)

SYSTEMACE
TQFP144-10X70

ACEFLASH
MOLEX55358

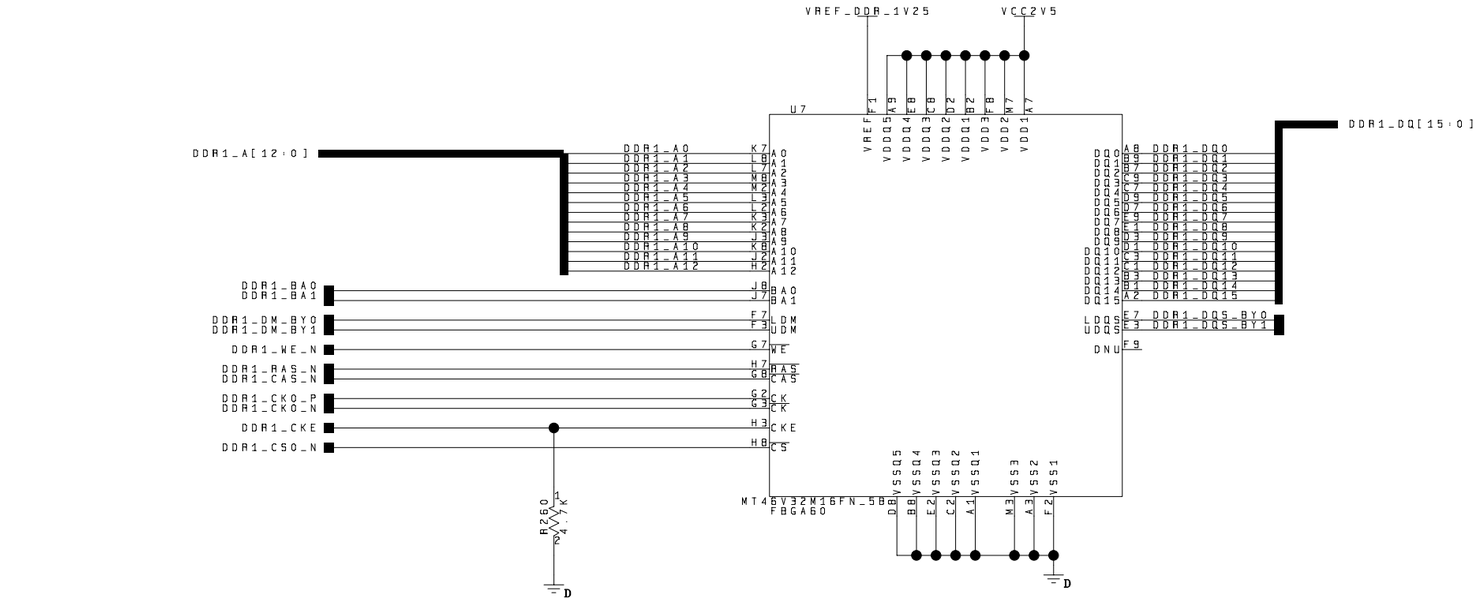
Place these resistors as close to System ACE as possible

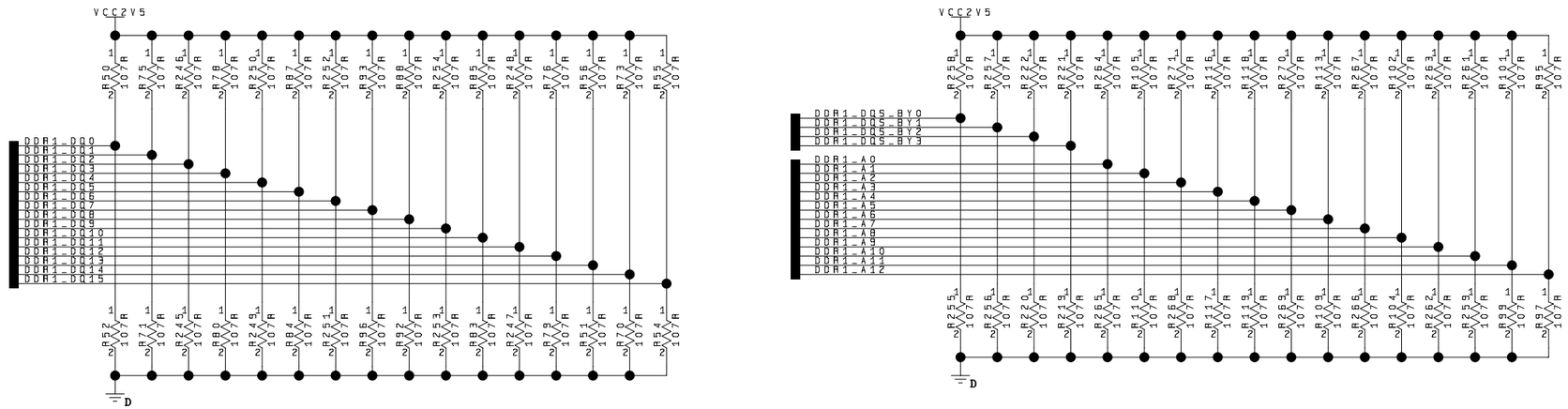
Silkscreen "System ACE" "Status LED"

Silkscreen "System ACE" "Error LED"

TITLE	Xilinx ML450 Rev3
	4VLX25FF668
SIZE	C
DWG NO	0381172
REV	0
DRAWN BY	<YOUR NAME HERE>
SCALE	
SHEET	15 of 27
	2-7-2005_13:35

XILINX®





107/107 R tree gives approx. 54 ohms impedance

DDR-1 Memory

Xilinx ML450 Rev3

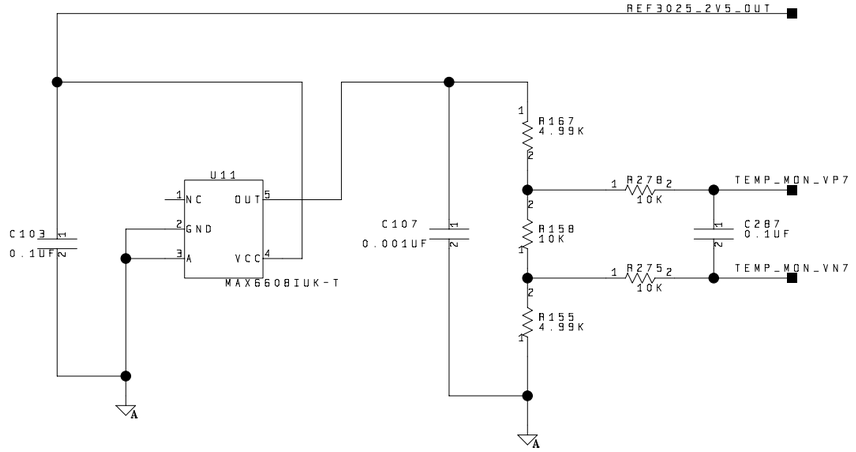
TITLE: 4VLX25FF668

SIZE	DWG NO	REV
C	0381172	0

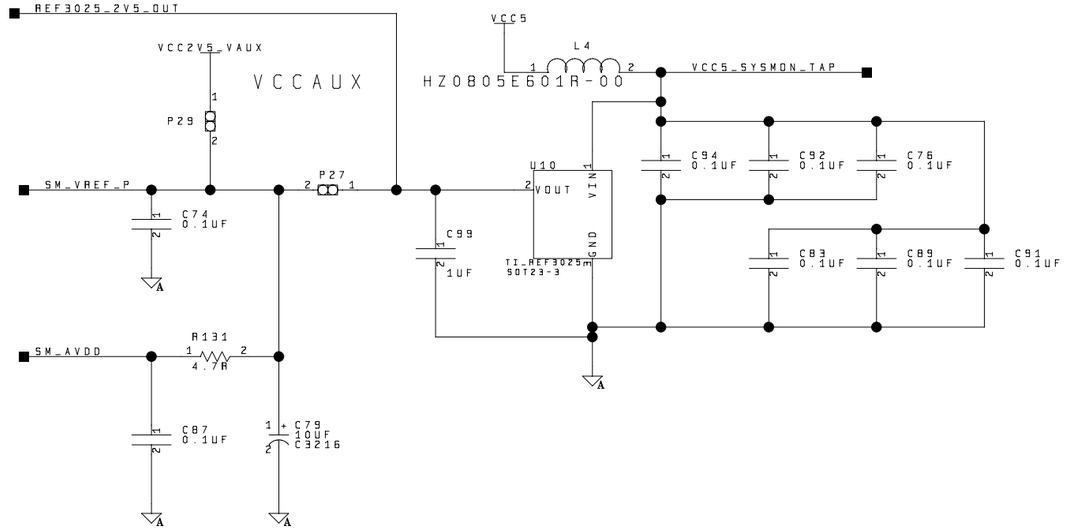
DRAWN BY	SCALE	SHEET	
<YOUR NAME HERE>		16 of 27	2-7-2005_13:35

XILINX®

Temperature Monitor

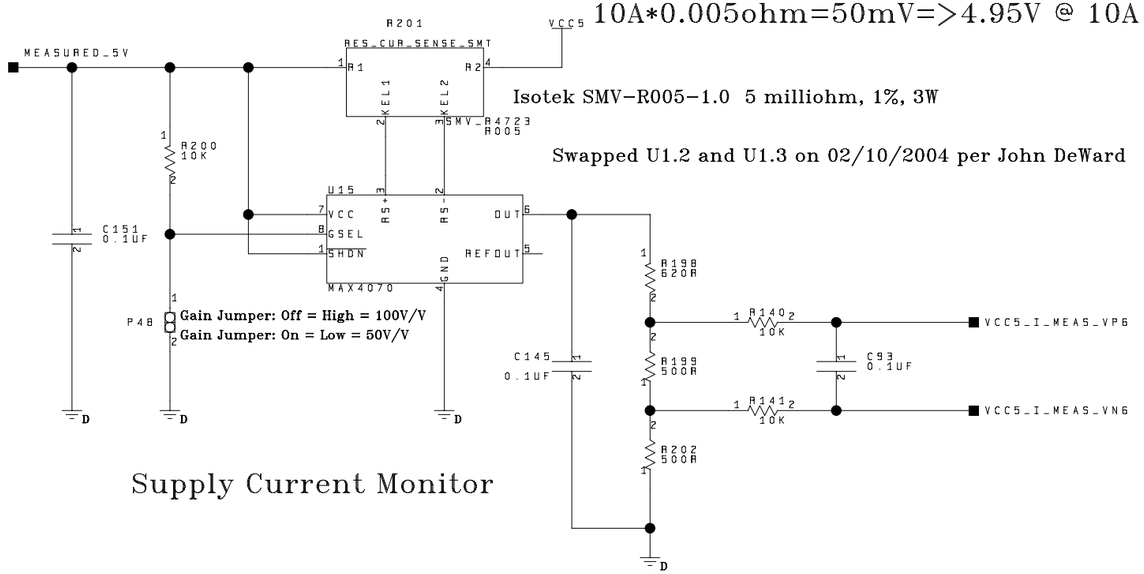


Vref TI REF3025 2.5V Reference



SMV internal connections: 1 & 3, 2 & 4

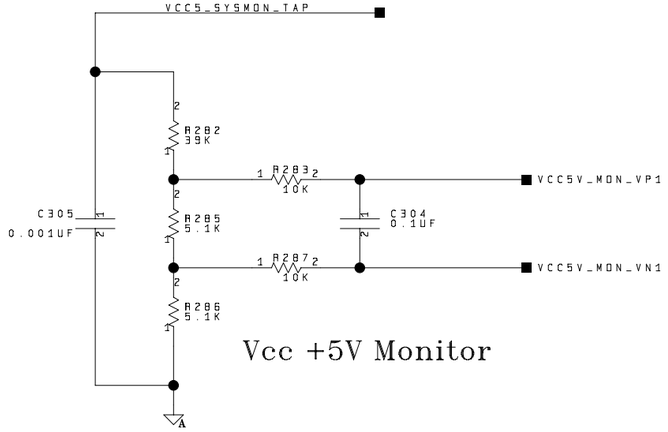
10A*0.005ohm=50mV=>4.95V @ 10A



Isotek SMV-R005-1.0 5 milliohm, 1%, 3W

Swapped U1.2 and U1.3 on 02/10/2004 per John DeWard

Supply Current Monitor



Vcc +5V Monitor

Xilinx ML450 Rev3

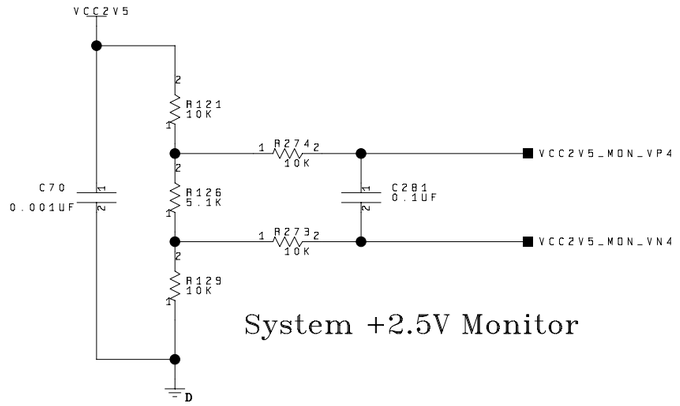
TITLE: 4VLX25FF668

SIZE: C | DWG NO: 0381172 | REV: 0

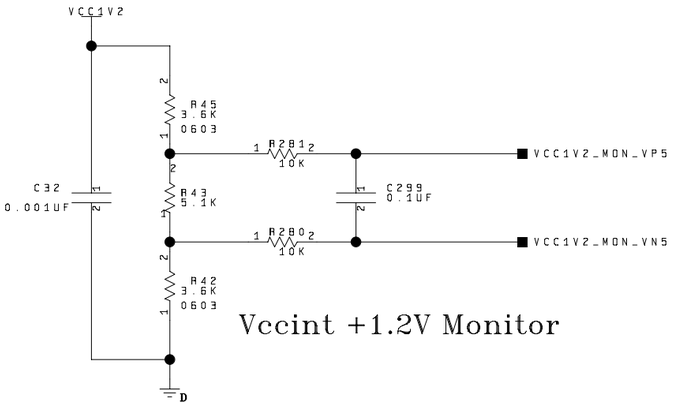
DRAWN BY: <YOUR NAME HERE> | SCALE: | SHEET: 17 of 27 | 2-7-2005_13:35

Analog Conditioning Page 1 of 2

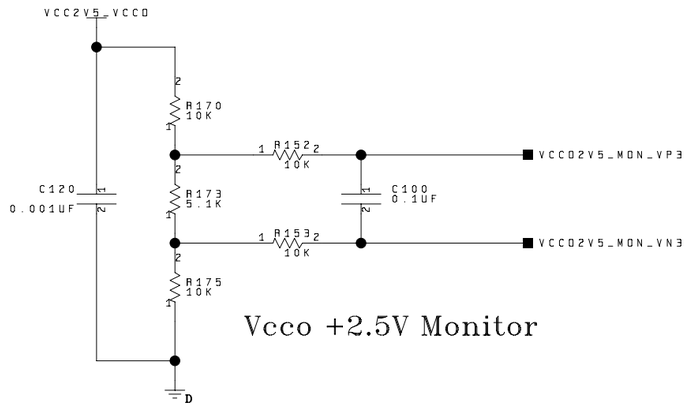
XILINX®



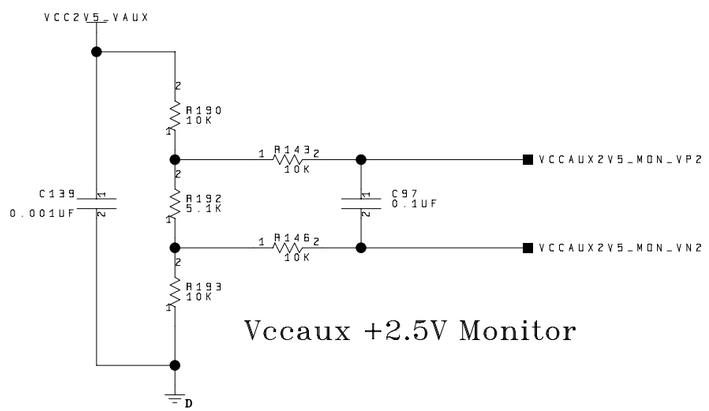
System +2.5V Monitor



Vccint +1.2V Monitor



Vcco +2.5V Monitor

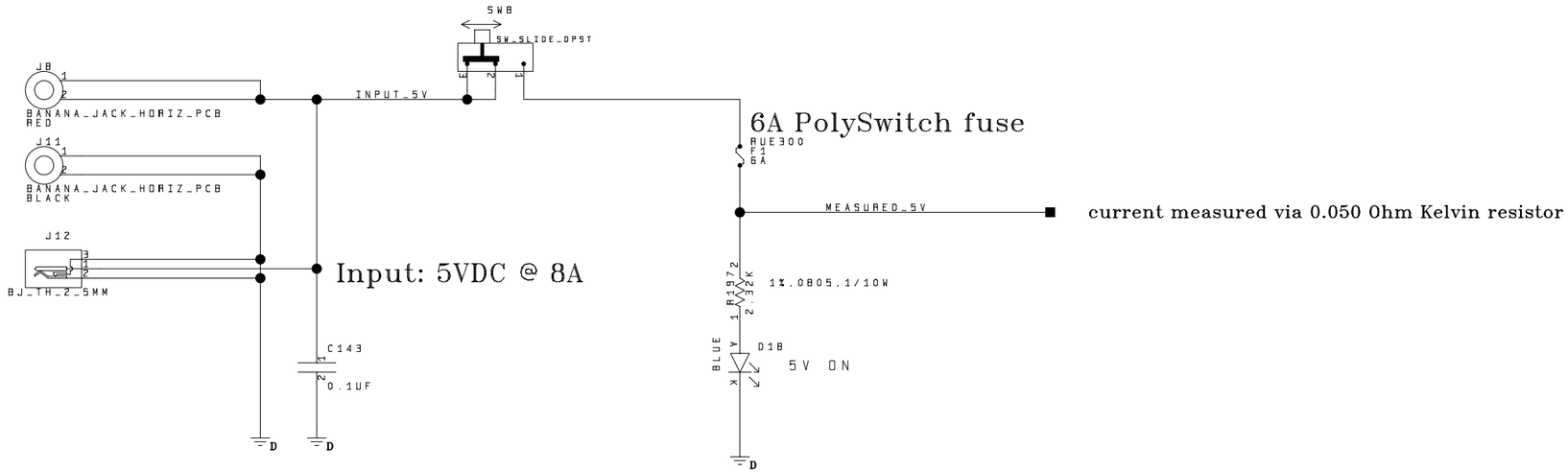


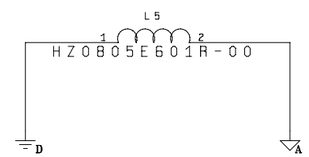
Vccaux +2.5V Monitor

Analog Conditioning Page 2 of 2

Xilinx ML450 Rev3			
TITLE: 4VLX25FF668			
SIZE: C	DWG NO: 0381172		REV: 0
DRAWN BY: <YOUR NAME HERE>	SCALE:	SHEET: 18 of 27	2-7-2005_13:35

XILINX®





Digital GND to Analog GND connection

Power Page 1 of 3: External Power Supply Input, 5VDC @ 8A

Xilinx ML450 Rev3

TITLE

4VLX25FF668

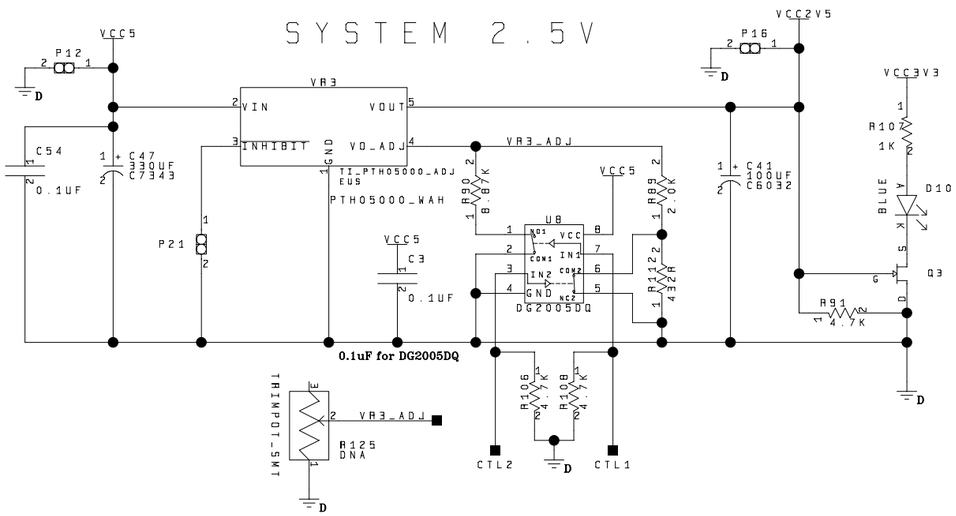
SIZE C | DWG NO 0381172 | REV 0

DRAWN BY <YOUR NAME HERE> | SCALE | SHEET 19 of 27 | 2-7-2005_13:35

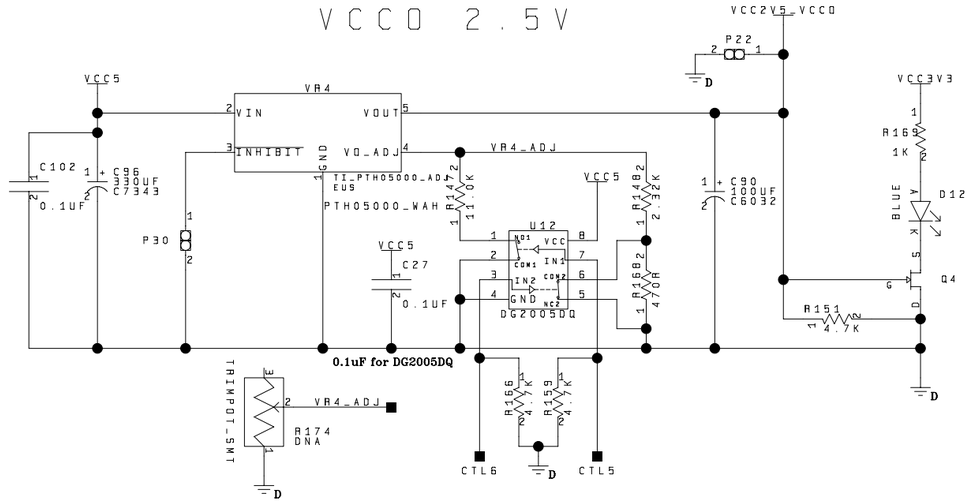
XILINX®

Set for 2.6V for Micron memories
for DDR400 Operation

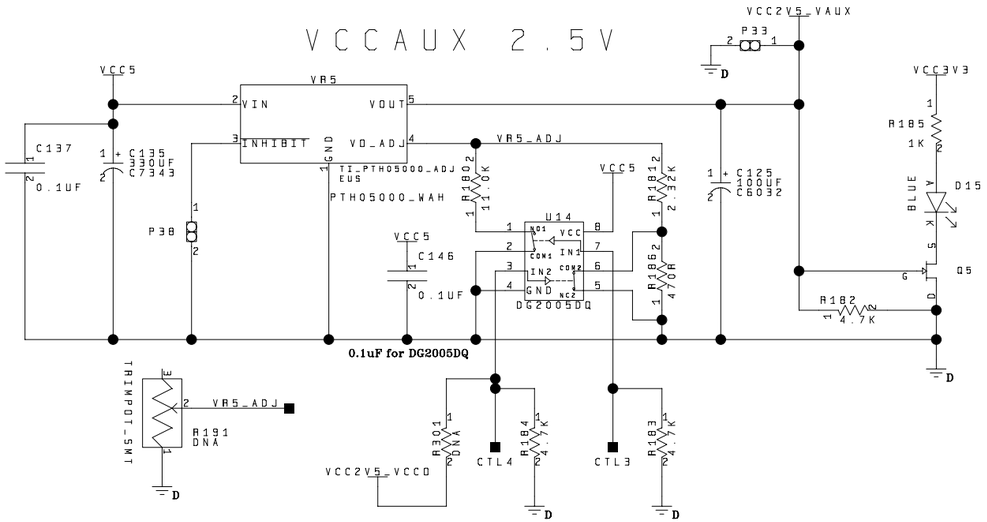
SYSTEM 2.5V



VCCO 2.5V



VCCAUX 2.5V



Install	Do Not Install	Vccint at power on
R301	R184	-5% = 2.375V
R184	R301	nominal 2.50V

open /INHIBIT pin 3 = power module output enabled

Rset = 10K x [0.891V / (Vout - 0.9V)] - 3.24K

Vout = [8910 / (Rset+3.24K)] + 0.9V

Rset = 2.0K ohm 1% for 2.6V

Rset = 2.32K ohm 1% for 2.5V

Power Page 2 of 3: TI PTH05000-W-AH 2.5V System, Vccaux, Vcco

Xilinx ML450 Rev3

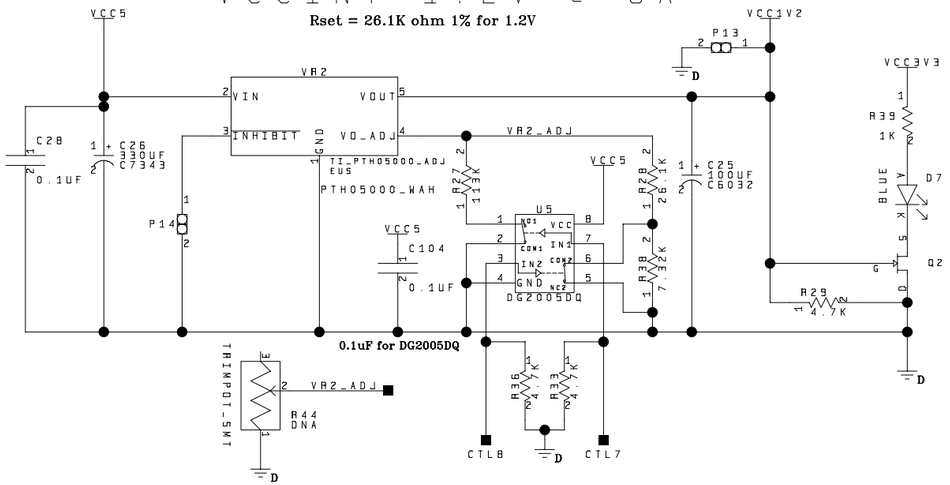
TITLE: 4VLX25FF668

SIZE: C | DWG NO: 0381172 | REV: 0

DRAWN BY: <YOUR NAME HERE> | SCALE: | SHEET 20 of 27 | 2-7-2005_13:53

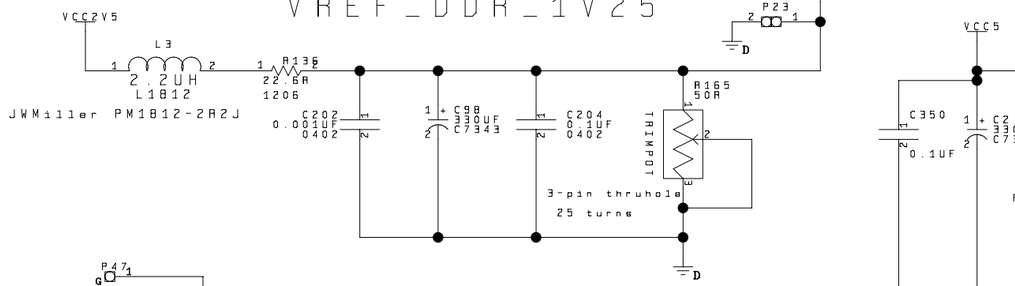
VCCINT 1.2V @ 6A

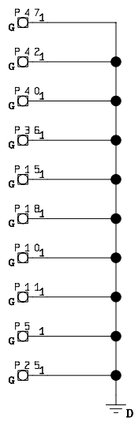
Rset = 26.1K ohm 1% for 1.2V



Set for 1.3V for Micron memories for DDR400 Operation

VREF_DDR_1V25

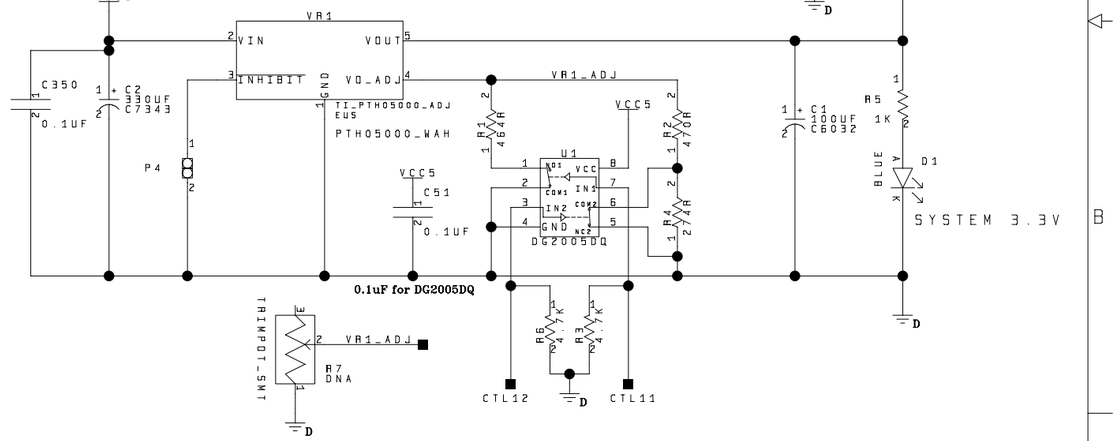




Digital GND testpoints

SYSTEM 3.3V

Rset = 475 ohm 1% for 3.3V

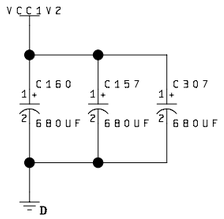


Power Page 3 of 3: TI PTH05000-W-AH 3.3V System, Vcco, and 1.2V Vccint

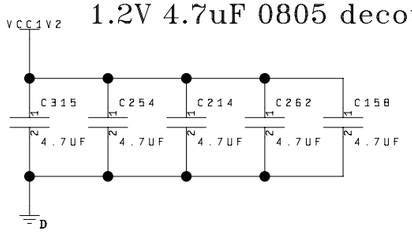
Xilinx ML450 Rev3		
TITLE: 4VLX25FF668		
SIZE: C	DWG NO: 0381172	REV: 0
DRAWN BY: <YOUR NAME HERE>	SCALE	SHEET: 21 of 27
		2-7-2005_13:53

XILINX®

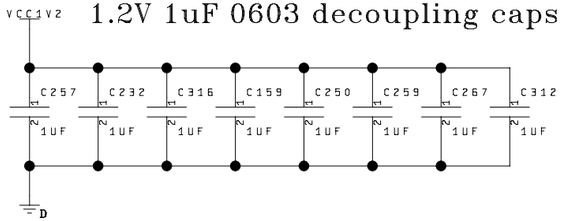
1.2V 680uF EIA "E" decoupling caps X 3



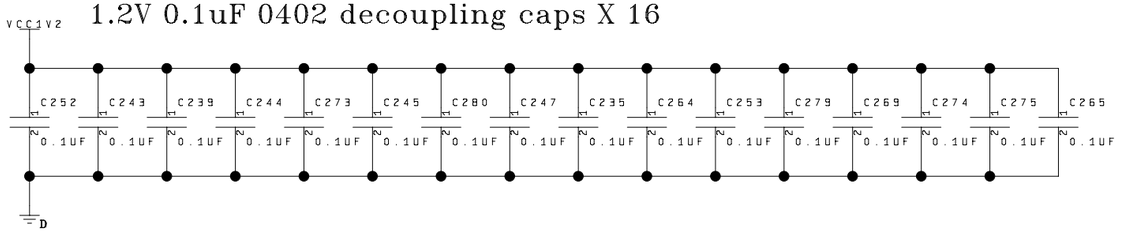
1.2V 4.7uF 0805 decoupling caps X 5



1.2V 1uF 0603 decoupling caps X 8



1.2V 0.1uF 0402 decoupling caps X 16

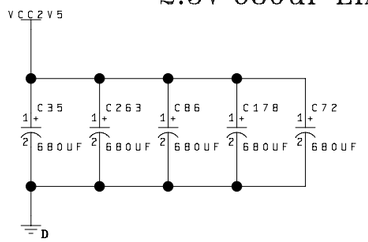


decoupling caps sheet 1 of 5: Vccint VCC1V2

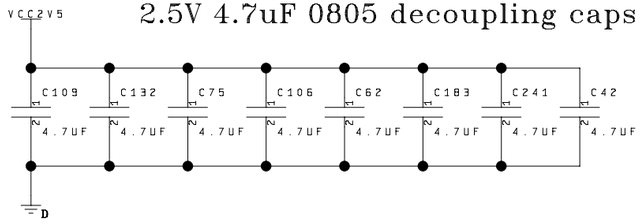
Xilinx ML450 Rev3			
TITLE: 4VLX25FF668			
SIZE: C	DWG NO: 0381172		REV: 0
DRAWN BY: <YOUR NAME HERE>	SCALE	SHEET 22 of 27	2-7-2005_13:35

XILINX®

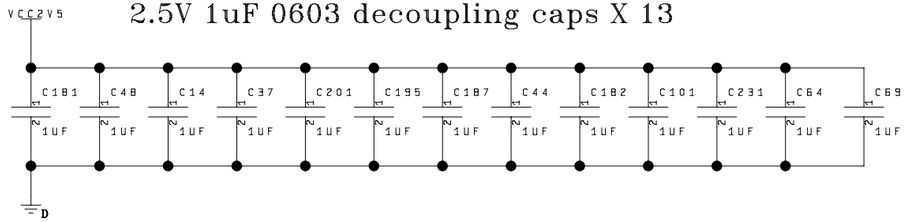
2.5V 680uF EIA "E" decoupling caps X 5



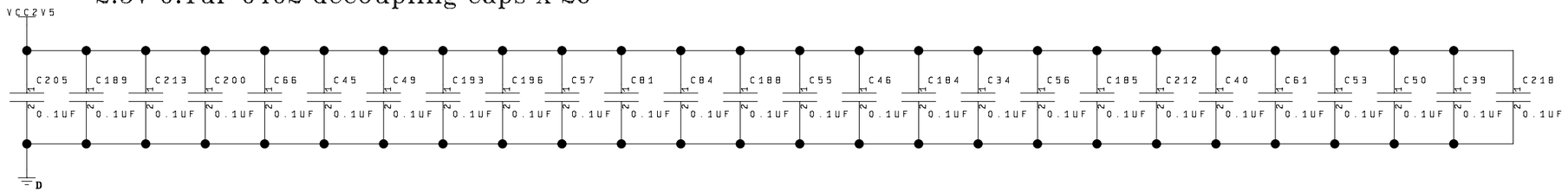
2.5V 4.7uF 0805 decoupling caps X 8



2.5V 1uF 0603 decoupling caps X 13



2.5V 0.1uF 0402 decoupling caps X 26



decoupling caps sheet 2 of 5: Vcc 2.5V System VCC2V5

DRAWN BY <YOUR NAME HERE>	SCALE	SHEET 23 of 27	2-7-2005_13:35

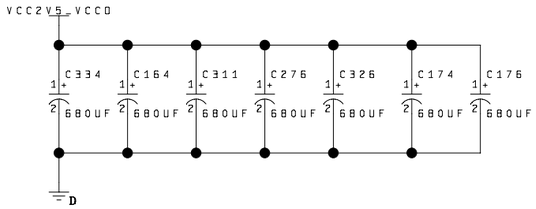
Xilinx ML450 Rev3

TITLE: 4VLX25FF668

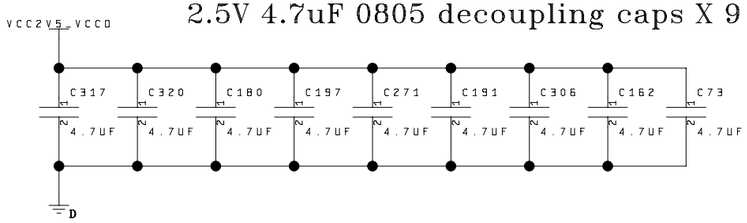
SIZE	DWG NO	REV
C	0381172	0

XILINX®

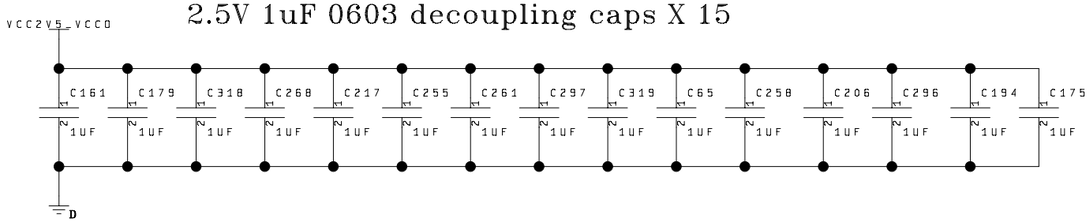
2.5V 680uF EIA "E" decoupling caps X 6



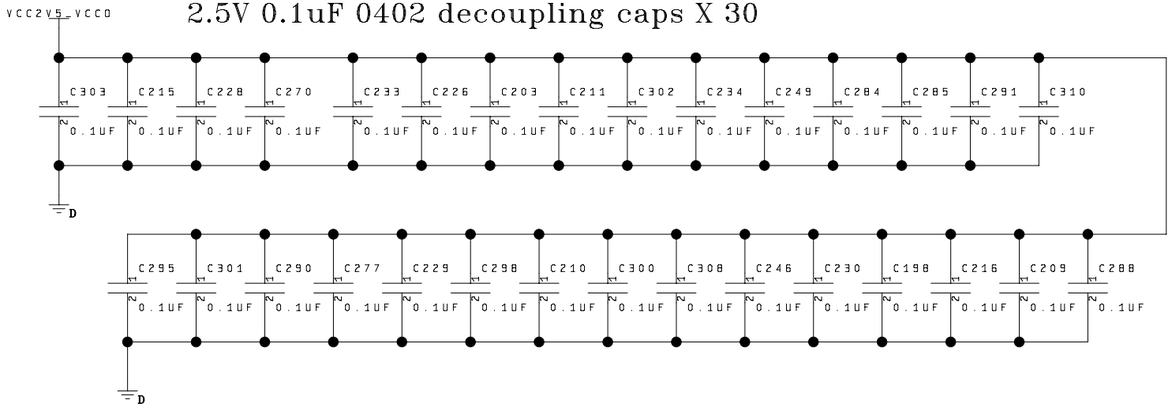
2.5V 4.7uF 0805 decoupling caps X 9



2.5V 1uF 0603 decoupling caps X 15



2.5V 0.1uF 0402 decoupling caps X 30

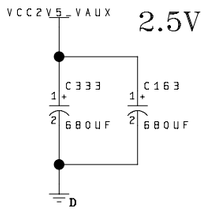


decoupling caps sheet 3 of 5: VCC 2.5V Vcco VCC2V5_VCCO

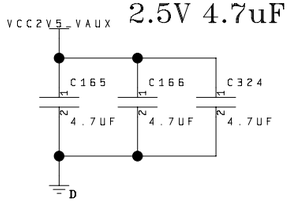
	Xilinx ML450 Rev3
TITLE	4VLX25FF668
SIZE / DWG NO	C / 0381172
REV	0
DRAWN BY	<YOUR NAME HERE>
SCALE	
SHEET	24 of 27
	2-7-2005_13:35

XILINX®

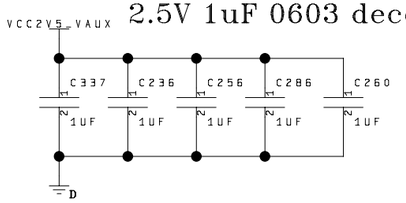
2.5V 680uF EIA "E" decoupling caps X 2



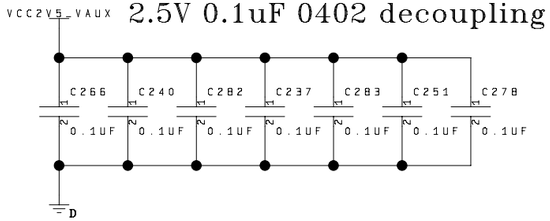
2.5V 4.7uF 0805 decoupling caps X 3



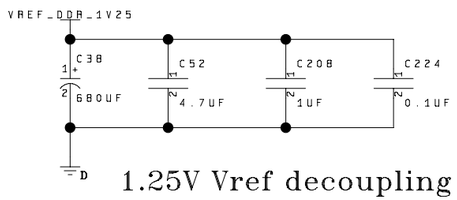
2.5V 1uF 0603 decoupling caps X 5



2.5V 0.1uF 0402 decoupling caps X 7

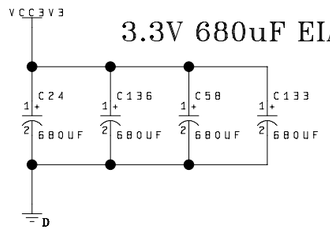


VREF_DDR_1V25

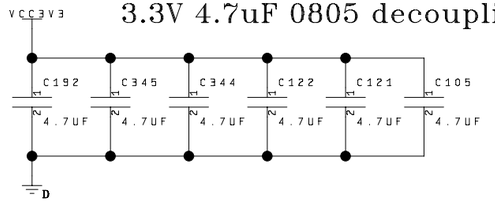


1.25V Vref decoupling caps x1 : 680uF EIA "E"; 4.7uF 0805; 1uF 0603; 0.1uF 0402

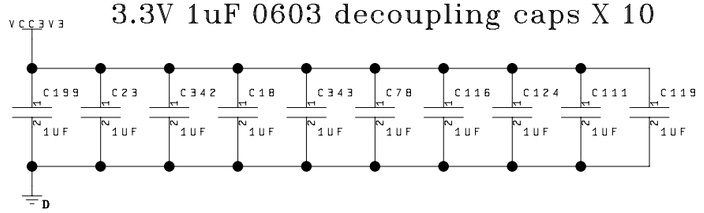
3.3V 680uF EIA "E" decoupling caps X 4



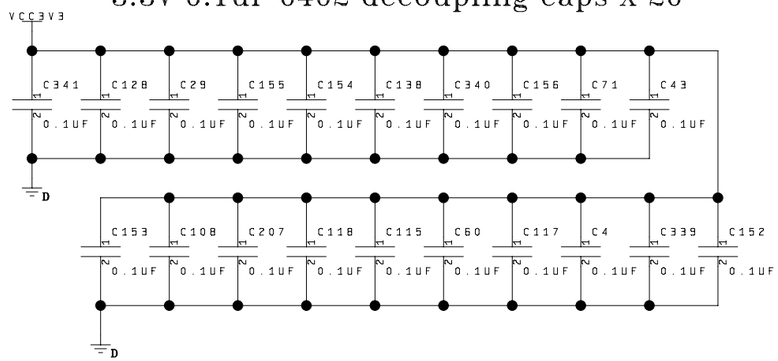
3.3V 4.7uF 0805 decoupling caps X 6



3.3V 1uF 0603 decoupling caps X 10



3.3V 0.1uF 0402 decoupling caps X 20



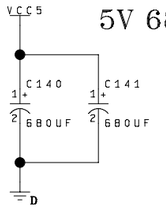
decoupling caps sheet 4 of 5: Vccaux VCC2V5_VAUX

Vcc 3.3V System VCC3V3

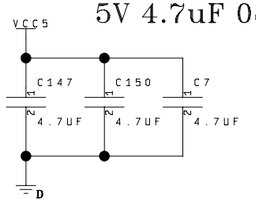
VRef 1.25V VREF_DDR_1V25

Xilinx ML450 Rev3			
TITLE: 4VLX25FF668			
SIZE: C	DWG NO: 0381172	REV: 0	
DRAWN BY: <YOUR NAME HERE>	SCALE	SHEET: 25 of 27	2-7-2005_13:35

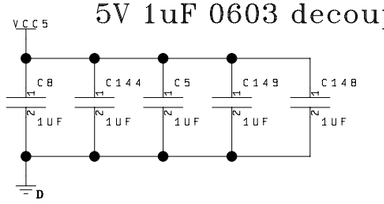
5V 680uF EIA "E" decoupling caps X 2



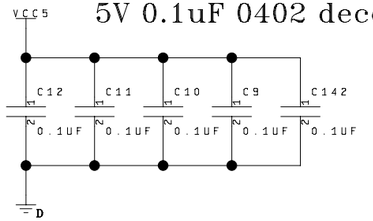
5V 4.7uF 0805 decoupling caps X 3



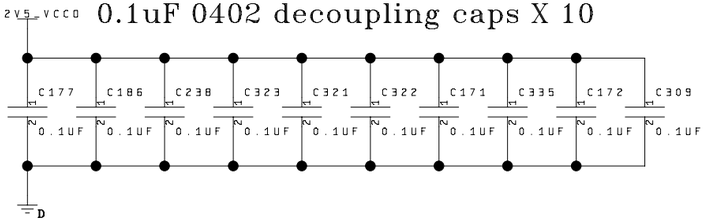
5V 1uF 0603 decoupling caps X 5



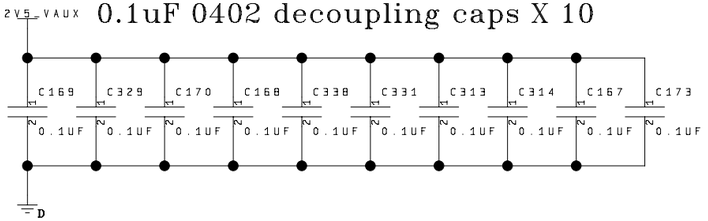
5V 0.1uF 0402 decoupling caps X 5



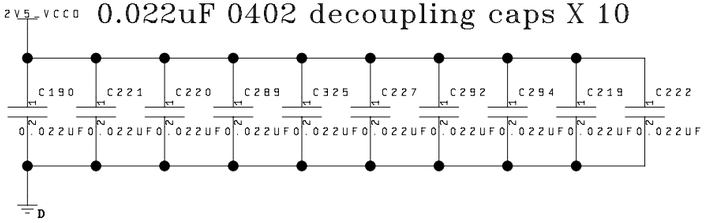
VCC2V5_VCCO 0.1uF 0402 decoupling caps X 10



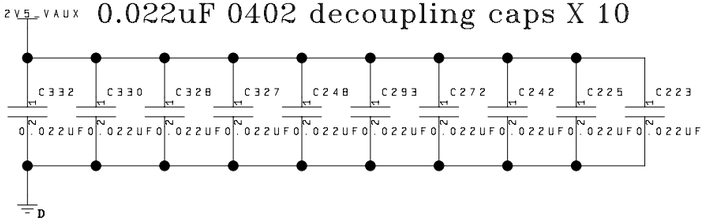
VCC2V5_VAUX 0.1uF 0402 decoupling caps X 10



VCC2V5_VCCO 0.022uF 0402 decoupling caps X 10



VCC2V5_VAUX 0.022uF 0402 decoupling caps X 10



decoupling caps sheet 5 of 5: VCC5 output of current sense resistor

Xilinx ML450 Rev3

TITLE: 4VLX25FF668

SIZE: C | DWG NO: 0381172 | REV: 0

DRAWN BY: <YOUR NAME HERE> | SCALE: | SHEET 26 of 27 | 2-7-2005_13:35

Page#	Description
1	LX25 Bank0 (Vcco=2.5V): XCONFIG P17 and Mezzanine Bd. Connector J22
2	LX25 Bank1 (Vcco=2.5V): Reset Sw, HT & mixed I/O
3	LX25 Bank2 (Vcco=2.5V): LVDS Transmit & Receive Clock & Frame signals
4	LX25 Bank3 (Vcco=2.5V): Clock Inputs - 2 X Clk Module, SMA pr.#1, Epson 250MHz osc.
5	LX25 Bank4 (Vcco=2.5V): Clock Inputs - 2 X Clk Module, SMA pr.#2, Epson 200MHz osc.
6	LX25 Bank5 (Vcco=2.5V): part of LVDS Transmit I/F & HT Receive I/F
7	LX25 Bank6 (Vcco=2.5V): part of LVDS Receive I/F & HT Transmit I/F
8	LX25 Bank7 (Vcco=2.5V): User Sw./LEDs, SystemAce I/F
9	LX25 Bank8 (Vcco=2.5V): DDR1 Memory I/F, "Spy Hole #1" SMA, Serial EEPROM and User LED's
10	LX25 Bank9 (Vcco=2.5V): part of LVDS Transmit I/F with 2 X Samtec Conn.
11	LX25 Bank10 (Vcco=2.5V): part of LVDS Receive I/F with 2 X Samtec Conn.
12	LX25 Power connections: Vccaux=2.5V, Vccint=1.2V
13	LCD (3.3V, 64x128pixel) I/F, MAX3316 RS232 I/F
14	Hypertransport Connector Samtec QSE-080 Series
15	System Ace Controller U9 (3.3V/2.5V), Compact Flash socket, JTAG & Parallel IV Cable Connectors
16	DDR1 Memory Micron MT46V32M16FN-5B BGA60, 16Meg x 16 with term. resistor array
17	Analog Conditioning, Pg.1 of 2: U4 VREF 2.5V, U1 Current Monitor Sense Amp, U8 Temp. Monitor
18	Analog Conditioning, Pg.2 of 2: Rnetworks for monitoring: system 2.5V, LX25 Vcco 2.5V, LX25 Vccaux 2.5V, LX25 Vccint 1.2V, Board input 5V
19	Power Supply Pg.1 of 3: +5V input, Digital GND to analog GND interconnect
20	Power Supply Pg.2 of 3: TI PTH05000-WAH: System 2.5V, LX25 Vccaux 2.5V, LX25 Vcco 2.5V
21	Power Supply Pg.3 of 3: TI PTH05000-WAH reg.:System 3.3V, LX25 Vcco 3.3V, LX25 Vccint 1.2V, 1.25V mem.I/F Vref tap
22	Decoupling caps Pg.1 of 5: LX25 Vccint 1.2V
23	Decoupling caps Pg.2 of 5: System 2.5V
24	Decoupling caps Pg.3 of 5: LX25 Vcco 2.5V
25	Decoupling caps Pg.4 of 5: LX25 Vccaux 2.5V, System 3.3V, mem. Vref 1.25V
26	Decoupling caps Pg.5 of 5: System 5V input
27	Page List

Latest Schematics Revision:
Rev0 on 02-07-2005

Xilinx PCB Schematic Number: 0381172

Xilinx ML450 Rev3

TITLE: 4VLX25FF668

SIZE: C | DWG NO: 0381172 | REV: 0

DRAWN BY: <YOUR NAME HERE> | SCALE: | SHEET: 27 of 27 | 2-7-2005_13:35

XILINX®