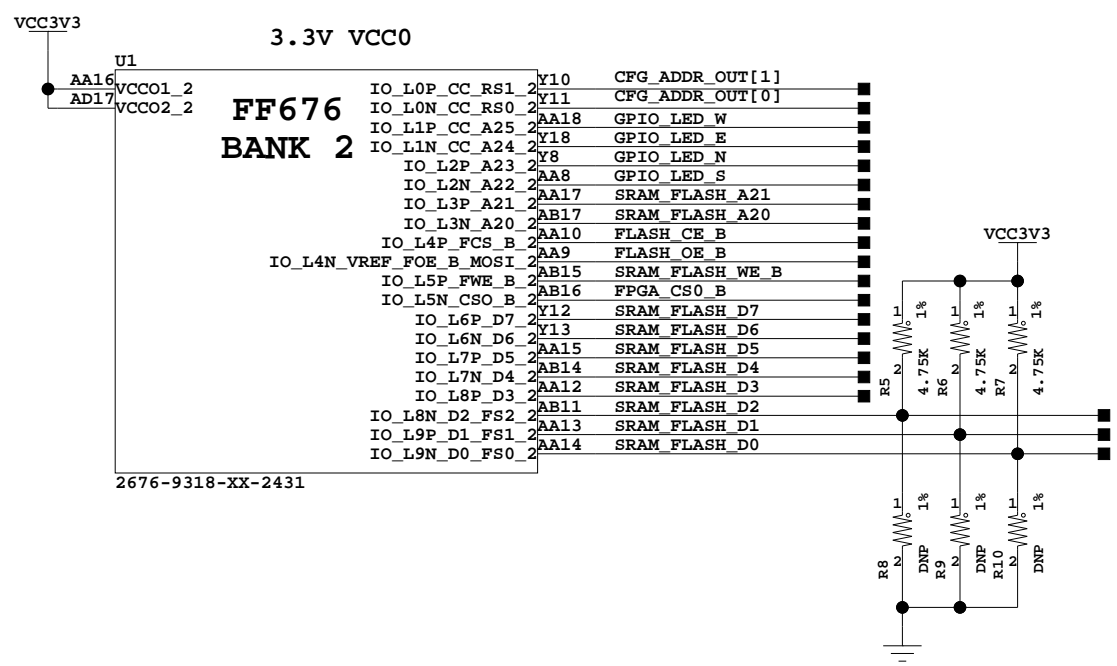
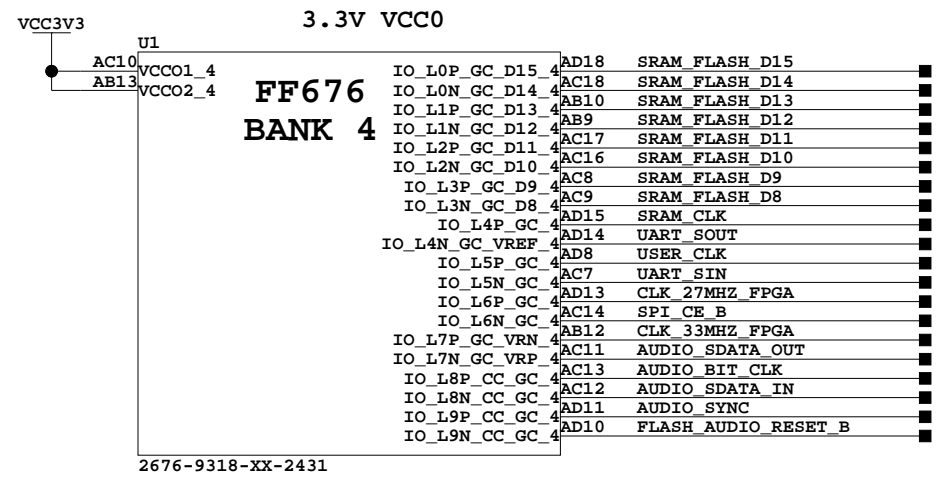
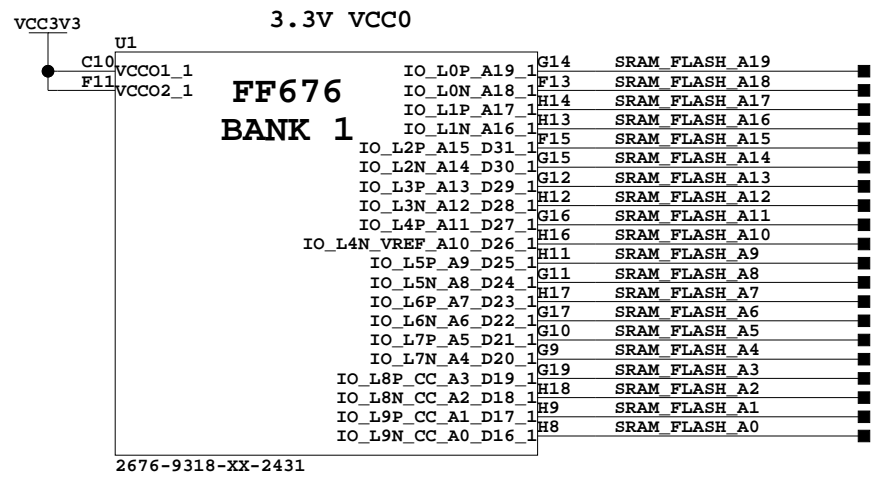
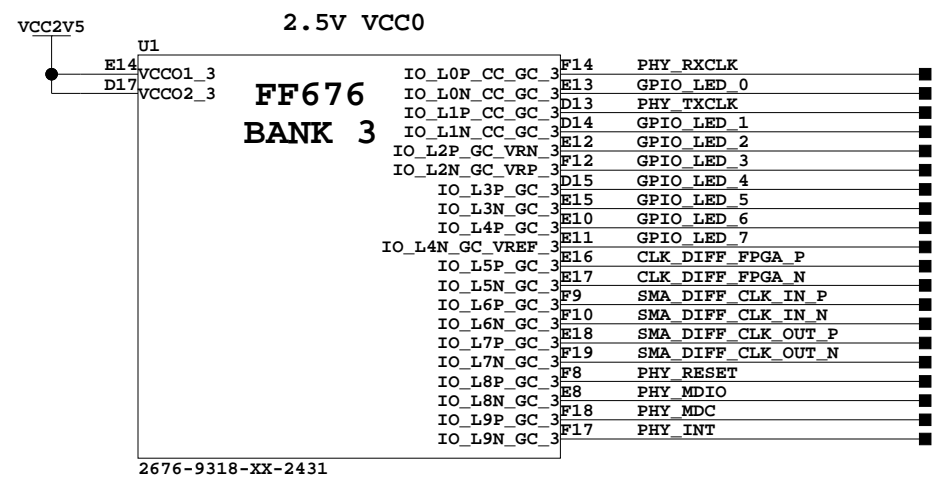
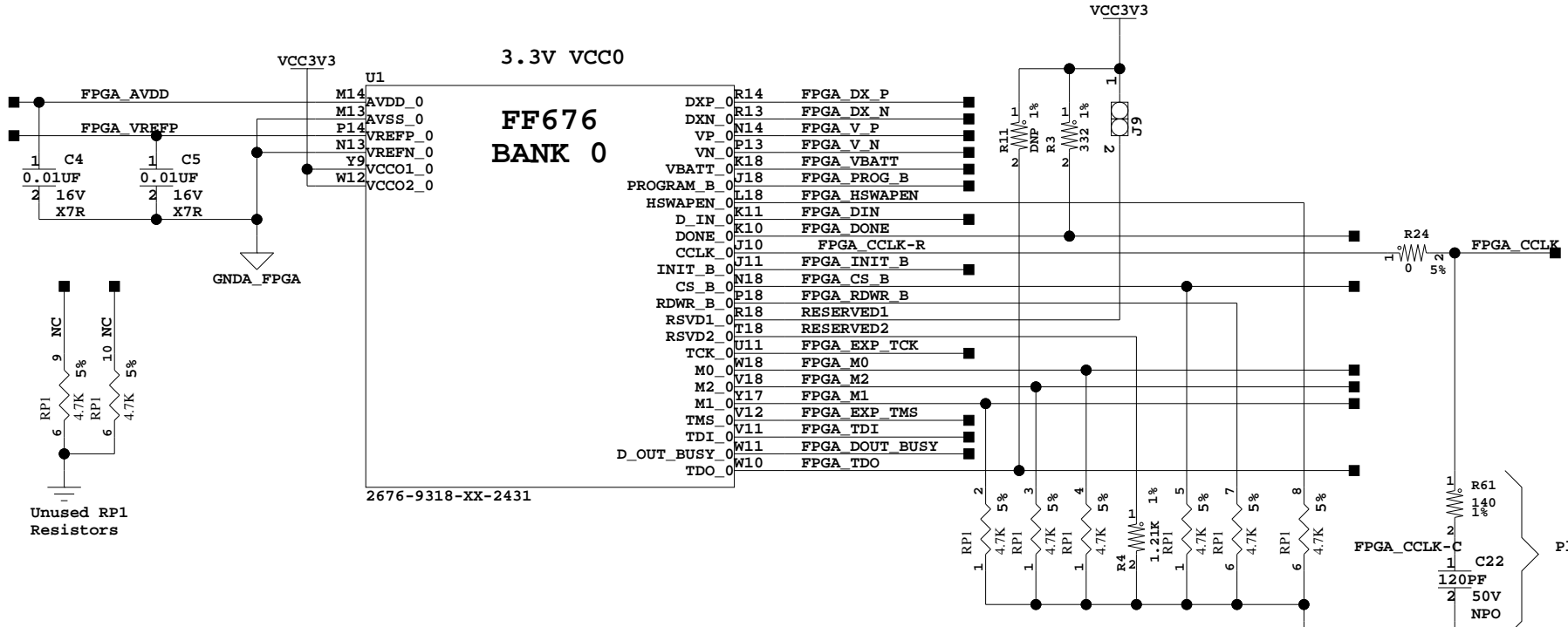


**XILINX**

Title: SCHEM, ROHS COMPLIANT, ML501 VIRTEX-5 LX EVALUATION PLATFORM, 1280412  
**0381239**

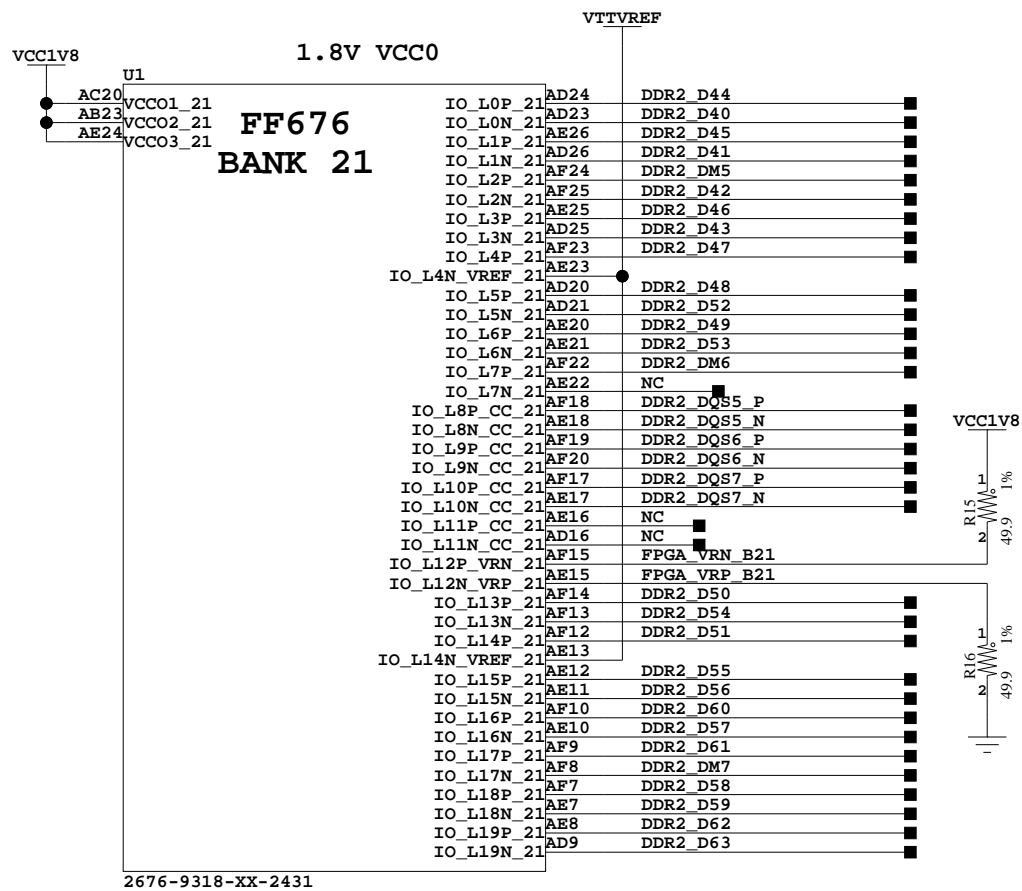
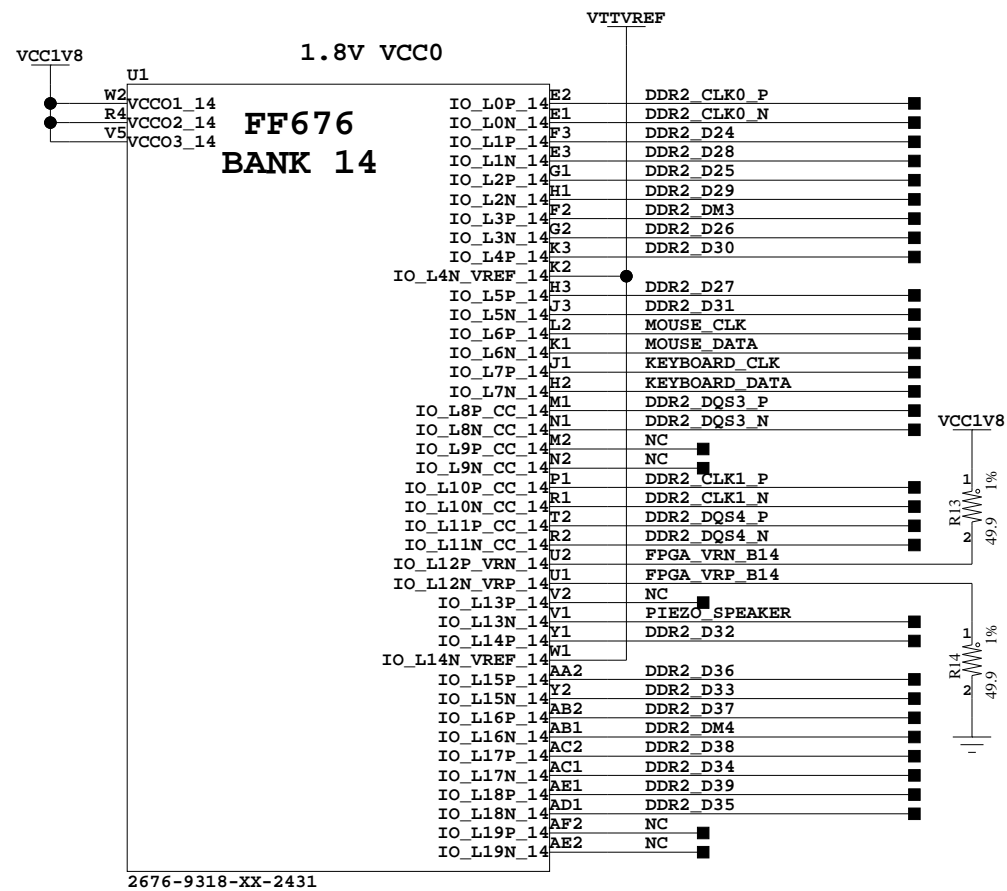
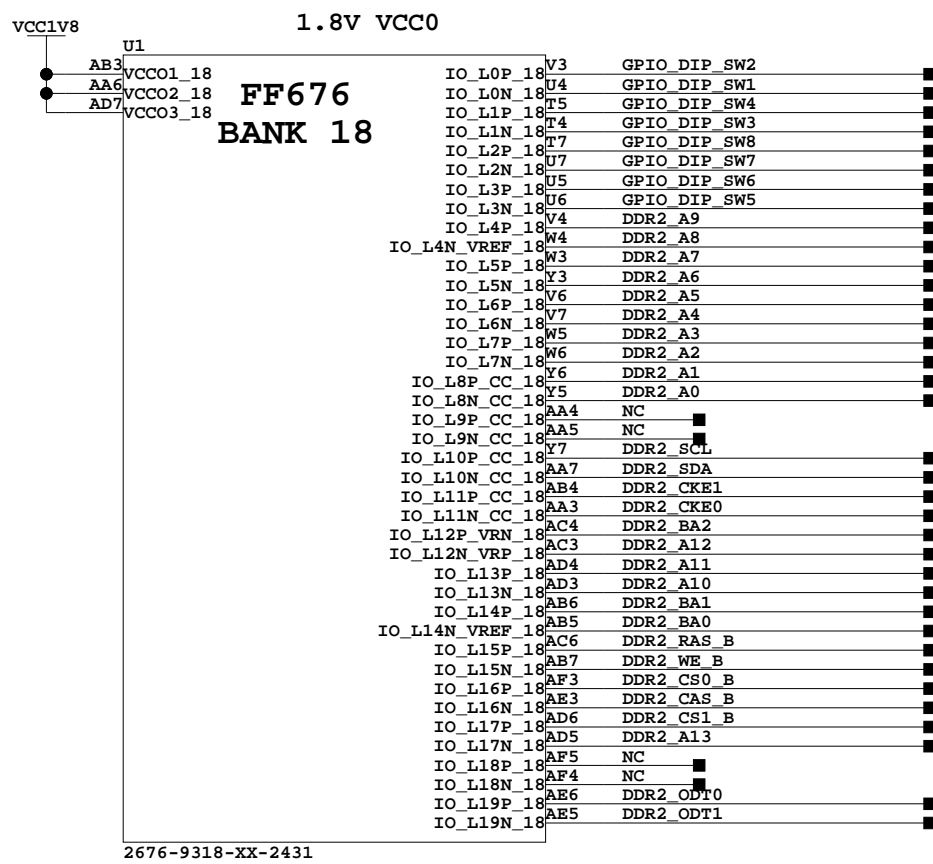
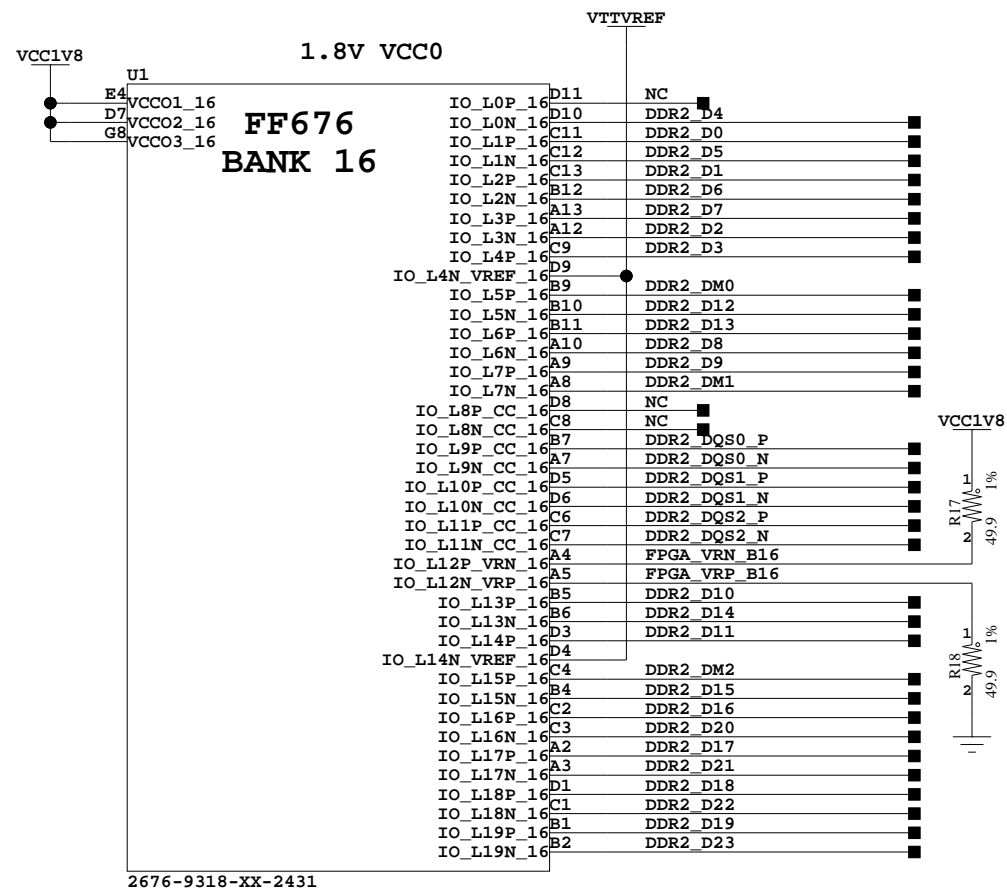
Date: 8-30-2006_16:33	Ver: 01
Sheet Size: B	Rev: B
Sheet <b>1</b> of <b>22</b>	Drawn By BP



**Banks 0,1,2,3,4  
Config, FLASH, SRAM,  
GPIO, CLKs**



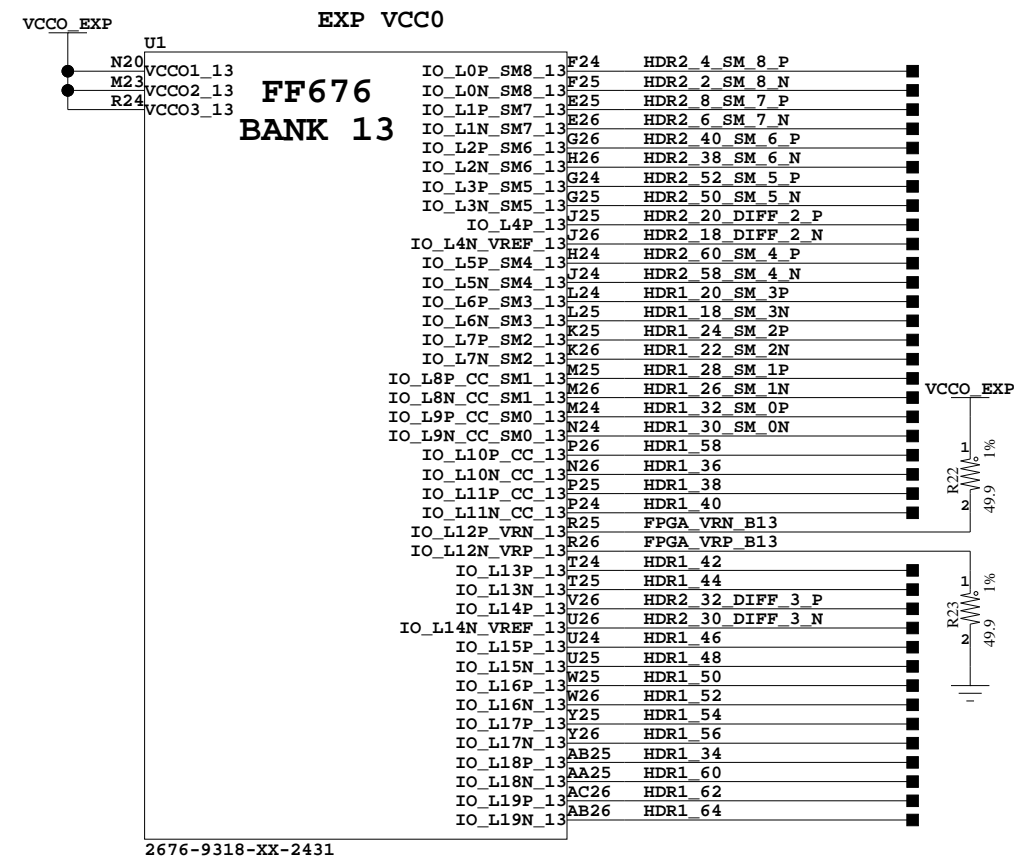
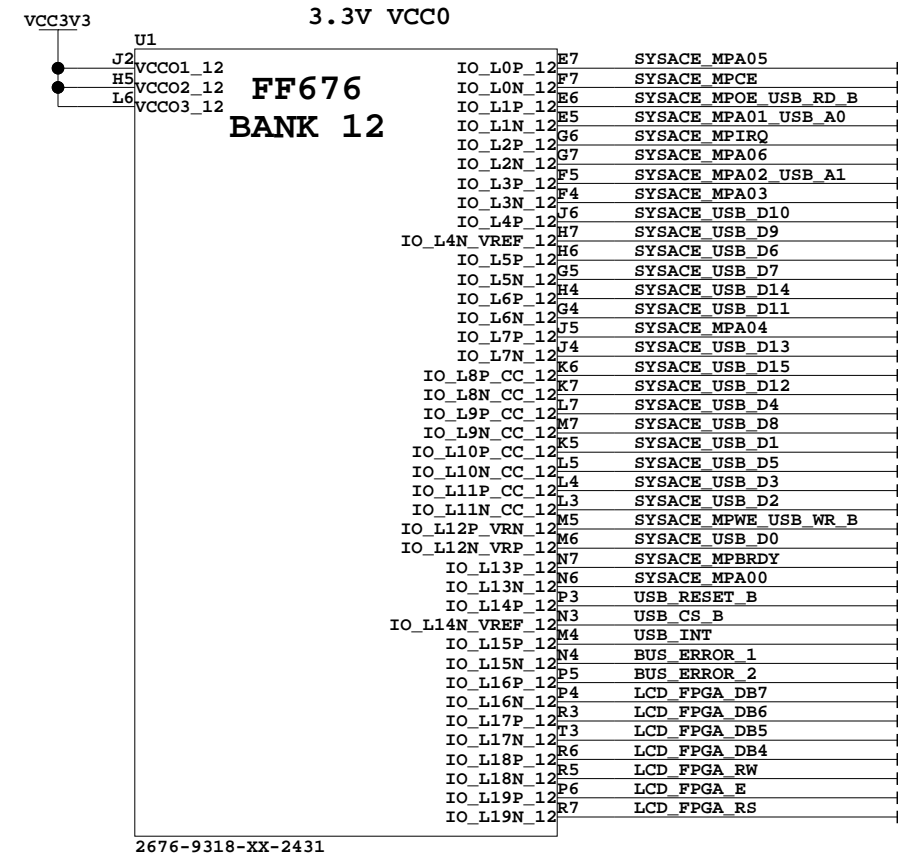
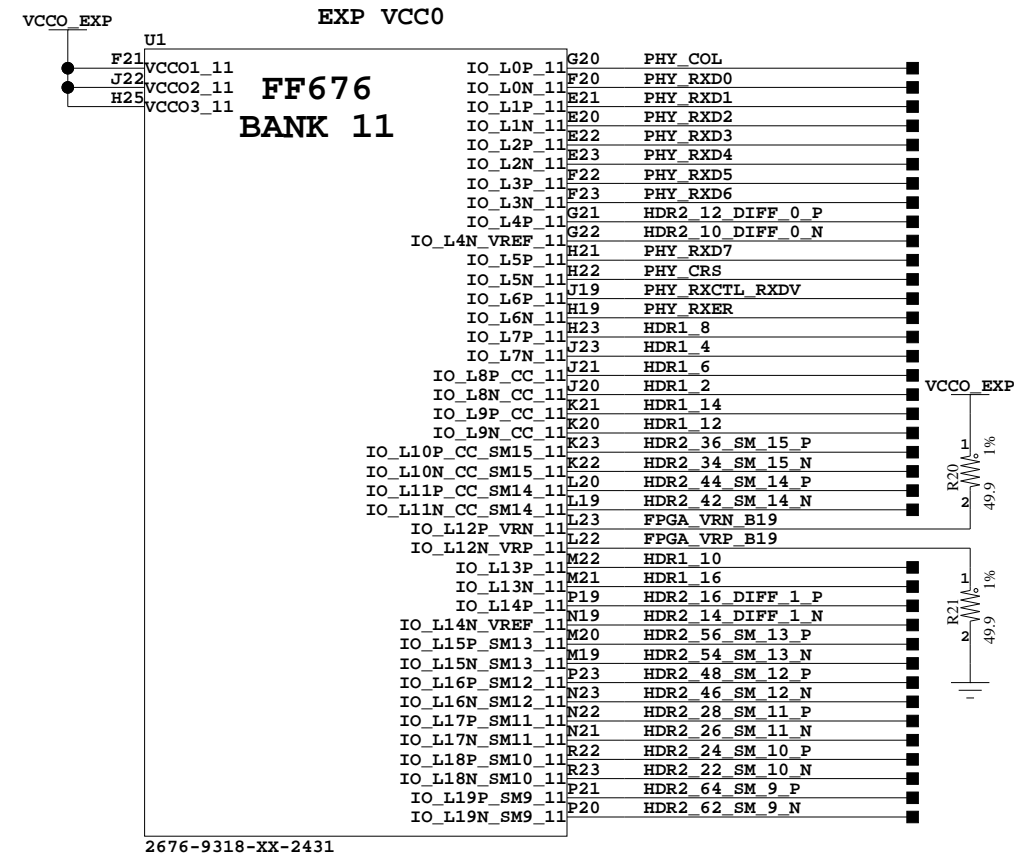
Title:		SCHEM, ML501 EVAL PLATFORM	
0381239		FPGA Banks 0,1,2,3,4 Config, FLASH, SRAM, GPIO, CLKs	
Date:	10-10-2006_13:25	Ver:	01
Sheet Size:	B	Rev:	B
Sheet	2 of 22	Drawn By	BP



**Banks 14,16,18,21  
DDR2, PS2, GPIO**



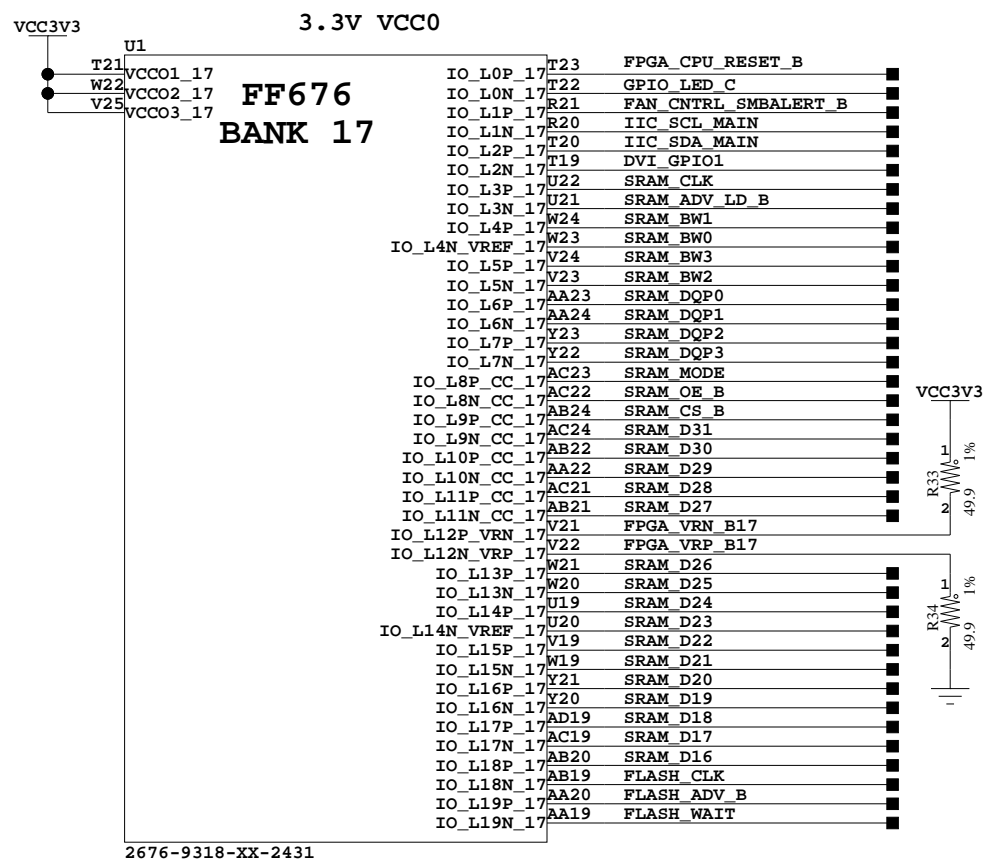
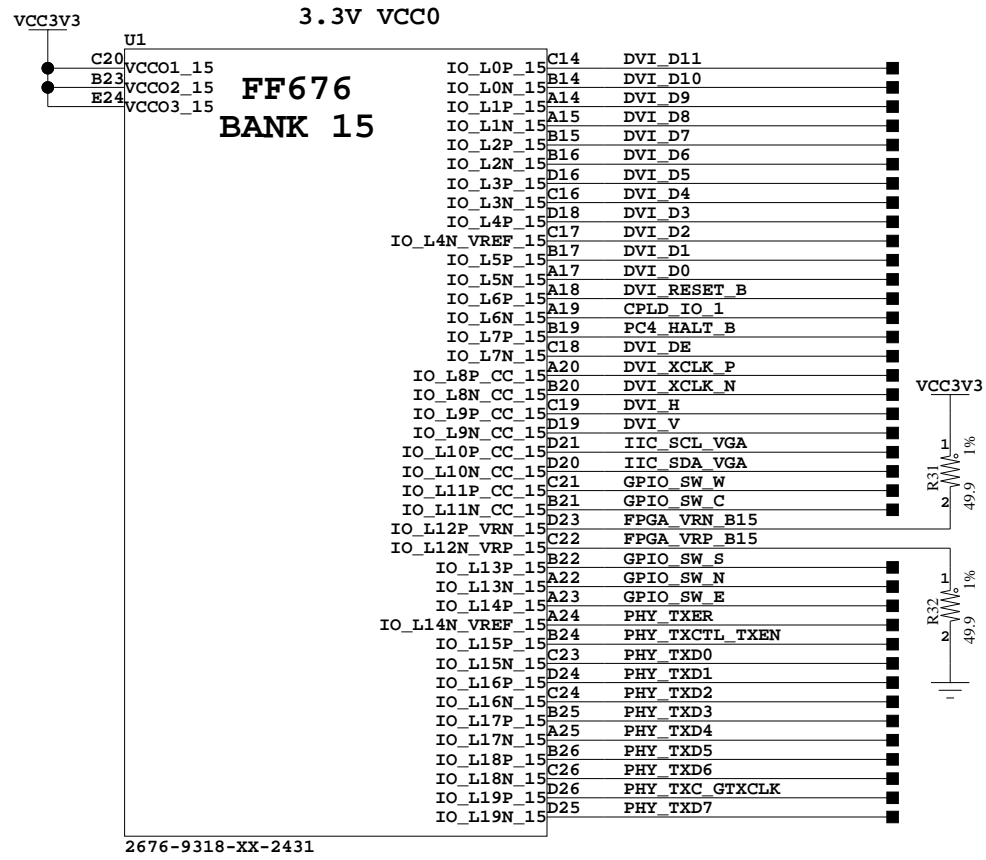
Title:		SCHEM, ML501 EVAL PLATFORM	
0381239		FPGA Bank 14, 16, 18, 21 DDR2, PS2, GPIO	
Date:	8-30-2006_16:33	Ver:	01
Sheet Size:	B	Rev:	B
Sheet	3 of 22	Drawn By	BP



Banks 11,12,13  
Sys ACE, XGI,  
PHY, LCD



Title:		SCHEM, ML501 EVAL PLATFORM	
0381239		Banks 11,12,13	
		Sys ACE, XGI, PHY, LCD	
Date:	8-30-2006_16:33	Ver:	01
Sheet Size:	B	Rev:	B
Sheet	4 of 22	Drawn By	BP

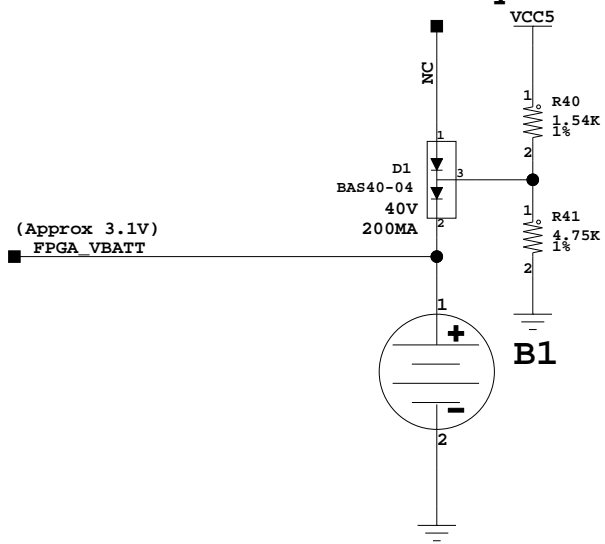


**Banks 15, 17**  
**DVI, IIC, PHY**  
**SRAM, FLASH, GPIO**

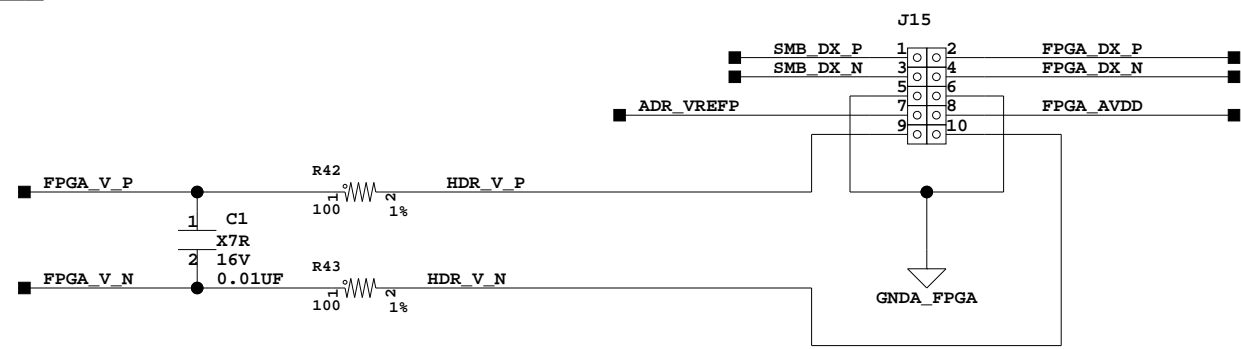


Title:		SCHEM, ML501 EVAL PLATFORM	
0381239		Banks 11,12,13	
		DVI, IIC, PHY, SRAM, GPIO	
Date:	8-30-2006_16:33	Ver:	01
Sheet Size:	B	Rev:	B
Sheet	5 of 22	Drawn By	BP

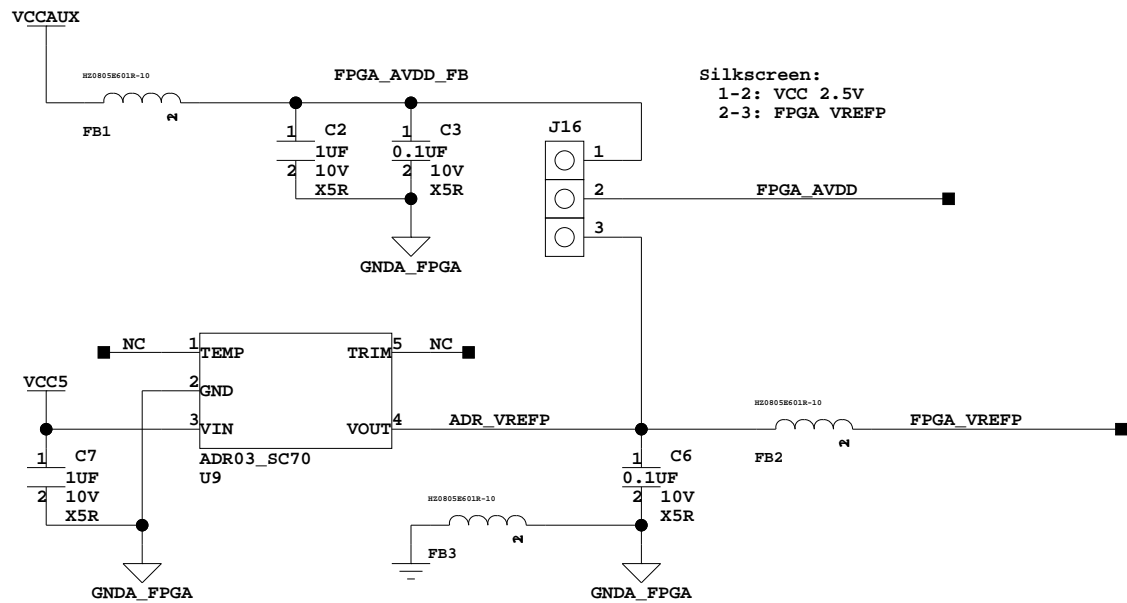
### Rechargeable Battery



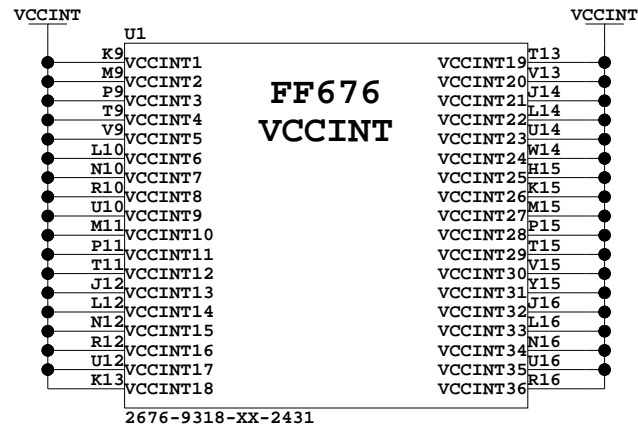
### System Monitor Header



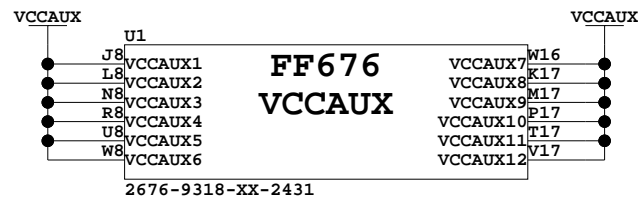
### FPGA AVDD Select



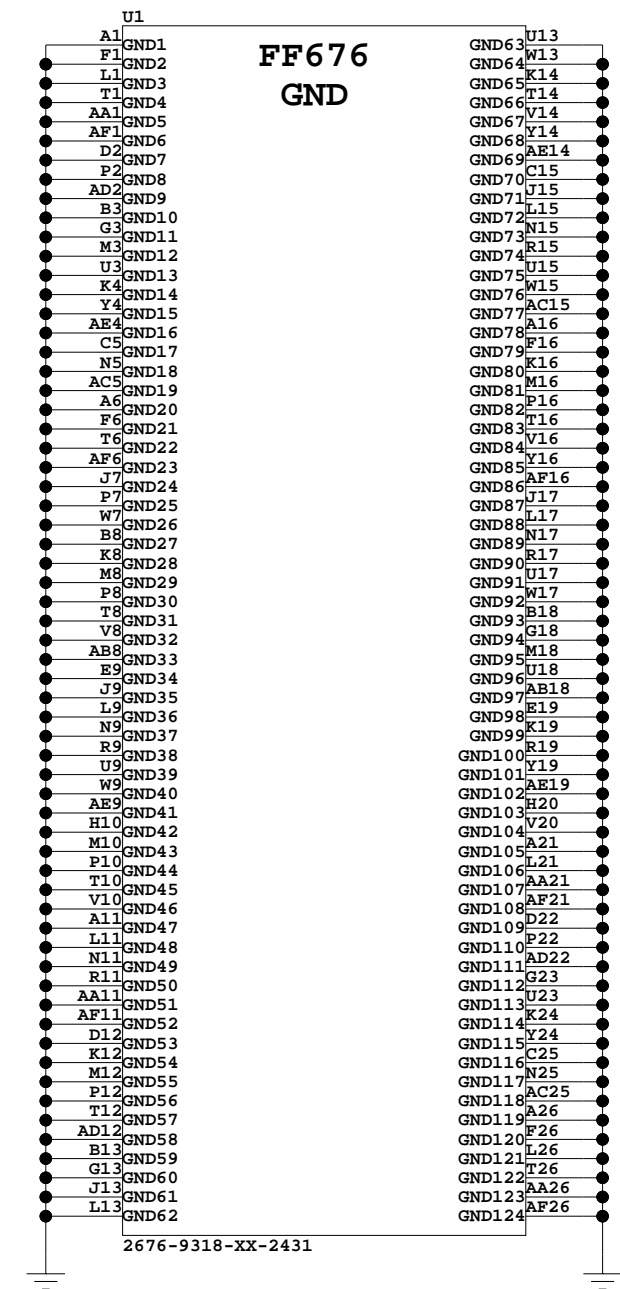
Silkscreen:  
1-2: VCC 2.5V  
2-3: FPGA VREFP



2676-9318-XX-2431



2676-9318-XX-2431

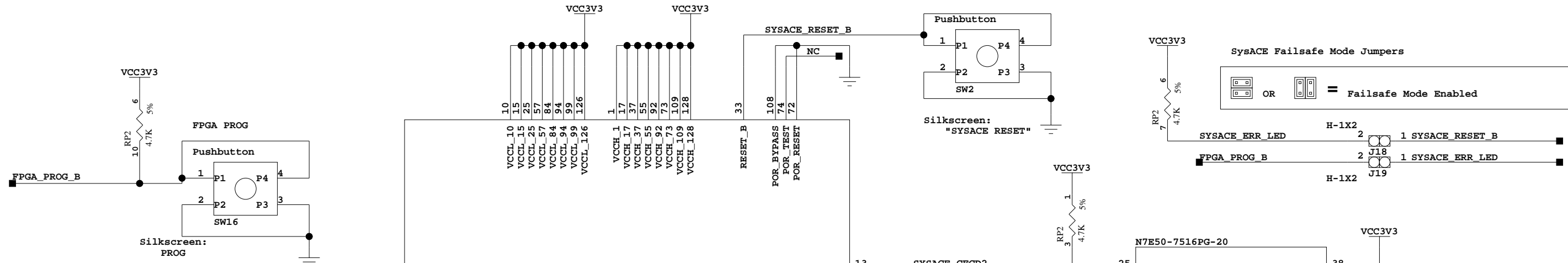


2676-9318-XX-2431

### Misc Banks VCCINT, VCCAUX, GND System Monitor



Title: 0381239 SCHEM, ML501 EVAL PLATFORM FPGA Misc VCCINT, VCCAUX, GND, Sys Mon	
Date: 8-30-2006_16:33	Ver: 01
Sheet Size: B	Rev: B
Sheet 6 of 22	Drawn By BP



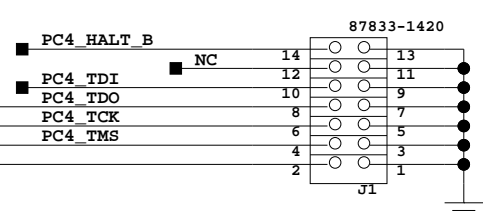
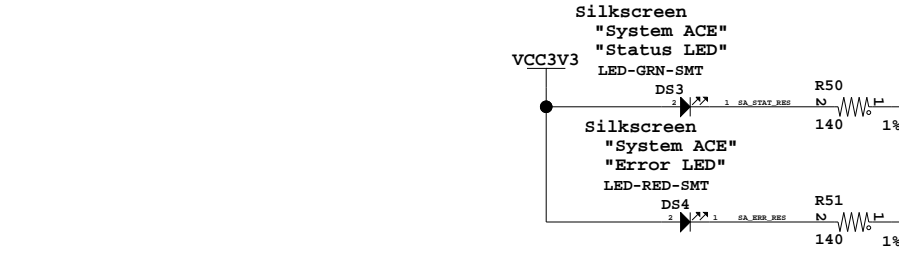
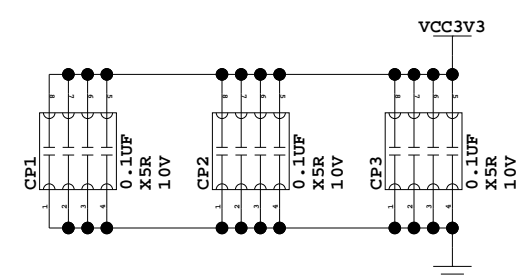
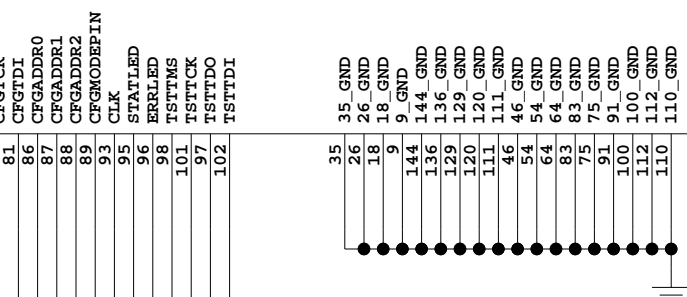
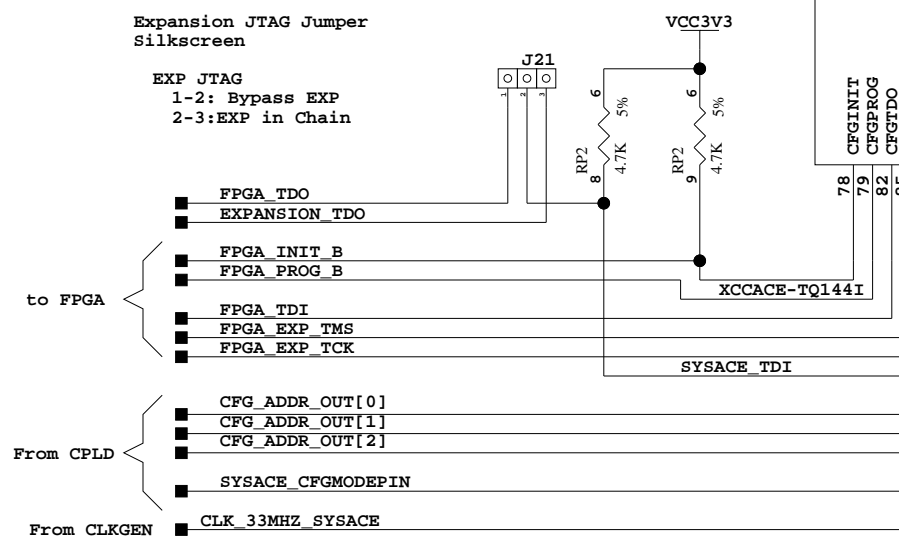
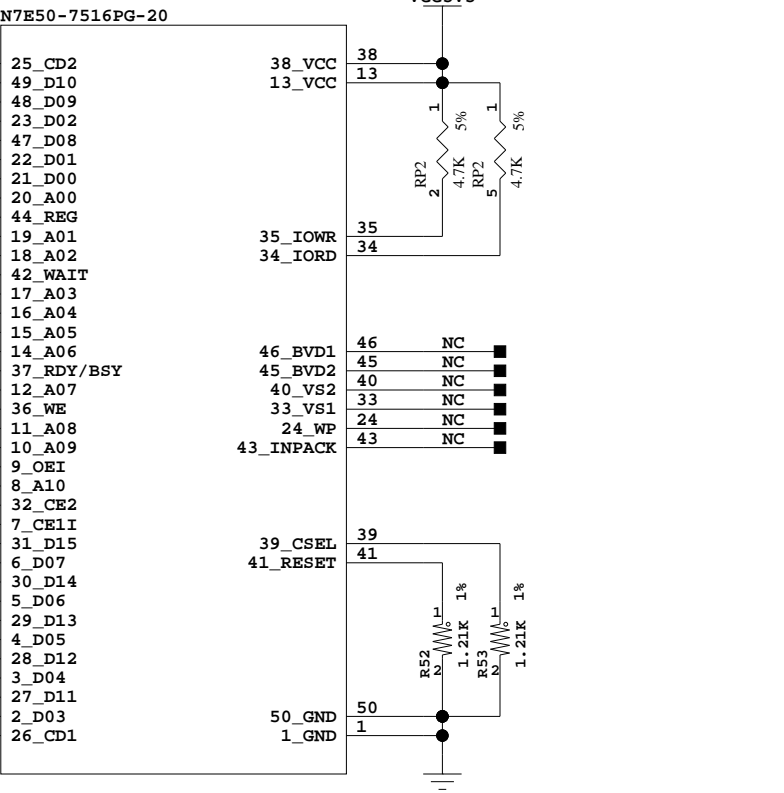
■ SYSACE MPBRDY	39	MPBRDY
■ SYSACE MPIRQ	41	MPIRQ
■ SYSACE MPCE	42	MPCE
■ SYSACE MPA06	43	MPA06
■ SYSACE MPA05	44	MPA05
■ SYSACE MPA04	45	MPA04
■ SYSACE USB D15	47	MPD15
■ SYSACE USB D14	48	MPD14
■ SYSACE USB D13	49	MPD13
■ SYSACE USB D12	50	MPD12
■ SYSACE USB D11	51	MPD11
■ SYSACE USB D10	52	MPD10
■ SYSACE USB D9	53	MPD09
■ SYSACE USB D8	56	MPD08
■ SYSACE USB D7	58	MPD07
■ SYSACE USB D6	59	MPD06
■ SYSACE USB D5	60	MPD05
■ SYSACE USB D4	61	MPD04
■ SYSACE USB D3	62	MPD03
■ SYSACE USB D2	63	MPD02
■ SYSACE USB D1	65	MPD01
■ SYSACE USB D0	66	MPD00
■ SYSACE MPA03	67	MPA03
■ SYSACE MPA02 USB A1	68	MPA02
■ SYSACE MPA01 USB A0	69	MPA01
■ SYSACE MPA00	70	MPA00
■ SYSACE MPWE USB WR B	76	MPWE
■ SYSACE MPOE USB RD B	77	MPOE

**SYSTEMACE  
TQFP144  
(DIE DOWN)**

PARTS=1  
LEVEL=STD

U2

CFCD2	13	SYSACE CFCD2	25	25_CD2
CFD10	12	SYSACE CFD10	49	49_D10
CFD09	11	SYSACE CFD09	48	48_D09
CFD02	8	SYSACE CFD02	23	23_D02
CFD08	7	SYSACE CFD08	47	47_D08
CFD01	6	SYSACE CFD01	22	22_D01
CFD00	5	SYSACE CFD00	21	21_D00
CFA00	4	SYSACE CFA00	20	20_A00
CFREG	3	SYSACE CFREG	44	44_REG
CFA01	142	SYSACE CFA01	19	19_A01
CFA02	141	SYSACE CFA02	18	18_A02
CFWAIT	140	SYSACE CFWAIT	42	42_WAIT
CFA03	139	SYSACE CFA03	17	17_A03
CFA04	137	SYSACE CFA04	16	16_A04
CFA05	135	SYSACE CFA05	15	15_A05
CFA06	134	SYSACE CFA06	14	14_A06
CFGRSVD	133	SYSACE CFGRDSY	37	37_RDY/BSY
CFA07	132	SYSACE CFA07	12	12_A07
CFWE	131	SYSACE CFWE	36	36_WE
CFA08	130	SYSACE CFA08	11	11_A08
CFA09	125	SYSACE CFA09	10	10_A09
CFCE2	123	SYSACE CFCE2	9	9_OEI
CFCE1	121	SYSACE CFCE1	8	8_A10
CFD15	118	SYSACE CFD15	31	31_D15
CFD07	117	SYSACE CFD07	6	6_D07
CFD14	116	SYSACE CFD14	30	30_D14
CFD06	115	SYSACE CFD06	5	5_D06
CFD13	114	SYSACE CFD13	29	29_D13
CFD05	113	SYSACE CFD05	4	4_D05
CFD12	107	SYSACE CFD12	28	28_D12
CFD04	106	SYSACE CFD04	3	3_D04
CFD11	105	SYSACE CFD11	27	27_D11
CFD03	104	SYSACE CFD03	2	2_D03
CFCD1	103	SYSACE CFCD1	26	26_CD1



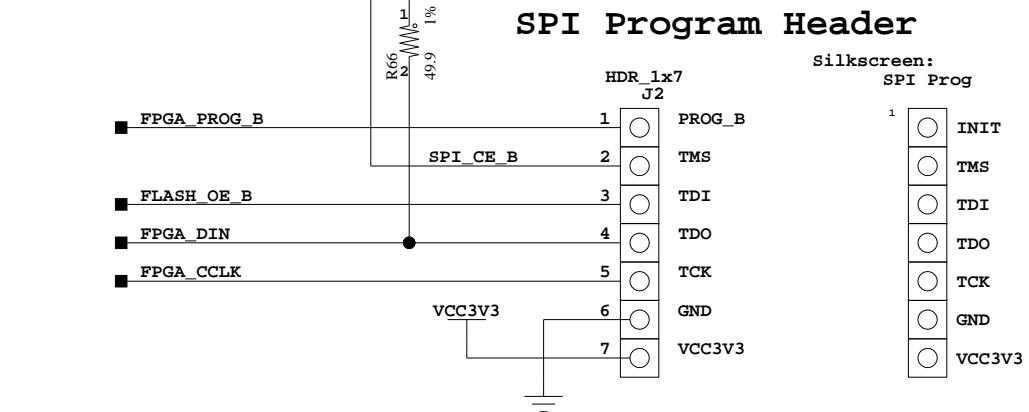
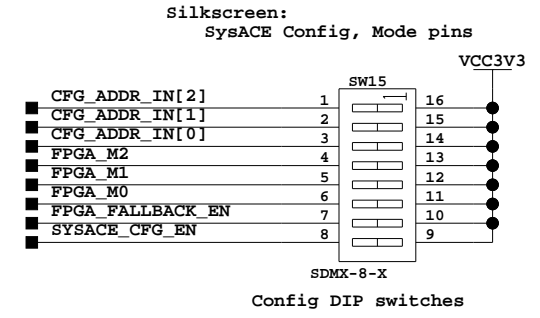
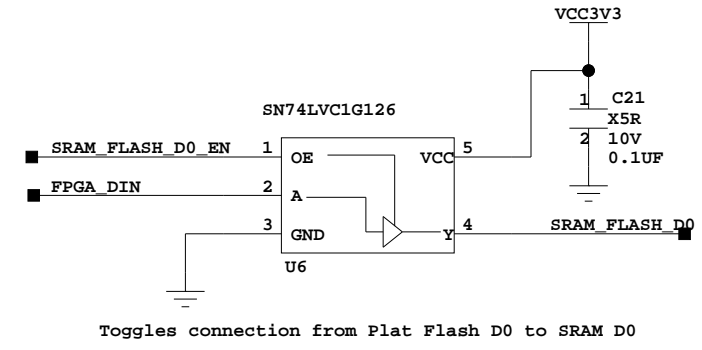
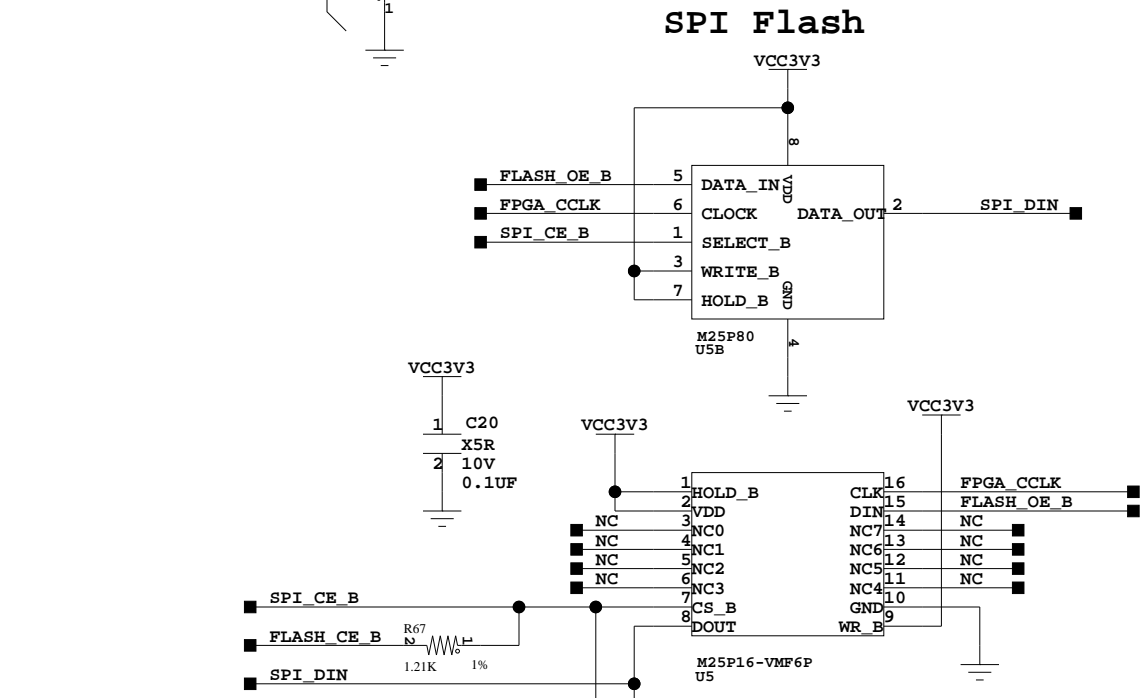
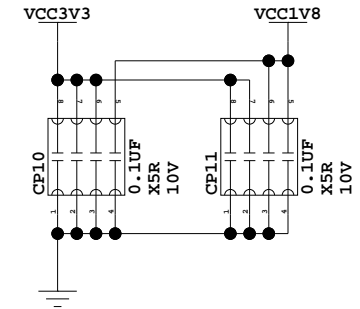
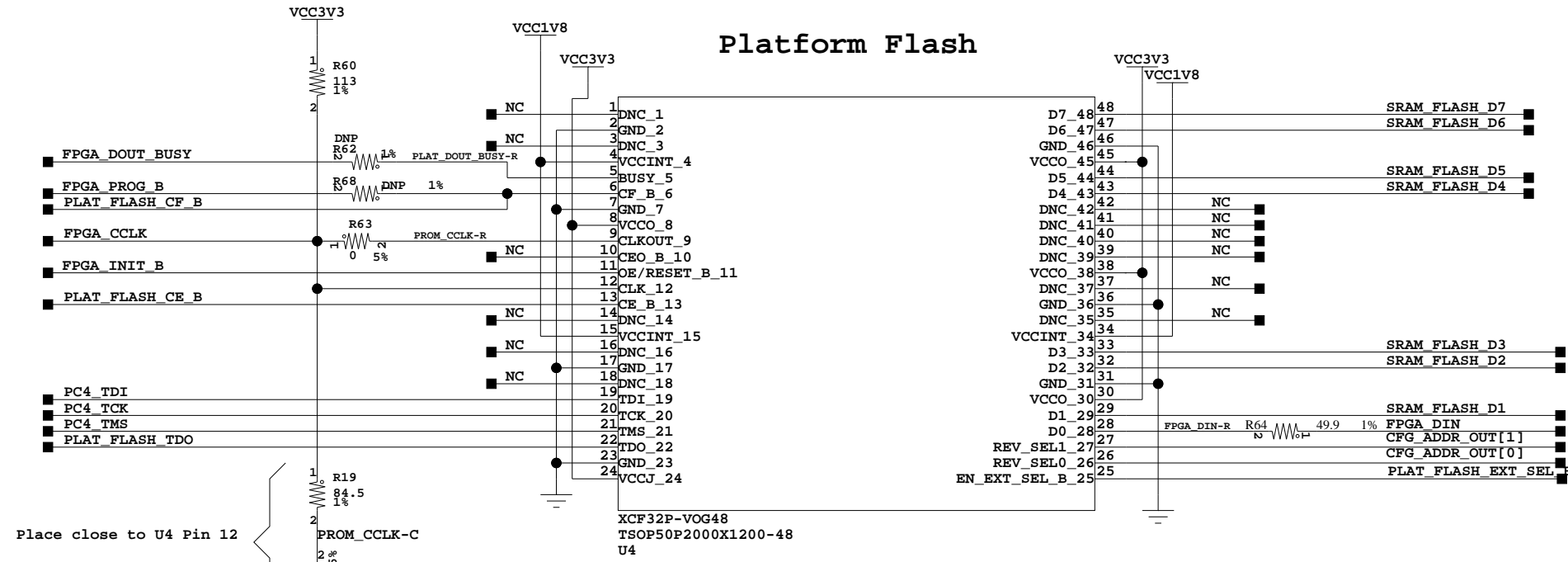
**System ACE**

Title: 0381239 SCHEM, ML501 EVAL PLATFORM System ACE

Date: 8-30-2006\_16:33 Ver: 01

Sheet Size: B Rev: B

Sheet 7 of 22 Drawn By BP

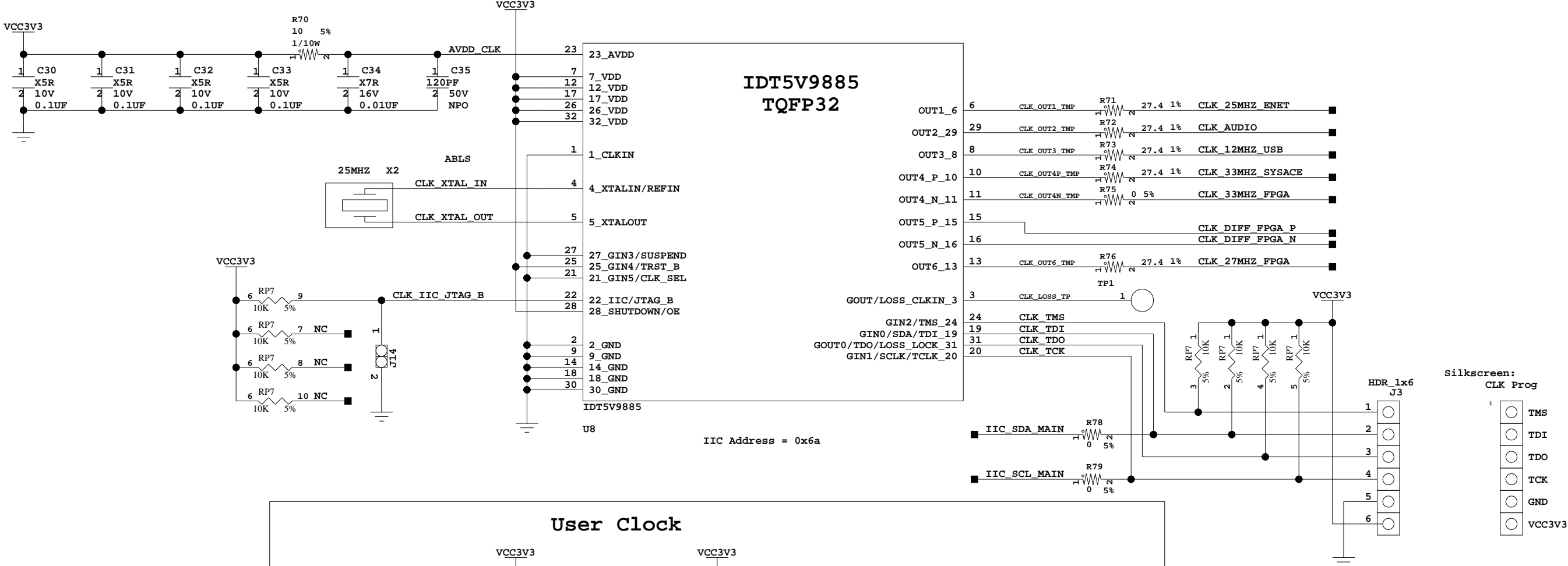


**Misc Config  
 Platform Flash,  
 SPI Flash**

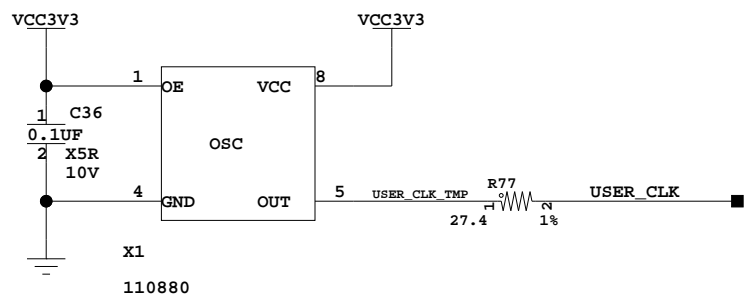
Title: 0381239 SCHEM, ML501 EVAL PLATFORM Misc Config Platform Flash, SPI Flash		
Date: 8-30-2006_16:33	Ver: 01	
Sheet Size: B	Rev: B	
Sheet 8 of 22	Drawn By BP	



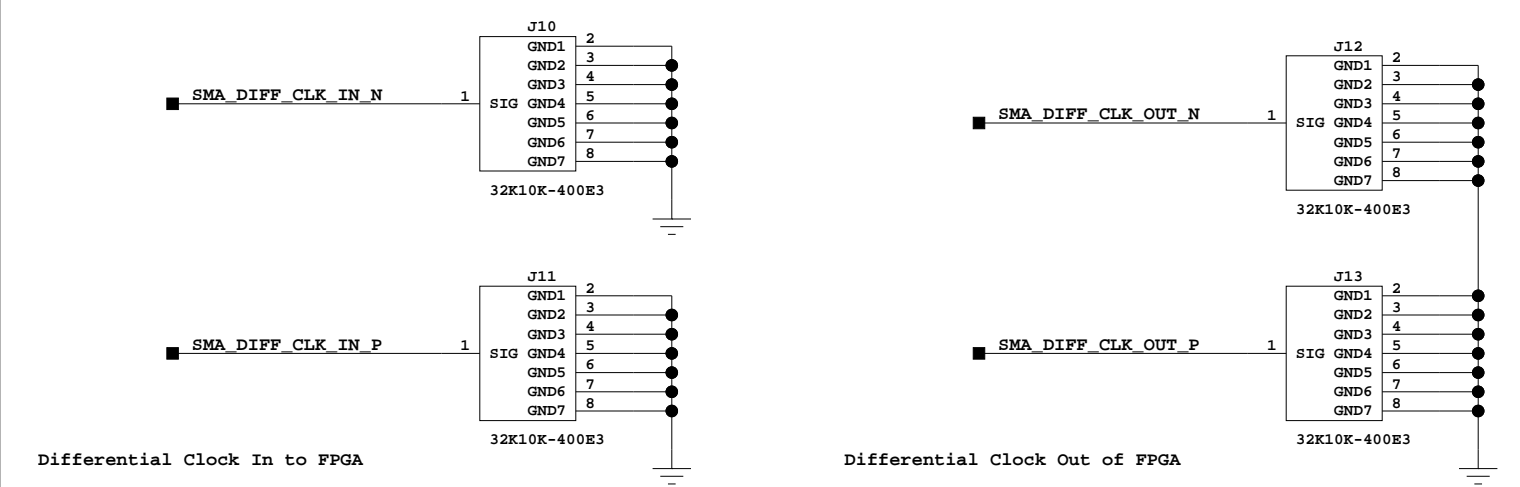
# Clock Generation



## User Clock



## SMA Differential Clocks



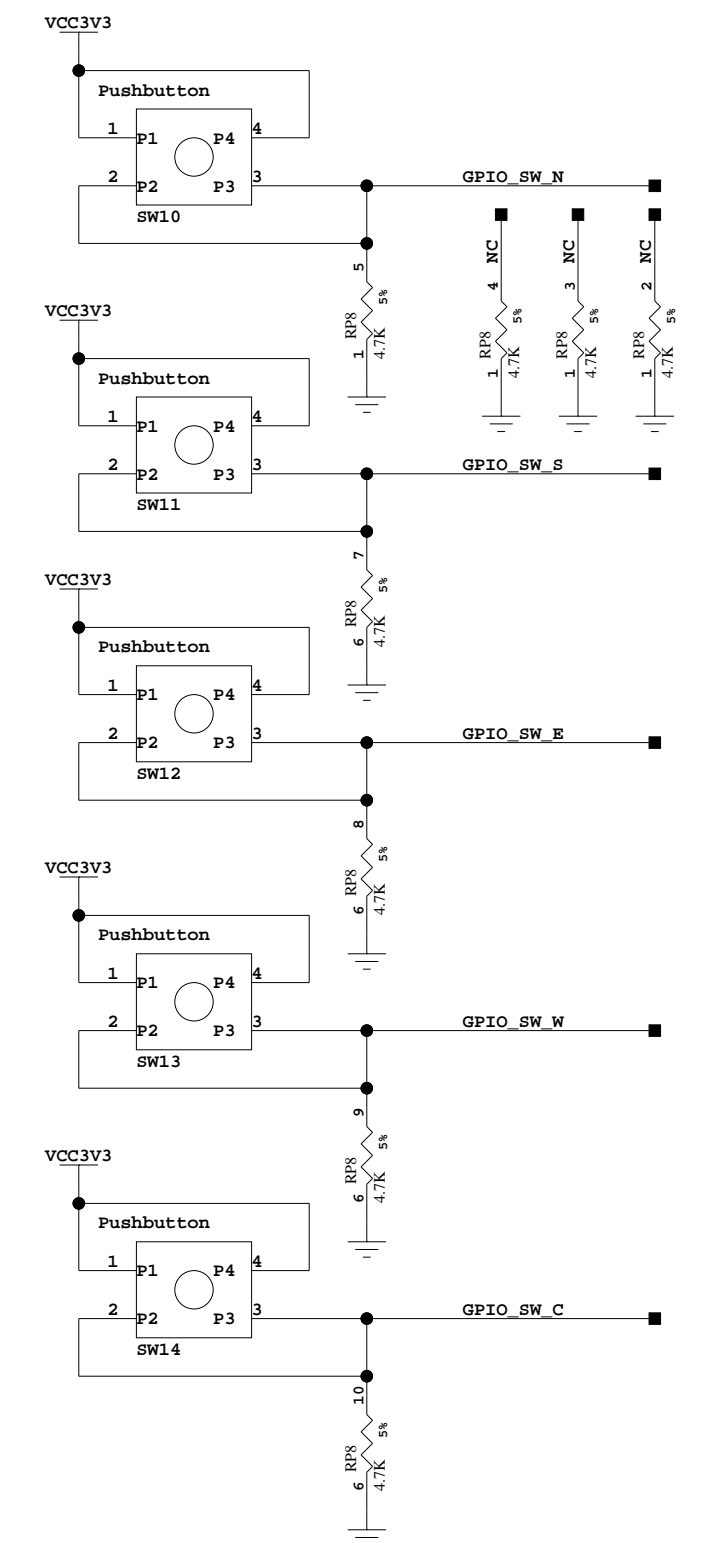
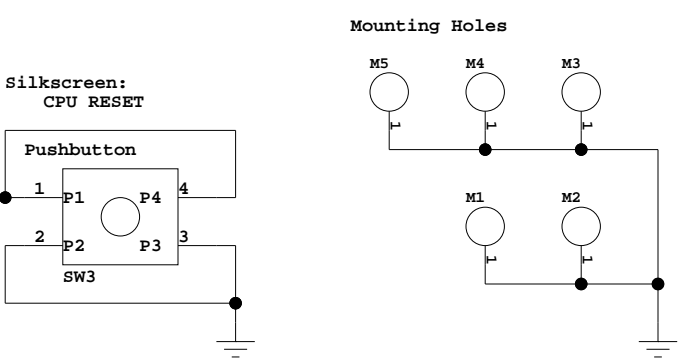
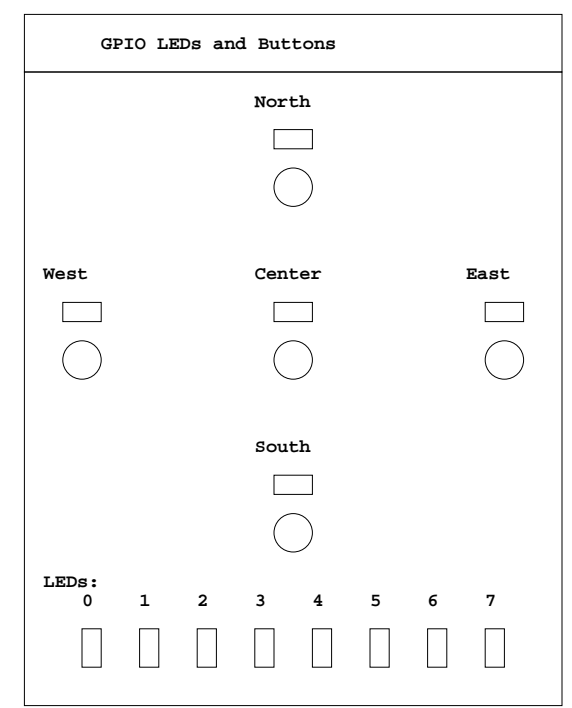
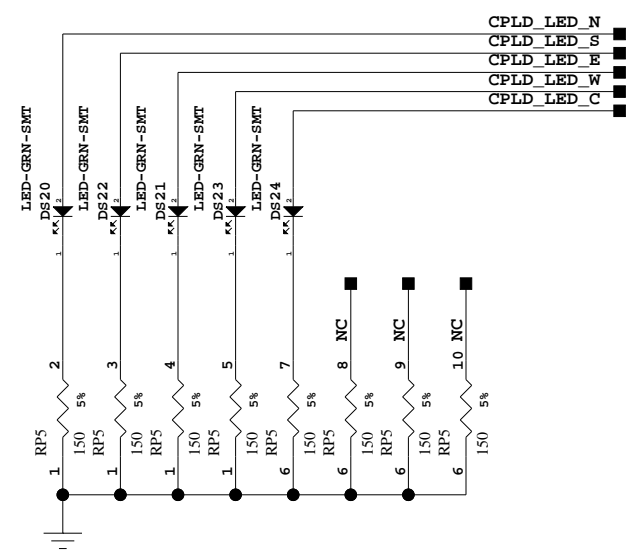
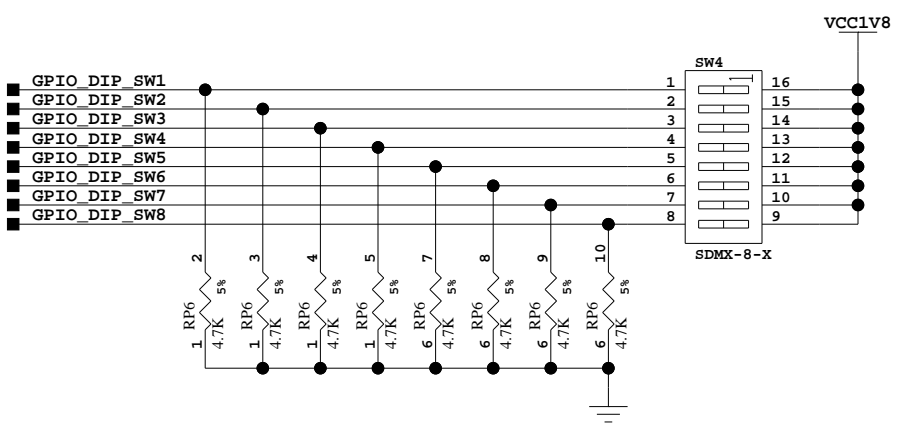
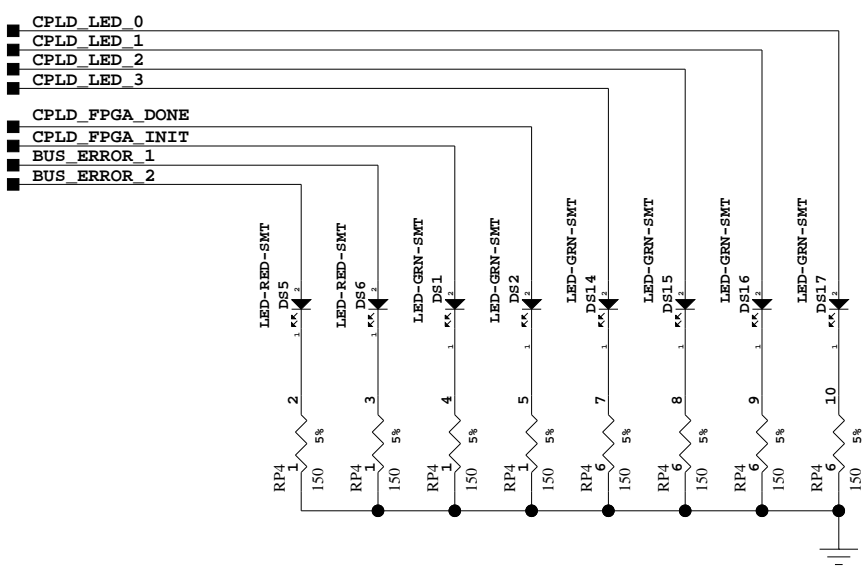
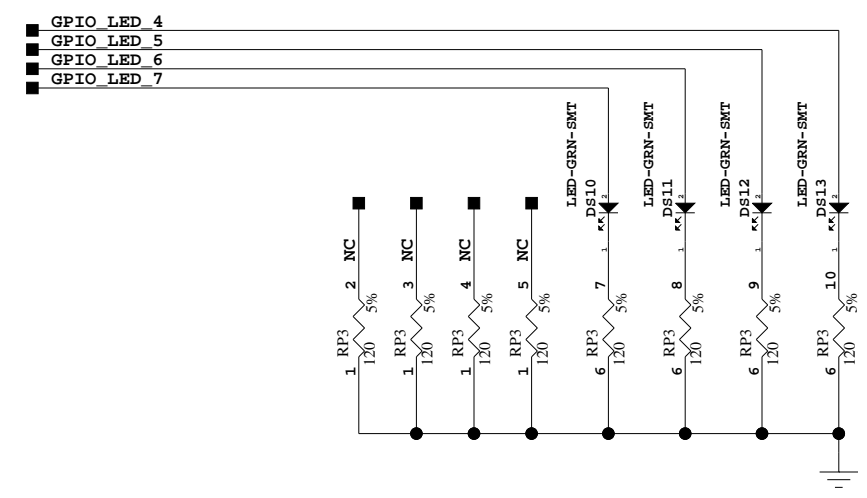
## Clocking - User Clk, Clk Generator, SMA CLK Connectors

Title: 0381239 SCHEM, ML501 EVAL PLATFORM Clock Generator, User Clock, SMA CLK Connectors

Date: 8-30-2006\_16:33 Ver: 01

Sheet Size: B Rev: B

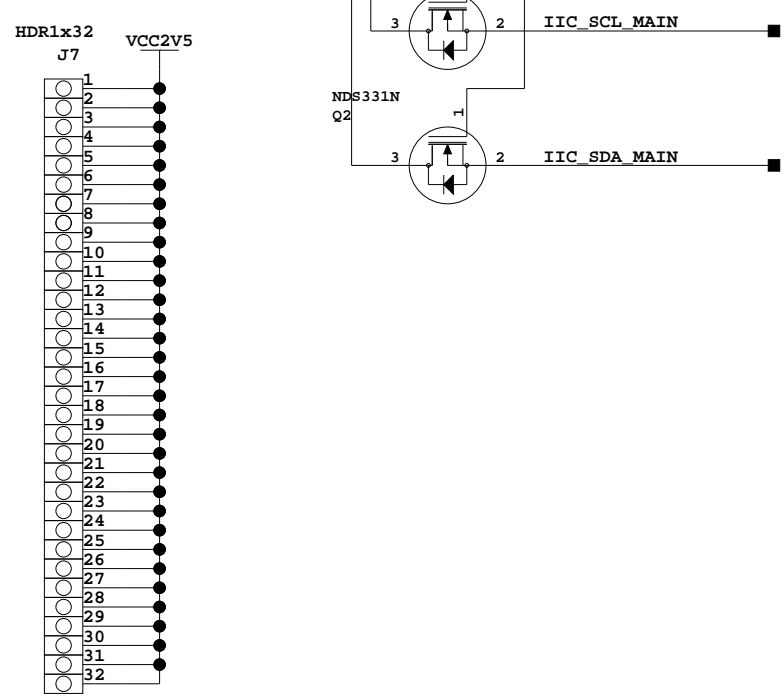
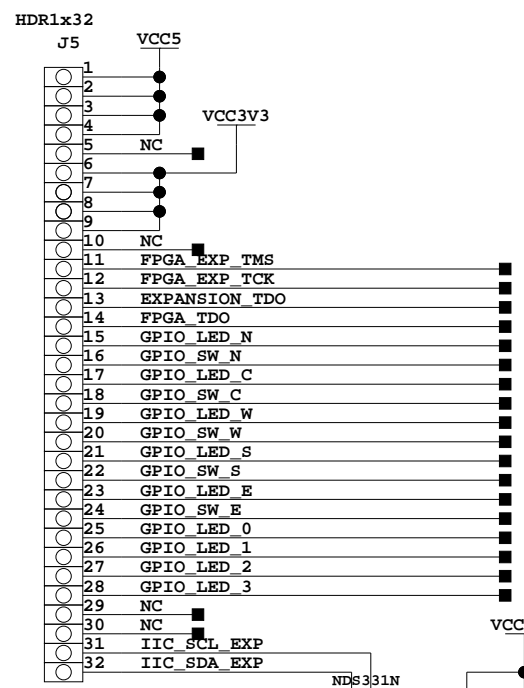
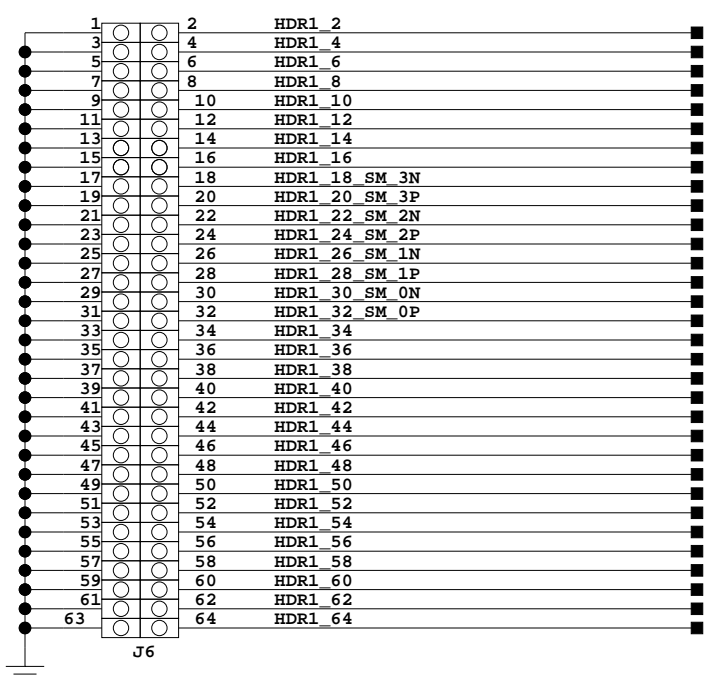
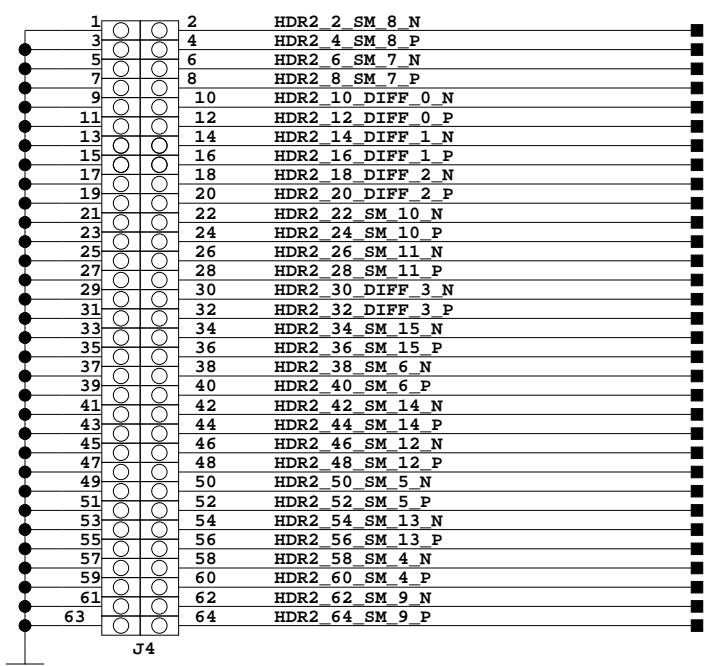
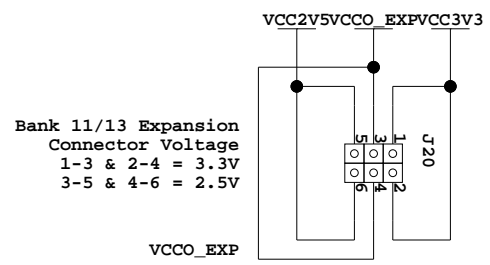
Sheet 9 of 22 Drawn By BP



**GPIO - Buttons, LEDs, Switches**



Title:		SCHEM, ML501 EVAL PLATFORM	
0381239		GPIO Buttons, LEDs, Switches	
Date:	8-30-2006_16:33	Ver:	01
Sheet Size:	B	Rev:	B
Sheet	10 of 22	Drawn By	BP



Matched Length Traces  
Differential Pairs

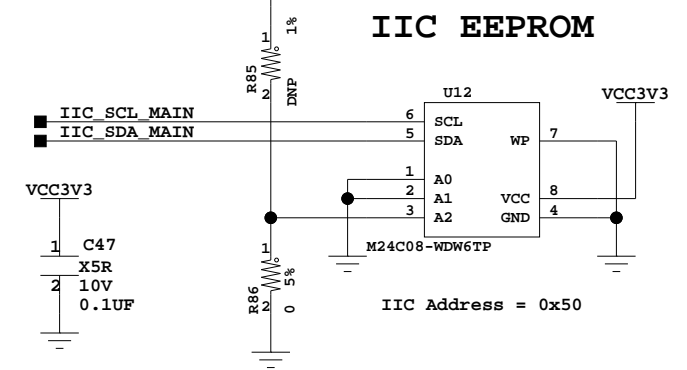
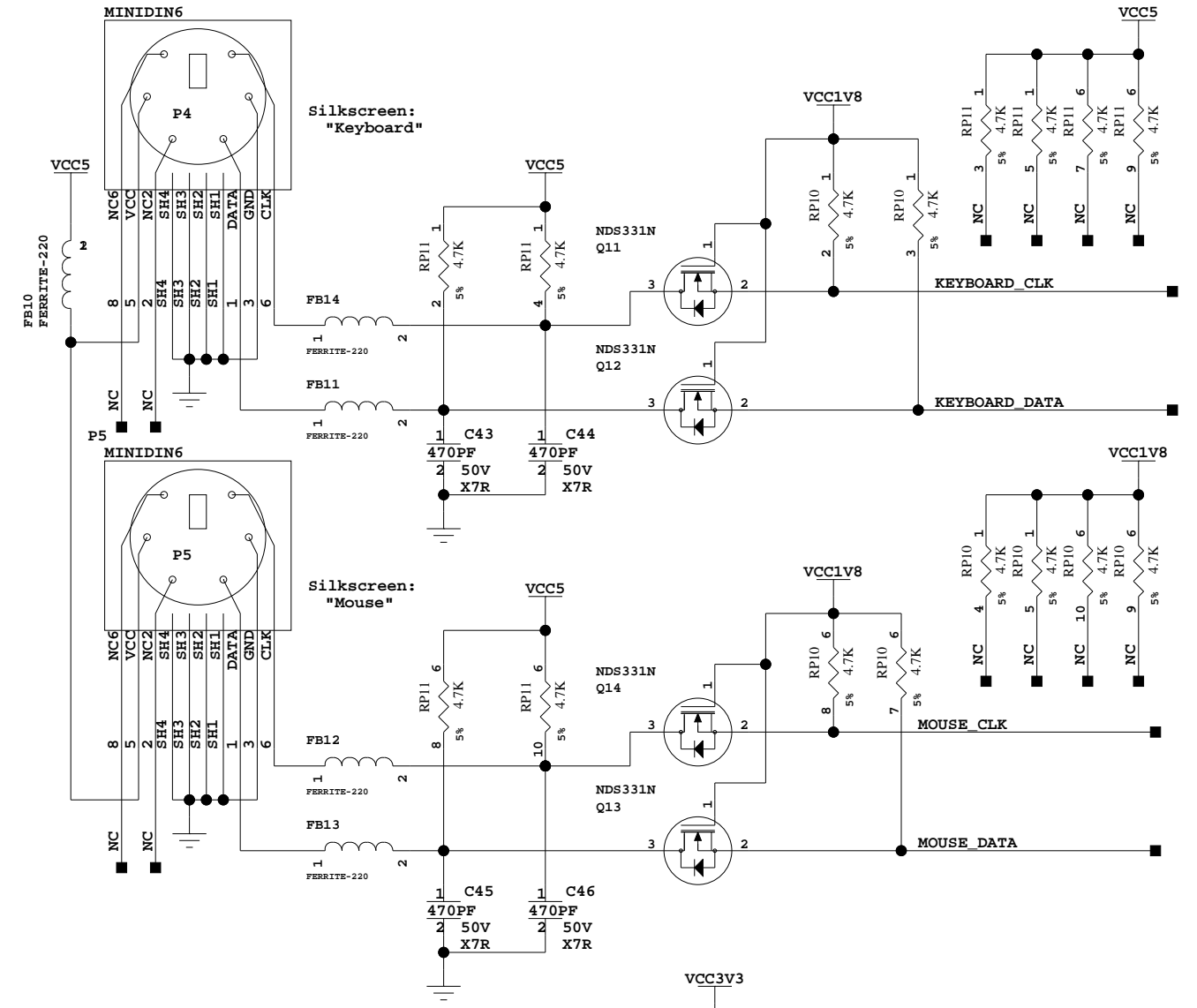
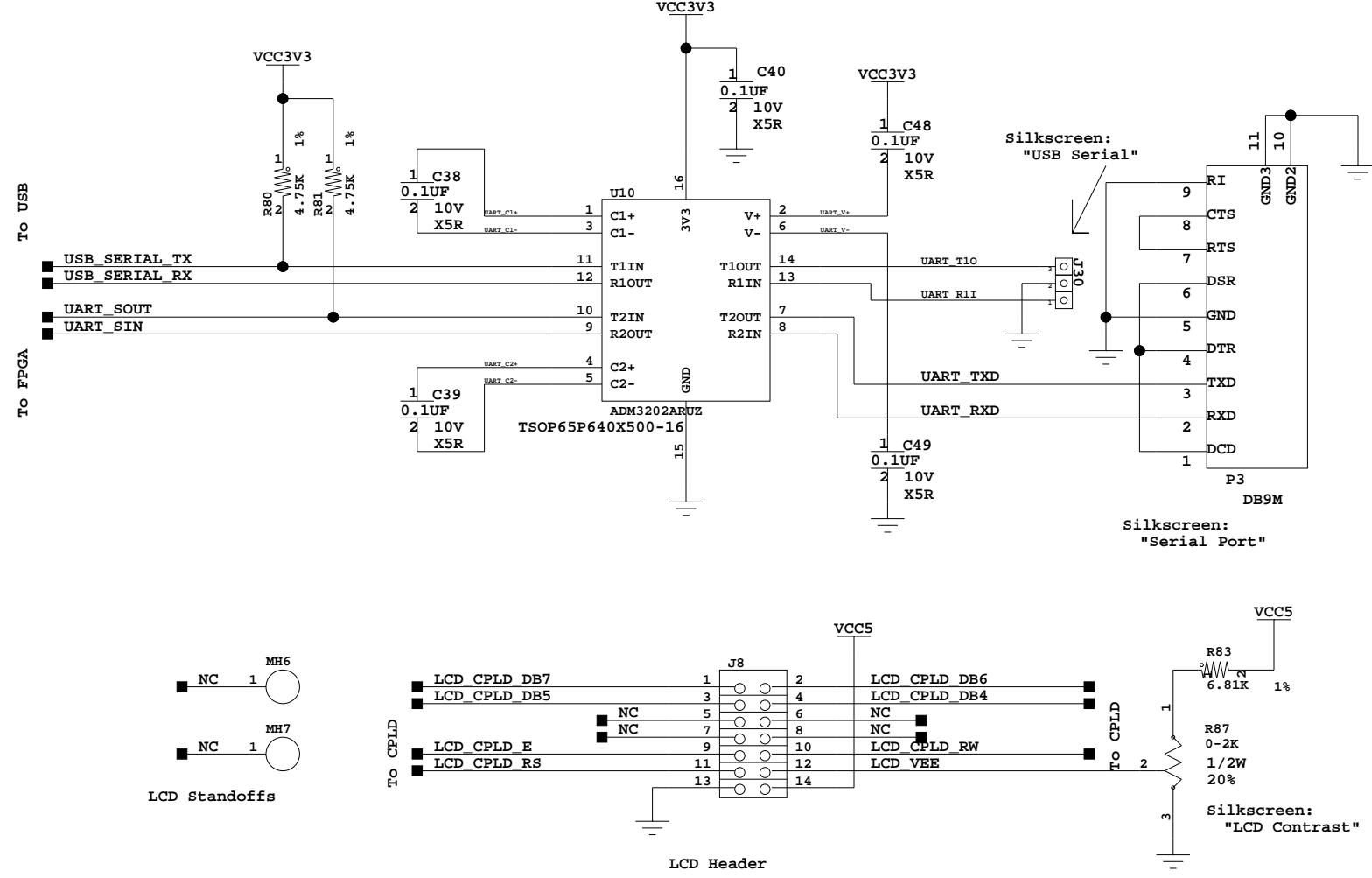
Matched Length Traces  
Independent signals

### XGI - Expansion Connector

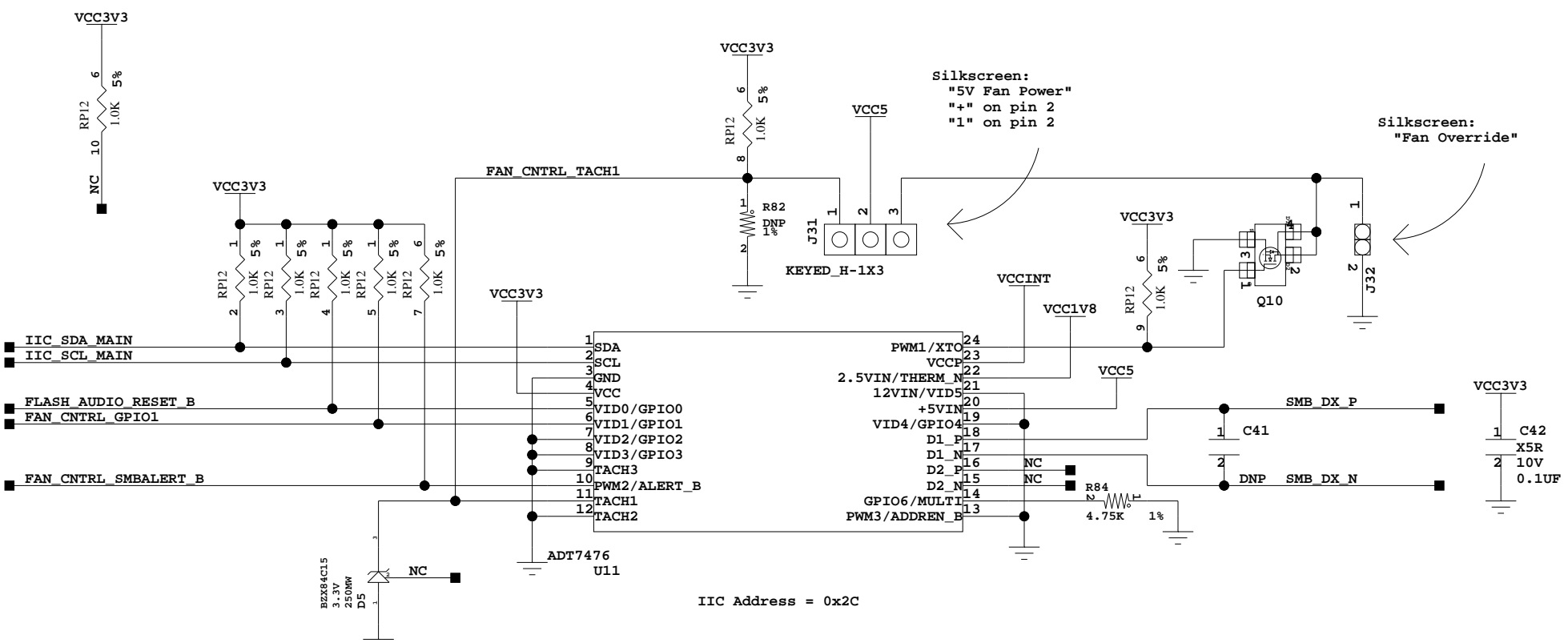


Title: 0381239		SCHEM, ML501 EVAL PLATFORM XGI - Expansion Headers	
Date:	8-30-2006_16:33	Ver:	01
Sheet Size:	B	Rev:	B
Sheet	11 of 22	Drawn By	BP

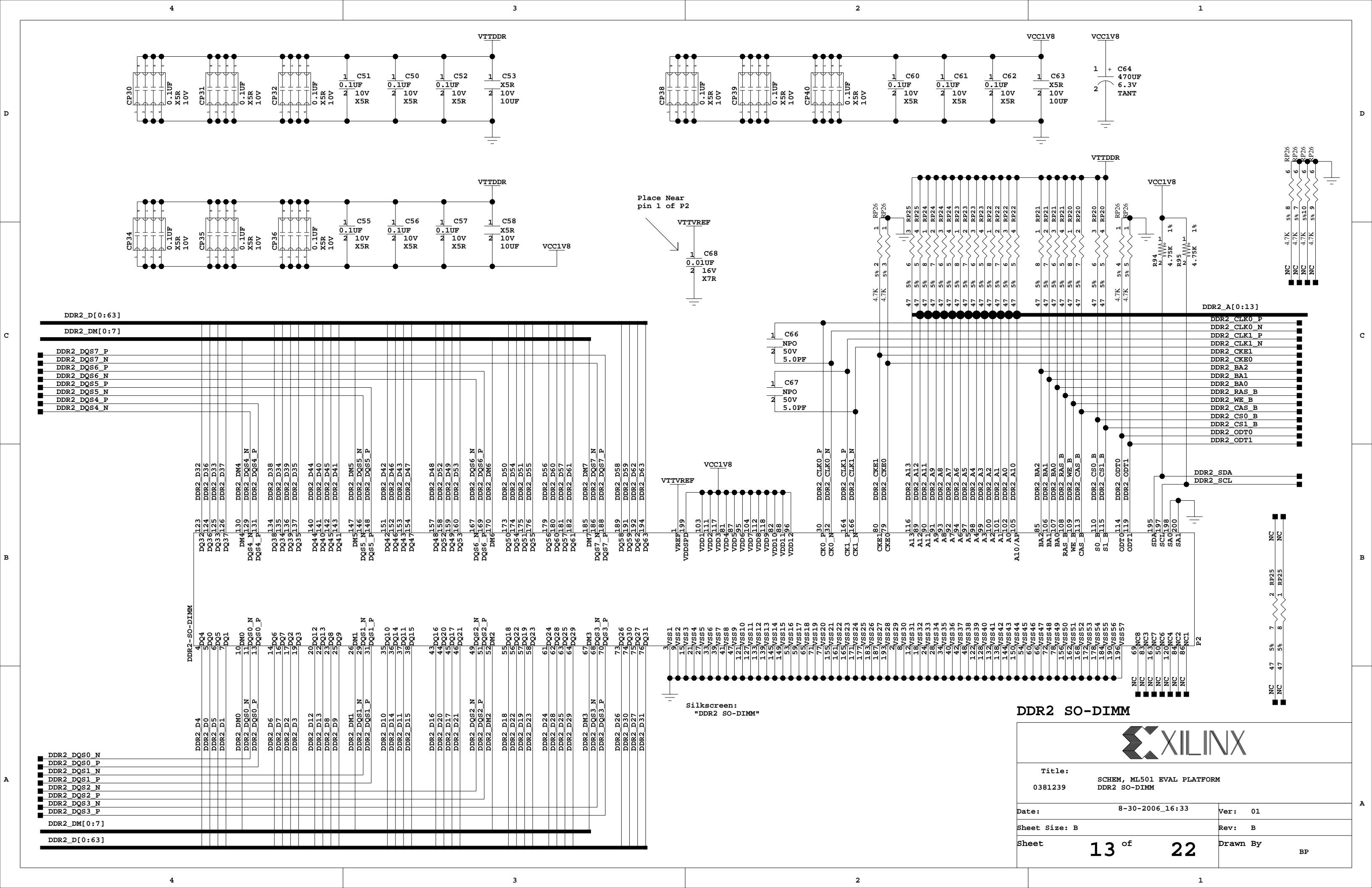
### DTE (Serial Host)



### Misc - LCD, PS2, UART, IIC EEPROM, Fan Cntlr



Title:		SCHEM, ML501 EVAL PLATFORM	
0381239		LCD, PS2, UART, IIC EEPROM	
		IIC Fan Controller	
Date:	9-6-2006_14:46	Ver:	01
Sheet Size:	B	Rev:	B
Sheet	12 of 22	Drawn By	BP

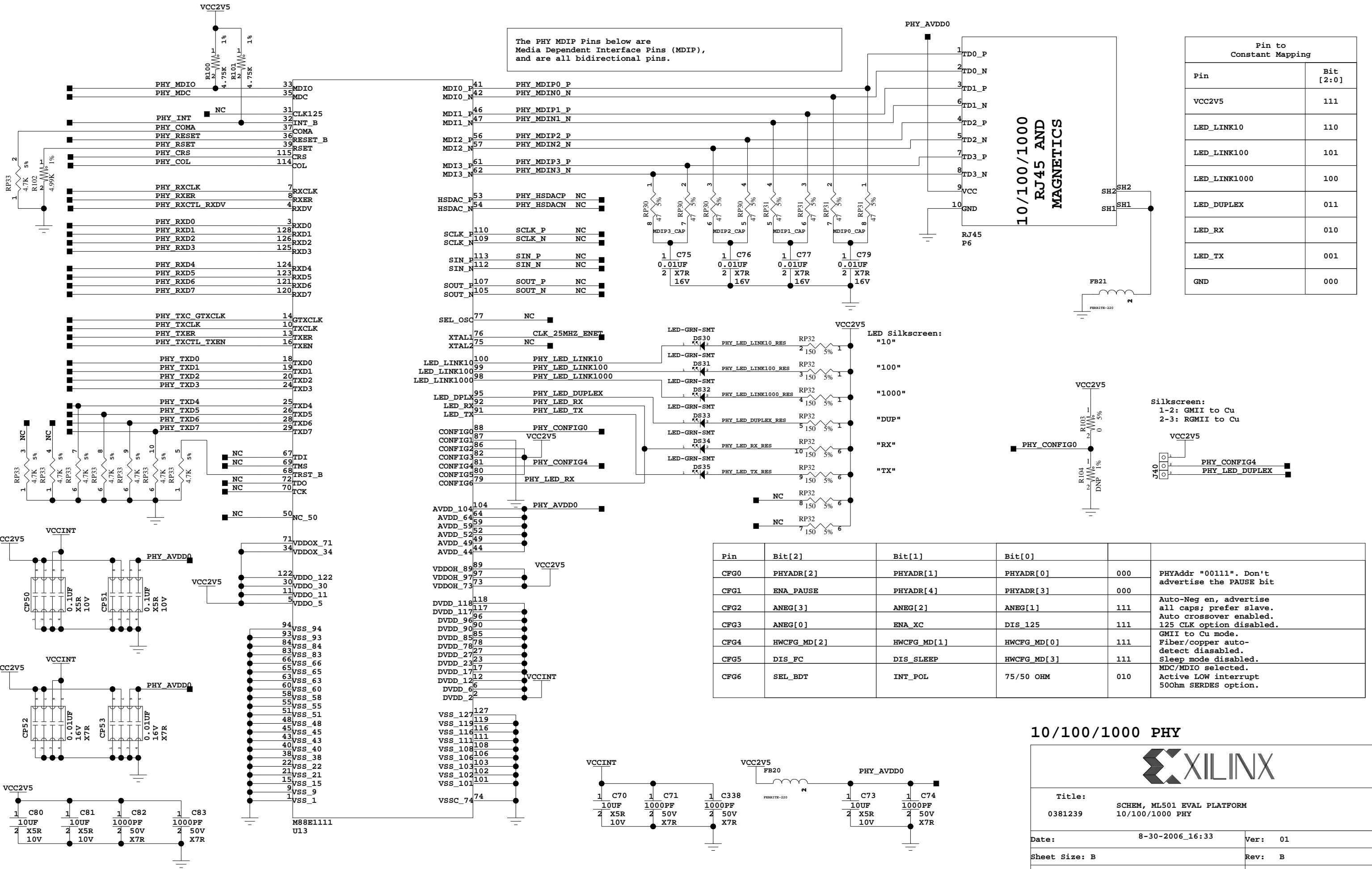


### DDR2 SO-DIMM



Title:		SCHEM, ML501 EVAL PLATFORM	
0381239		DDR2 SO-DIMM	
Date:	8-30-2006_16:33	Ver:	01
Sheet Size:	B	Rev:	B
Sheet	13 of 22	Drawn By	BP

The PHY MDIP Pins below are Media Dependent Interface Pins (MDIP), and are all bidirectional pins.



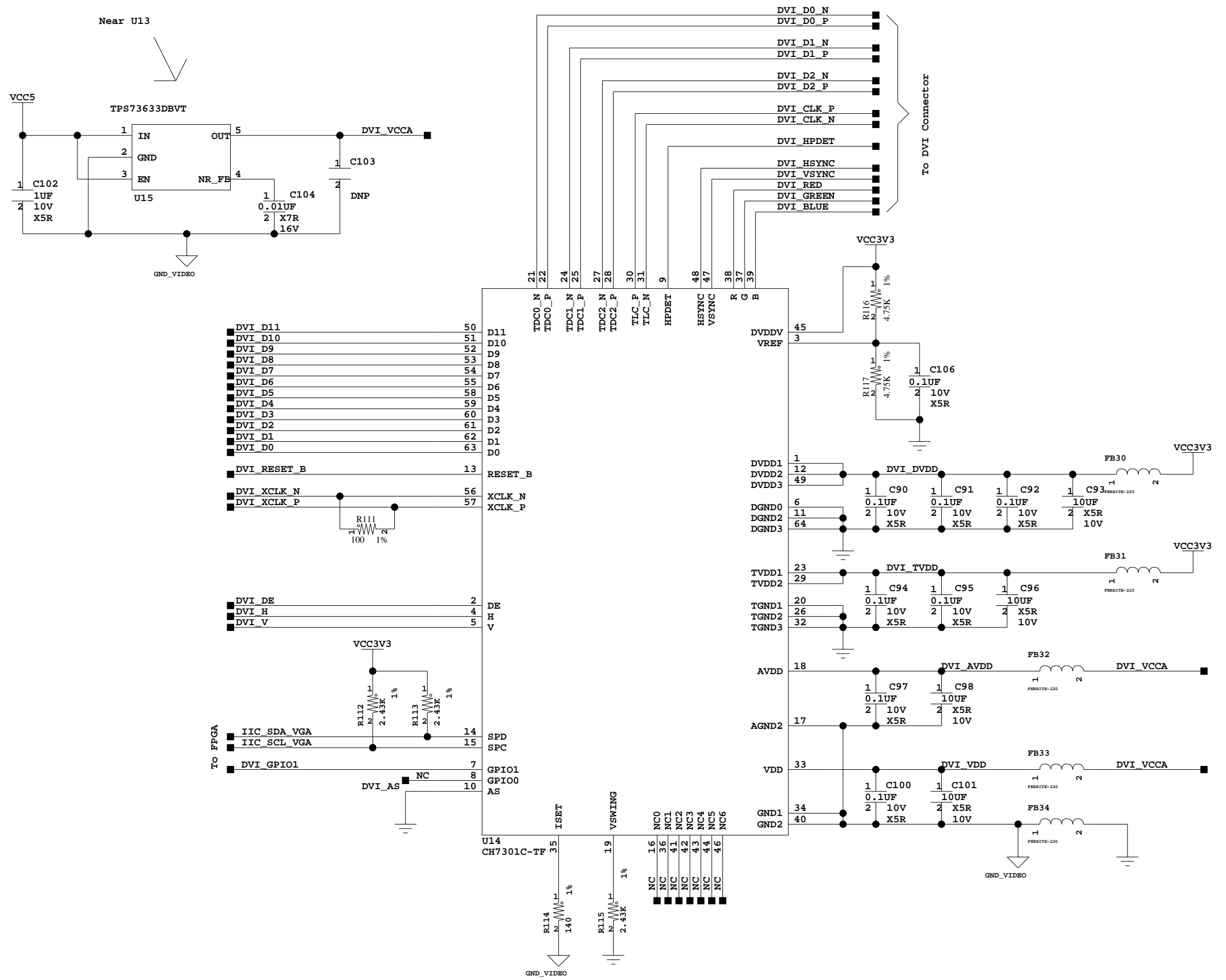
Pin to Constant Mapping	
Pin	Bit [2:0]
VCC2V5	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
GND	000

Pin	Bit[2]	Bit[1]	Bit[0]		
CFG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	000	PHYAddr "00111". Don't advertise the PAUSE bit
CFG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000	Auto-Neg en, advertise all caps; prefer slave. Auto crossover enabled. 125 CLK option disabled.
CFG2	ANEG[3]	ANEG[2]	ANEG[1]	111	GMII to Cu mode. Fiber/copper auto-detect disabled. Sleep mode disabled.
CFG3	ANEG[0]	ENA_XC	DIS 125	111	MDC/MDIO selected. Active LOW interrupt 500hm SERDES option.
CFG4	HWCFG MD[2]	HWCFG MD[1]	HWCFG MD[0]	111	
CFG5	DIS_FC	DIS_SLEEP	HWCFG MD[3]	111	
CFG6	SEL_BDT	INT_POL	75/50 OHM	010	

10/100/1000 PHY



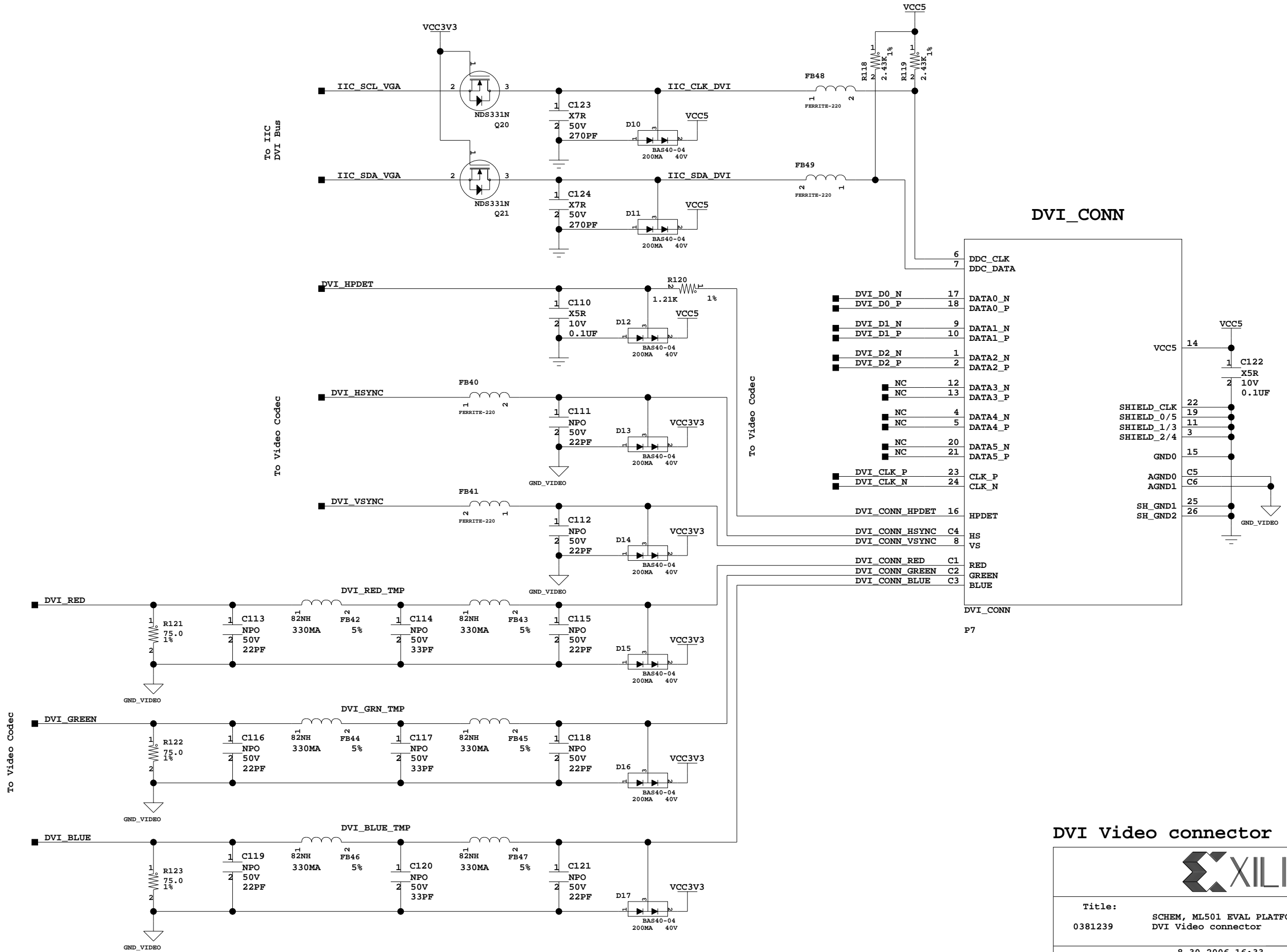
Title:		SCHEM, ML501 EVAL PLATFORM	
0381239		10/100/1000 PHY	
Date:	8-30-2006_16:33	Ver:	01
Sheet Size:	B	Rev:	B
Sheet	14 of 22	Drawn By	BP



DI Codec



Title:		SCHEM, ML501 EVAL PLATFORM	
0381239		DVI Codec	
Date:	8-30-2006_16:33	Ver:	01
Sheet Size:	B	Rev:	B
Sheet	15 of 22	Drawn By	BP



### DVI\_CONN

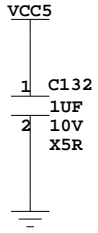
6	DDC_CLK	
7	DDC_DATA	
17	DATA0_N	DVI_D0_N
18	DATA0_P	DVI_D0_P
9	DATA1_N	DVI_D1_N
10	DATA1_P	DVI_D1_P
1	DATA2_N	DVI_D2_N
2	DATA2_P	DVI_D2_P
12	DATA3_N	NC
13	DATA3_P	NC
4	DATA4_N	NC
5	DATA4_P	NC
20	DATA5_N	NC
21	DATA5_P	NC
23	CLK_P	DVI_CLK_P
24	CLK_N	DVI_CLK_N
16	HPDET	DVI_CONN_HPDET
C4	HS	DVI_CONN_HSYNC
8	VS	DVI_CONN_VSYNC
C1	RED	DVI_CONN_RED
C2	GREEN	DVI_CONN_GREEN
C3	BLUE	DVI_CONN_BLUE

### DVI Video connector



Title:		SCHEM, ML501 EVAL PLATFORM	
0381239		DVI Video connector	
Date:	8-30-2006_16:33	Ver:	01
Sheet Size:	B	Rev:	B
Sheet	16 of 22	Drawn By	BP

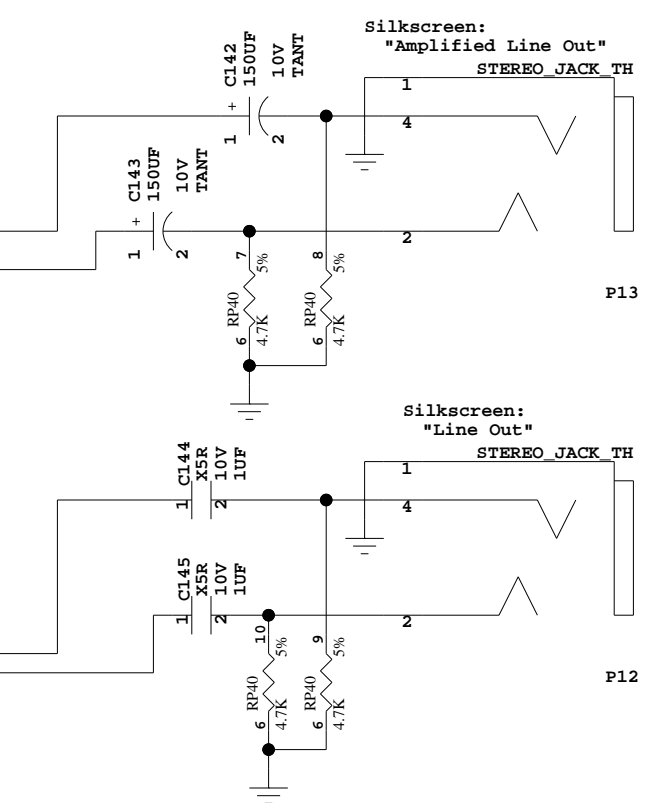
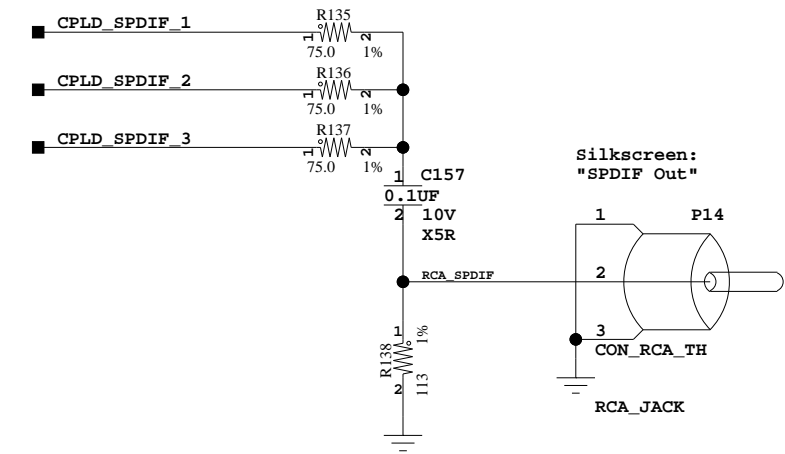
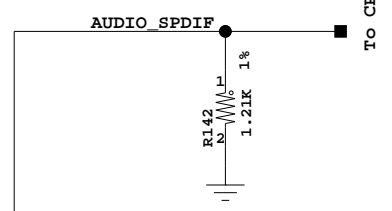
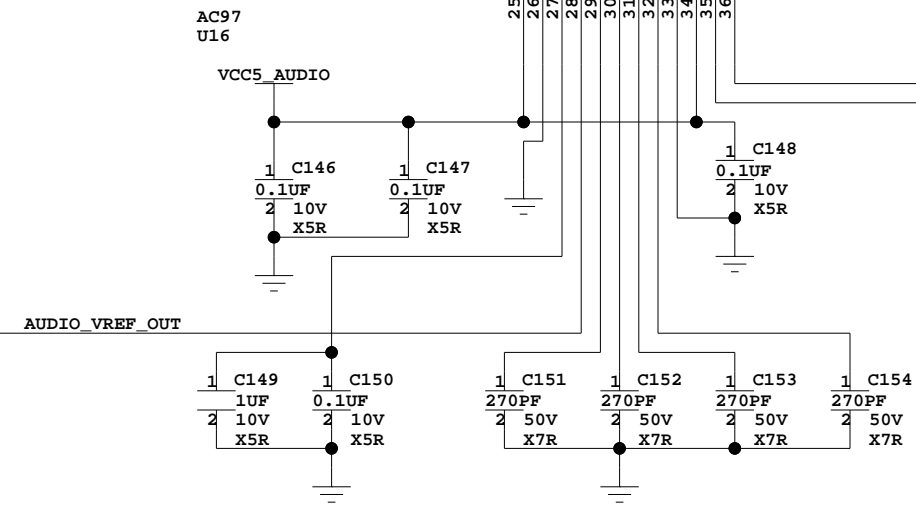
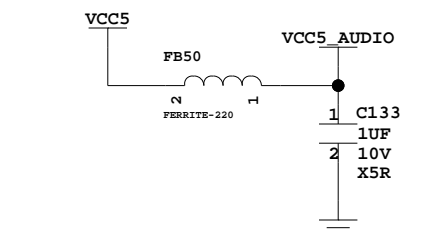
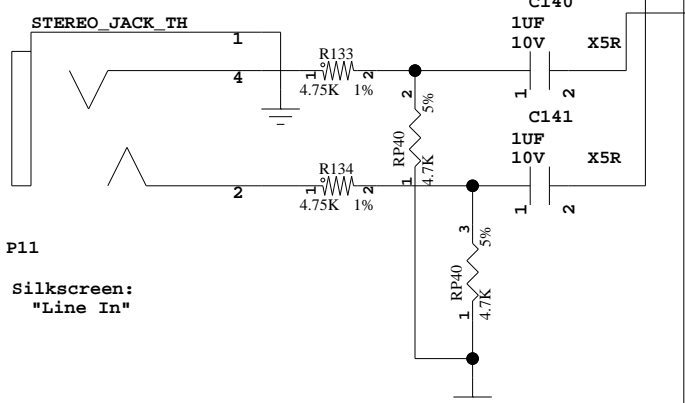
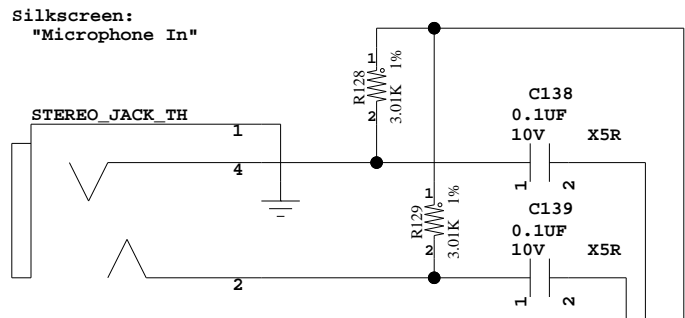
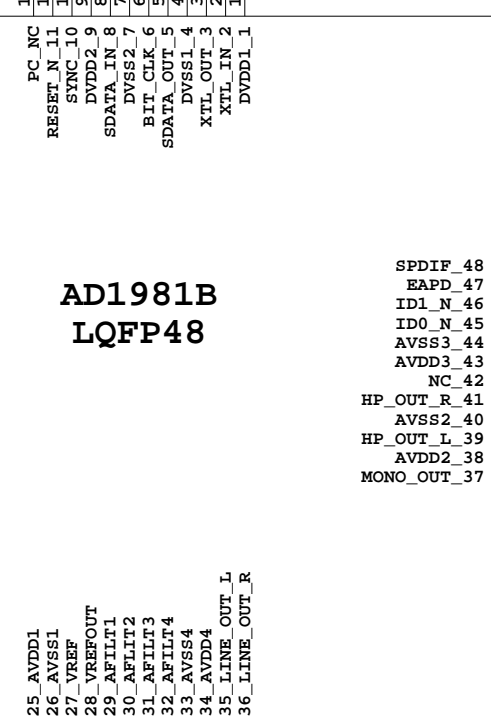
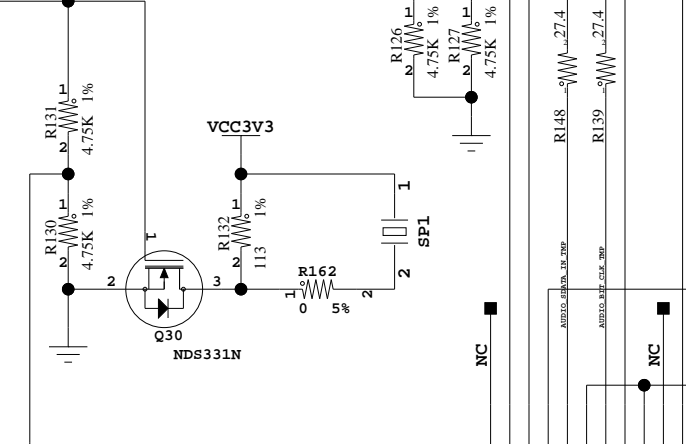




Portions of the design above this line are "Digital Ground", and should be outside the moat

Portions of the design below this line are "Analog Ground", and should be inside the moat

- CLK\_AUDIO
- AUDIO\_SDATA\_OUT
- AUDIO\_BIT\_CLK
- AUDIO\_SDATA\_IN
- AUDIO\_SYNC
- FLASH\_AUDIO\_RESET\_B
- PIEZO\_SPEAKER

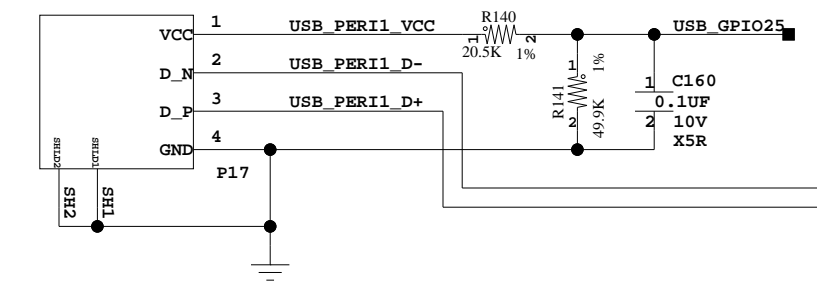


Audio Codec

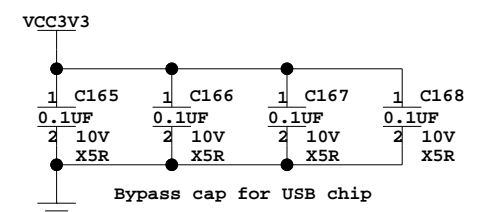
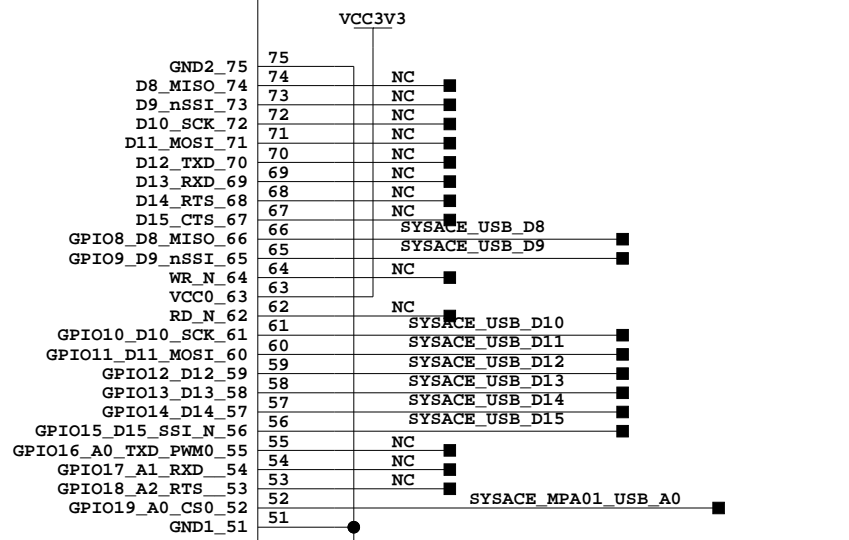
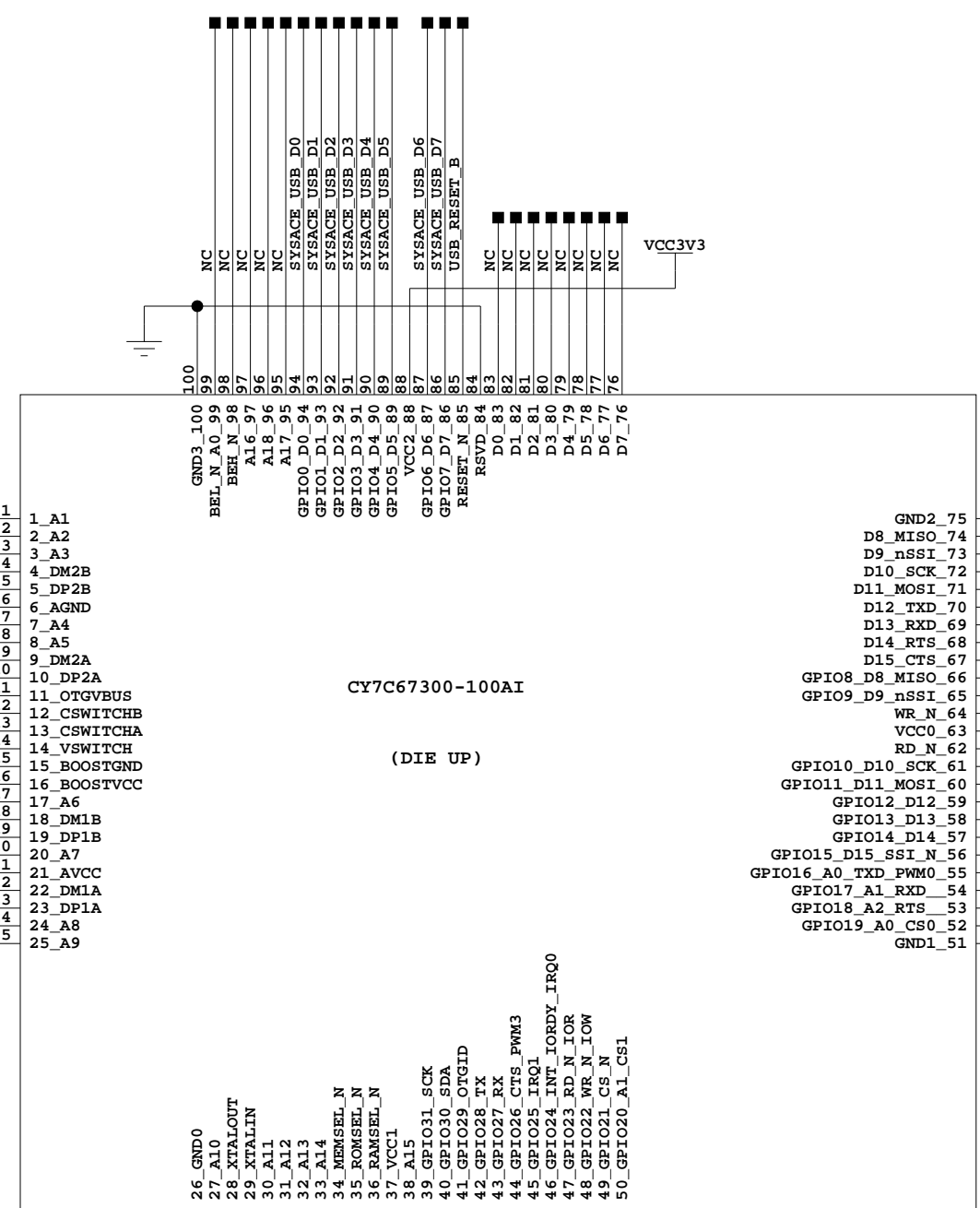
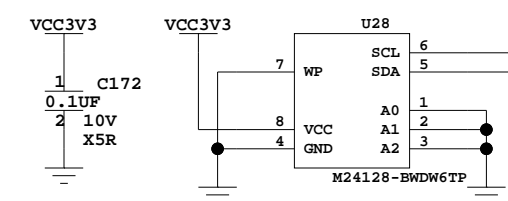
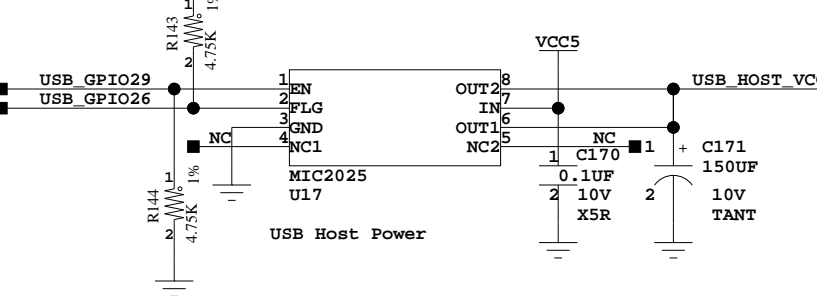
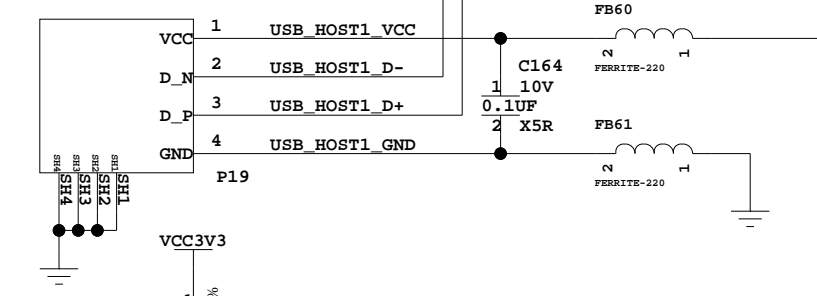


Title: 0381239		SCHEM, ML501 EVAL PLATFORM Audio Codec	
Date:	8-30-2006_16:33	Ver:	01
Sheet Size:	B	Rev:	B
Sheet	17 of 22	Drawn By	BP

Silkscreen:  
"USB Peripheral 1"



Silkscreen:  
"USB Host"



### USB Controller

Title: SCHEM, ML501 EVAL PLATFORM 0381239 USB Controller	
Date: 8-30-2006_16:33	Ver: 01
Sheet Size: B	Rev: B
Sheet 18 of 22	Drawn By BP

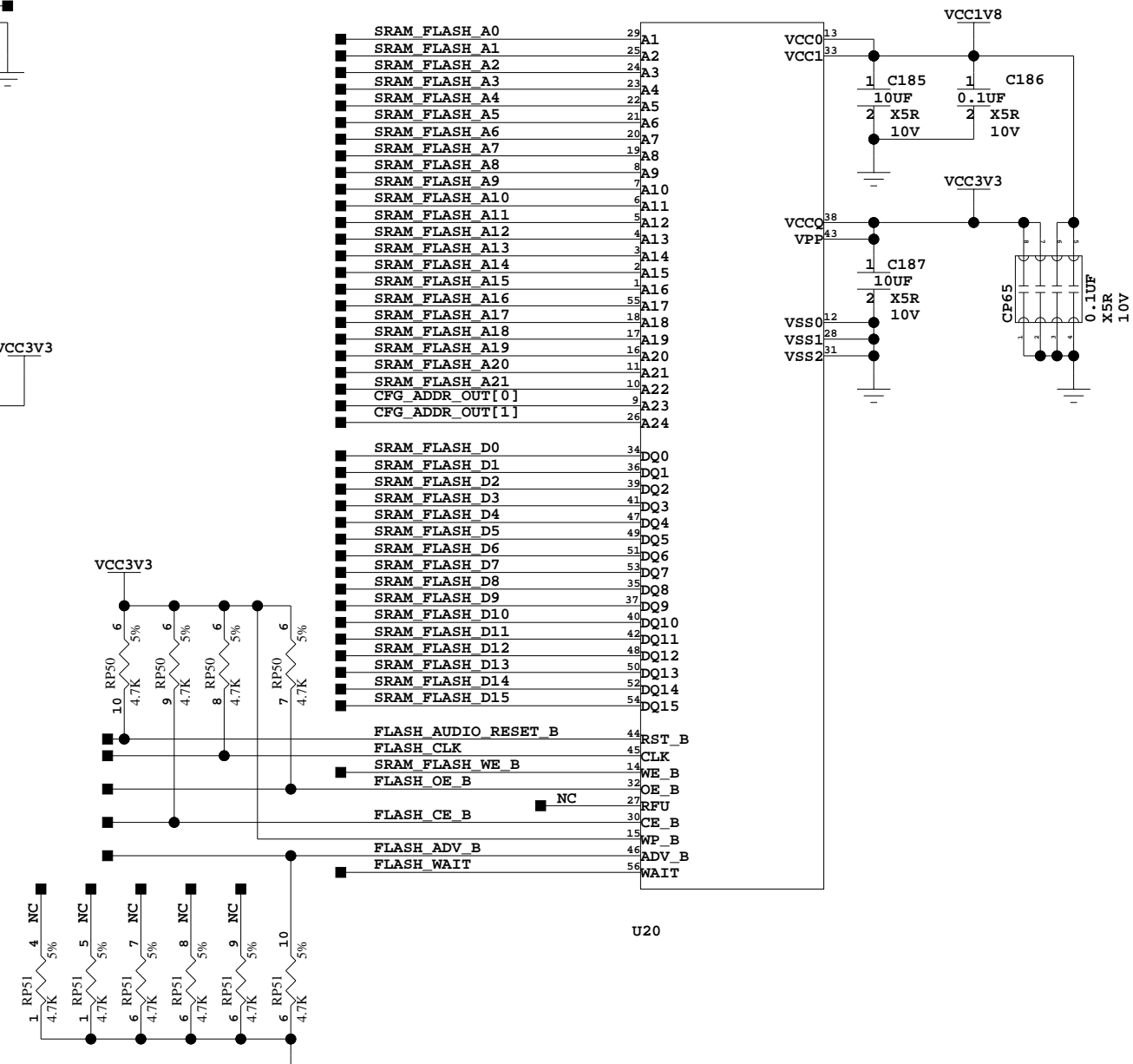
The burst order mode of the SRAM is set to "Linear" by default

Silkscreen:  
"Synchronous SRAM"  
"9 MBit - 36 X 256K"



SRAM\_ZBT\_256KX36  
U19

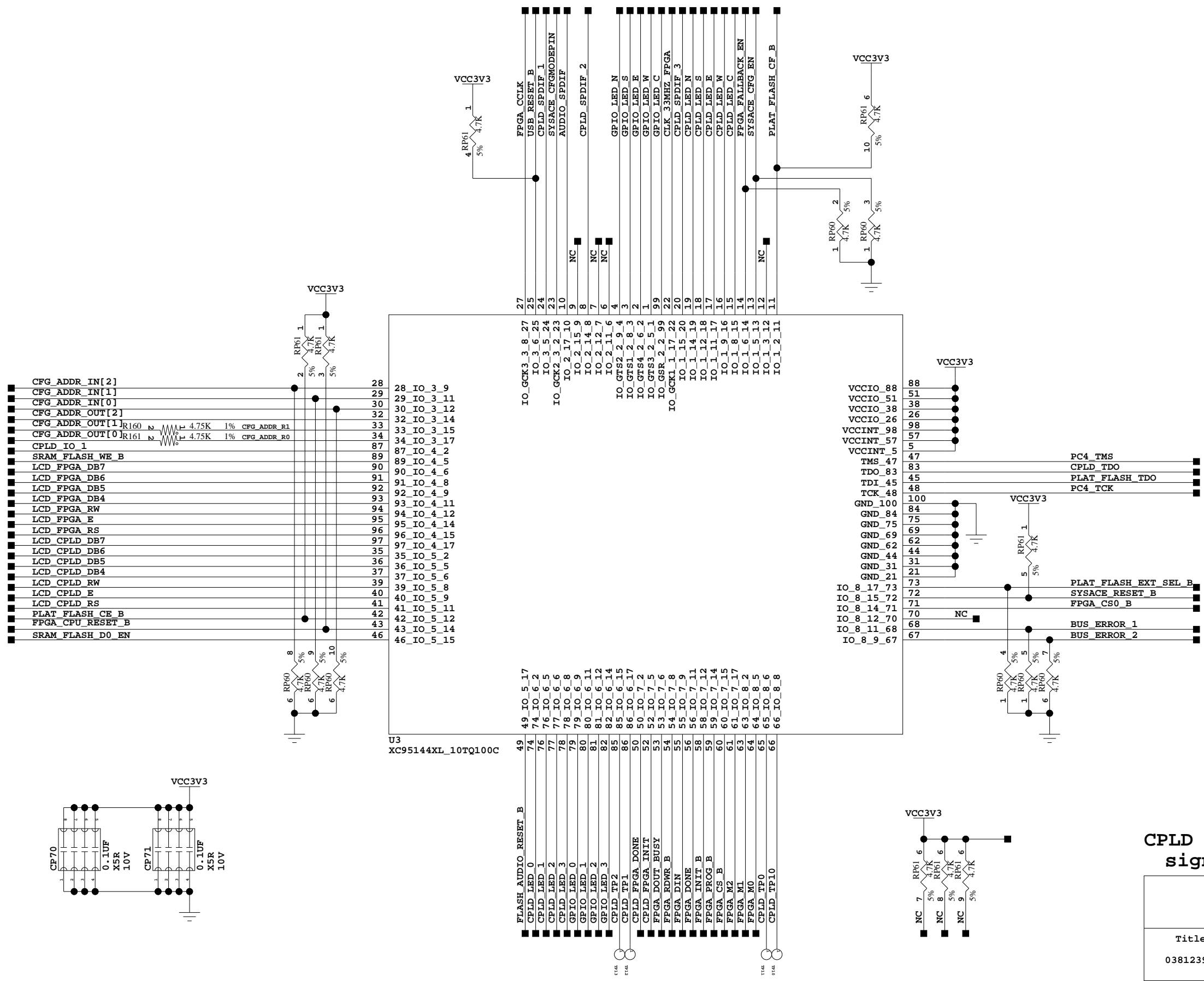
Silkscreen:  
"Strata FLASH"  
"256 MBit"



Memory:  
Synchronous SRAM,  
Strata FLASH



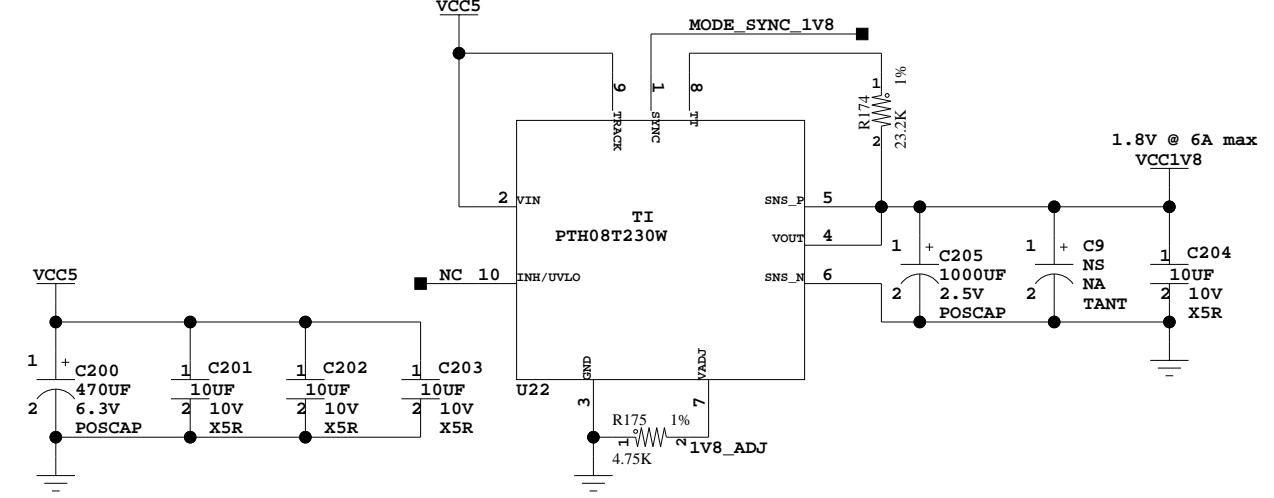
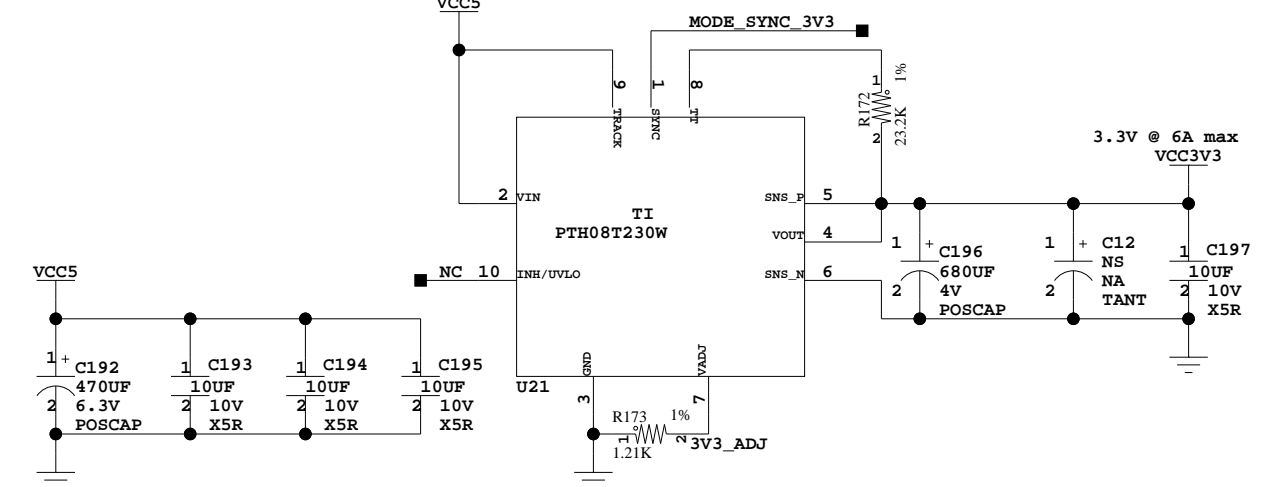
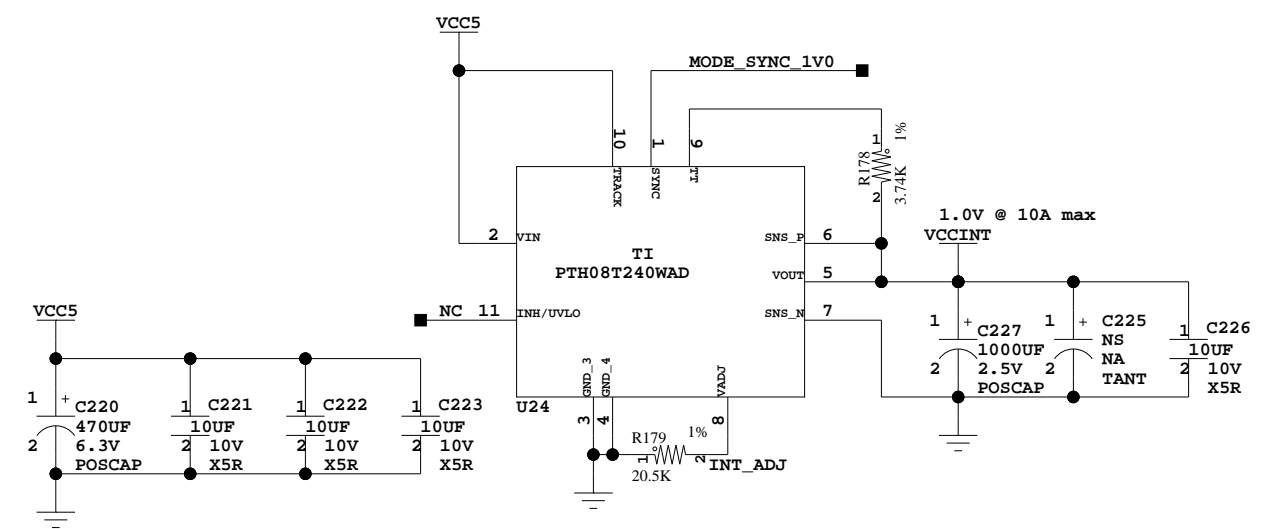
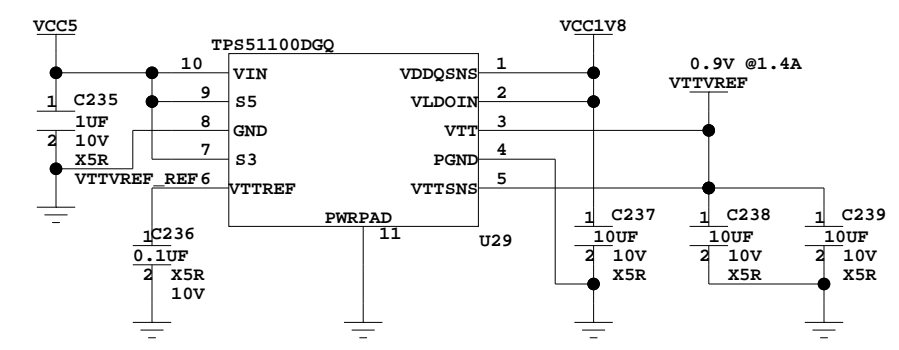
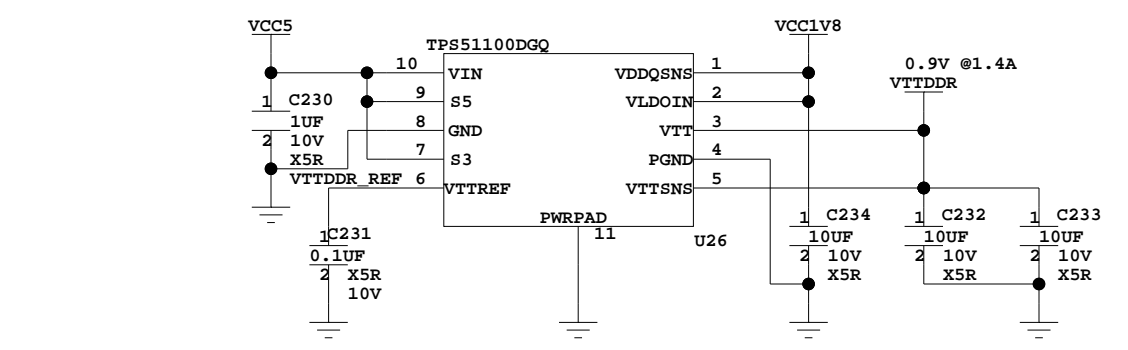
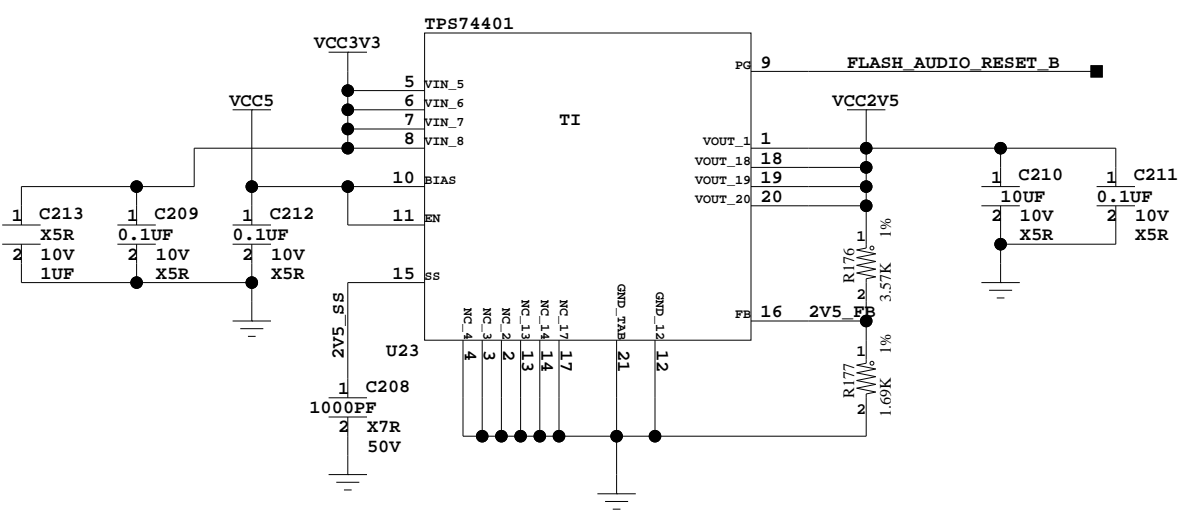
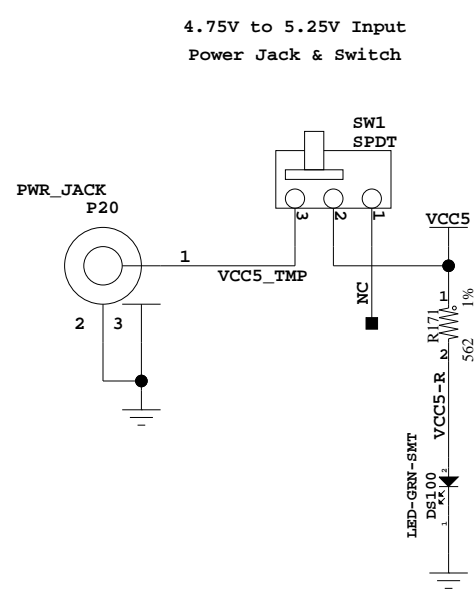
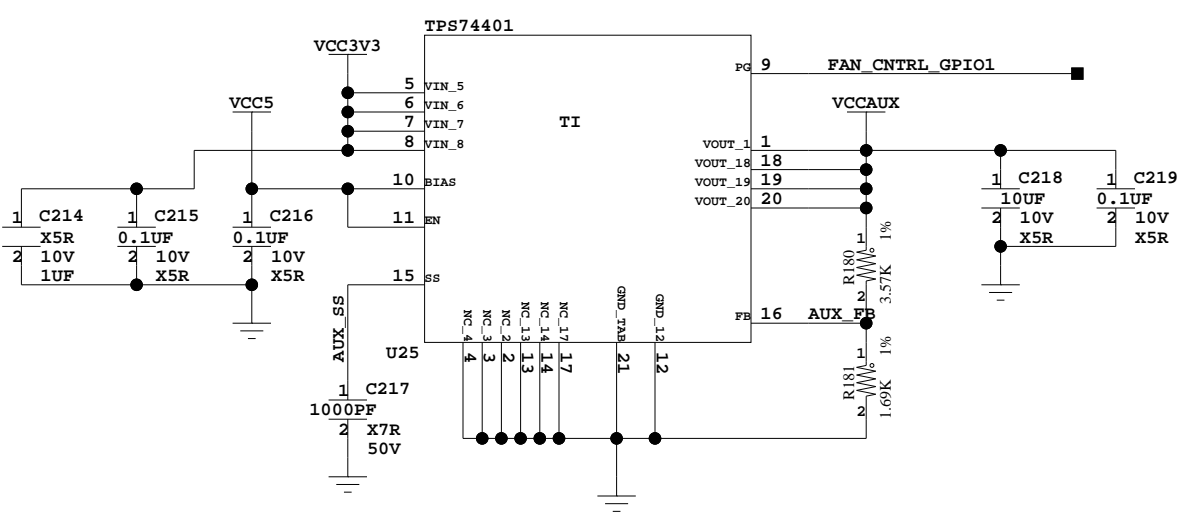
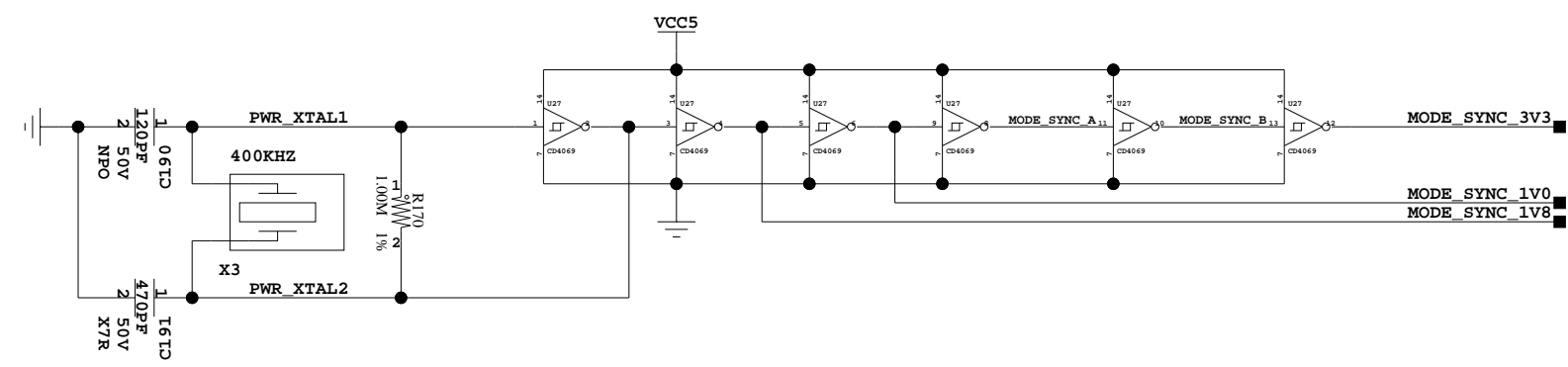
Title: 0381239		SCHEM, ML501 EVAL PLATFORM Sync. SRAM, FLASH	
Date:	8-30-2006_16:33	Ver:	01
Sheet Size:	B	Rev:	B
Sheet	19 of 22	Drawn By	BP



CPLD - Misc  
signal control



Title:		SCHEM, ML501 EVAL PLATFORM	
0381239		CPLD - Misc signal control	
Date:	8-30-2006_16:33	Ver:	01
Sheet Size:	B	Rev:	B
Sheet	20 of 22	Drawn By	BP

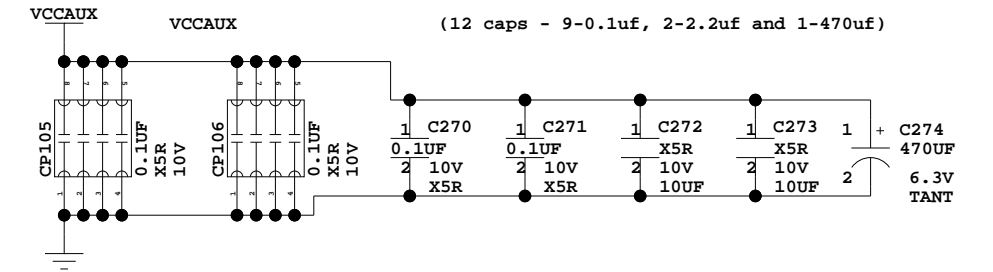
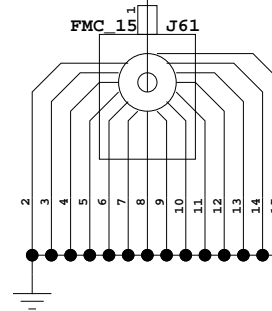
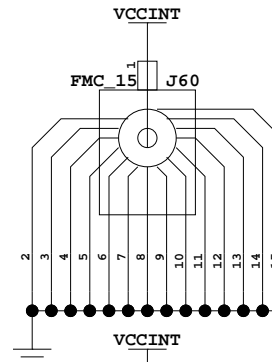
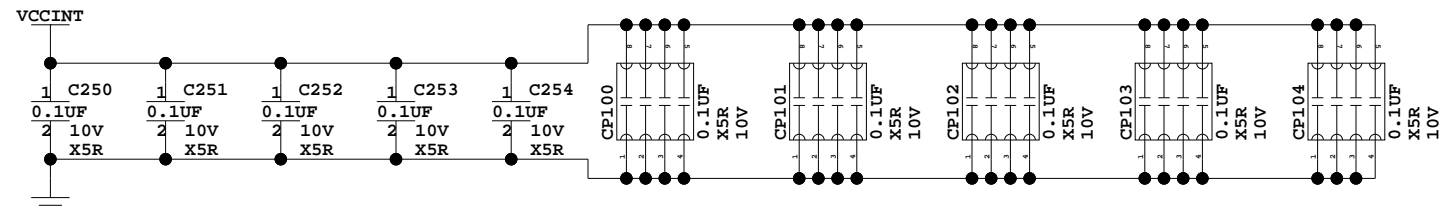
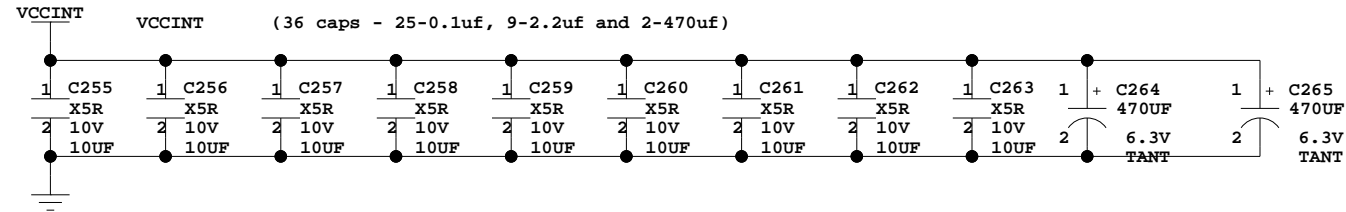


**Power Supplies**

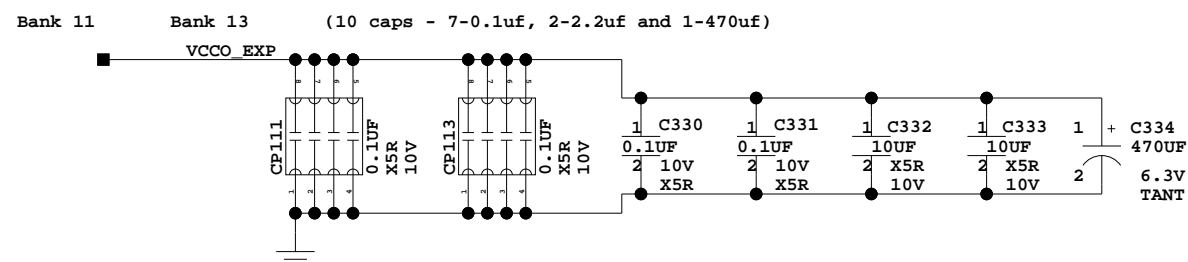
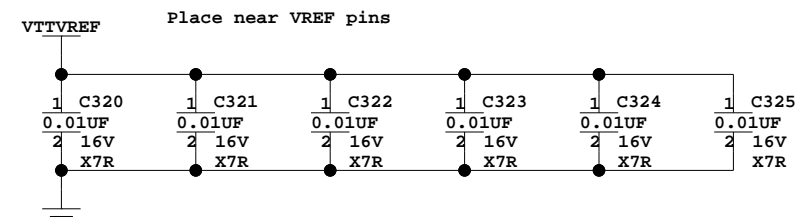
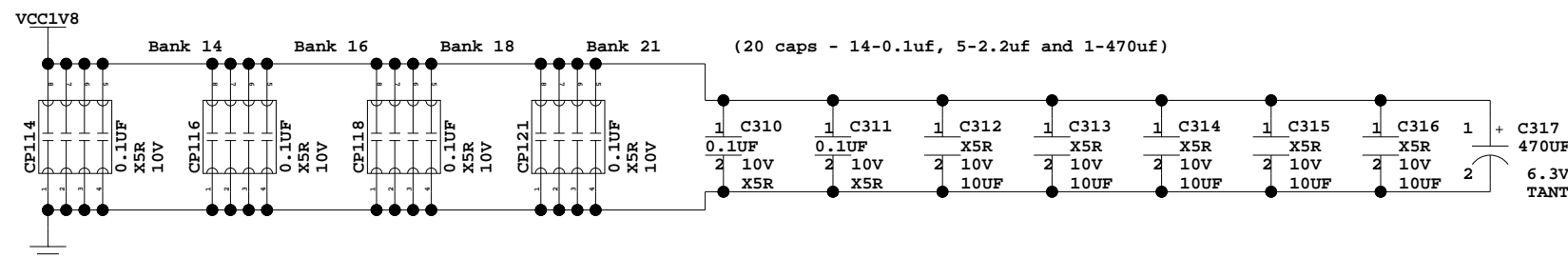
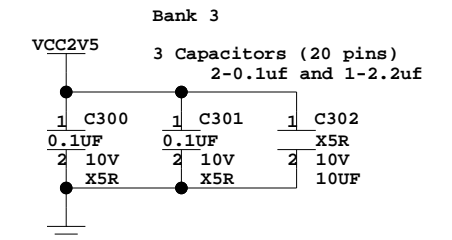
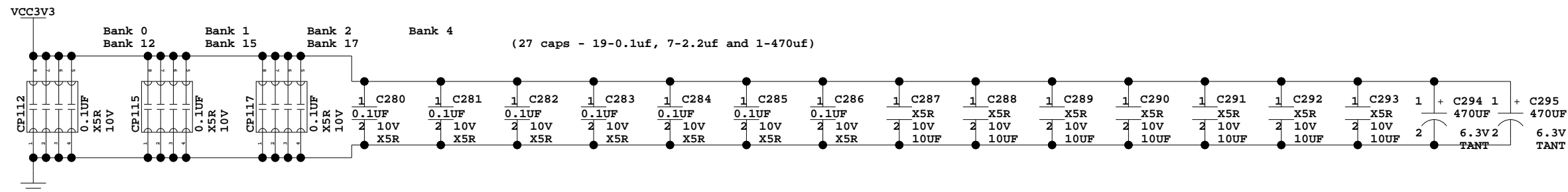


Title: 0381239		SCHEM, ML501 EVAL PLATFORM Power Supplies	
Date:	8-30-2006_16:33	Ver:	01
Sheet Size:	B	Rev:	B
Sheet	21 of 22	Drawn By	BP

### VCCINT Caps



### VCCO Caps



Title:		SCHEM, ML501 EVAL PLATFORM FPGA Decoupling	
Date:	8-30-2006_16:33	Ver:	01
Sheet Size:	B	Rev:	B
Sheet	22 of 22	Drawn By	BP