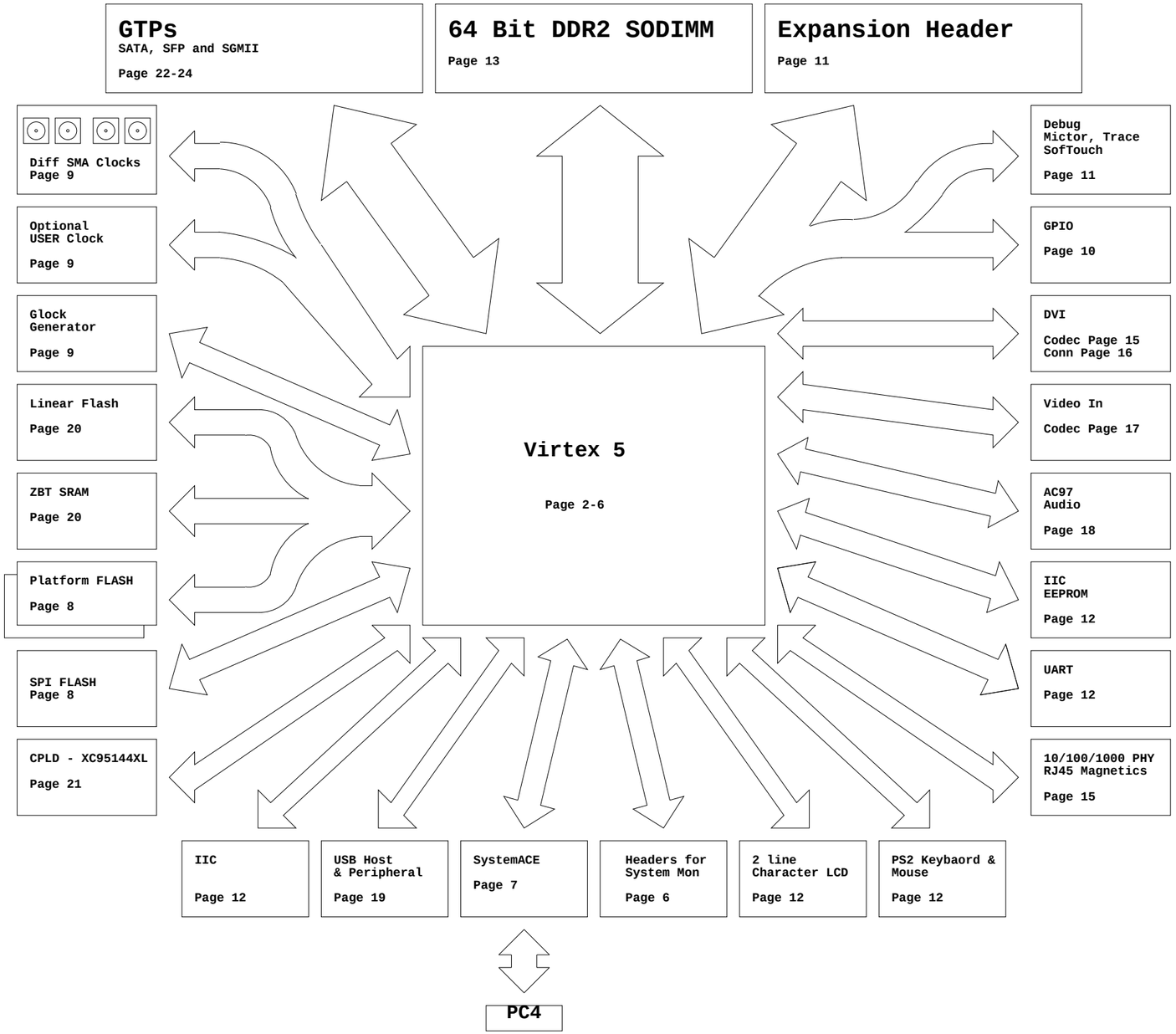

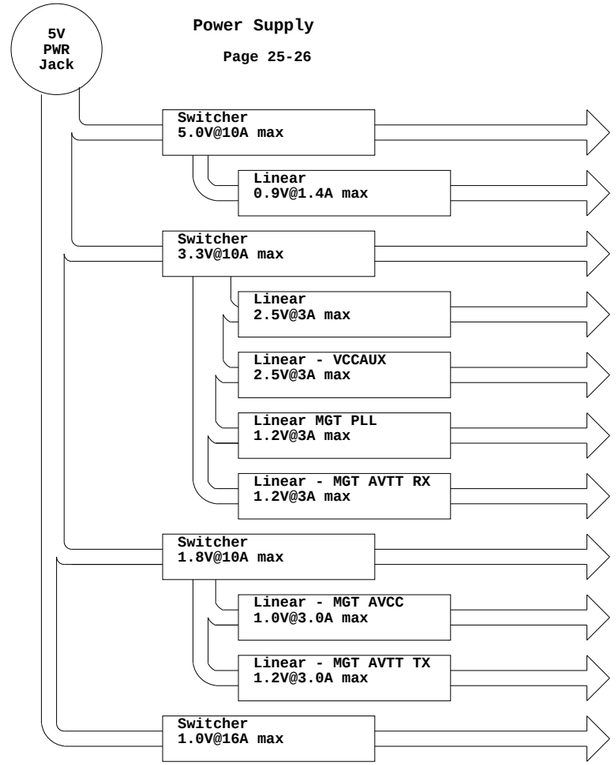

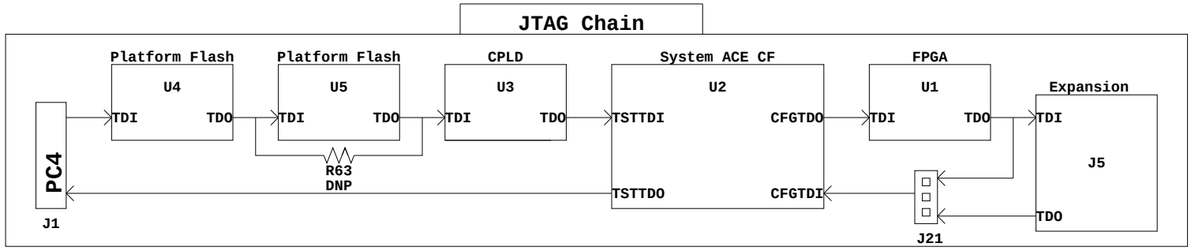

XILINX

Title:	ML505 Block Diagram SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	12-5-2006_10:49	Ver:	02
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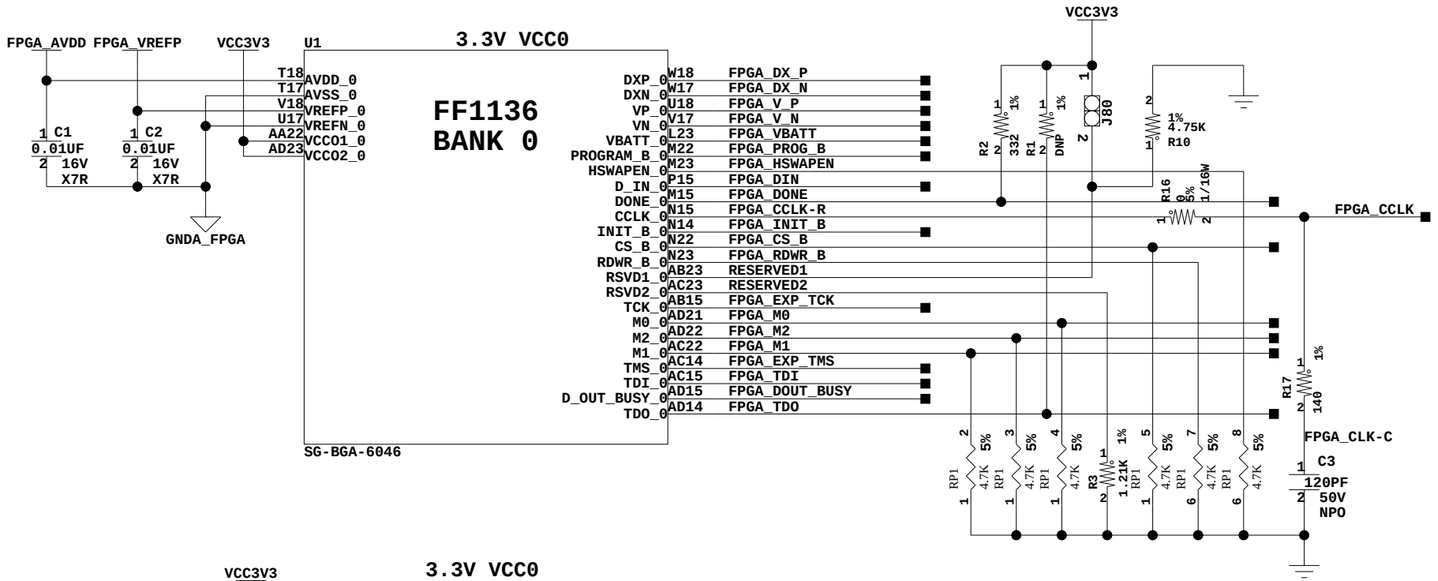
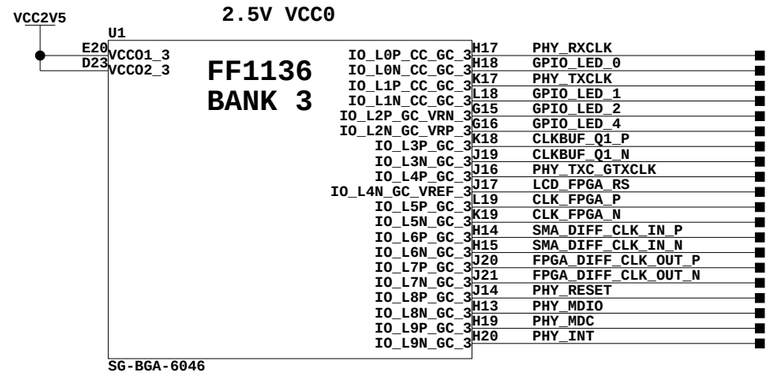
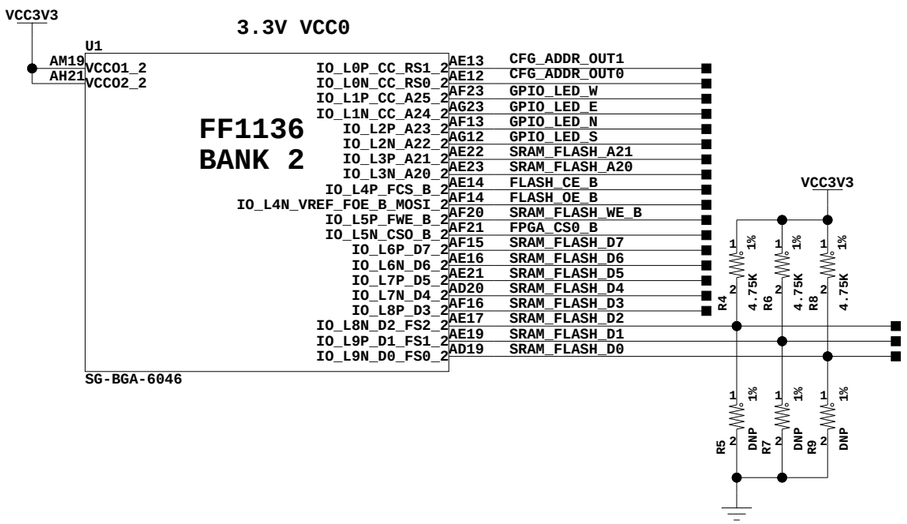
Sheet	1 of 27	Drawn By	BP



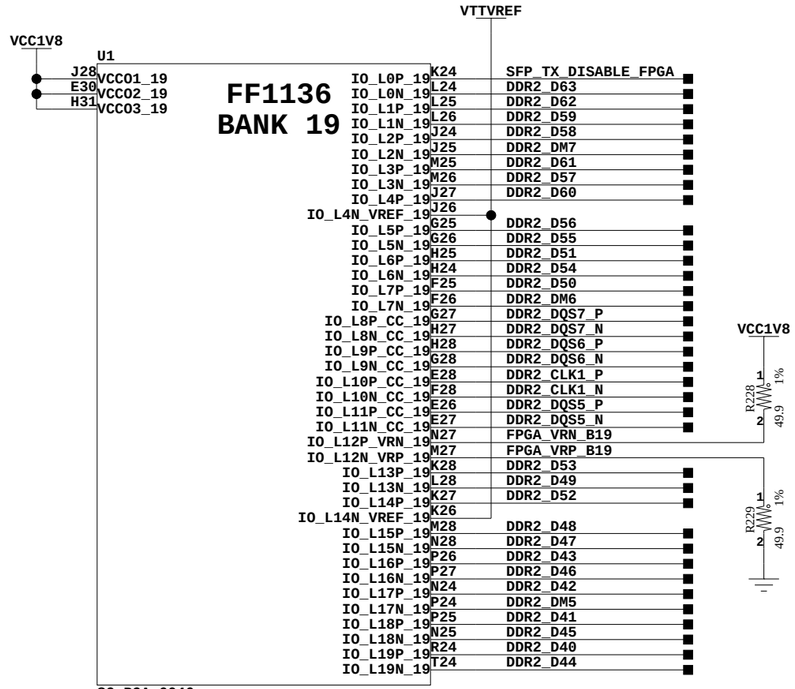


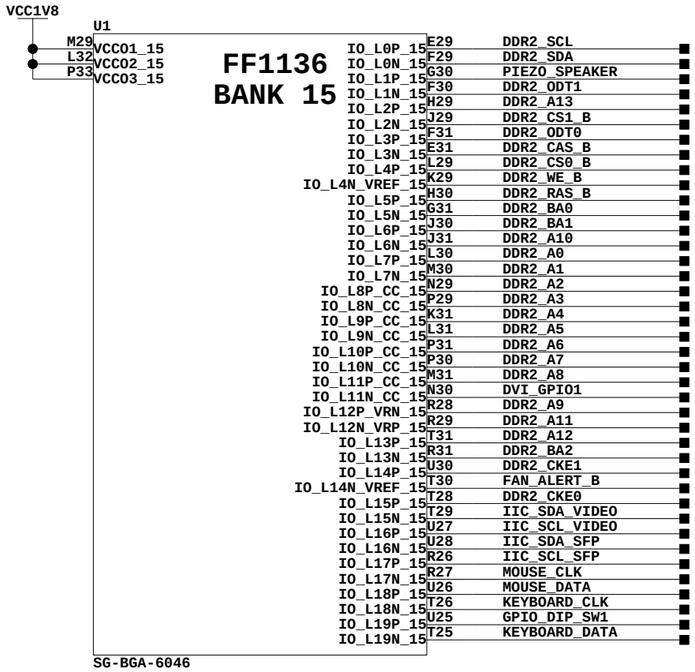


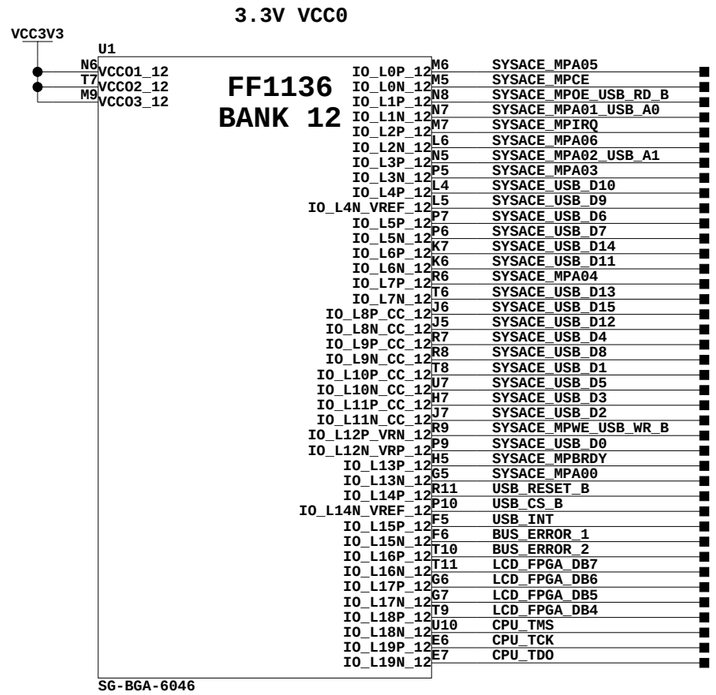
Banks 0,1,2,3,4
Config, FLASH, SRAM, GPIO, CLKs

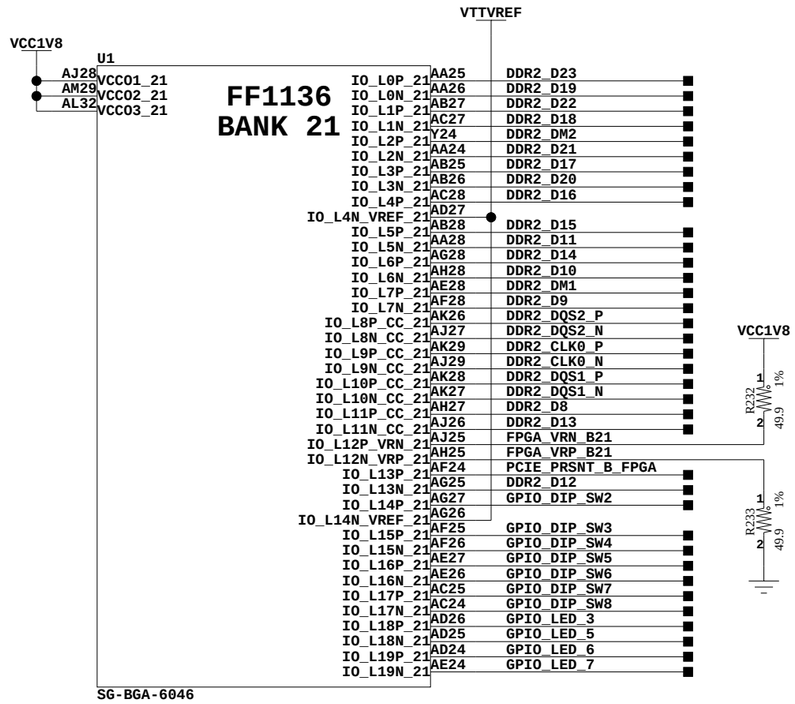
XILINX

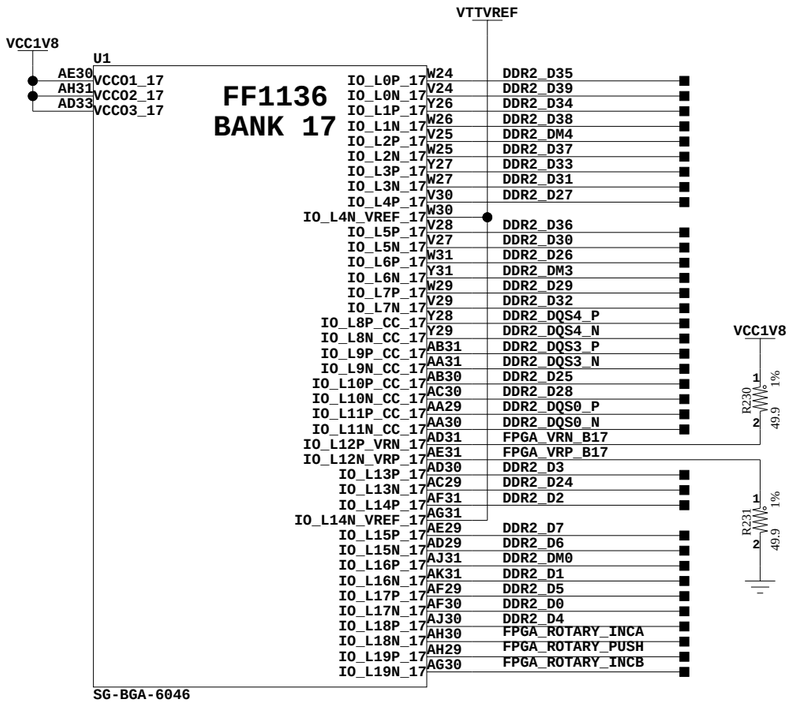
Title:	FPGA Banks 0,1,2,3,4 Config, FLASH, SRAM, GPIO, CLKs SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	12-5-2006_10:49	Ver:	02
Sheet Size: B		Rev:	A
Sheet	2 of 27	Drawn By	BP











Banks 14,16,18,21
DDR2, PS2, GPIO

Title:	FPGA Bank 14, 16, 18, 21DDR2, PS2, GPIO SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	12-5-2006_10:49	Ver:	02
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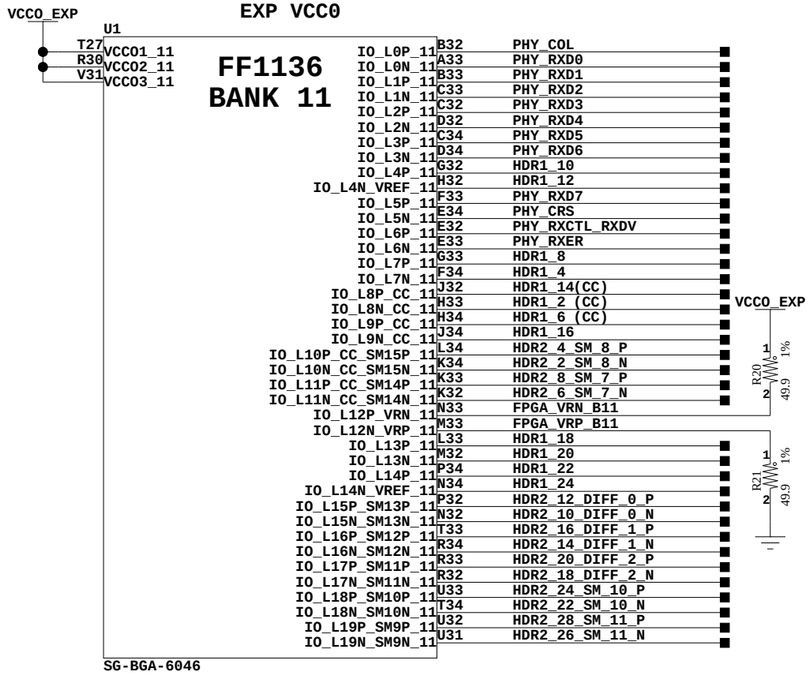

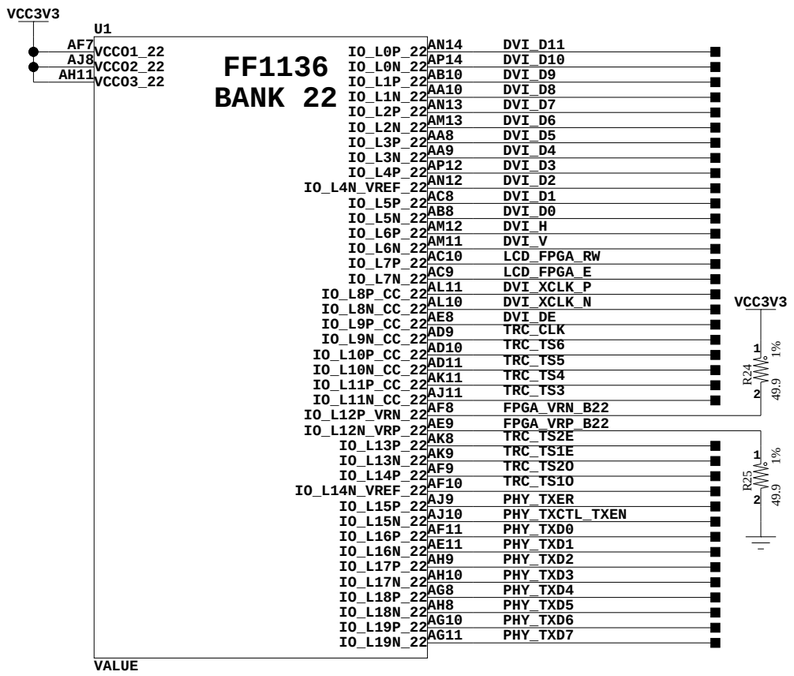

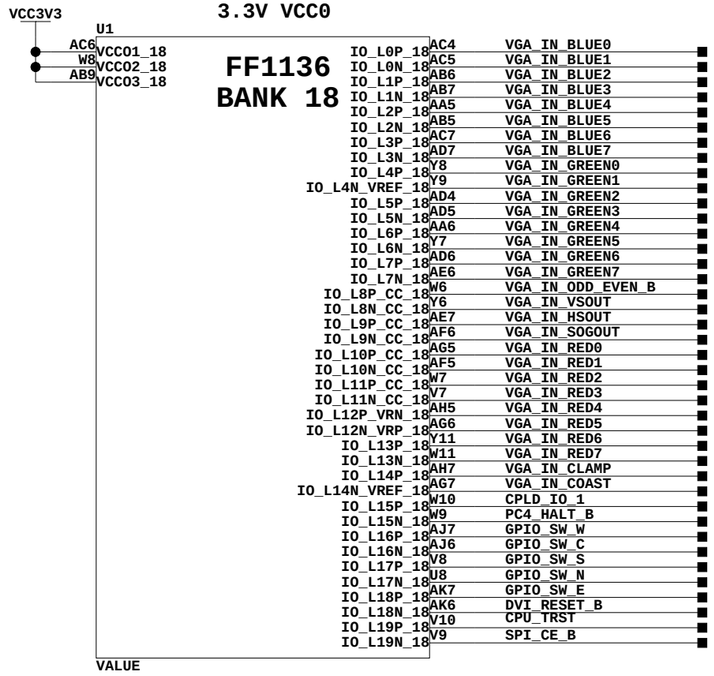

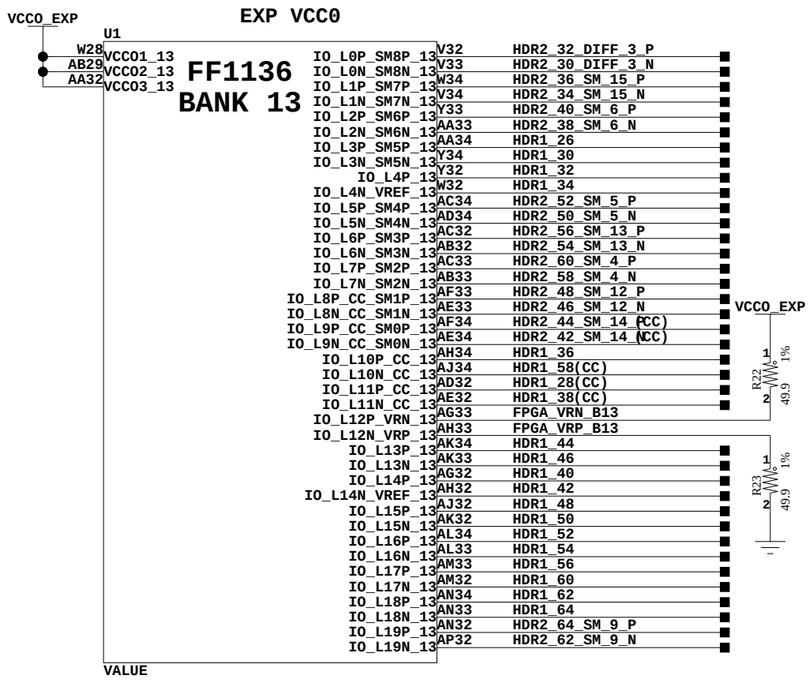

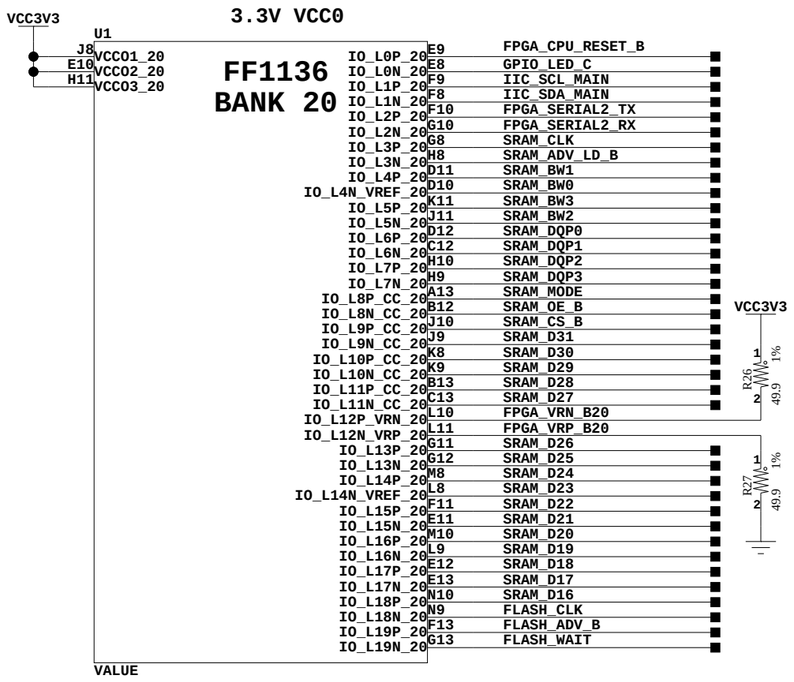

Banks 11,12,13
Sys ACE, XGI, PHY, LCD

XILINX

Title:	Banks 11,12,13 Sys ACE, XGI, PHY, LCD SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
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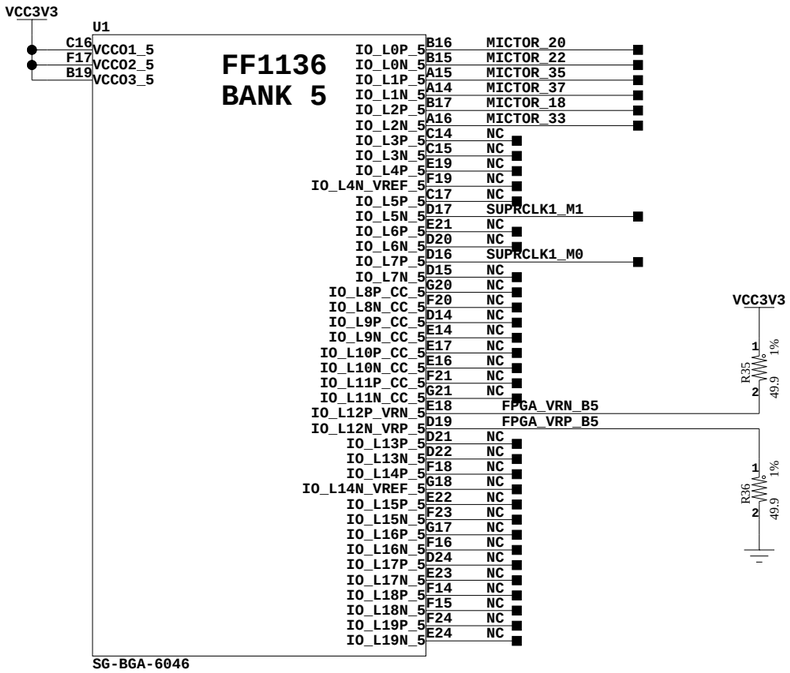
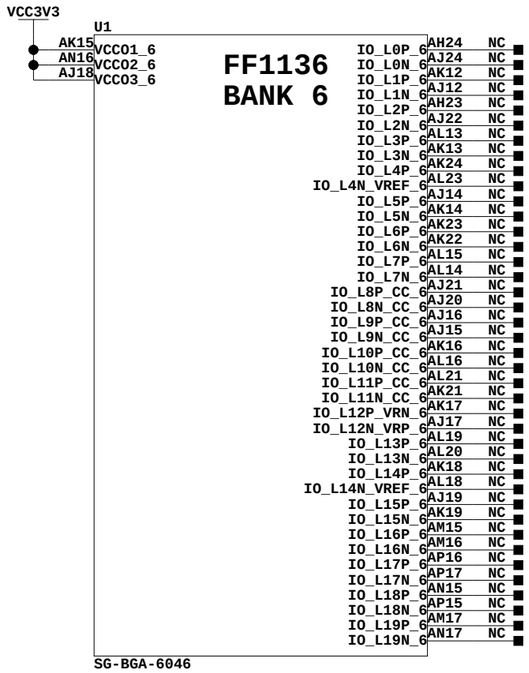
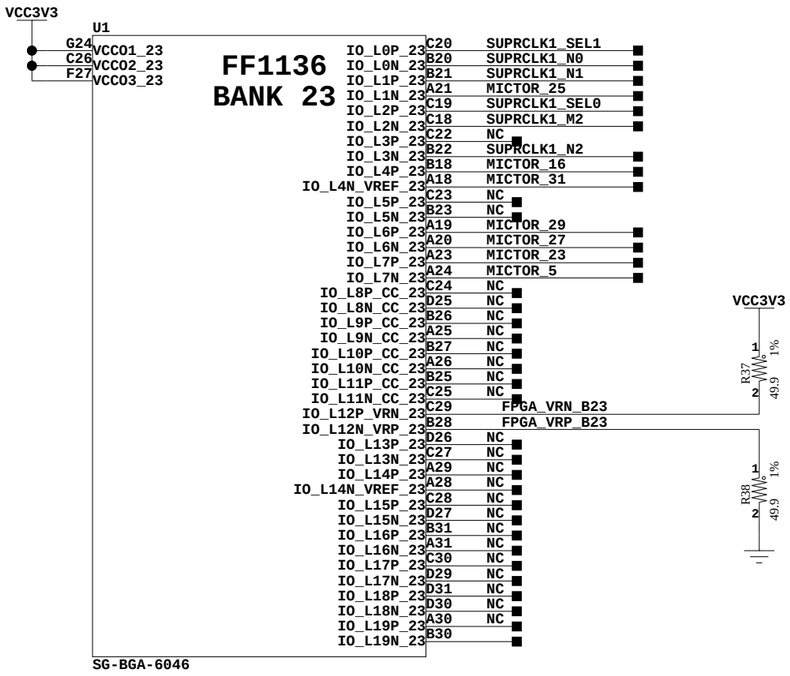
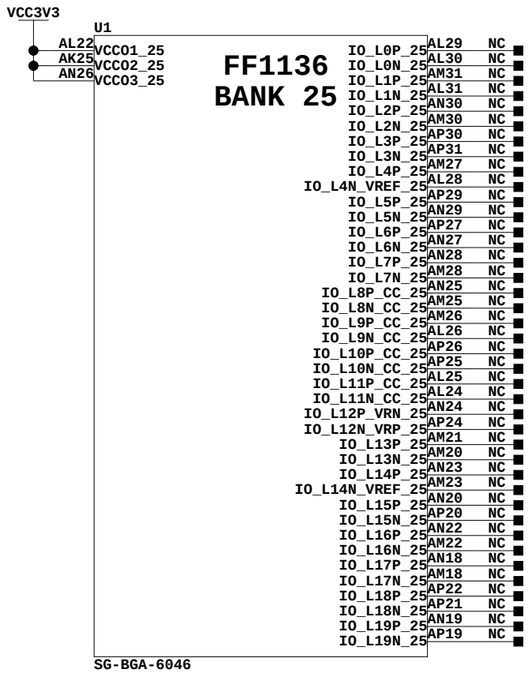
Unused banks on the LX50T and SX50T









Banks 15, 17
VGA, IIC, PHY
SRAM, FLASH, GPIO

XILINX

Title:	Banks 11,12,13 VGA, IIC, PHY, SRAM, GPIO SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	12-5-2006_10:49	Ver:	02
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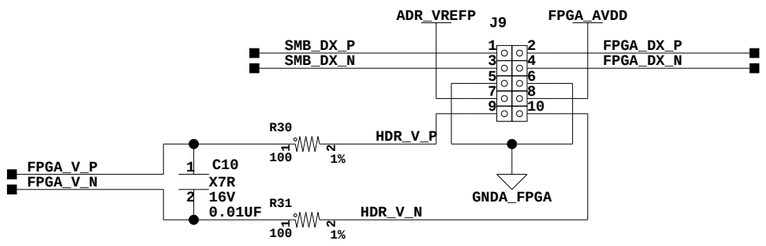
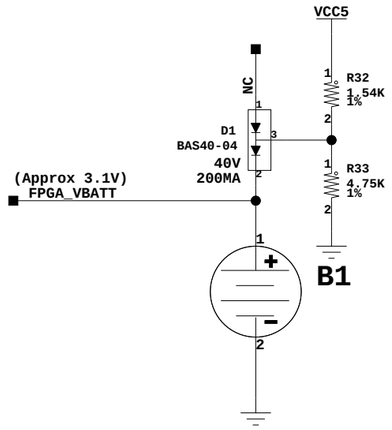
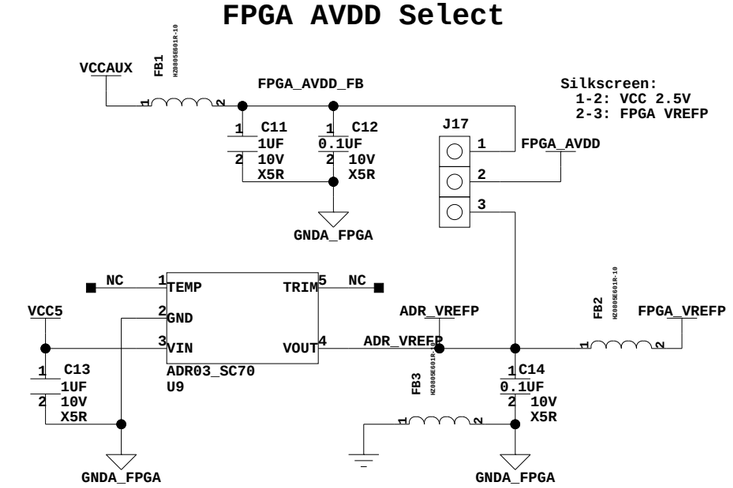
System Monitor Header

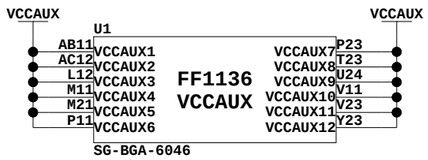


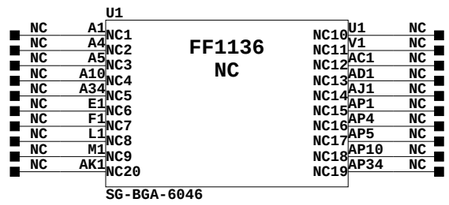
Rechargeable Battery

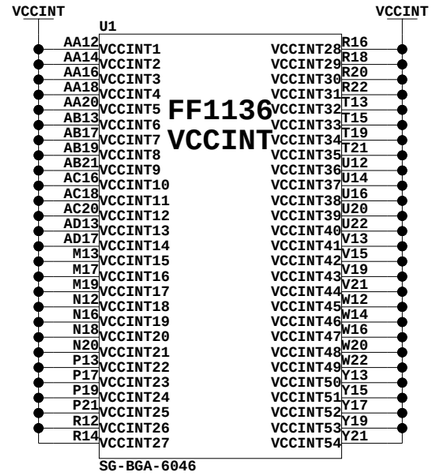


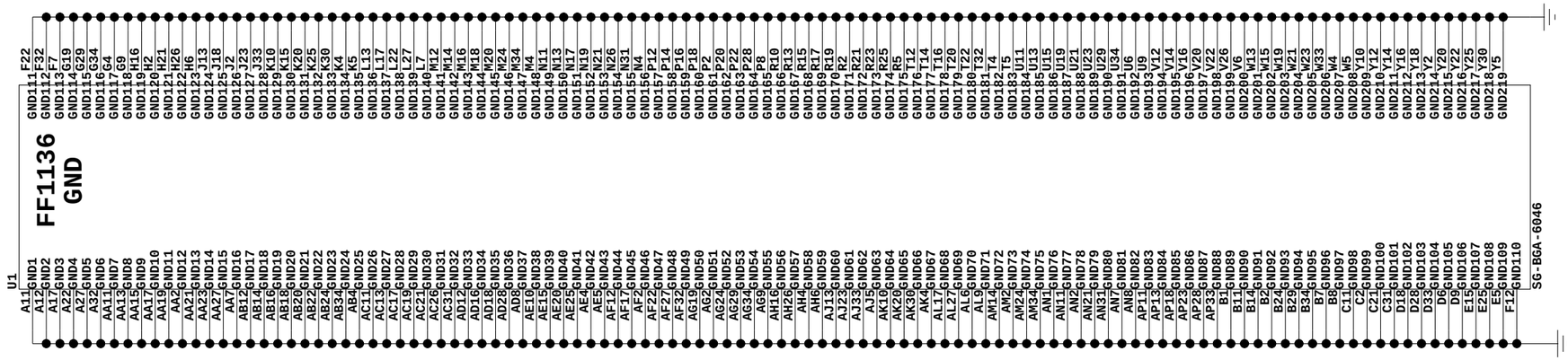
FPGA AVDD Select











Power and Misc FPGA Banks VCCINT, VCCAUX, NCs, GND Battery and System Moniter

Title:	FPGA Misc, VCCINT, VCCAUX, GND, Sys Mon SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	12-5-2006_10:49	Ver:	02
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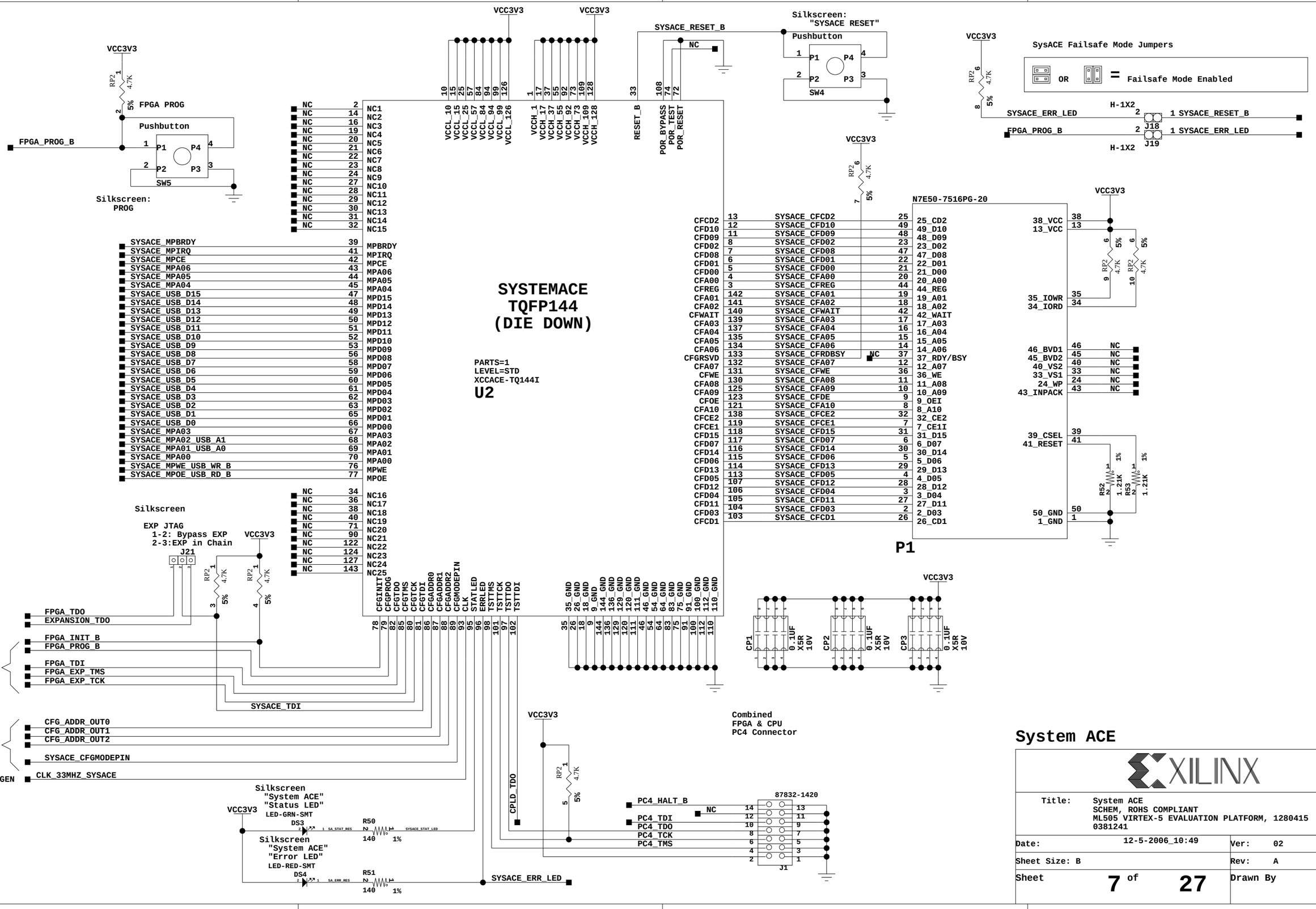

System ACE

Title:	System ACE SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	12-5-2006_10:49	Ver:	02
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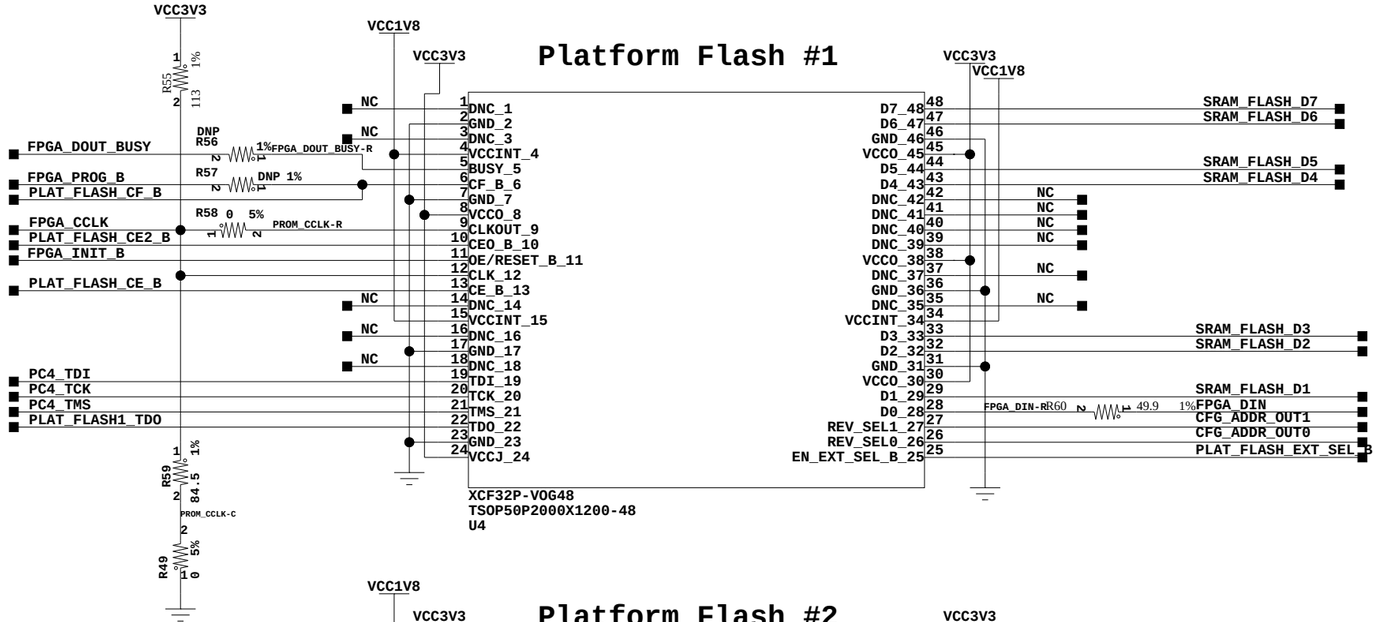
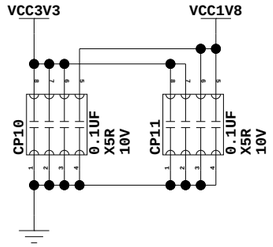
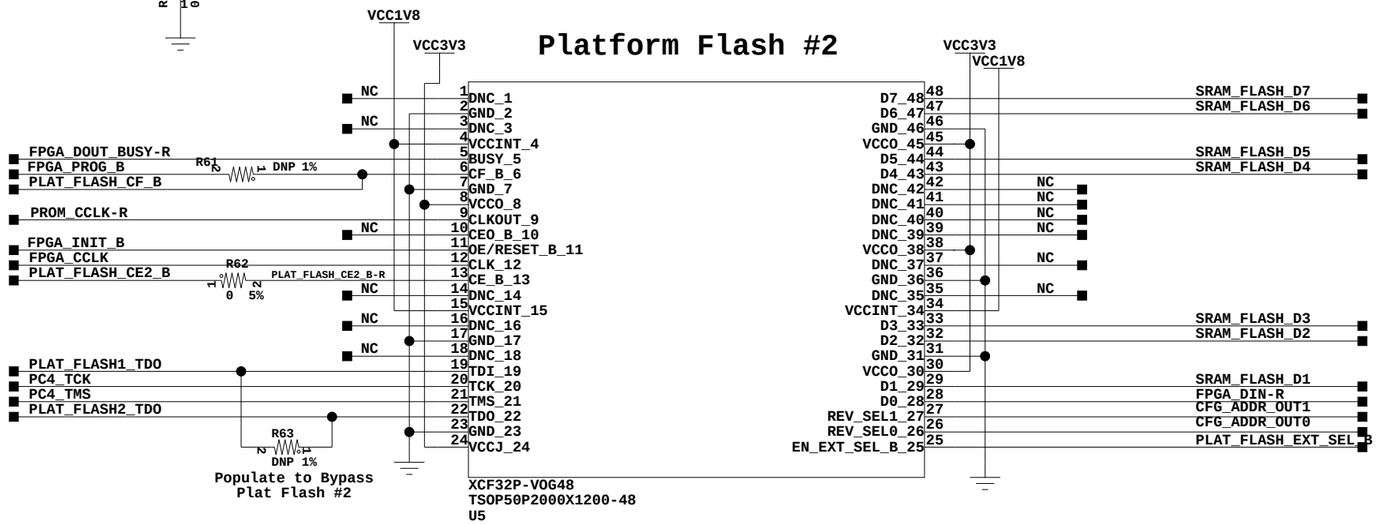
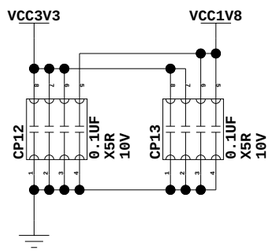
Platform Flash #1



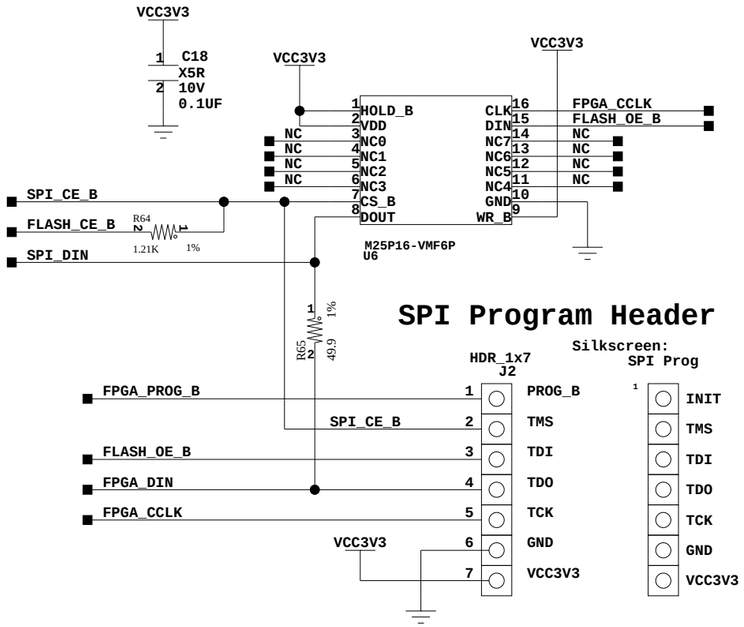


Platform Flash #2

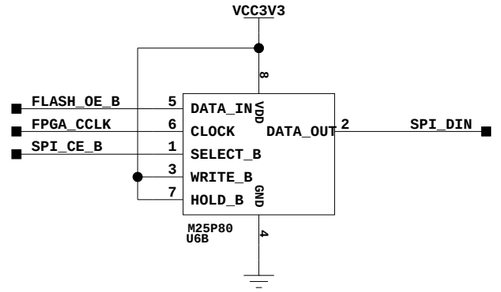




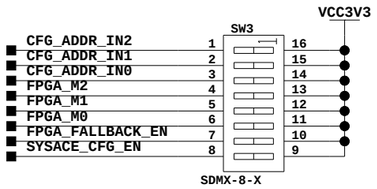
SPI Program Header



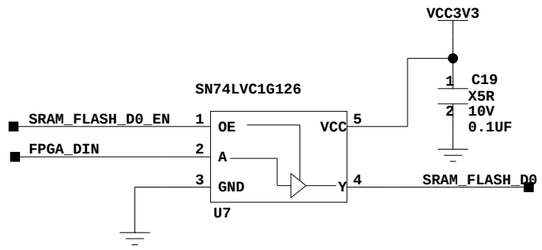
SPI Flash



Silkscreen:
SysACE Config, Mode pins



Config DIP switches



Toggles connection from Plat Flash D0 to SRAM D0

Misc Config
Platform Flash, SPI Flash

Title:	Misc Config,Platform Flash, SPI Flash SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
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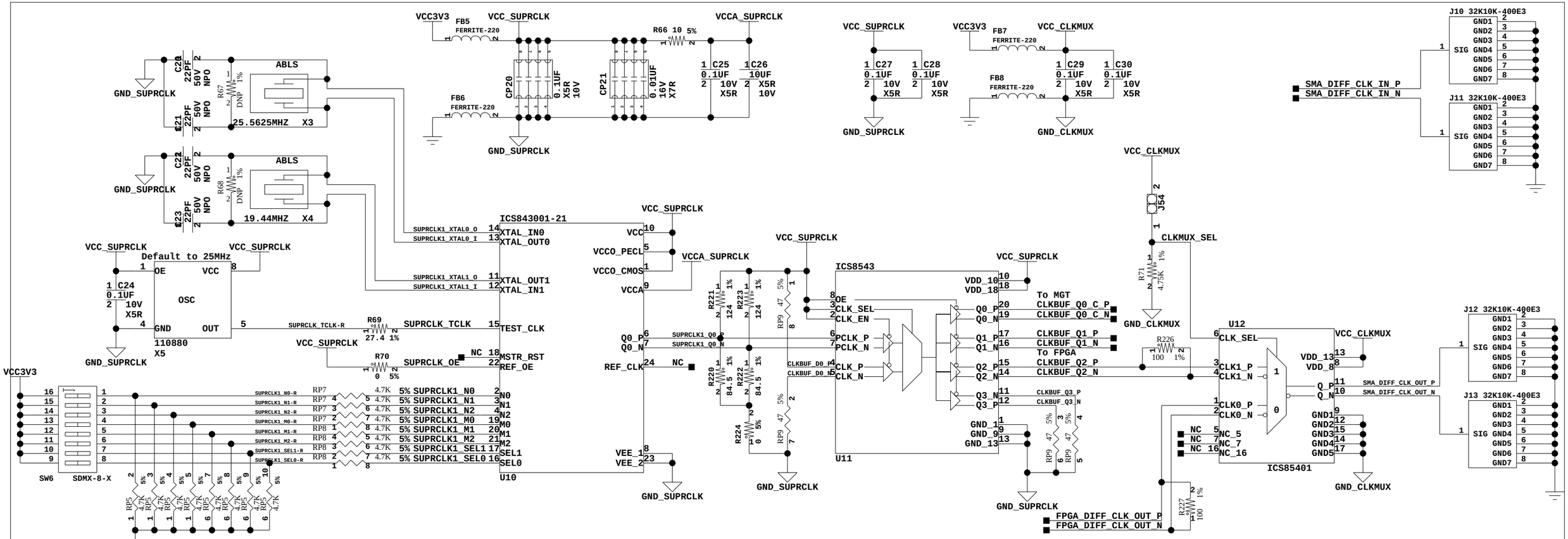
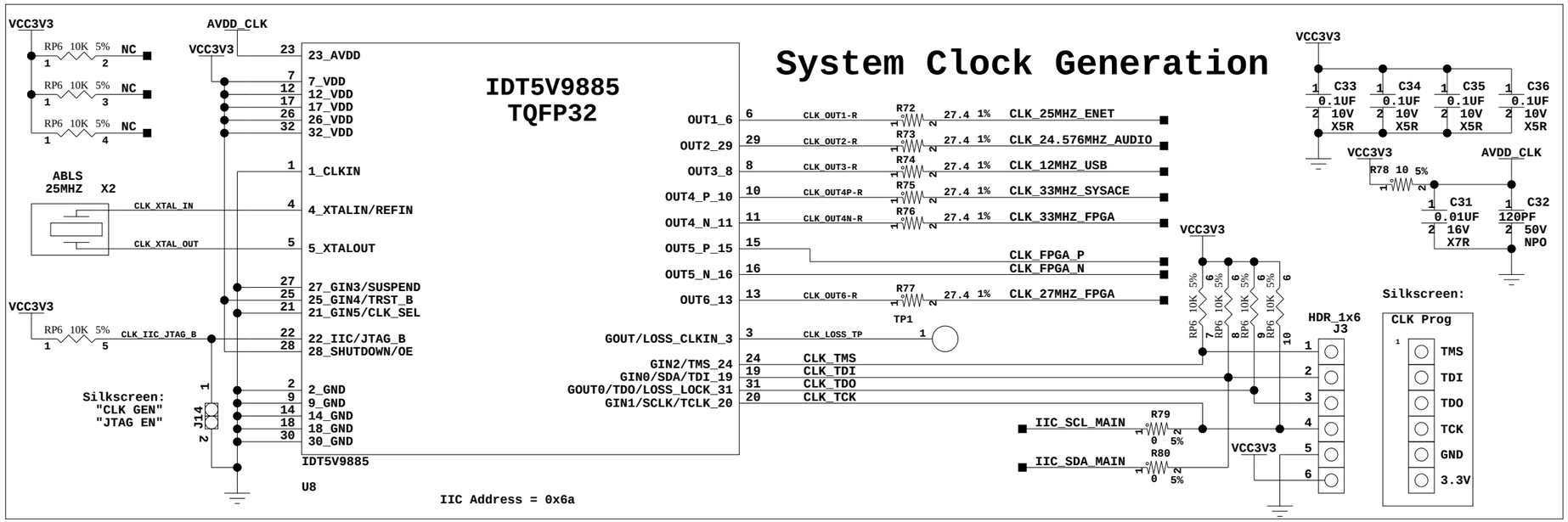
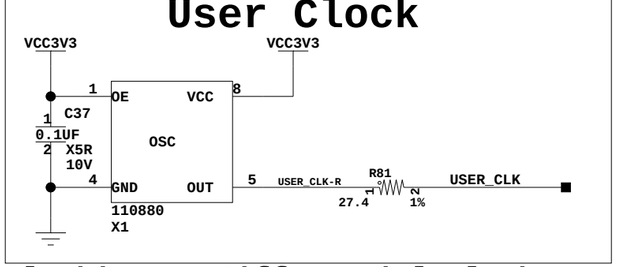
Diff Clocks: SMAs, Generation, MUX and Buffer



System Clock Generation



User Clock



Clocking - Differential Clock, System Clock & User Clock

XILINX

Title:	Differential Clock, System Clock, User Clock SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241
Date: 12-5-2006_10:49	Ver: 02
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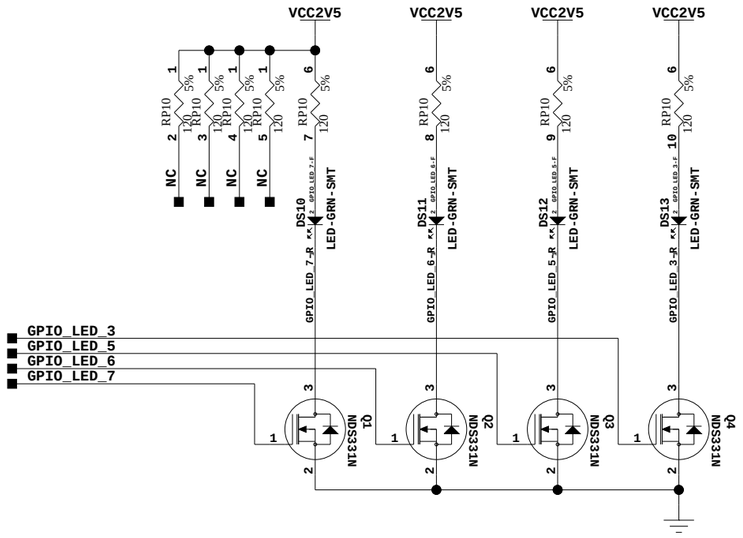
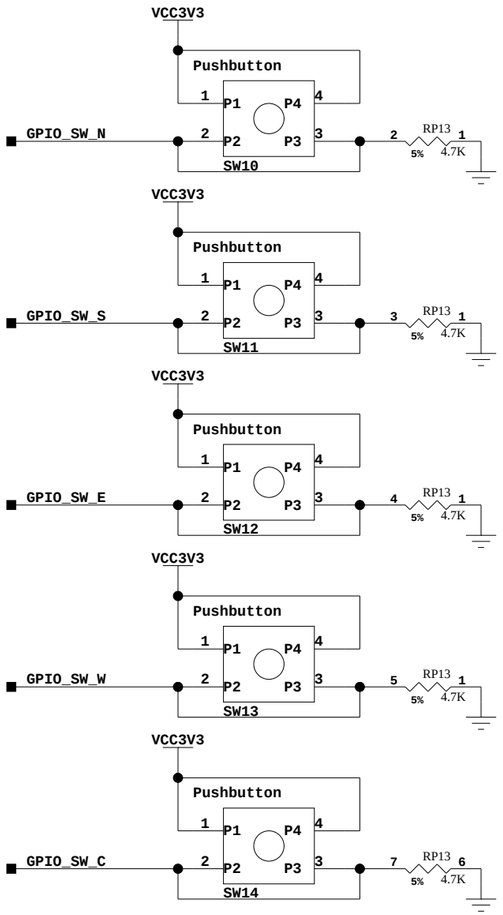
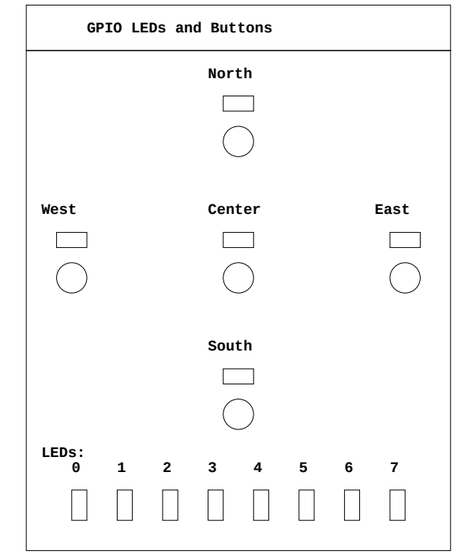
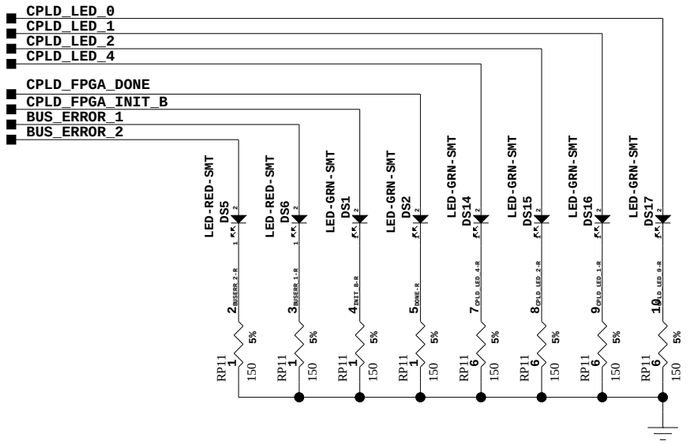
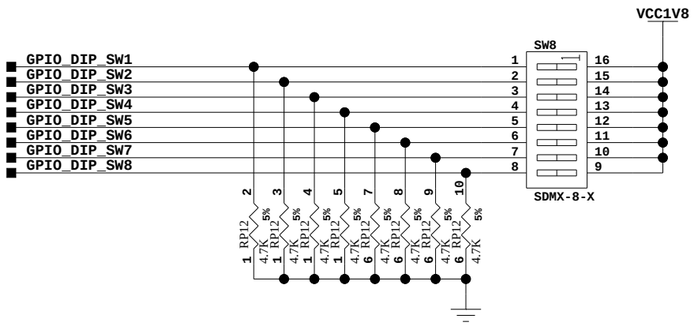


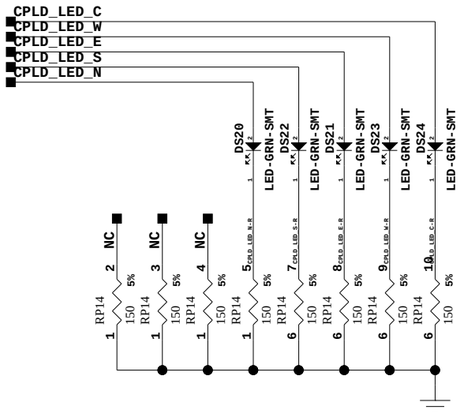








Mounting Holes



Edge Drive Jog Encoder Switch

GPIO - Buttons, LEDs, Switches

Title:	GPIO Buttons, LEDs, Switches, GPIO SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	12-5-2006_10:49	Ver:	02
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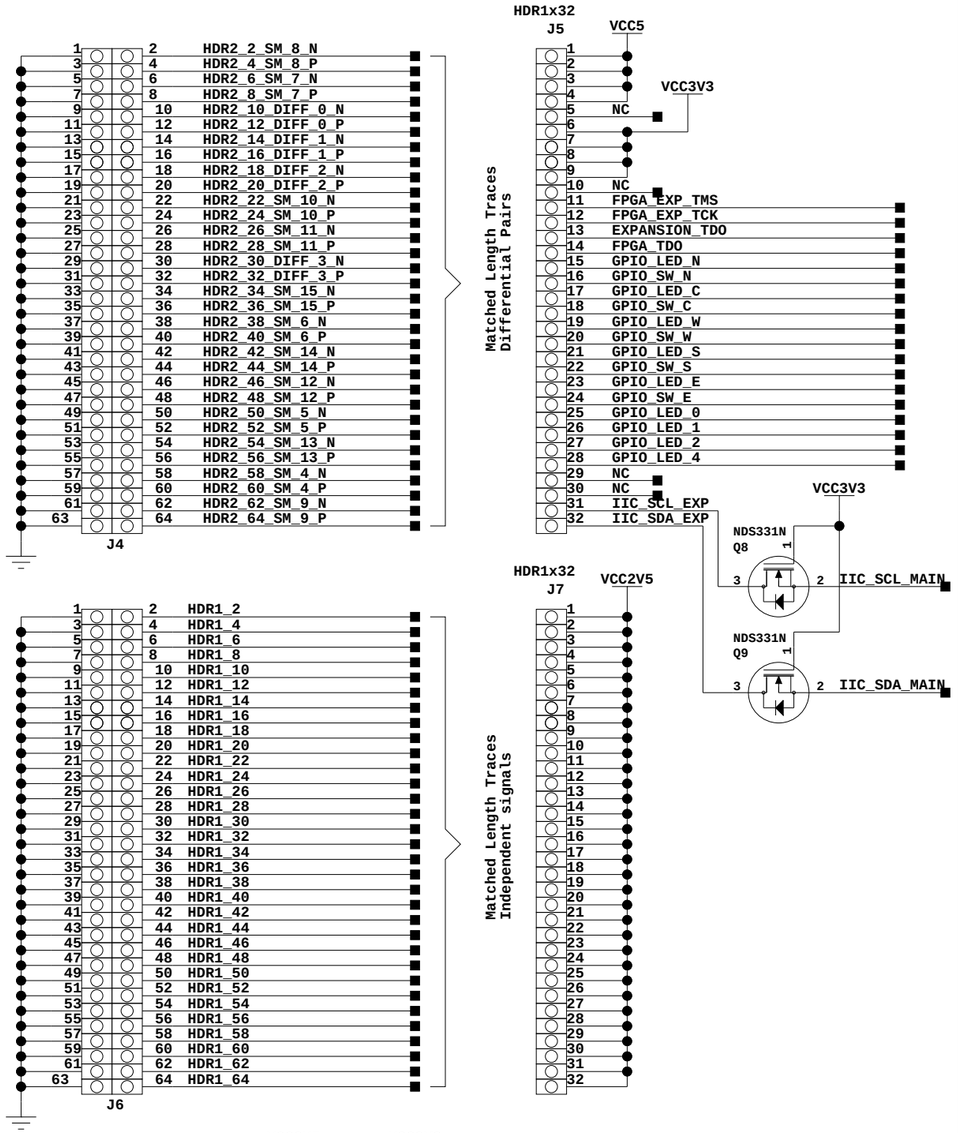
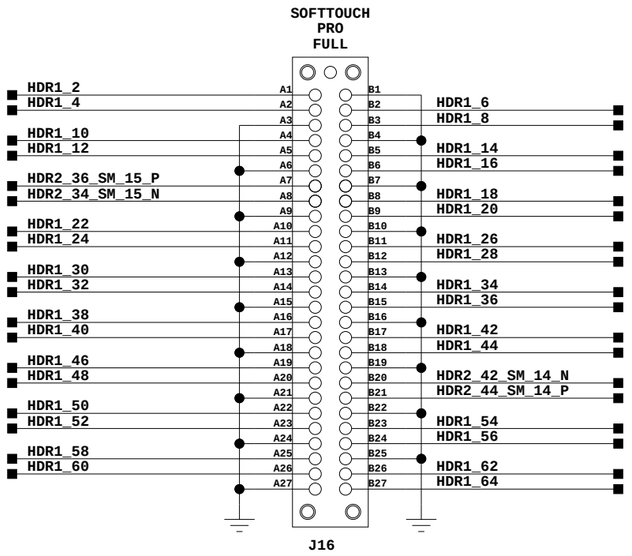
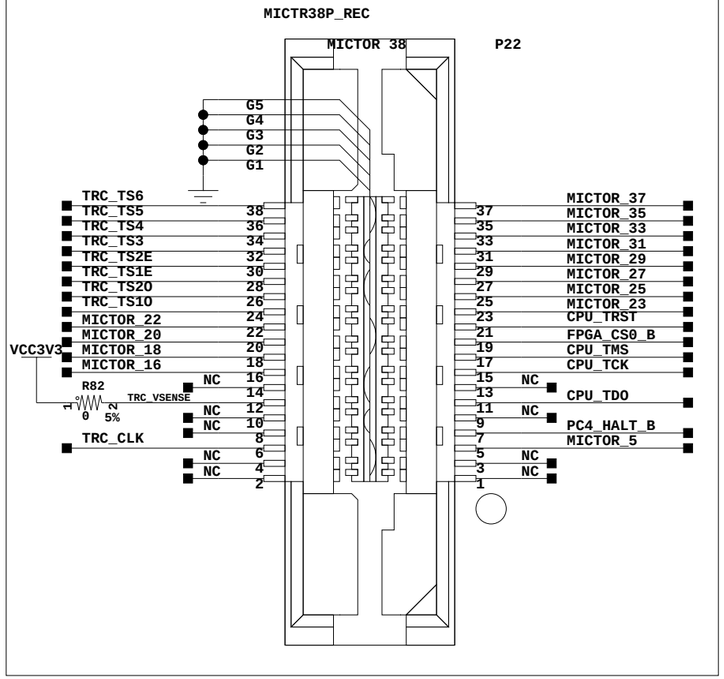
XGI Expansion Interface



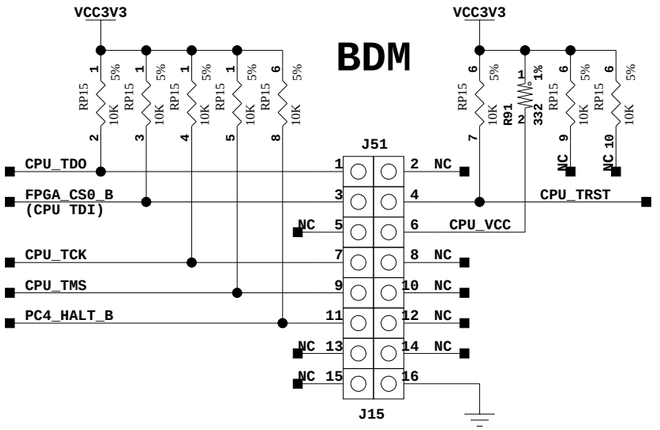
SoftTouch Pro



Mictor



BDM



XGI - Expansion Connector

Title:	XGI - Expansion Headers SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
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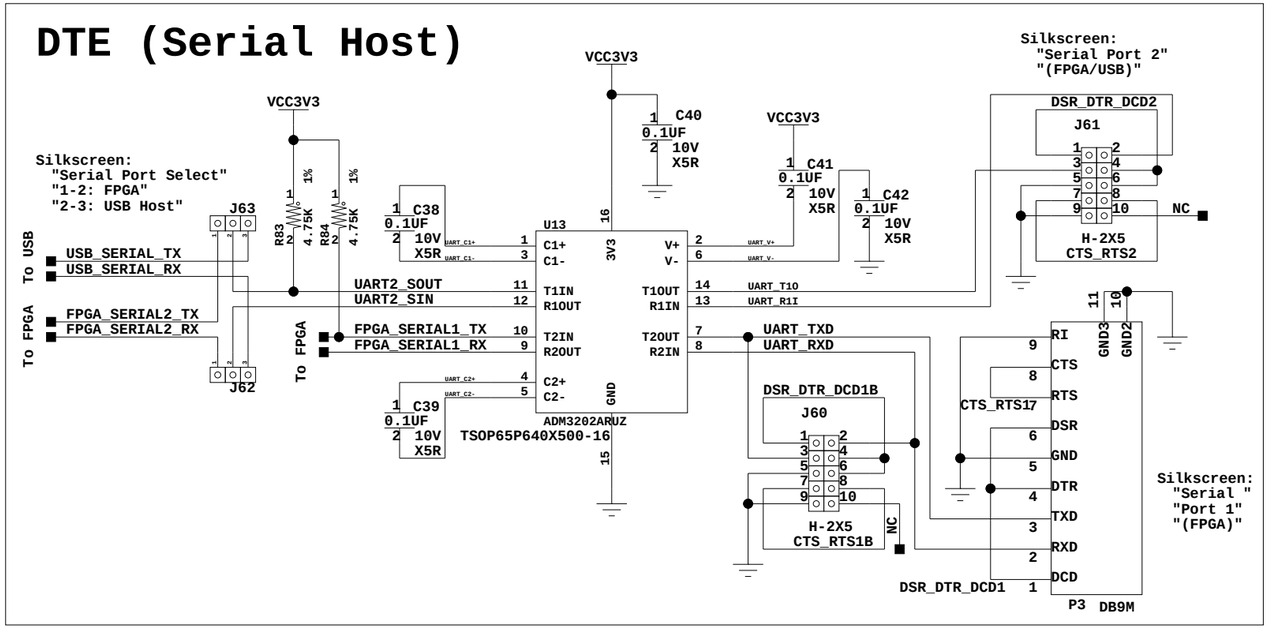
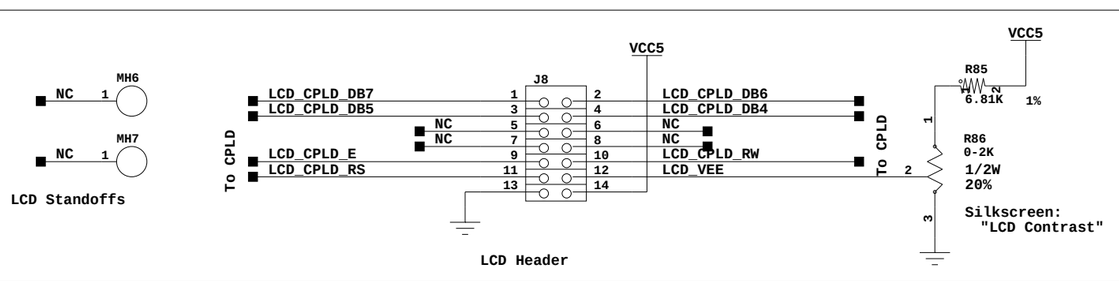
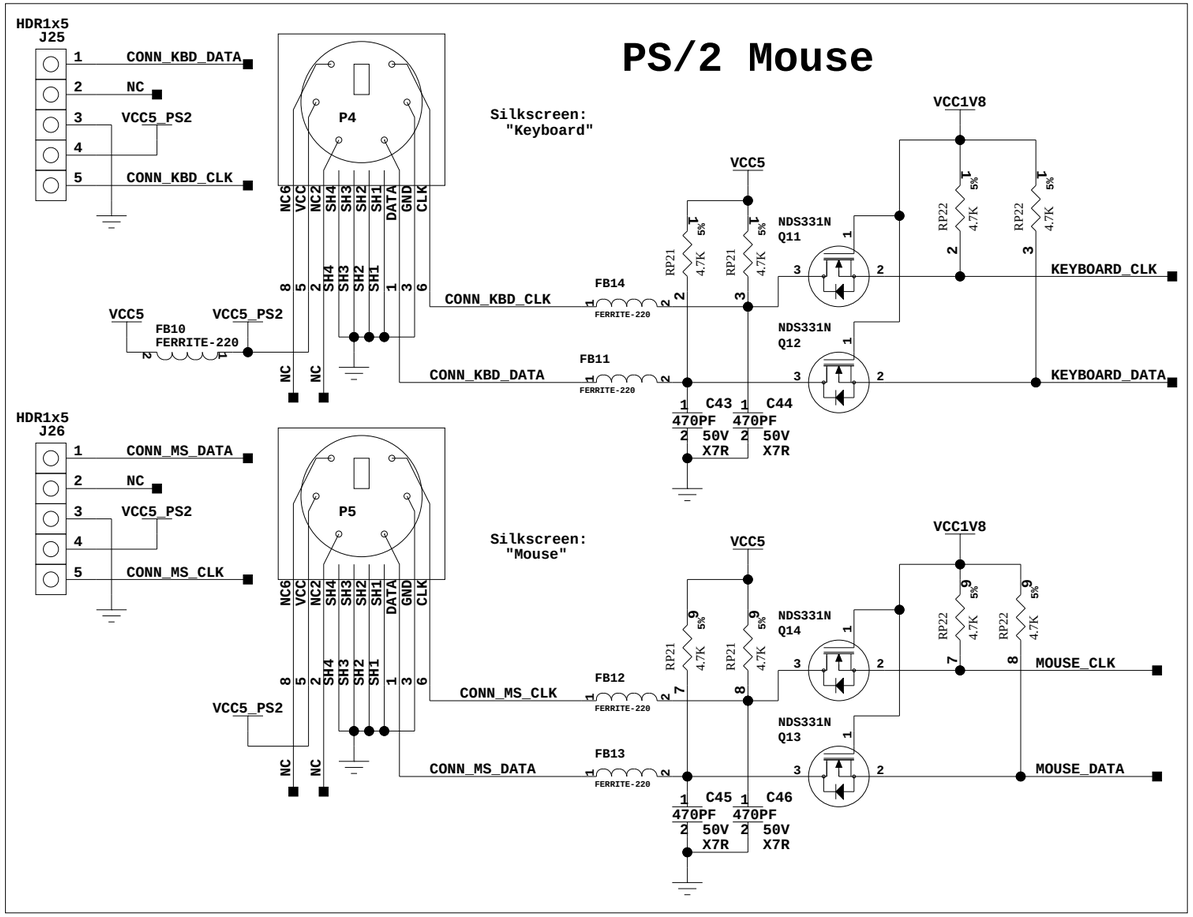
DTE (Serial Host)

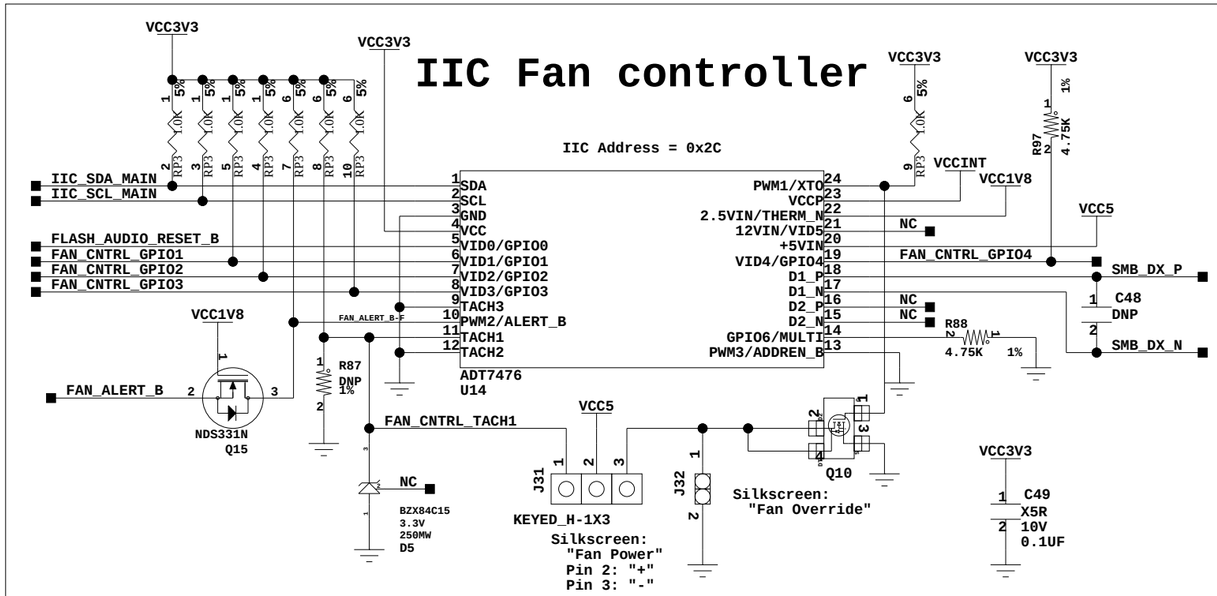




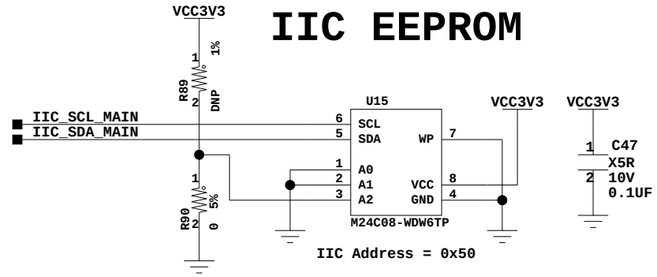
PS/2 Mouse

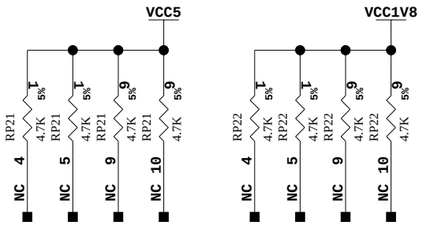


IIC Fan controller



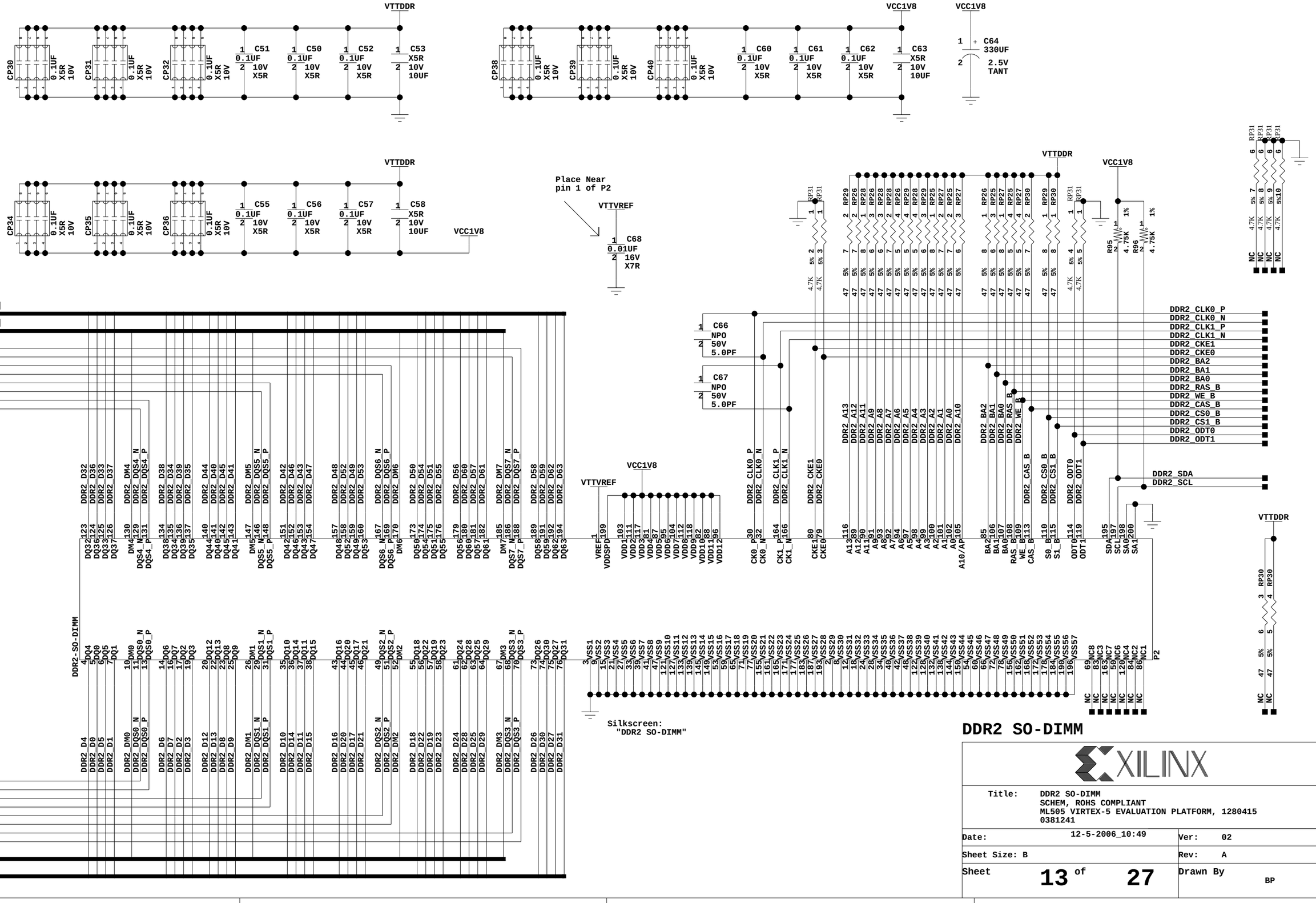
IIC EEPROM





Misc - LCD, PS2, UART, Fan Controller

Title:	LCD, PS2, UART, IIC EEPROM, IIC Fan Controller SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	12-5-2006_10:49	Ver:	02
Sheet Size: B		Rev:	A
Sheet	12 of 27	Drawn By	BP



DDR2 SO-DIMM

XILINX

Title:	DDR2 SO-DIMM SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	12-5-2006_10:49	Ver:	02
Sheet Size: B		Rev:	A
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The PHY MDIP Pins below are
Media Dependent Interface Pins (MDIP),
and are all bidirectional pins.

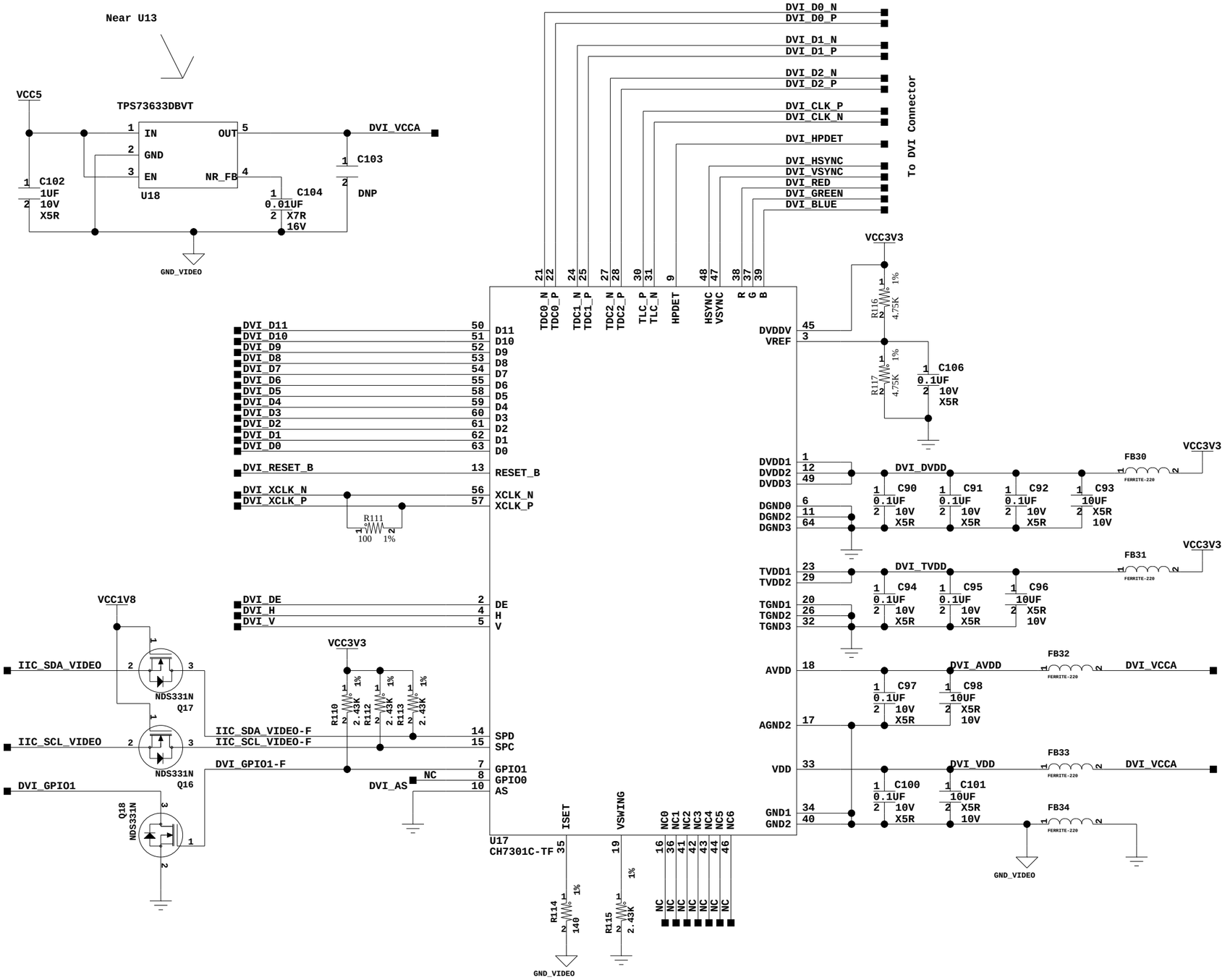
Pin to Constant Mapping	
Pin	Bit [2:0]
VCC2V5	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
GND	000

J22, J23 pins 1-2: GMII/MII to Cu
J22, J23 pins 2-3: SGMII to Cu, no clk
J22 pins 1-2, J24 ON: RGMII, modified MII in Cu

Pin	Bit[2]	Bit[1]	Bit[0]		
CFG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	000	PHYAddr "00111". Don't advertise the PAUSE bit
CFG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000	
CFG2	ANEG[3]	ANEG[2]	ANEG[1]	111	Auto-Neg en, advertise all caps; prefer slave. Auto crossover enabled. 125 CLK option disabled.
CFG3	ANEG[0]	ENA_XC	DIS_125	111	
CFG4	HWCFG_MD[2]	HWCFG_MD[1]	HWCFG_MD[0]	111	GMII to Cu mode. Fiber/copper auto-detect diasabled. Sleep mode disabled.
CFG5	DIS_FC	DIS_SLEEP	HWCFG_MD[3]	111	
CFG6	SEL_BDT	INT_POL	75/50 OHM	010	MDC/MDIO selected. Active LOW interrupt 50Ohm SERDES option.

10/100/1000 PHY

Title:	10/100/1000 PHY SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241
Date:	12-5-2006_10:49
Ver:	02
Sheet Size: B	
Rev:	A
Sheet	14 of 27
Drawn By	BP

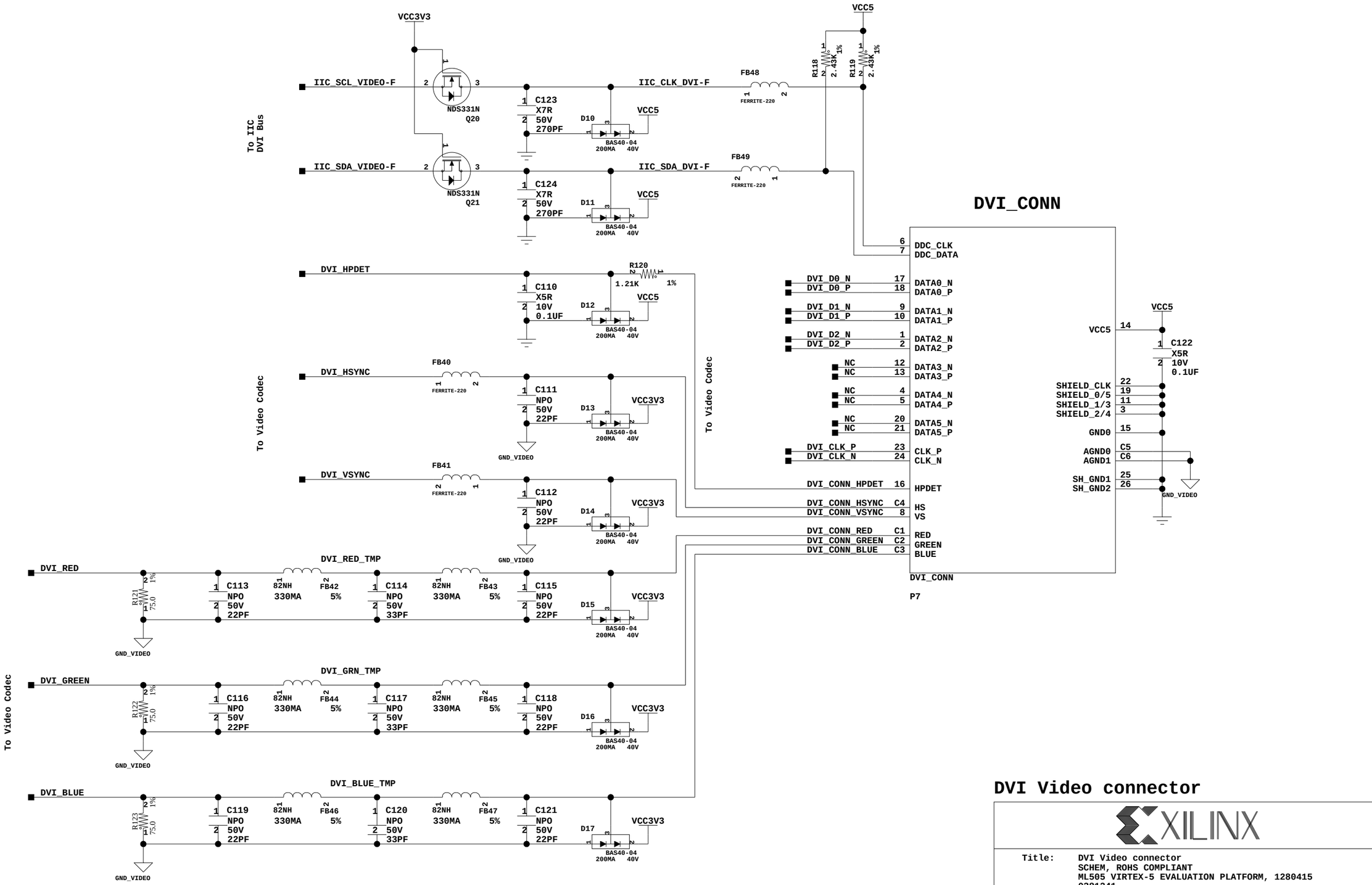


IIC Address = 0x76

VGA Out Codec

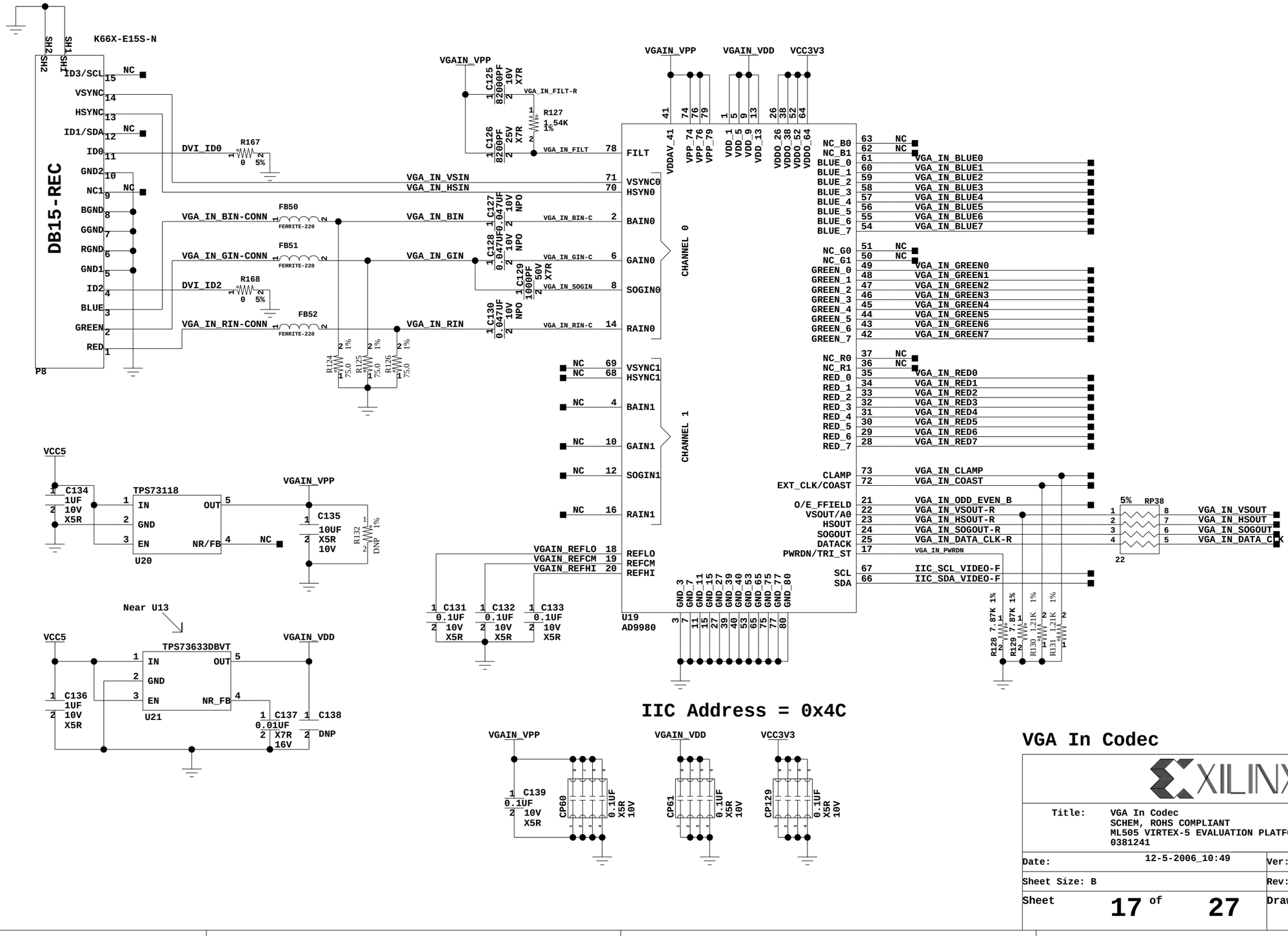
XILINX

Title:	VGA Out Codec SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	12-5-2006_10:49	Ver:	02
Sheet Size: B		Rev:	A
Sheet	15 of 27	Drawn By	BP



DVI Video connector

Title:	DVI Video connector SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	12-5-2006_10:49	Ver:	02
Sheet Size: B		Rev:	A
Sheet	16 of 27	Drawn By	BP



VGA In Codec

XILINX

Title:	VGA In Codec SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	12-5-2006_10:49	Ver:	02
Sheet Size: B		Rev:	A
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CLK_24.576MHZ_AUDIO
AUDIO_SDATA_OUT
AUDIO_BIT_CLK
AUDIO_SDATA_IN
AUDIO_SYNC
FLASH_AUDIO_RESET_B
PIEZO_SPEAKER

Portions of the design above this line are "Digital Ground", and should be outside the moat

Portions of the design below this line are "Analog Ground", and should be inside the moat

VCC3V3 SN74LVC1G126 VCC3V3
U45

R135 4.75K 1%
R136 4.75K 1%
R137 4.75K 1%
R138 4.75K 1%
R139 0 5%
R140 3.01K 1%
R141 3.01K 1%
R142 4.75K 1%
R143 4.75K 1%
R144 75.0 1%
R145 75.0 1%
R146 75.0 1%
R147 100 1%
R148 27.4 1%
R149 27.4 1%
R204 1.21K 1%
R205 1.21K 1%
R206 1.21K 1%
R157 4.75K 1%
R158 4.75K 1%

C140 1UF 10V X5R
C141 10UF X5R 10V
C142 1UF 10V X5R
C143 0.1UF 10V X5R
C144 0.1UF 10V X5R
C145 10UF X5R 10V
C146 0.1UF 10V X5R
C147 0.1UF 10V X5R
C148 0.1UF 10V X5R
C149 1UF 10V X5R
C150 0.1UF 10V X5R
C151 270PF 50V X7R
C152 270PF 50V X7R
C153 270PF 50V X7R
C154 270PF 50V X7R
C155 X5R 10V 0.1UF
C156 10UF X5R 10V
C157 1UF 10V X5R
C158 10V 0.1UFX5R
C159 10V 0.1UFX5R
C160 10V 1UF X5R
C161 10V 1UF X5R
C162 150UF 10V TANT
C163 150UF 10V TANT
C164 X5R 10V 1UF
C165 X5R 10V 1UF
C166 0.1UF 10V X5R

SP1

VCC5
VCC3V3
VCC5_AUDIO

AUDIO_SPDIF
To CPLD and Back
CPLD_SPDIF_1
CPLD_SPDIF_2
CPLD_SPDIF_3
RCA_SPDIF

Silkscreen: "SPDIF Out"
P14
CON_RCA_TH
RCA_JACK

Silkscreen: "Microphone In"
STEREO_JACK_TH
MIC2_CONN
MIC1_CONN
P10

STEREO_JACK_TH
P11
Silkscreen: "Line In"

AUDIO_PHONE
AUDIO_VREF_OUT
MIC1_IC
MIC2_IC
LINE_IN_L_IC
LINE_IN_R_IC
LINE_OUT_R_IC
LINE_OUT_L_IC

NC
PC_NC
RESET_N_11
SYNC_10
DVDD2_9
SDATA_IN_8
DVSS2_7
BIT_CLK_6
SDATA_OUT_5
DVSS1_4
XTL_OUT_3
XTL_IN_2
DVDD1_1

13_PHONE_IN
14_AUX_L
15_AUX_R
16_JS1
17_JS0
18_CD_L
19_CD_GND_REF
20_CD_R
21_MIC1
22_MIC2
23_LINE_IN_L
24_LINE_IN_R

25_AVDD1
26_AVSS1
27_VREF
28_VREFOUT
29_AFLT1
30_AFLT2
31_AFLT3
32_AFLT4
33_AVSS4
34_AVDD4
35_LINE_OUT_L
36_LINE_OUT_R

SPDIF_48
EAPD_47
ID1_N_46
ID0_N_45
AVSS3_44
AVDD3_43
NC_42
HP_OUT_R_41
AVSS2_40
HP_OUT_L_39
AVDD2_38
MONO_OUT_37

HP_OUT_R_IC
HP_OUT_L_IC

AD1981B
LQFP48
AC97
U22

FB55
FERRITE-220

RP41 4.7K

J28
H-2X5

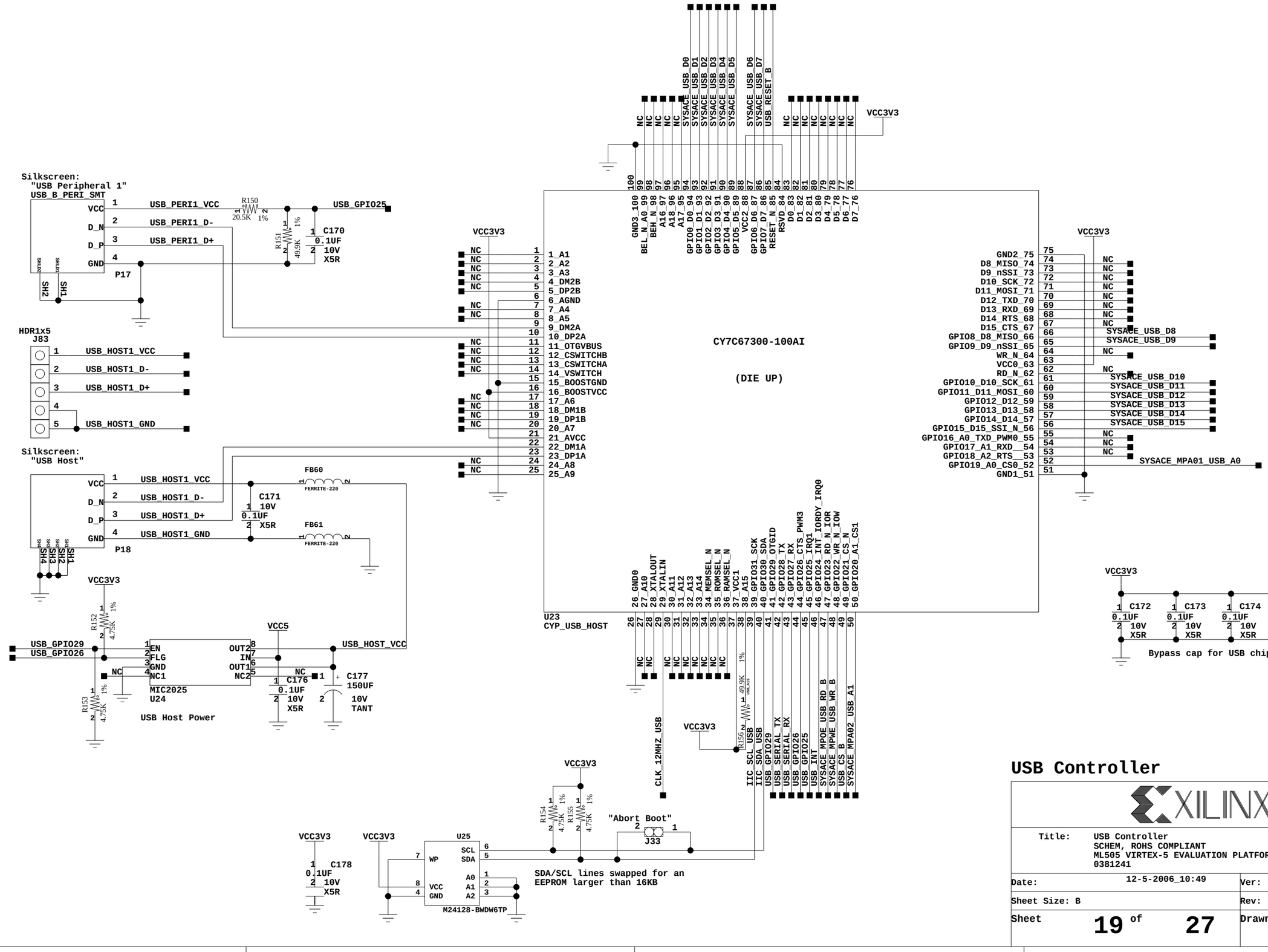
HP_OUT_R_CONN
HP_OUT_L_CONN
LINE_OUT_R_CONN
LINE_OUT_L_CONN

STEREO_JACK_TH
P13
Silkscreen: "Amplified Line Out"
P12
Silkscreen: "Line Out"

Audio Codec

XILINX

Title:	Audio Codec SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	12-5-2006_10:49	Ver:	02
Sheet Size: B		Rev:	A
Sheet	18 of 27	Drawn By	BP

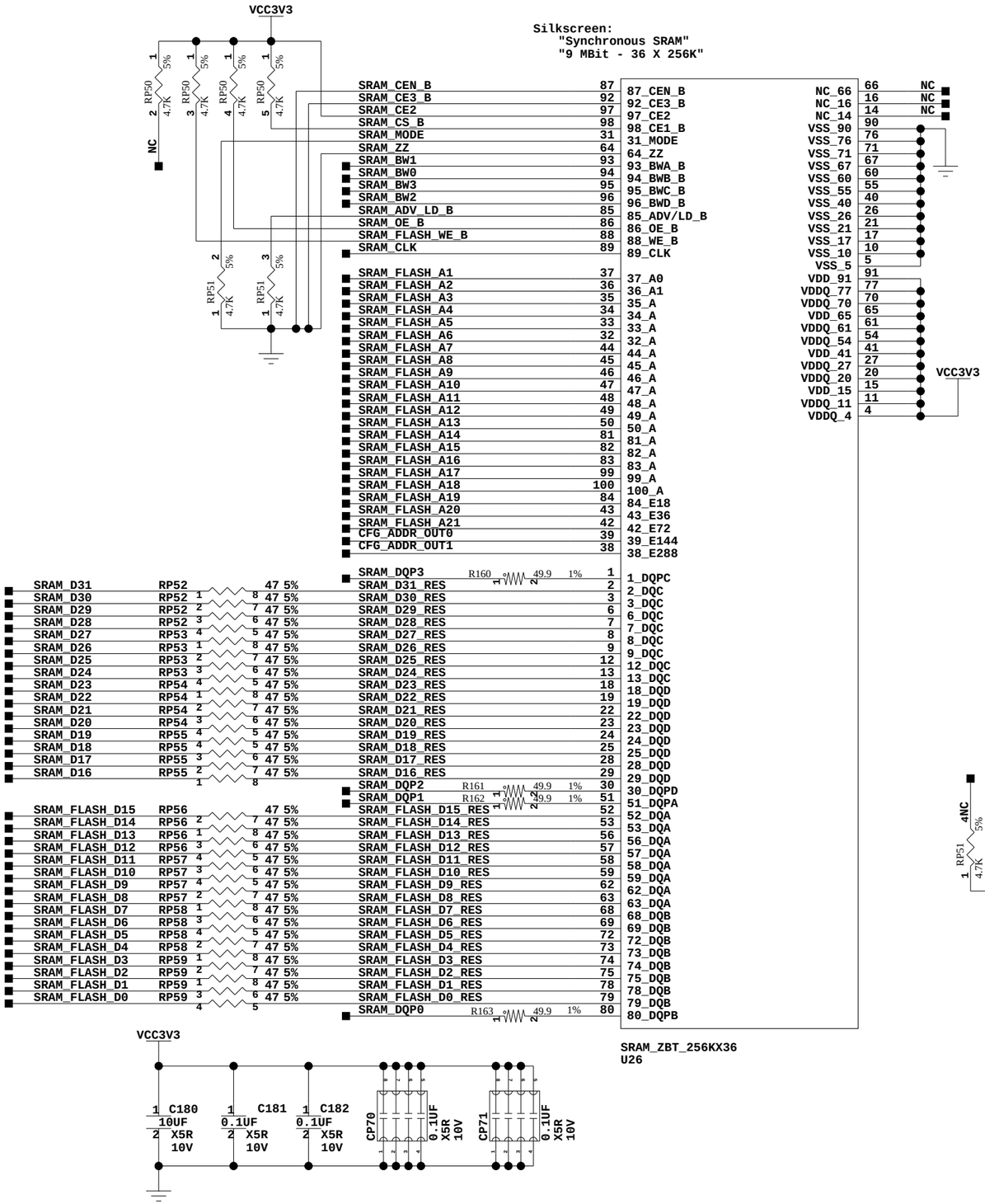


USB Controller

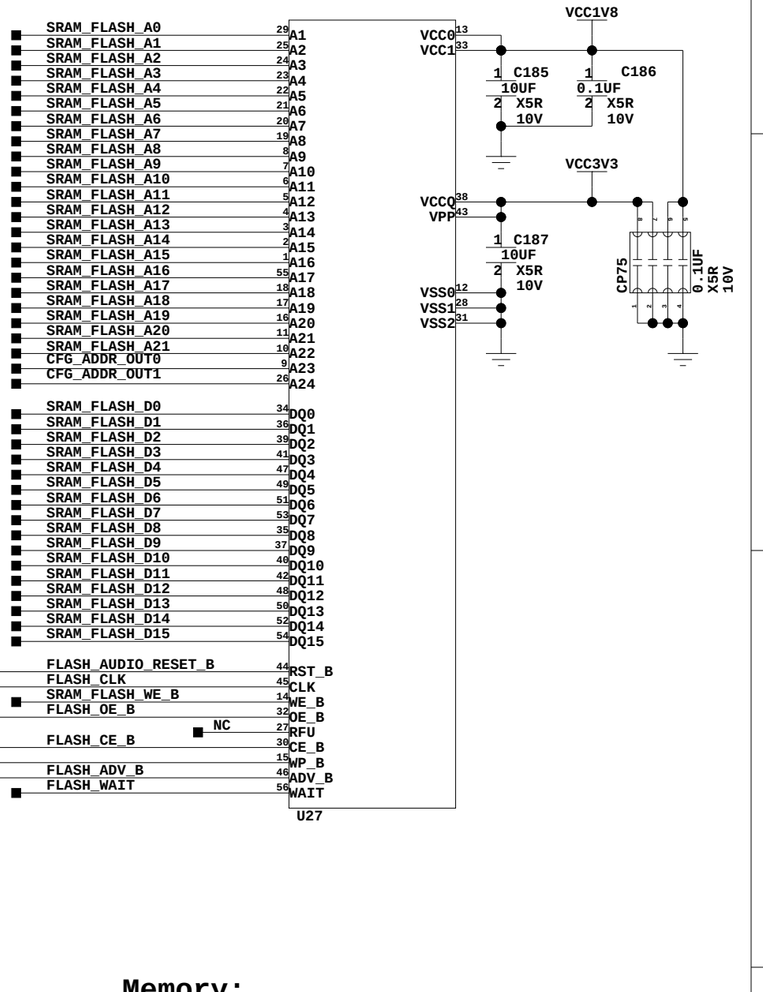
Title:	USB Controller SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	12-5-2006_10:49	Ver:	02
Sheet Size: B		Rev:	A
Sheet	19 of 27	Drawn By	BP

The burst order mode of the SRAM is set to "Linear" by default

Silkscreen:
"Synchronous SRAM"
"9 MBit - 36 X 256K"



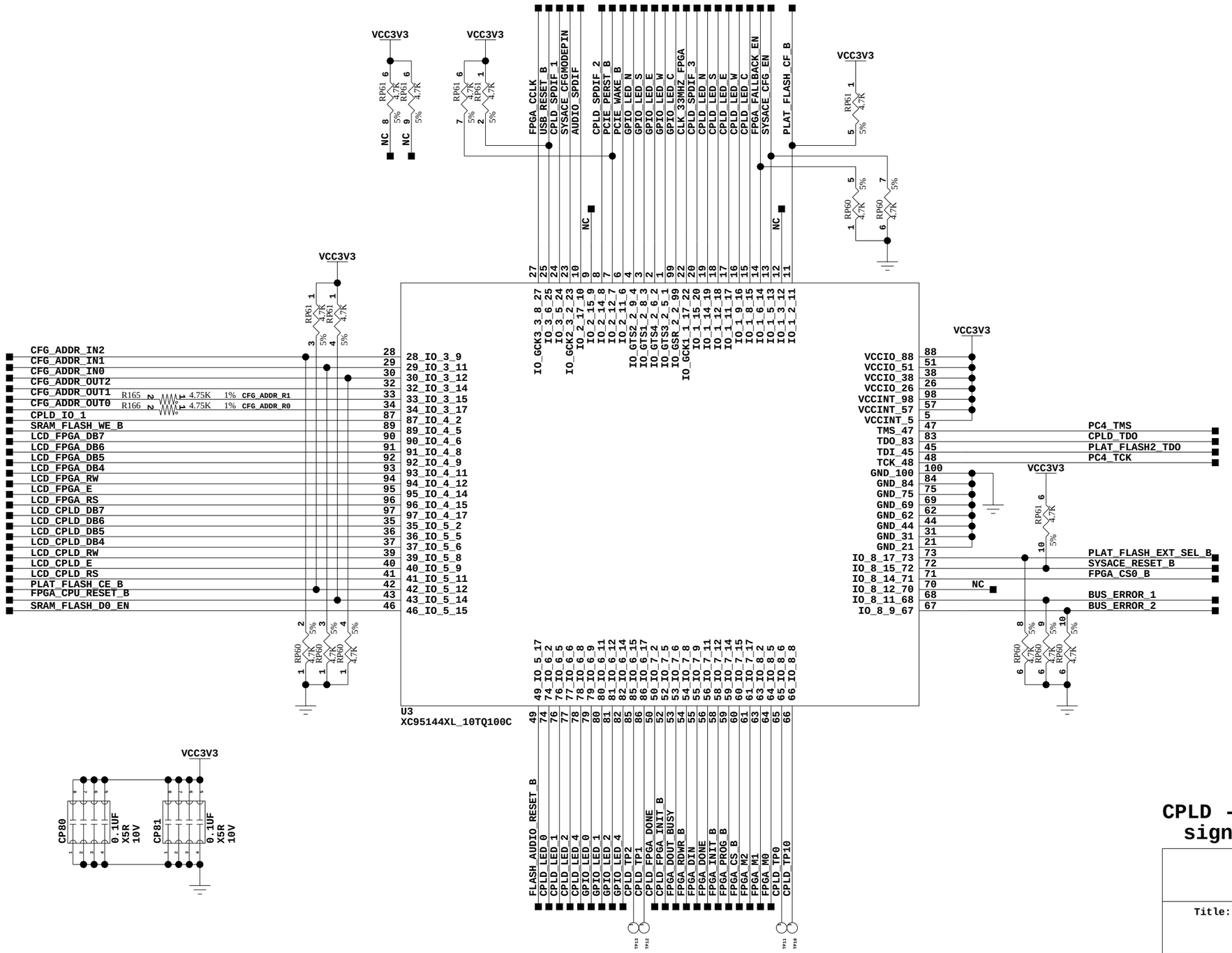
Silkscreen:
"Strata FLASH"
"256 MBit"



Memory:
Synchronous SRAM,
Strata FLASH

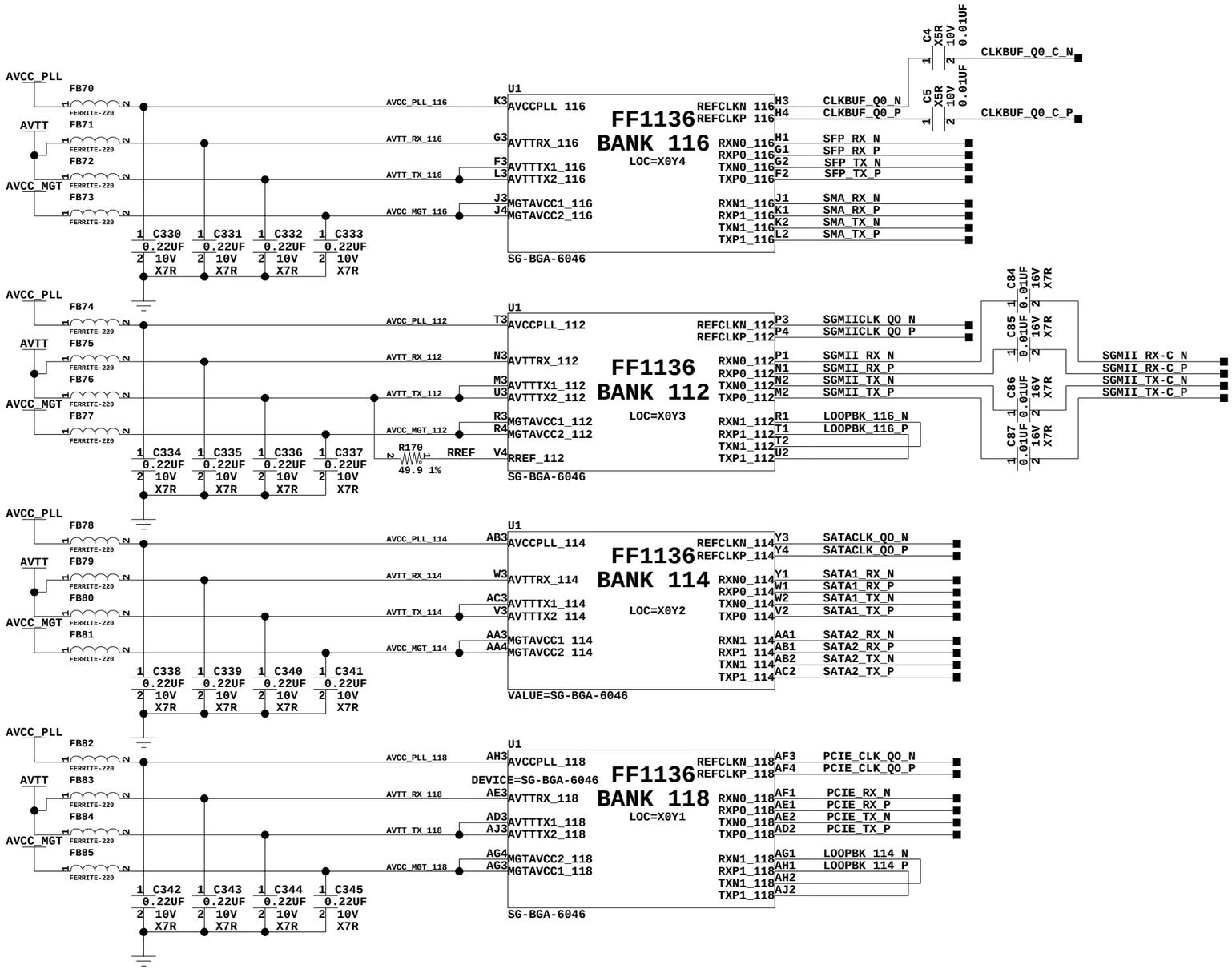
XILINX

Title:	Sync. SRAM, FLASH SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	12-5-2006_10:49	Ver:	02
Sheet Size: B		Rev:	A
Sheet	20 of 27	Drawn By	BP



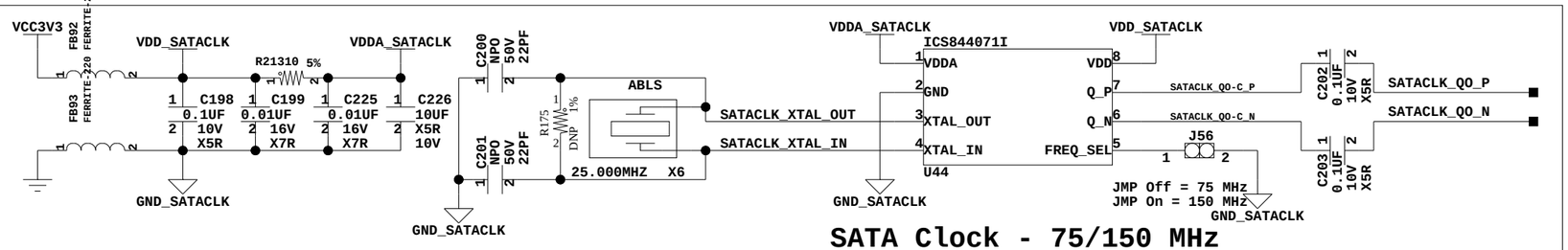
CPLD - Misc signal control

Title:	CPLD - Misc signal control SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	12-5-2006_10:49	Ver:	02
Sheet Size: B		Rev:	A
Sheet	21 of 27	Drawn By	BP

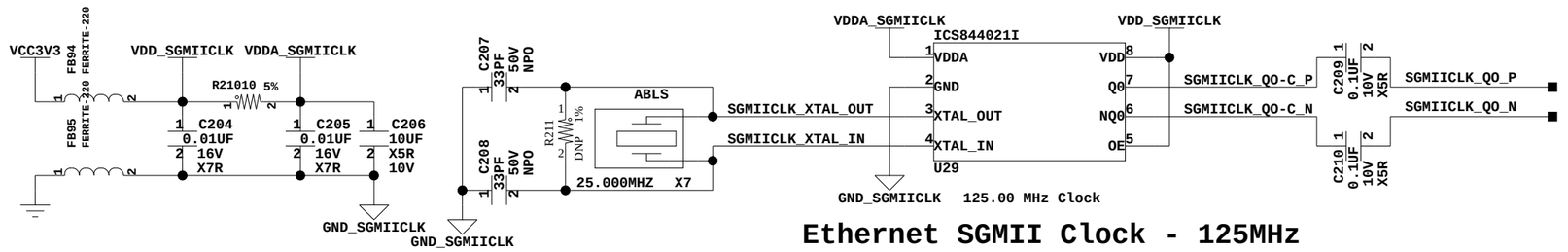


XILINX

Title:	MGT Banks SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	2-4-2008_13:43	Ver:	02
Sheet Size: B		Rev:	A
Sheet	22 of 27	Drawn By	BF

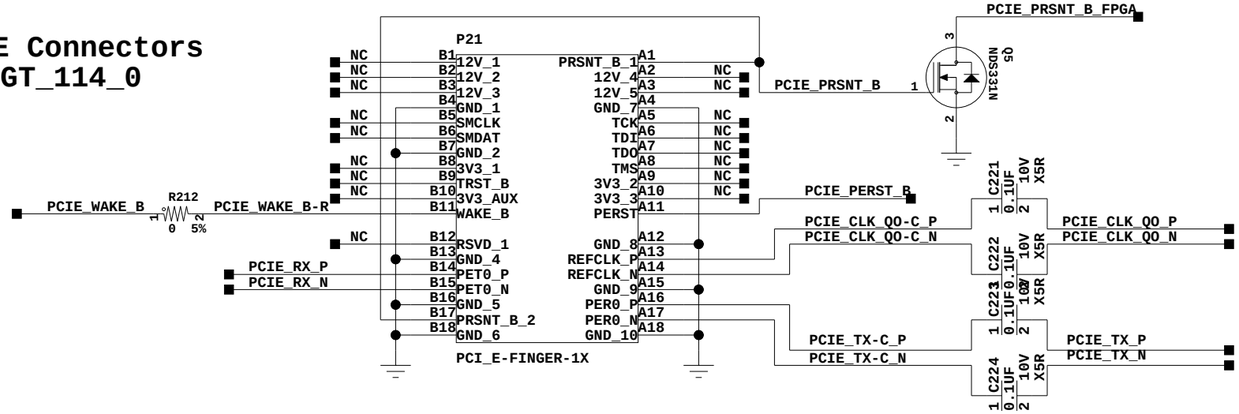


SATA Clock - 75/150 MHz

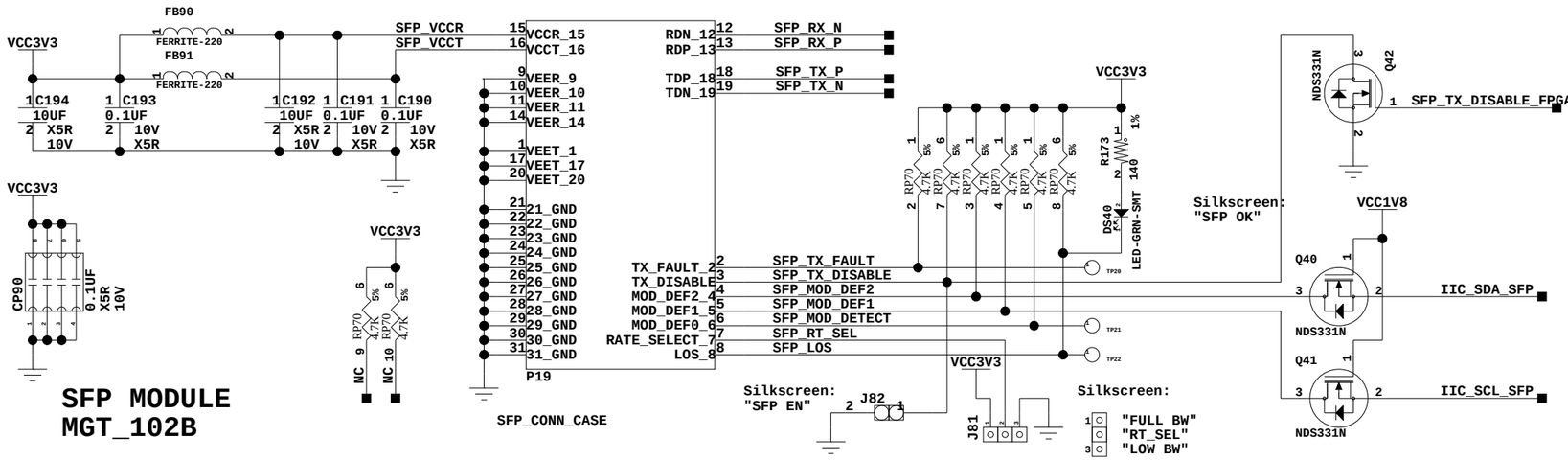


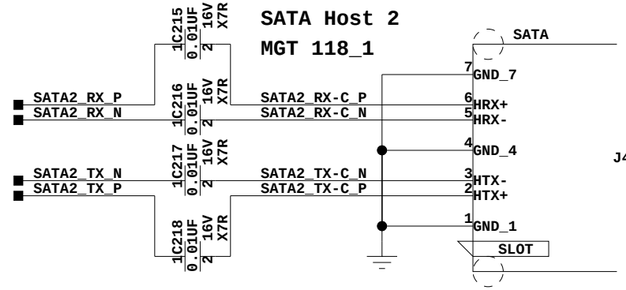
Ethernet SGMII Clock - 125MHz

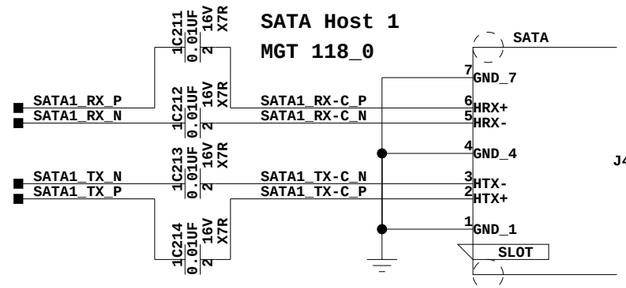
PCI-E Connectors
MGT_114_0

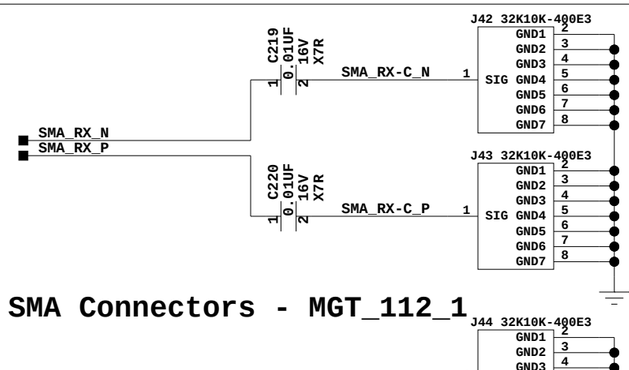


SFP MODULE
MGT_102B

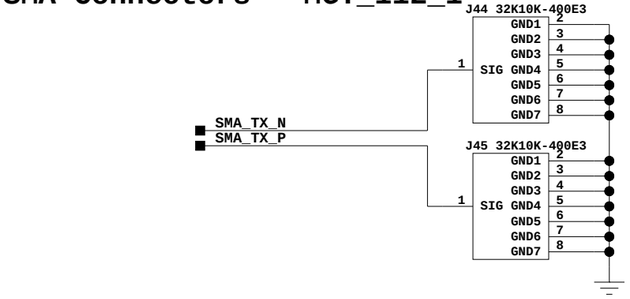








SMA Connectors - MGT_112_1



MGT Clocks and Connectors

Title:	MGT Connectors SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	12-5-2006_10:49	Ver:	02
Sheet Size: B		Rev:	A
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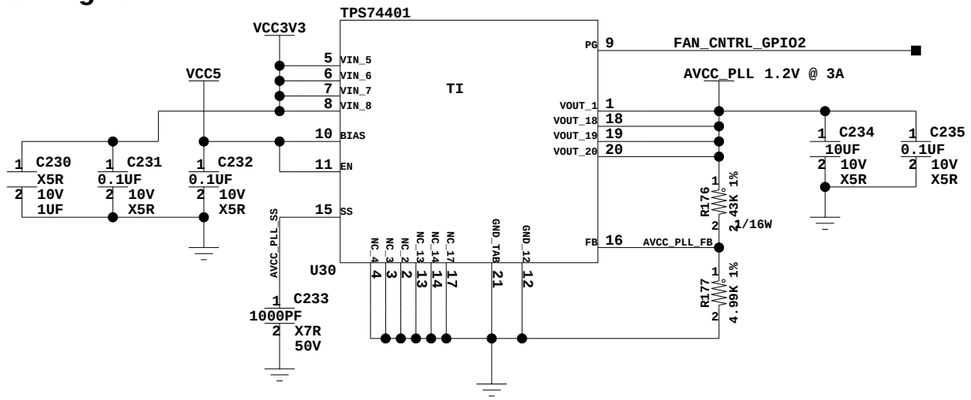
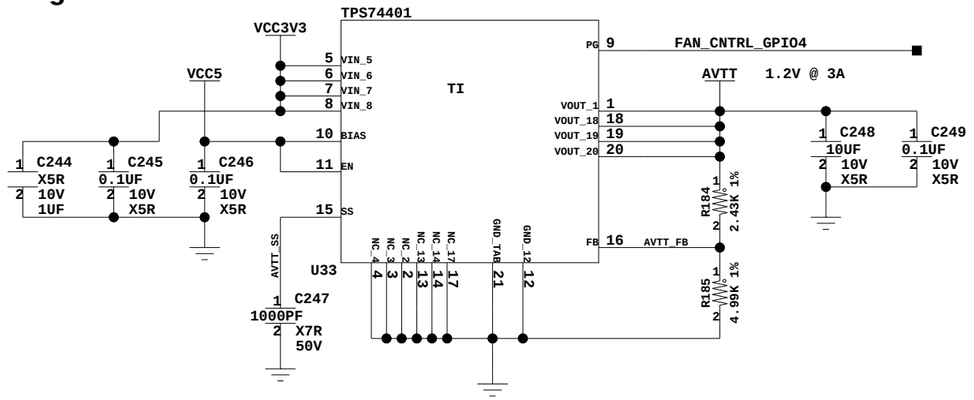
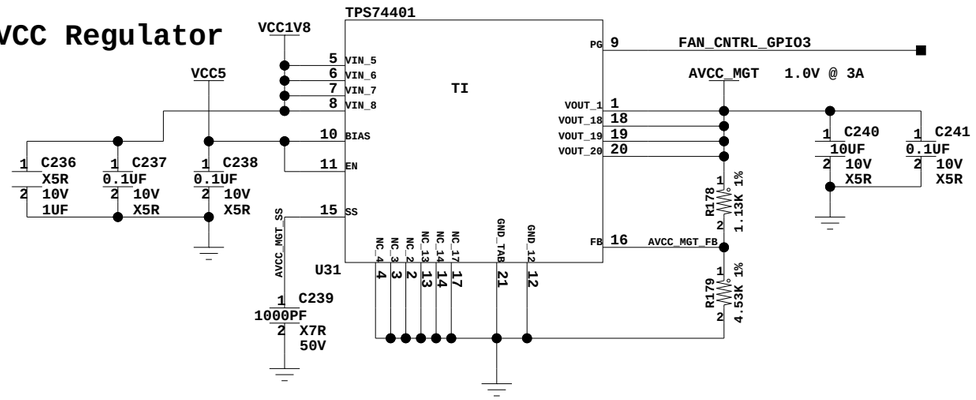
MGT PLL Regulator



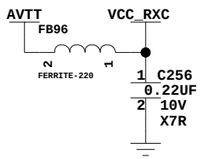
MGT VTT Regulator



MGT AVCC Regulator



MGT RXC Regulator



MGT Power Supplies

XILINX

Title:	MGT Power Supplies SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	12-5-2006_10:49	Ver:	02
Sheet Size: B		Rev:	A
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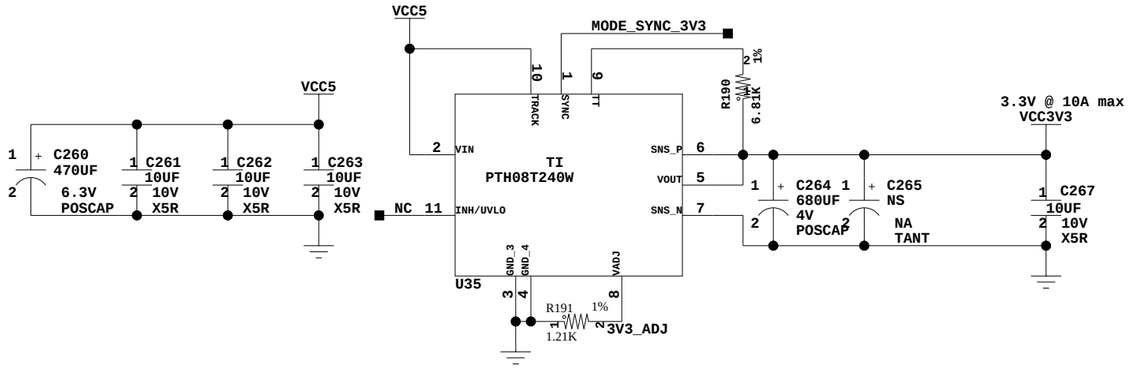
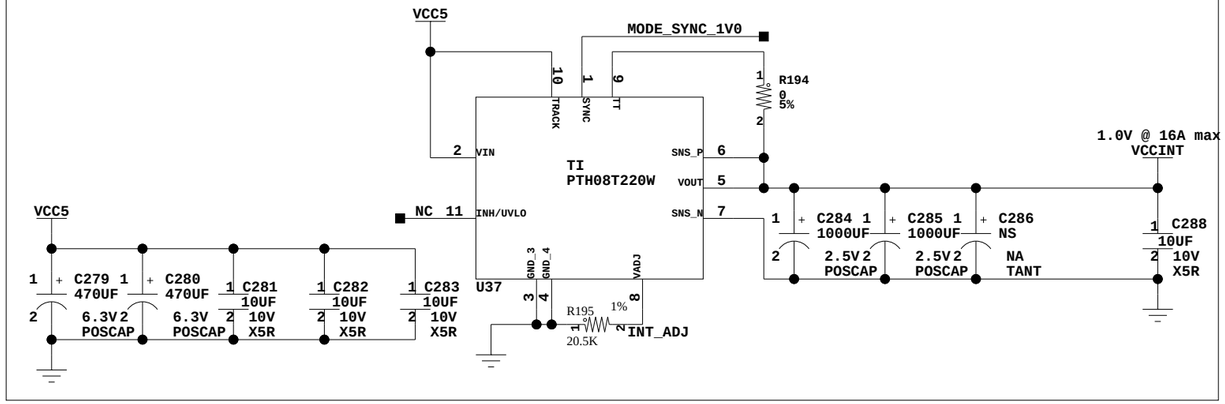
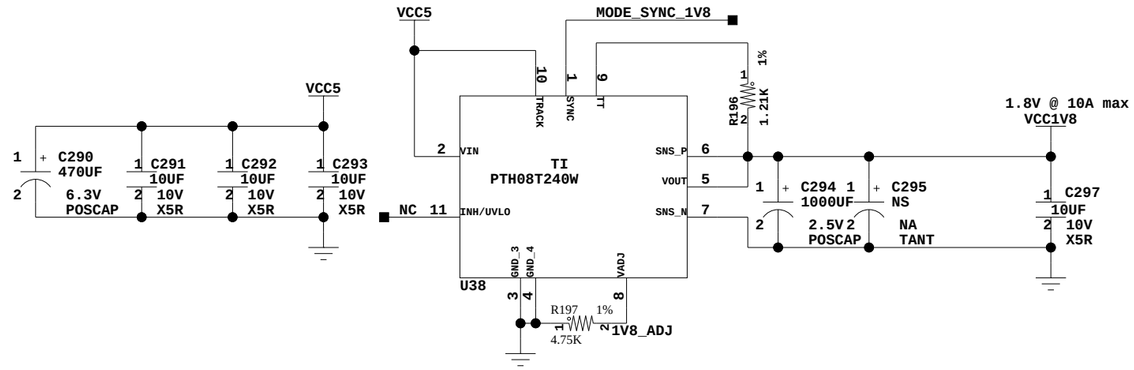
5v to 3.3V Regulator



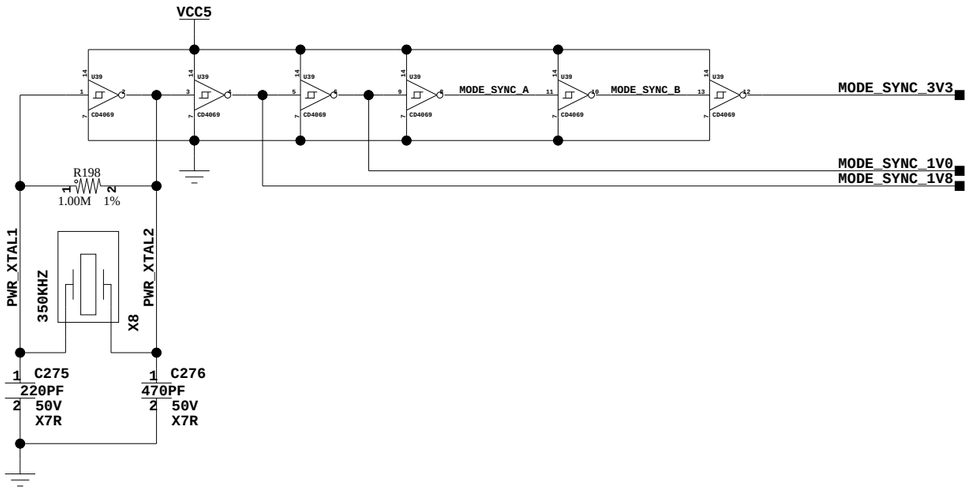
5v to 1.0V Regulator



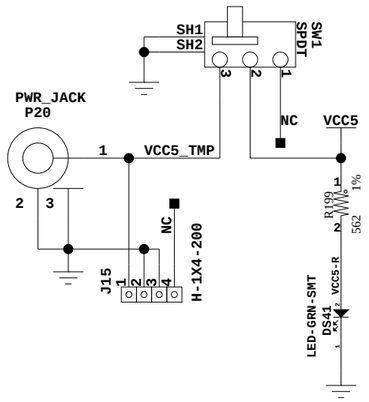
5v to 1.8V Regulator



5V Power Synchronizing Circuit



5V Power - Jack, Switch and LED



5V Power Supplies

XILINX

Title:	Power Supplies SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	12-5-2006_10:49	Ver:	02
Sheet Size: B		Rev:	A
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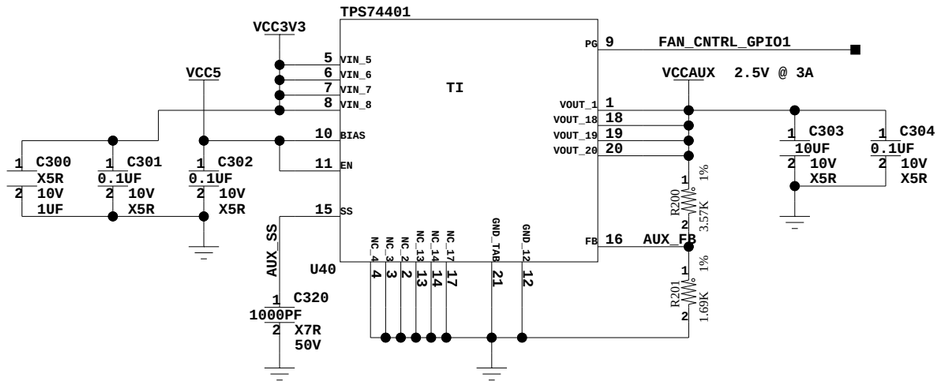
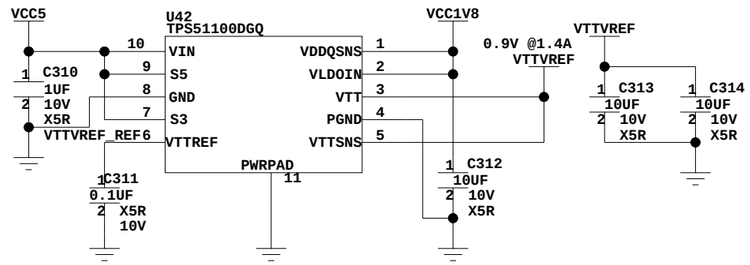
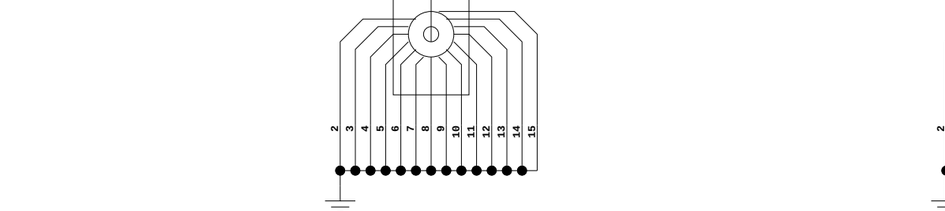
3.3v to 2.5V (VCC AUX) Regulator



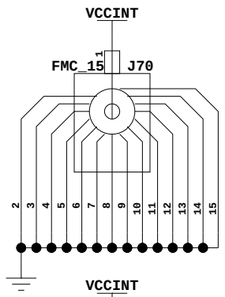
5V to 0.9V (DDR VTT VREF) Regulator

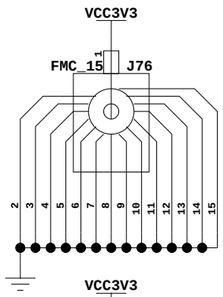


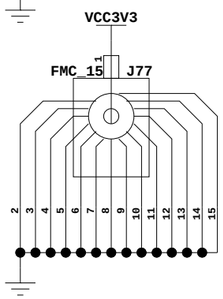
3.3v to 2.5V Regulator



5V to 0.9V (DDR2 VTT DDR) Regulator







5V and 3.3V Power Supplies

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Sheet	26 of 27	Drawn By	BP

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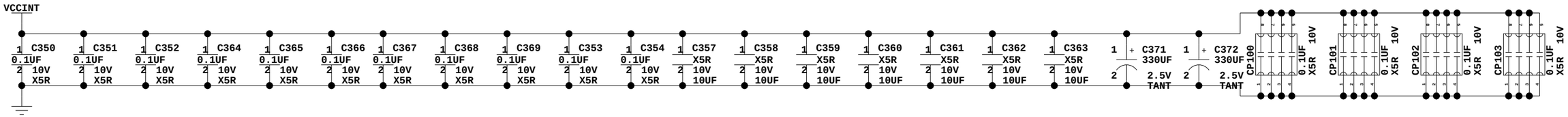

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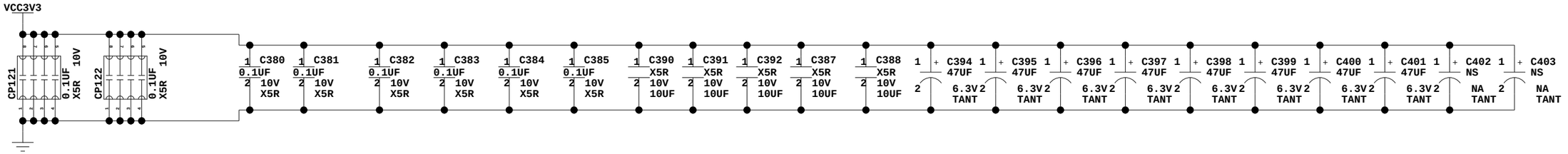

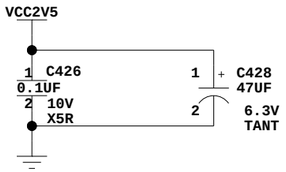

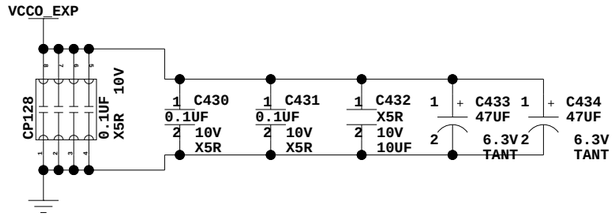

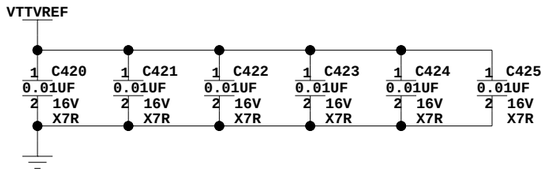

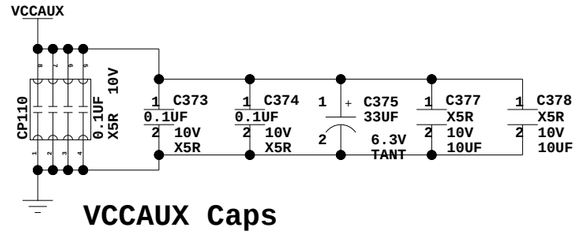

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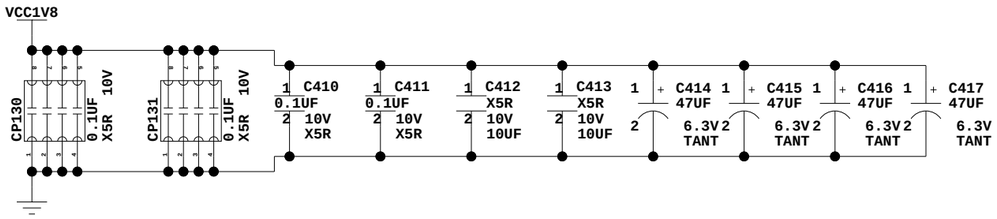

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Sheet 27 of 27	Drawn By BP